A Novel Open-Circuit Fault Detection and Localization Scheme for Cascaded H-Bridge Stage of a Three-Stage Solid-State Transformer

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***Abstract*—A three-stage solid-state transformer (SST) is a preferred replacement for line frequency transformer as it provides ancillary services in addition to stepping-up/down of grid voltages. Each active switch in SST is a potential source of failure, and a quick fault detection and isolation help in reducing the downtime. In this article, a novel fault detection and localization algorithm is proposed to localize the open-circuit (OC) faults (be it a single switch fault or multiple switch faults in multiple modules) in the cascaded H-bridge (CHB) stage of the SST. The proposed method is designed such that only one voltage sensor is needed to measure the grid-side voltage of the CHB for fault detection and localization. By comparing the estimated grid-side voltage of the CHB with the measured values, OC fault is detected. Once the fault is detected, the modulation scheme is switched from phase-shifted unipolar sinusoidal pulsewidth modulation (SPWM) to phase-shifted bipolar SPWM to localize the faults. The difference in the measured grid-side voltage of the CHB before and after each module's state change is calculated and faults are localized. The presented algorithm is substantiated using experimental results from a 1-kVA SST prototype. The main advantage of the proposed algorithm is that it requires only $2n$ comparisons to localize the faulty modules in a CHB with n H-bridges, which takes less than a line cycle to complete.**

***Index Terms*—Cascaded multilevel converter (MMC), fault detection and localization, multiple switch failures, open-circuit (OC) faults, solid-state transformer (SST).**

I. Introduction

IN GENERAL, a fault-tolerant control scheme consists of identification, localization, and isolation of faults, and post-fault restoration, as shown in Fig. 1. These control schemes have been given utmost importance in modern machine-critical converters, such as solid-state transformers (SSTs) in smart grid [3], MMCs in high voltage direct current (HVdc) systems and offshore oil rigs [4], [5], where the economic loss due to the downtime is significant. A quick fault detection, localization, and isolation (FDLI) scheme can help overcome such issues. Before going into the details of the FDLI methods for SSTs, classification of faults in SST modules is presented in Table I. Among the faults, the short-circuit (SC) faults are catastrophic and should be detected immediately [6]. Even though an open-circuit (OC) fault in a switch (due to bond wire lift-off or gate drive failure, etc.) with a healthy antiparallel diode does not create any immediate damage to the module, prolonged operation can cause overvoltage and overcurrent stresses on rest of the modules [7].

Broadly, the FDLI methods can be divided into two: Hardware FDLI (H-FDLI) [10], [12]–[15] and computational FDLI

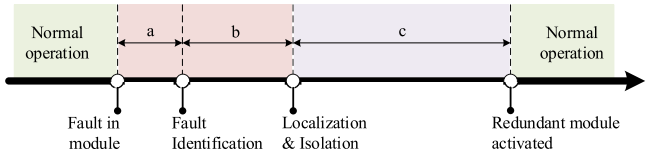

Fig. 1. General framework for fault-tolerant operation. Time taken for fault identification and localization in an 11-level multilevel converter (MMC) is about 16 ms (*a*+*b*) [1] and time taken for the redundant module to resume the normal operation 4 s (*c*) [2].

TABLE I
Types of Faults in SST Module

Fault types	Causes	Reason	FDLI methods
Switch open-circuit faults	Bond wire lift-off	Mismatch in thermal expansion coefficient of Si and Al [8]	Computational
	Gate drive failure	Failure of gate drive is equivalent to open circuit fault [9]	Computational
Switch short circuit faults	Thermal runaway and thermal surges	Shoot through faults, over voltage and currents [10]	Hardware
DC link capacitor faults	Aging	Dielectric material degradation due to contamination [11]	Computational
		Electrolytic vaporization due to ambient temperature and ripple current [11]	Computational

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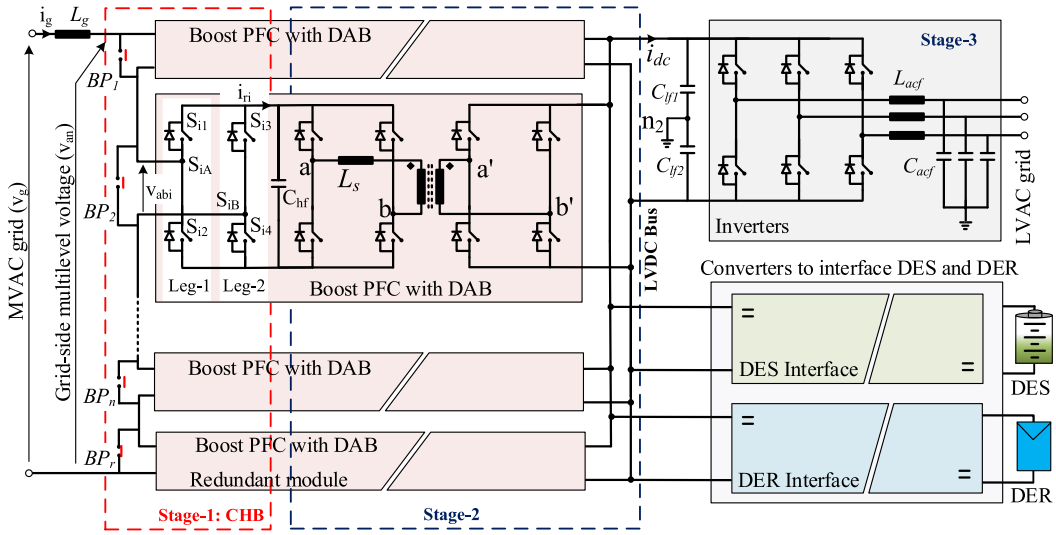

Fig. 2. Three-stage cascaded modular SST for smart grid applications with distributed energy storage (DES) and distributed energy resources (DERs) integration at the LVdc bus.

(C-FDLI) [1], [16]–[21]. The H-FDLI methods use additional current and/or voltage sensors to compare the measured quantities against a threshold value, and bypass switches are triggered based on the comparison outcome [12]–[14]. Also, faults, such as shoot-through of leg, SC of switch in a module, can be detected and isolated using advanced gate drivers, which have inbuilt protection circuits [10], [15]. The H-FDLI methods are suitable to detect faults that can cause immediate and severe damage to the system. Alternatively, the C-FDLI methods are used to detect faults that are not catastrophic and requires additional processing of measurement data, e.g., OC faults of switches in a module, aging of capacitors, etc. Such computational methods use either an extracted feature (e.g., switching frequency component of the module [20]) or the estimated states of the system (e.g., the estimated line-to-neutral voltage of cascaded H-bridge (CHB) [1]) to detect and localize the faults. The C-FDLI methods are classified as feature-based [18]–[21] and model-based [1], [16], [17], [22].

In a unipolar sinusoidal pulsewidth modulated (SPWM) H-bridge, the first switching frequency harmonic components in the pole-to-pole voltage (v_{ab_i}) appear at $2f_s$ under healthy operating conditions, where f_s is the switching frequency of H-bridge [23]. When *"n"* such H-bridges are cascaded to form a CHB MMC and modulated with phase-shifted unipolar SPWM, the effective switching frequency of grid-side multilevel voltage (v_{an}) becomes $2nf_s$. However, during OC faults in any of the switches in CHB MMC, the first switching frequency harmonic component in v_{ab_i} appears at f_s, say it is v_{hf_s}. The magnitude and phase angle of this component have been chosen as fault signatures to identify and localize an OC fault in flying capacitor multilevel configuration [18], [19] and CHB [20].

The CHB stage along with isolation stages of a three-stage SST is shown in Fig. 2. The magnitudes and phase angles of v_{hf_s} for OC faults at various switches in the CHB stage of the SST are shown in Fig. 3. As shown in the figure, v_{hf_s} for OC faults in S_1 of module-1 [see Fig. 3(b)] and S_2 of module-3 [see Fig. 3(c)] show a distinct signature compared to the healthy operation [see Fig. 3(a)]. Also, the fault signatures for faults in different modules are distinct from each other to localize the fault. However, the magnitude and phase angle of v_{hf_s} when there is an OC fault in both S_1 and S_3 simultaneously, as shown in Fig. 3(d), are similar to the healthy operation in Fig. 3(a). Such conditions occur when either both the top switches or the bottom switches fail at the same time. During the aforementioned conditions, it is impossible to identify and localize the faults using f_s component as a fault signature. In [21], a fault localization method is proposed where the carrier frequency of each module in the CHB is modified to be distinct after the fault is detected. The phase current/voltage of the CHB is screened for the carrier frequency signals to locate the faulty module. This method also fails in case of simultaneous failures in top two switches or bottom two switches in any H-bridge of CHB.

Unlike the feature-based FDLI methods, the model-based methods use the converter's mathematical model to detect any anomaly in the system. Few selected states (e.g., grid currents, capacitor voltages, etc.) of the system are continuously estimated based on the system's model and compared with the measured values. Several estimation methods, such as sliding-mode observers [24] and Kalman filter based observers [25], have been proposed to estimate the states of the converter. The error between the estimated and the measured states is used to detect and localize the faults. System residuals, which are very specific to the location of the OC faults, have been proposed to localize and isolate the fault for single-phase PWM rectifiers [17]. The maximum change in the system residuals is high enough to distinguish a fault from noise, making it less susceptible to parameter variations and measurement noise. However, the number of system residuals increases with the combination of faults, making it less applicable to MMCs. The model-based FDLI for CHB inverter with phase-shift carrier modulation has been proposed [1]. The line-to-neutral voltage of each phase is estimated using the switching sequence and dc

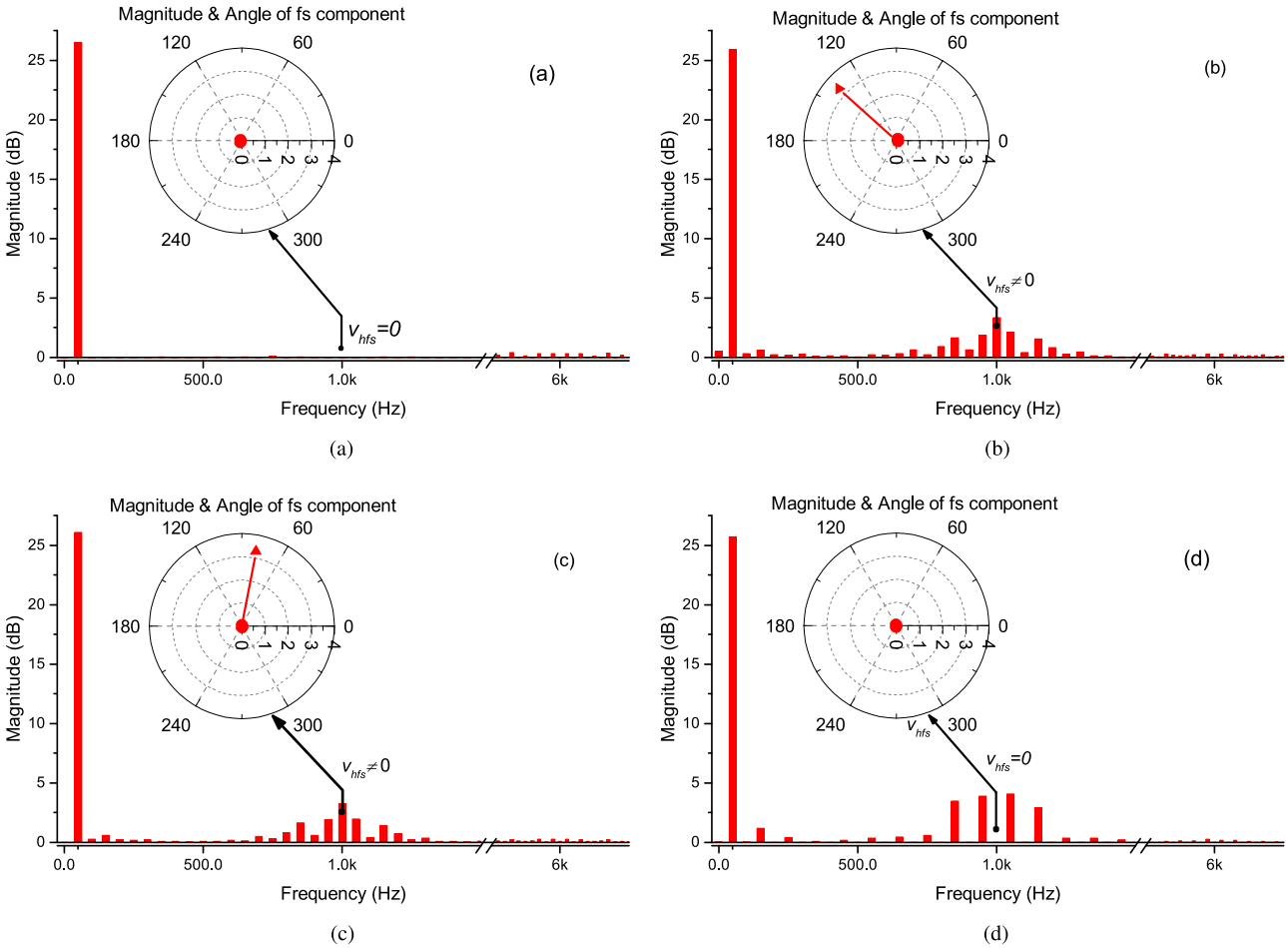

Fig. 3. Switching frequency harmonic components during OC faults at various locations in a module of CHB for OC fault detection and localization. v_{hfs} is the harmonic component at switching frequency (in this case, it is 1-kHz component) used for OC fault detection and localization. (a) Healthy/normal operation. (b) OC fault in s_1 of module-1. (c) OC fault in s_2 of module-3. (d) OC fault in s_1 and s_3 of module-1.

bus input voltages, and compared with the measured voltage. Even though the fault detection and isolation is completed in $2n$ measurement cycles (n being the number of cascaded modules) for single switch faults, faults in multiple switches in multiple modules may demand considerably high computational time. Despite the accurate fault detection and localization capability of the model-based FDLI methods, the increased computational complexity for detecting multiple faults in multiple devices is hindering their wide adaptability.

In this article, a novel model-based fault detection and localization algorithm is proposed to localize the OC faults (be it a single switch fault in a modules or multiple faults in multiple modules) in the CHB stage of an SST. Any considerable deviations in the estimated grid-side voltage of CHB from the measured voltage triggers a fault flag. Once the fault is detected, the modulation scheme is switched from phase-shifted unipolar SPWM to phase-shifted bipolar SPWM to localize the fault. Instances where only one module changes the switching state are identified. The difference in the measured grid-side voltage before and after each module's state change is calculated and fault is localized. The two key advantages of the proposed technique are that it uses only one voltage sensor for fault detection and localization, and the fault detection and localization completes in less than a line cycle irrespective of the number of faults. The rest of this article is organized as follows. The overview and control scheme of a three-stage SST are discussed in Section II. Section III outlines the operation of CHB stage of the SST under normal operating conditions as well as during faults. Section IV introduces the proposed fault detection and localization method. Experimental results illustrating the performance of the proposed scheme are presented in Section V. Finally, Section VI concludes this article.

II. Three-Stage SST

In this section, the three-stage SST, its modular nature, and control scheme are introduced.

A. Overview of SST

As shown in Fig. 2, SST is the most suitable architecture for smart grid applications as it has not only a stiff low voltage dc (LVdc) port to integrate DERs and DES, but also the ability to control real and reactive power flow at medium voltage ac (MVac) and low voltage ac (LVac) grids. Also, the energy buffer

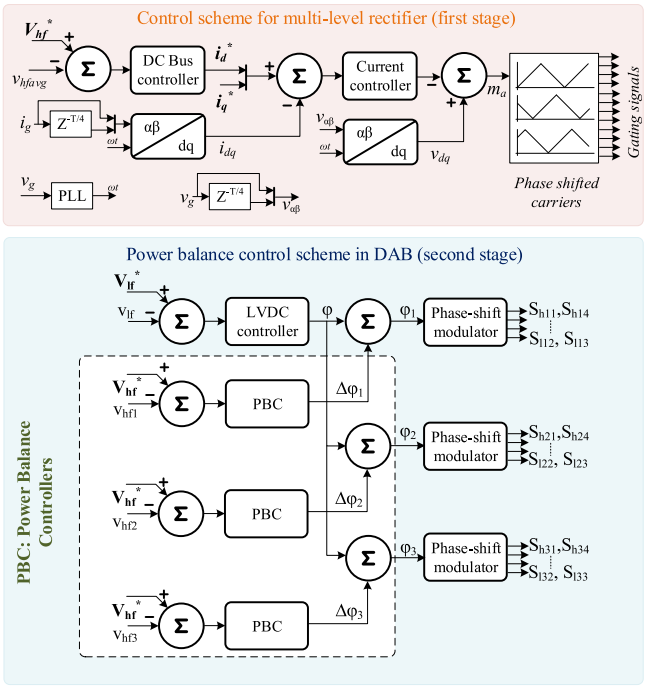

Fig. 4. Cascaded two-loop control in the first stage and single-loop voltage and power balance controllers (PBC) in the second stage.

formed by the LVdc port decouples the disturbances from MVac side on LVac side and vice versa. The SST consists of a CHB multilevel rectifier in stage-1 to regulate active and reactive power flow at the MVac grid and maintain a low grid current total harmonic distortion (THD). Each H-bridge in the CHB stage of SST is connected to a high-frequency isolated dual active bridge (DAB) dc–dc converter in stage-2. All the outputs of DABs are connected in parallel at the LVdc bus. Each DAB regulates power flow between the CHB stage and the LVdc bus. A three-phase inverter is connected to the LVdc bus either to create a regulated LVac grid or interface to an existing LVac grid. The stage-3 of the SST is omitted in the discussions from now on as it does not affect the analysis presented in this article.

B. Control Scheme for SST

The control scheme for stage-1 and -2 of the SST is shown in Fig. 4. The conventional two-loop *d-q* control scheme is used to control the CHB stage of the SST. The *"dc bus controller"* provides the *d*-axis current reference (i_d^*), whereas the *q*-axis current reference (i_q^*) is provided by the grid operator. The measured grid current is considered as α-component and the orthogonal component (β-component) is obtained by delaying the α-component by a quarter line cycle (0.25T). A phase-shifted carrier with a phase shift of $(2\pi/n)$ between each carrier is used in stage-1. Here, n is the number of cascaded modules in stage-1. Unipolar SPWM is used as the modulation scheme for stage-1 as it increases the effective switching frequency to $2nf_s$ [23], where f_s is the switching frequency of individual modules. A single-loop voltage controller implemented in stage-2 makes sure the LVdc voltage (V_{lf}) is regulated at the reference (V_{lf}^*). Even though an average dc bus voltage controller is implemented in stage-1, it does not guarantee equal dc bus voltages in practice due to parameters mismatch in stage-2 (series inductor of DAB). Therefore, as shown in Fig. 4, the PBCs are implemented in stage-2 to ensure equal dc bus voltages in stage-1. As the bandwidth of isolation stage is higher compared to stage-1, any deviations in the individual dc bus voltages are corrected immediately [26].

C. Redundancy in SST

The SST architecture is modular in nature, as shown in Fig. 2. Additional redundant modules, which are inactive during normal operation, are integrated into the architecture to improve the fault-tolerant capability. Once the fault in any module is identified and the corresponding faulty module is bypassed, it is necessary to reconfigure the system as well as control such that normal operation is restored. The redundant module is activated during the postfault restoration to resume normal operation [27]. For instance, as shown in Fig. 2, the redundant module is connected using a bypass switch BP_r. Under normal operating conditions, the bypass switch BP_r is switched ON and redundant module is bypassed. Similarly, each module is equipped with a bypass switch (BP_1, BP_2,..., BP_n) and all of them are switched OFF during normal operation

$$\mathrm{BP}_i = 0; \mathrm{BP}_r = 1$$
$$\text{where } i \in \{1, .., n\} \text{ and } r \notin i. \tag{1}$$

The redundant module ($r_1 \in r$) should be activated and brought into operation as soon as the faulty module ($f \in i$) is identified and bypassed

$$\mathrm{BP}_i = 0; \mathrm{BP}_{r_1} = 0; \mathrm{BP}_f = 1; \mathrm{BP}_{r-r_1} = 1$$
$$\text{where} i \in \{1, .., n\} \text{and} \{r - r_1, f\} \notin i. \tag{2}$$

In (1) and (2), *"i"* is the set of active modules in the SST; *"r"* is the set of inactive redundant modules; *"f"* is the set of faulty modules; and *"r_1"* is the set of redundant modules that replaces the set of faulty modules. Before going further into details of the proposed fault detection and localization algorithm, the operation of CHB stage during OC faults is studied.

III. Operation of CHB Stage of the SST

The H-bridge is the basic building block of CHB stage in an SST. To understand the operation of CHB under all conditions (normal as well as faulty operating conditions), it is necessary to thoroughly analyze the operation of H-bridge under all such scenarios. Therefore, special emphasis is given to understand the operation of H-bridge during normal operating conditions as well as operation during OC faults. The details are given below.

A. Normal Operating Conditions

The grid-side voltage and output current of the ith H-bridge in CHB stage, i.e., $[V_{abi}, I_{ri}]$ for all possible switching combinations $[s_{i1}, s_{i3}]$ are given in Table II. Under normal operating

TABLE II
GRID-SIDE VOLTAGE (V_{abi}) AND RECTIFIER OUTPUT CURRENT (I_{ri}) DEVIATIONS OF iTH H-BRIDGE UNDER VARIOUS OC FAULT CONDITIONS

ϵ	**Fault location**	$[V_{abi}, I_{ri}]$ when				**Comments**	**PBC inactive**
		$[s_{i1}, s_{i3}]$ **[0, 0]**	$[s_{i1}, s_{i3}]$ **[0, 1]**	$[s_{i1}, s_{i3}]$ **[1, 0]**	$[s_{i1}, s_{i3}]$ **[1, 1]**		
1	No fault	$[0, 0]$	$[-V_{dci}, -I_g]$	$[+V_{dci}, +I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
0		$[0, 0]$	$[-V_{dci}, +I_g]$	$[+V_{dci}, -I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
1	s_{i1}	$[0, 0]$	$[-V_{dci}, -I_g]$	$[+V_{dci}, +I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
0		$[0, 0]$	$[-V_{dci}, +I_g]$	$[0, 0]$	$[-V_{dci}, +I_g]$	C_{hfi} always charging	$V_{dci} > V_{hf}^*$
1	s_{i2}	$[+V_{dci}, +I_g]$	$[0, 0]$	$[+V_{dci}, +I_g]$	$[0, 0]$	C_{hfi} always charging	$V_{dci} > V_{hf}^*$
0		$[0, 0]$	$[-V_{dci}, +I_g]$	$[+V_{dci}, -I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
1	s_{i3}	$[0, 0]$	$[0, 0]$	$[+V_{dci}, +I_g]$	$[+V_{dci}, +I_g]$	C_{hfi} always charging	$V_{dci} > V_{hf}^*$
0		$[0, 0]$	$[-V_{dci}, +I_g]$	$[+V_{dci}, -I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
1	s_{i4}	$[0, 0]$	$[-V_{dci}, -I_g]$	$[+V_{dci}, +I_g]$	$[0, 0]$	Normal operation	$V_{dci} = V_{hf}^*$
0		$[-V_{dci}, +I_g]$	$[-V_{dci}, +I_g]$	$[0, 0]$	$[0, 0]$	C_{hfi} always charging	$V_{dci} > V_{hf}^*$

conditions, there are three modes of operation in an H-bridge, which are as follows:

(1) charging mode: $[V_{abi}, I_{ri}] = \{[+V_{dci}, +I_g]$ or $[-V_{dci}, +I_g]\}$;
(2) freewheeling mode: $[V_{abi}, I_{ri}] = [0, 0]$;
(3) discharging mode: $[V_{abi}, I_{ri}] = \{[+V_{\text{dc}i}, -I_g]$ or $[-V_{\text{dc}i}, -I_g]\}$.

The charging and discharging modes are considered as power transferring modes as power is exchanged between the input and output of the H-bridge during these intervals. On the other hand, power is circulated inside the H-bridge during freewheeling mode. Under normal operating conditions, the CHB is switched such that all the three modes are used to achieve the charge-sec balance in the output filter capacitor (C_{hfi}) in steady state. As a result, $V_{hfi} = V_{hf}^*$.

B. Operation With OC Faults

When there is an OC fault in one of the switches in the ith H-bridge of CHB (with a healthy antiparallel diode), the grid-side voltage of the faulty H-bridge (V_{abi}) and its output current (I_{ri}) depend on the direction of grid current (ϵ) and the applied switching state $[s_{i1}, s_{i3}]$. In this analysis, $\epsilon = 1$ indicates the positive direction of current (current entering into the CHB stage of SST) and $\epsilon = 0$ indicates the negative direction of current. For all possible OC fault locations in the ith H-bridge, $[V_{abi}, I_{ri}]$ is affected in two switching modes, as shown in Table II: freewheeling mode where $[s_{i1}, s_{i3}] = \{[0, 0]\text{or}[1, 1]\}$ and power transferring mode where $[s_{i1}, s_{i3}] = \{[0, 1]\text{or}[1, 0]\}$. These changes are summarized as follows.

(1) The discharging modes $[V_{abi}, I_{ri}] = \{[+V_{\text{dc}i}, -I_g]\text{or}[-V_{\text{dc}i}, -I_g]\}$ are replaced by the freewheeling mode, i.e., $[V_{abi}, I_{ri}] = [0, 0]$.
(2) The freewheeling modes $[V_{abi}, I_{ri}] = [0, 0]$ are replaced by the charging modes, i.e., $[V_{abi}, I_{ri}] = \{[+V_{\text{dc}i}, +I_g]\text{or}[-V_{\text{dc}i}, +I_g]\}$.

As a result, the faulty H-bridge in CHB operates either in the charging mode or freewheeling mode but never in the discharging mode. The mode trajectories of $[V_{abi}, I_{ri}]$ during the normal operation and OC faults are shown in Fig. 5. It can be seen clearly from this figure that the modes always transit between the charging mode and freewheeling mode, and discharging mode is completely bypassed. Therefore, for the faulty H-bridge, $V_{\text{dc}i} > V_{hf}^*$. However, due to the implementation of PBCs in stage-2, power of the DAB connected to the faulty H-bridge increases and $V_{\text{dc}i} = V_{hf}^*$ is achieved even during faults [28]–[31]. Unlike the fault detection from dc bus voltages in MMCs [25], [32], it is not possible to detect and localize faults considering the deviations in the dc bus voltages of SST with PBCs. Even though the OC faults does not cause an immediate damage to rest of the healthy network, the prolonged operation of CHB stage with faults may lead to increase in current stress on healthy devices (particularly in the isolation stage connected to the faulty module) and introduces additional harmonics in the grid currents. Therefore, it is necessary to detect and localize the faulty modules, and isolate them from rest of the healthy system to improve reliability of the system. A novel yet simple OC fault detection and localization method is presented in the next section to localize OC faults in the CHB stage of the SST within one line cycle irrespective of the number of faults. Unlike the algorithms presented in [24] and [25], the proposed method is much simple to implement and uses only one voltage sensor for measuring the grid-side multilevel voltage to detect and localize the faults.

IV. PROPOSED MODEL-BASED FDLI METHOD

The proposed method consists of two parts: fault identification and fault localization. The design details of the proposed method are given below.

A. Fault Identification

The grid-side multilevel voltage of the CHB stage of the SST is measured to identify and localize the OC faults. The error $[e_f(k)]$ between the estimated and measured grid-side multilevel voltages of the CHB stage is monitored whenever there is a change in the switching state at $(k-1)$th instant

$$e_f(k) = V_{ane}(k) - V_{anm}(k) \tag{3}$$

where $V_{ane}(k)$ and $V_{anm}(k)$ are the estimated and measured grid-side voltages of CHB stage, respectively.

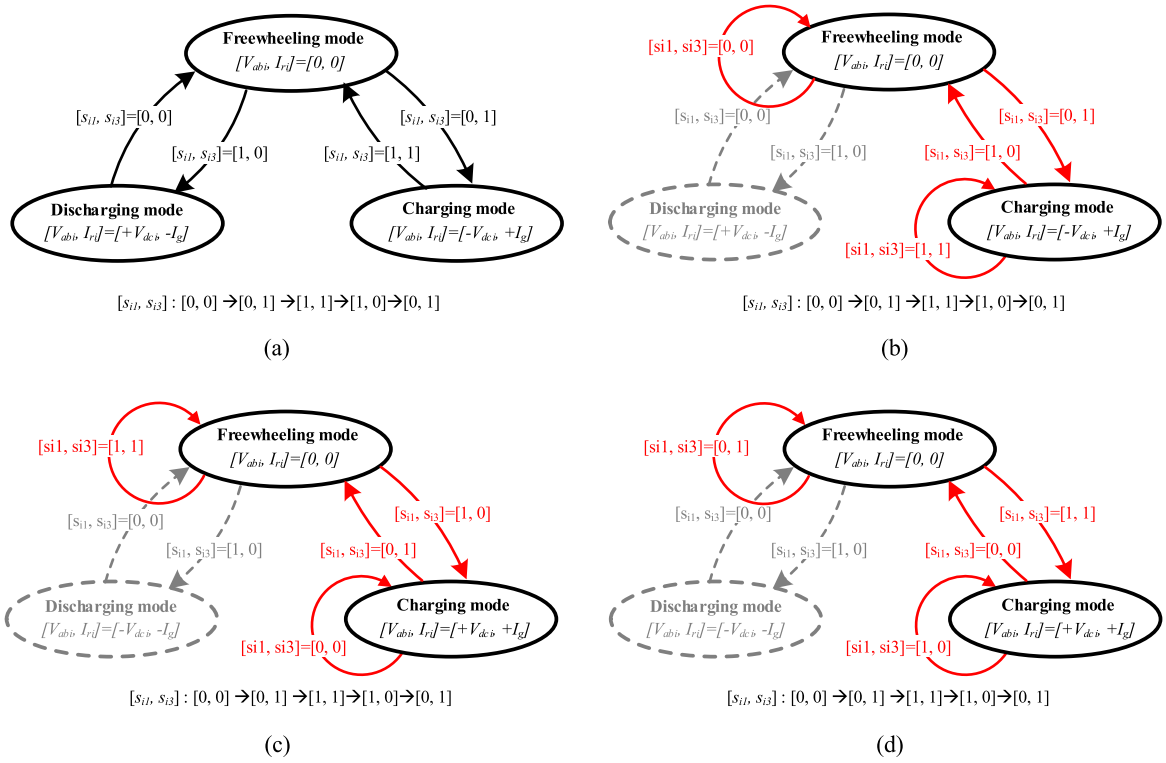

Fig. 5. Mode trajectory of $[V_{abi}, I_{ri}]$ during (a) normal operation, (b) faulty in s_{i1}, (c) faulty in s_{i2}, and (d) faulty in s_{i3} for a particular switching sequence. Mode transition is always between freewheeling mode and charging mode, and discharging mode is completely bypassed.

TABLE III
TRUTH TABLE FOR iTH H-BRIDGE IN STAGE-1 OF SST

s_{i1}	s_{i2}	s_{i3}	s_{i4}	s_{iA}		s_{iB}	
				$\epsilon=1$	$\epsilon=0$	$\epsilon=1$	$\epsilon=0$
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	0	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1

Karnaugh map for s_{iA}

	$s'_{i1}s'_{i2}$	$s'_{i1}s_{i2}$	$s_{i1}s_{i2}$	$s_{i1}s'_{i2}$
ϵ'	0	0	X	1
ϵ	1	0	X	1

Karnaugh map for s_{iB}

	$s'_{i3}s'_{i4}$	$s'_{i3}s_{i4}$	$s_{i3}s_{i4}$	$s_{i3}s'_{i4}$
ϵ'	1	0	X	1
ϵ	0	0	X	1

Note: s_{iA} and s_{iB} are the logical representation of leg-1 and -2 of ith H-bridge for various switching combinations (s_{i1}–s_{i4}).

Fault identification at one sample period (T_s) after the change in switch state minimizes the false trigger due to the measurement noise at leading edges of V_{anm} [33]. The flowchart for the proposed fault detection is shown in Fig. 6. The fault is detected when $\mid e_f(k) \mid$ is greater than a predefined threshold value (ξ_{th}). Once the fault is detected, the fault localization subroutine is triggered, as shown in Fig. 6. The design of ξ_{th} is always challenging in the model-based detection methods. Therefore, special emphasis is given for the design of ξ_{th} and calculation of V_{ane}.

1) Estimated Grid-Side Voltage (V_{ane}): The truth table for the ith H-bridge under normal operating conditions is illustrated in Table III. Given the gating signals of active devices (s_{i1}–s_{i4}), leg-1 and -2 of the ith H-bridge (see Fig. 2) are logically represented as s_{iA} and s_{iB}, respectively. The truth table for s_{iA} and s_{iB} is also depicted in Table III. In this article, Karnaugh maps are used to simplify the logic functions s_{iA} and s_{iB} as they are much quicker and easier compared to Boolean algebra [34]. For obtaining the expression for s_{iA}, the green and blue cells in Table III are grouped as $\epsilon s'_{i2}$, and the blue and orange cells are grouped to obtain $s_{i1}s'_{i2}$. Similarly, the expression for s_{iB} is obtained

$$s_{iA} = s'_{i2}(\epsilon + s_{i1}); s_{iB} = s'_{i4}(\epsilon' + s_{i3}) \tag{4}$$

where s_{i1}, s_{i2}, s_{i3}, and s_{i4} are the gating signals for switches S_{i1}, S_{i2}, S_{i3}, and S_{i4} of the ith H-bridge, respectively; s'_{i1}, s'_{i2}, s'_{i3}, and s'_{i4} are the complementary logic signals to s_{i1}, s_{i2}, s_{i3}, and s_{i4}, respectively. Similarly, ϵ' is a complementary logic signal to ϵ.

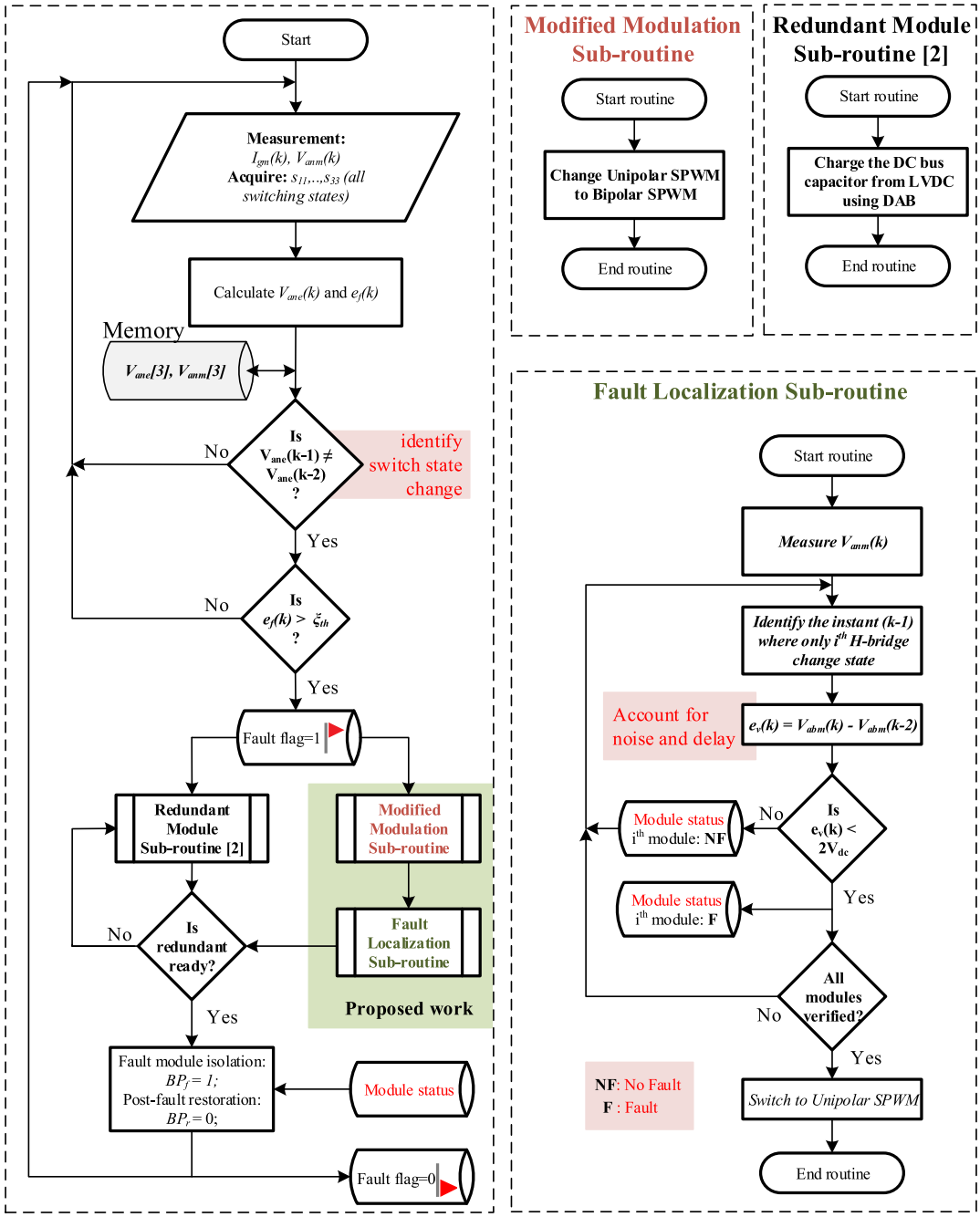

Fig. 6. Flowchart for the proposed fault detection and localization of an OC fault in the CHB stage of SST with detailed sub-routines.

The estimated grid-side multilevel voltage of the CHB is given as follows:

$$V_{ane} = \sum_{i=1}^{n} V_{abi} = \sum_{i=1}^{n} (s_{iA} - s_{iB}) V_{hfi} \tag{5}$$

where V_{hfi} is the dc bus voltage of the ith H-bridge.

2) Design of Error Threshold (ξ_{th}): As shown in Table II and Fig. 5, the absolute value of difference between the healthy operation (no fault case) and faulty operation is V_{hfi} when a faulty switch is involved. Considering the conduction of healthy antiparallel diodes of the faulty switches, the error threshold can be set as

$$\xi_{\text{th}} = V_{hf} - 2V_d \tag{6}$$

where V_d is the conduction drop in the antiparallel diodes.

B. Fault Localization

To localize fault in the CHB stage of the SST, a novel fault localization algorithm is proposed in this article. Once fault is detected, the modulation scheme is switched from unipolar

TABLE IV
POLE-TO-POLE VARIATION OF iTH H-BRIDGE (V_{abi}) IN CHB WITH UNIPOLAR AND BIPOLAR SPWM ($\epsilon = 1$ REPRESENTS POSITIVE DIRECTION OF CURRENT AND $\epsilon = 0$ REPRESENTS NEGATIVE DIRECTION)

ϵ	**Fault location**	**Unipolar SPWM** [V_{abi}, I_{ri}]				**Bipolar SPWM** [V_{abi}, I_{ri}]	
		[s_{i1}, s_{i3}] **[0, 0]**	[s_{i1}, s_{i3}] **[0, 1]**	[s_{i1}, s_{i3}] **[1, 0]**	[s_{i1}, s_{i3}] **[1, 1]**	[s_{i1}, s_{i3}] **[1, 0]**	[s_{i1}, s_{i3}] **[0, 1]**
1	No fault	[0, 0]	[$-V_{dci}$, $-I_g$]	[$+V_{dci}$, $+I_g$]	[0, 0]	[$+V_{dci}$, $+I_g$]	[$-V_{dci}$, $-I_g$]
0		[0, 0]	[$-V_{dci}$, $+I_g$]	[$+V_{dci}$, $-I_g$]	[0, 0]	[V_{dci}, $-I_g$]	[$-V_{dci}$, $+I_g$]

SPWM to bipolar SPWM without changing the carrier phase shift between the H-bridges of the CHB. The key advantage of bipolar SPWM over unipolar SPWM during fault localization is that the number of possible switching combinations in bipolar SPWM is only two, whereas it is four in unipolar SPWM, as shown in Table IV. As a result, it is required to verify only half of the switching combinations in bipolar SPWM compared to its counterpart to localize the faults. The proposed algorithm further alleviates the computational burden on the processor by screening for the switching combinations that cause the state change of one module at a time. The proposed fault localization has the following steps.

1) *Step-1:* Identify the switching instants where only one H-bridge in CHB undergoes a switching transition. Say $(k-1)$ is the instant where only ith H-bridge undergone a switching transition.
2) *Step-2:* Calculate the difference between the measured V_{an} before and after the switching transition of the ith H-bridge. To avoid false triggering due to measurement noise at the leading edge of V_{abm}, it is advisable to take the measured voltage after the transition, i.e., $V_{anm}(k)$ in this step but not during the transition [33]

$$\zeta_i = \mid (V_{anm}(k) - V_{anm}(k-2)) \mid . \tag{7}$$

3) *Step-3:* Fault in the ith module is decided based on the following logic:

$$\text{Fault flag}(i) = \begin{cases} 0, & \text{if } \zeta_i = 2V_{\text{dc}i} \\ 1, & \text{if } \zeta_i < 2V_{\text{dc}i}. \end{cases} \tag{8}$$

This procedure is repeated until all the modules in the CHB are finished. The proposed method only requires 2*n* selected switching transitions to localize *n* faults. For better understanding of the proposed fault localization procedure, a 1-*ph* three-stage SST with the specifications shown in Table V was simulated. The simulation results describing the fault localization procedure of an OC fault in S_1 of module-1 is shown in Fig. 7. The time instants T_1, T_2, T_3, T_4, and T_5 are identified as the instants where only one module changes the state. The difference between the measured V_{an} before and after these time instants is calculated to localize the fault. The following discussion illustrates the proposed fault localization procedure.

1) At $t = T_1$, S_1 and S_4 of module-3 have changed their states. The circuit configurations before and after $t = T_1$ are shown in Fig. 7(b). It can be seen from Fig. 7(a) that the value of measured V_{an} before $t = T_1$ is $-10\,500$ V, and it is equal to -3500 V after $t = T_1$. The difference between the measured V_{an} before and after $t = T_1$ is 7000 V, which is equal to $2V_{\text{dc}i}$. Therefore, module-3 is considered healthy during this transition and the corresponding fault flag is not set.
2) Switches S_1 and S_4 of module-1 have changed their states at $t = T_3$. The circuit configurations before and after $t = T_3$ are shown in Fig. 7(c). It can be seen from Fig. 7(a) that the value of measured V_{an} before $t = T_3$ is $-10\,500$ V, and it is equal to -7000 V after $t = T_3$. The difference between the measured V_{an} before and after $t = T_3$ is 3500 V, which is less than $2V_{\text{dc}i}$. Therefore, module-1 is considered faulty during this transition and the corresponding fault flag is set.
3) Similarly, S_1 and S_4 of module-2 have changed their states at $t = T_5$. The circuit configurations before and after the transition $t = T_5$ are shown in Fig. 7(d). The difference between the measured V_{an} before and after $t = T_5$ is 7000 V, which is equal to $2V_{\text{dc}i}$. According to

TABLE V
SIMULATION PARAMETERS

Parameter name	Symbol	Value
Grid voltage	V_g	6.6 kV
Grid frequency	f_g	50 Hz
Nominal power	P_n	150 kVA
Specification of stage-1		
Grid side inductor	L_g	50 mH
DC link capacitor (individual)	C_{hf}	3.3 mF
Individual DC link voltage	V_{hf}	3500 V
No. of H-bridges	n	3
No. of levels	N_l	$(2n+1)$=7
Switching frequency of each H-bridge	f_{sh}	1 kHz
Phase shift between carriers	ϕ_c	$2\pi/3$
Specification of stage-2		
Series inductor	L_s	126 μH
Switching frequency	f_{sd}	50 kHz
Filter capacitor	C_{lf}	300 μF

TABLE VI
HARDWARE PARAMETERS

Parameter name	Symbol	Value
Grid voltage	V_g	115 V
Grid frequency	f_g	50 Hz
Nominal power	P_n	1 kVA
Specification of stage-1		
Grid side inductor	L_g	5 mH
DC link capacitor (individual)	C_{hf}	3.3 mF
Individual DC link voltage	V_{hf}	55 V
No. of H-bridges	n	3
No. of levels	N_l	$(2n+1)$=7
Switching frequency of each H-bridge	f_{sh}	0.5 kHz
Phase shift between carriers	ϕ_c	$2\pi/3$
Specification of stage-2		
Series inductor	L_s	63 μH
Switching frequency	f_{sd}	100 kHz
Filter capacitor	C_{lf}	300 μF

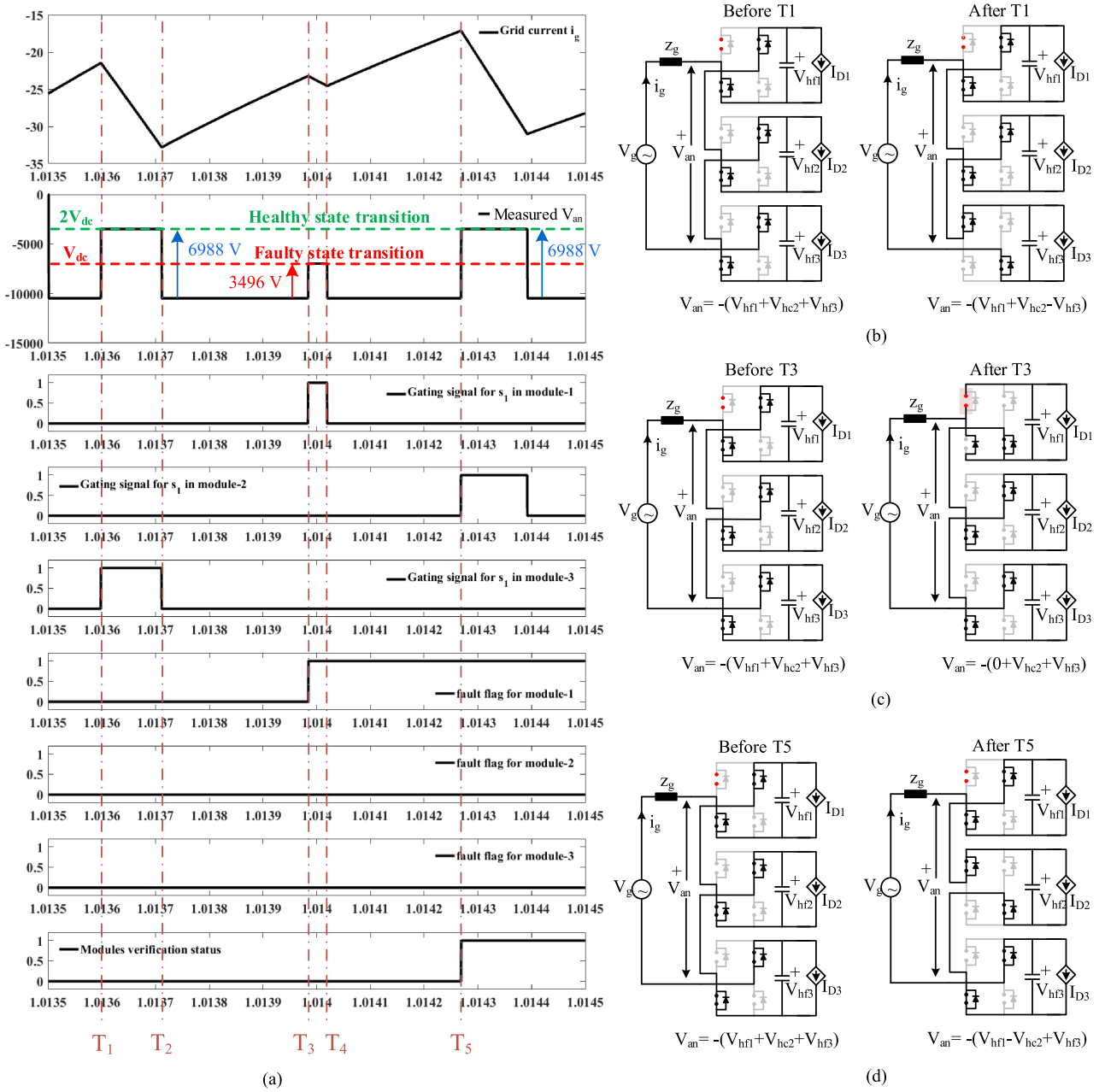

Fig. 7. (a) Simulation results illustrating the fault localization procedure for OC fault in s_1 of module-1. The circuit configurations before and after the time instances T_1, T_3,and T_5 are illustrated in (b), (c) and (d), respectively.

the proposed algorithm, module-2 is considered healthy during this transition and the corresponding fault flag is not set.

4) It should be noted here that the fault localization process has to be carried out for the entire line cycle to verify all switches as the fault localization depends on the direction of current. Similar analysis can be extended to the time instances T_2, T_4, and T_6. Once all the time instants are verified, module verification status flag will be set.

To validate the proposed model-based FDLI method, the SST with OC faults is implemented on a hardware prototype and results are presented in the next section.

V. Results and Discussion

The experimental verification of the proposed OC fault detection and localization technique is presented in this section for the specifications as highlighted in Table VI. The sensors and controllers arrangements for this experiment are illustrated in Fig. 8. The conventional two-loop *d-q* control scheme (see Fig. 4) is implemented for stage-1 in the central controller (PLECS RT box) along with the LVdc voltage controller for stage-2. The modulation indices are communicated to the local controllers (stage-1 control and stage-2 control implemented using two TMS320f28335 DSPs, as shown in Fig. 8), where switching

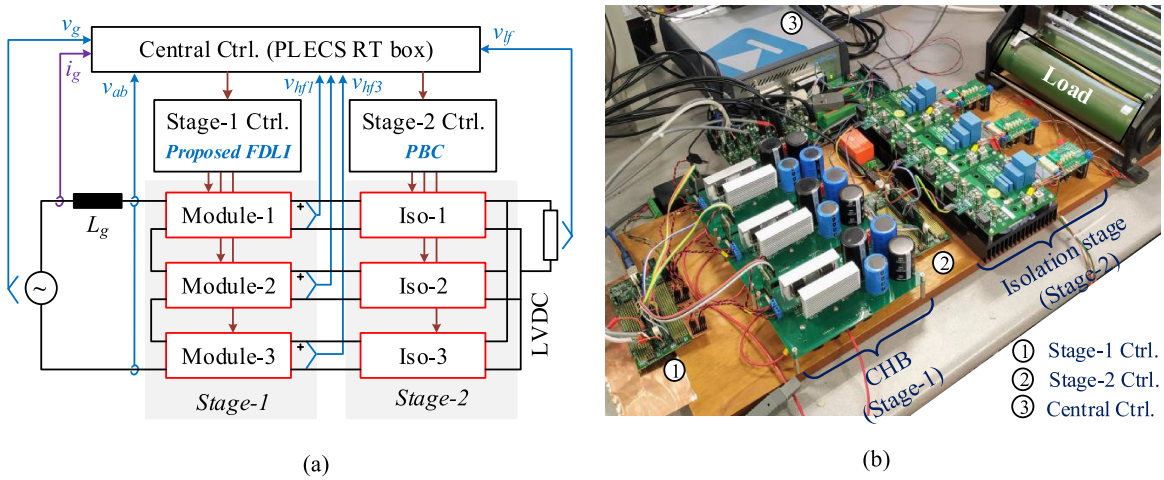

Fig. 8. Block diagram explaining the organization of laboratory test setup and actual laboratory test setup of 1-*ph* SST. Central controller is implemented in a PLECS RT box, where the conventional two-loop control scheme is implemented for stage-1 and voltage mode control is implemented for stage-2. The local controllers for stage-1 and -2 are implemented using TMS320f28335. The proposed fault detection and localization scheme is implemented in Stage-1 Ctrl. and Stage-2 Ctrl. consists of PBCs.

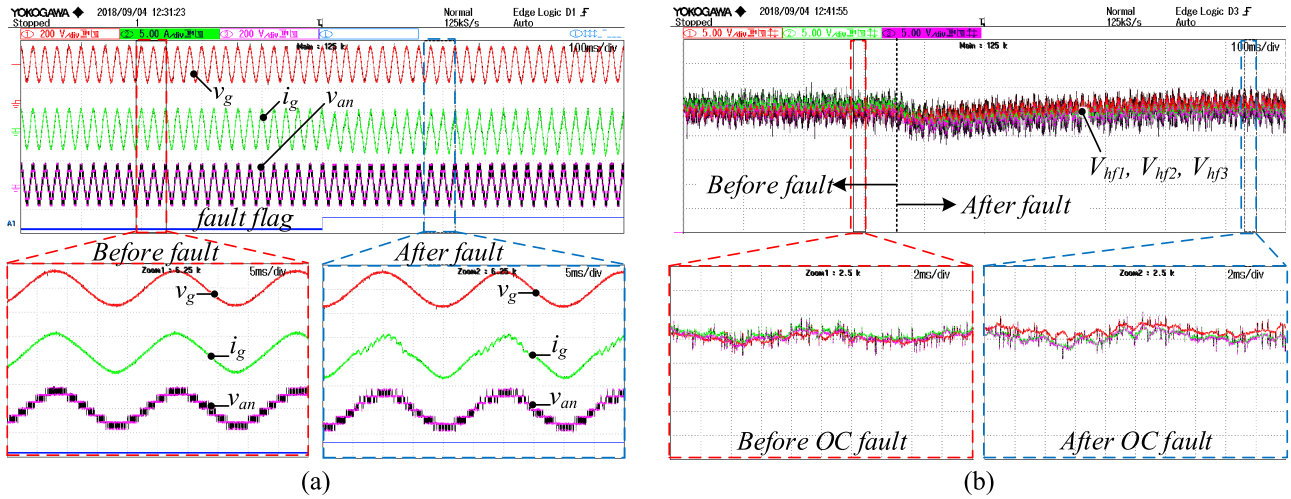

Fig. 9. Experimental results demonstrating the operation of SST controller before and after OC failures in S_3 of module-2 without activating the proposed fault localization algorithm. (a) Grid voltage (v_g), grid current (i_g), grid-side multilevel voltage (v_{ab}), and fault flag showing the instant at which OC faults are created. (b) DC bus voltages at the output of CHB stage (V_{hf1}, V_{hf2}, and V_{hf3}) before and after the fault.

signals are generated for the individual stages. The PBCs shown in Fig. 4 are implemented in stage-2 local controller, and the proposed fault detection and localization technique is implemented in stage-1 local controller. The OC faults are created in various active switches of the CHB by forcing the respective PWM signal to logic low from the stage-1 controller. To prevent the false triggering during the zero crossing of i_g due to the measurement noise, the proposed technique is implemented for the current magnitudes greater than 0.2 A. The transitions that happen during these periods are named as undetectable transitions (UTs) and are ignored for detecting the faults. Since the main focus of this article is the fault detection and localization, the postfault restoration is not shown in the presented experimental results. Unlike Lamb and Mirafzal [1], the experimental results illustrating the fault detection capability of the proposed algorithm for simultaneous multiple switch failures in addition to the single switch failures are presented. As discussed in Table II, the OC faults are detectable either in the positive or negative half cycles of i_g, depending on the location of failed switch in H-bridge. Since the fault can happen at any instant of the line cycle, the fault detection time may vary depending on the location of the OC fault. For better understanding, the faults are categorized into three: single switch faults, multiple switch faults in one module, and multiple switch faults in multiple modules. The experimental results demonstrating the detection and localization capability of the proposed algorithm for the aforementioned three cases are presented in Figs. 9–14. The detailed analysis is presented below.

Experimental results demonstrating the operation of SST during an OC fault in switch S_3 of module-2 without activating the proposed fault localization algorithm are shown in Fig. 9. Before an OC fault occurs in the CHB stage of SST, the grid

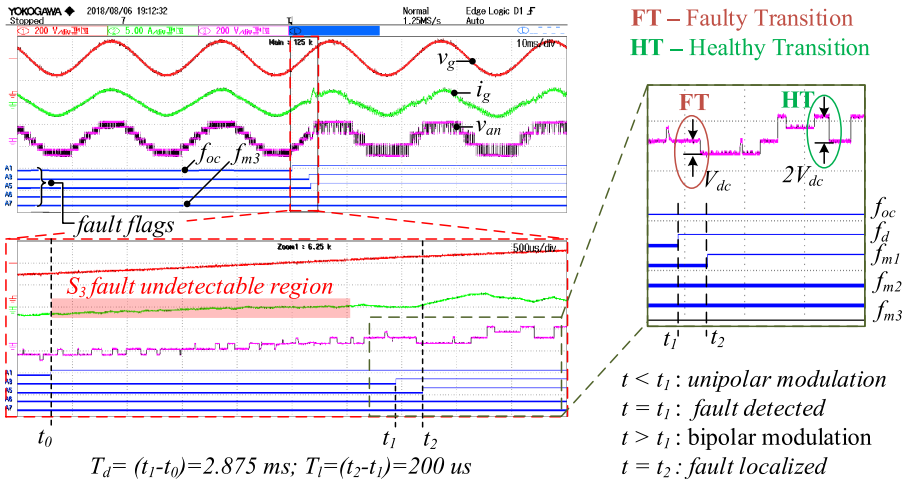

Fig. 10. Experimental results illustrating the performance of the proposed algorithm for OC failures in S_3 of module-1. Grid voltage (v_g), grid current (i_g), grid-side multilevel voltage (v_{ab}), $f_{\rm oc}$: fault flag showing the instant at which OC faults is created, f_d: fault flag showing the instant at which fault is detected, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3.

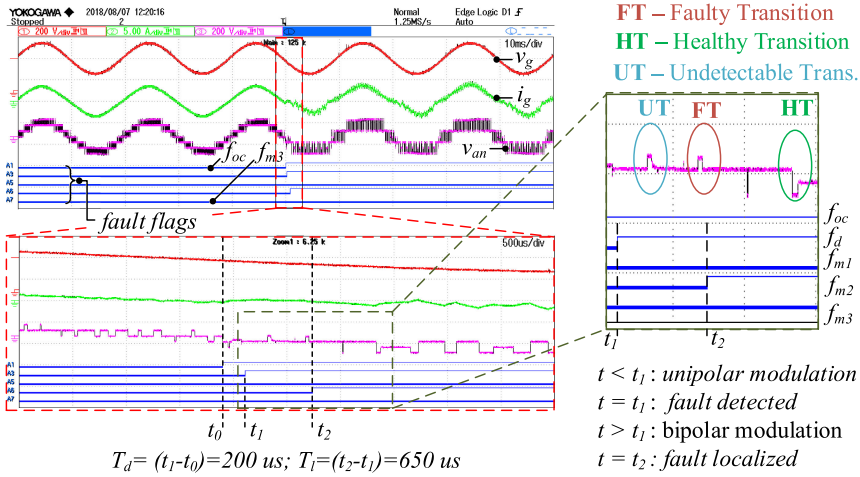

Fig. 11. Experimental results illustrating the performance of the proposed algorithm for OC failures in S_1 of module-2. $f_{\rm oc}$: OC fault flag, f_d: fault detection flag, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3.

current (i_g) is sinusoidal with a THD of 4.1%. It can be observed from this figure that the grid-side multilevel voltage (V_{an}) has abnormal switching pattern after the fault, resulting in a distorted grid current during positive half cycle. Due to the presence of power balance controllers in the isolation stage, any deviations in the individual dc bus voltages (V_{hf1}, V_{hf2}, and V_{hf3}) from their average value are corrected immediately. This can be clearly observed from Fig. 9, which substantiates the analysis presented earlier that the dc bus voltages cannot be used as fault indicators in SST with PBCs. The experimental results illustrating the performance of the proposed fault localization algorithm are presented below.

A. Single Switch Fault cases

The performance of the proposed algorithm for OC fault in switch S_3 of module-1 is shown in Fig. 10. As shown in the figure, an OC fault occurred in S_3 of module-1 in the negative half cycle of i_g at t_0. The OC fault in S_3 is not detectable in the negative half cycle of i_g due to the conduction of antiparallel diode. Therefore, it is detected in the subsequent positive half cycle of i_g at t_1. In this case, the time taken to detect the fault (T_d) is 2.875 ms. Once the fault is detected, i.e., at $t = t_1$, the modulation scheme is switched from unipolar SPWM to bipolar SPWM to localize the fault. In bipolar modulation, the grid-side voltage (v_{an}) undergoes a change of $2V_{\rm dc}$ upon each switching under normal operating conditions, which is referred to as healthy transition (HT). However, the change in v_{an} is not equal to $2V_{\rm dc}$ when the transition involves a failed switch, which is referred to as faulty transition (FT). The HT and FT in the v_{an} waveform are depicted in Fig. 10. As shown in the figure, the fault is localized by detecting the FT in v_{an} and identifying the module that triggered the change. The fault in this case is localized in module-1 at $t = t_2$, and the localization time (T_l) is 200 μs. As shown in Fig. 11, an OC fault occurred in switch S_1 of module-2 at the start of the

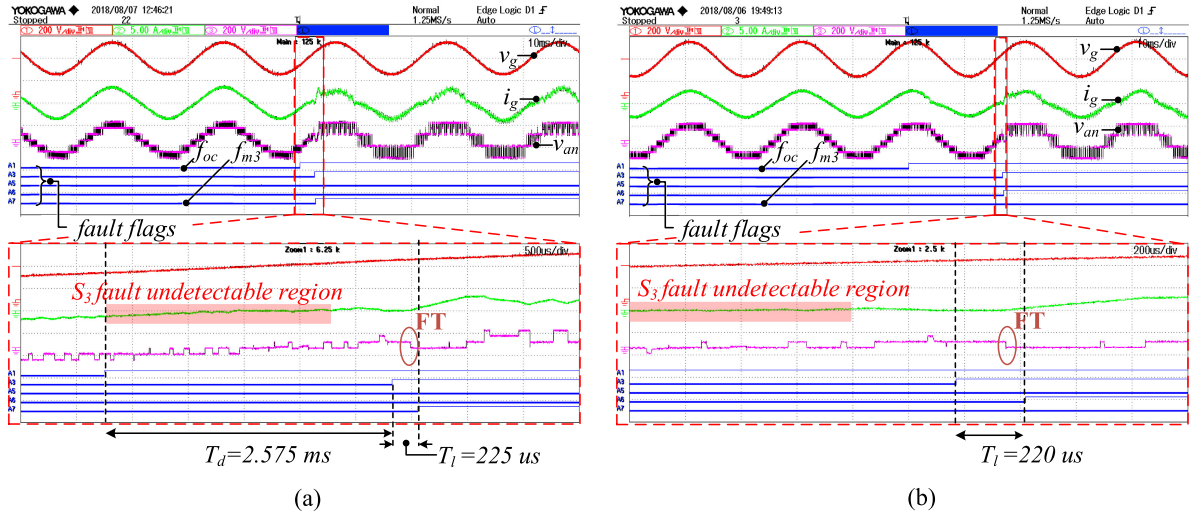

Fig. 12. Experimental results illustrating the performance of the proposed algorithm for OC failures in various modules. $f_{\rm oc}$: OC fault flag, f_d: fault detection flag, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3. (a) Fault in S_3 of module-3. (b) Fault in S_3 of module-2.

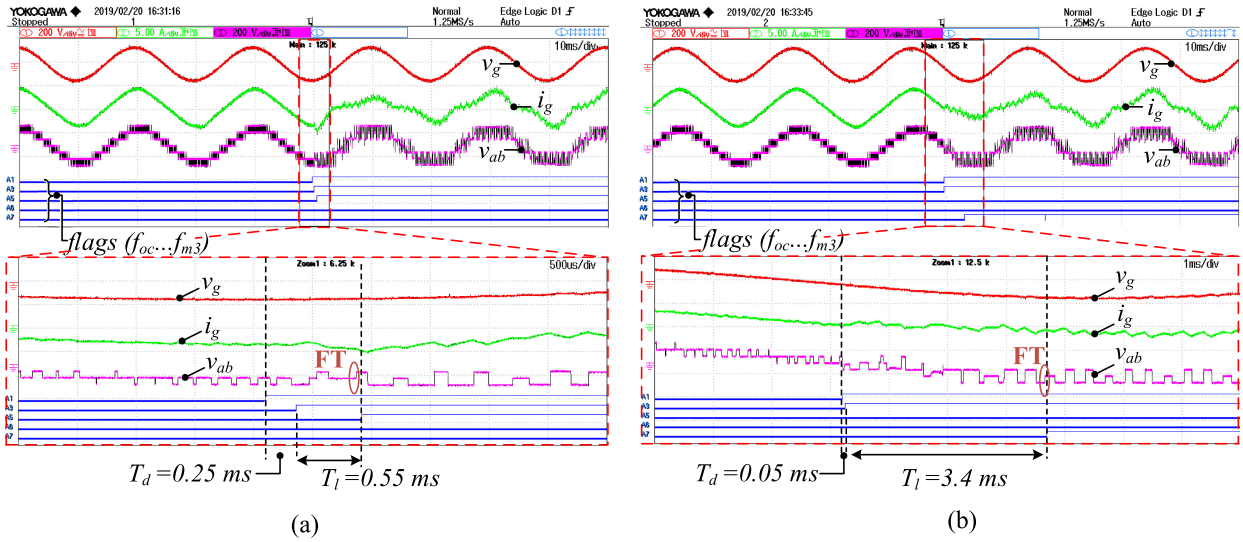

Fig. 13. Experimental results illustrating the performance of the proposed algorithm for OC failures in both the switches of same leg in various modules. $f_{\rm oc}$: OC fault flag, f_d: fault detection flag, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3. (a) Failures in switches S_3 and S_4 (leg-2) of module-1. (b) Failures in switches S_1 and S_2 (leg-1) of module-3.

negative half cycle of i_g at $t = t_0$. As mentioned in Table II, the OC fault in S_1 is detectable only during the negative half cycle of i_g. Hence, the fault is detection in 200 μs at $t = t_1$. Once the fault is detected, the modulation scheme is switched from unipolar SPWM to bipolar SPWM, and change in v_{an} at each module's switch transition is calculated. FT is detected at $t = t_2$, and the fault is localized in module-2. Similar results are presented illustrating the capability of the proposed algorithm to detect and localize the OC faults in S_3 of module-3 and S_3 of module-2 in Fig. 12. The performance of the proposed algorithm for single switch fault cases is summarized in Table VIII. The proposed algorithm yields satisfactory results in terms of detecting and localizing the single switch OC faults in stage-1 of the SST.

B. Multiple Faults in One Module Cases

A momentary over current in an H-bridge can lead to simultaneous OC faults in two switches of same leg (for, e.g., S_1 and S_2 of leg-1 or S_3 and S_4 of leg-2 in Fig. 2). To illustrate the performance of the proposed control scheme for such cases, the experimental results for OC faults in S_3 and S_4 of module-1 and S_1 and S_2 of module-3 are illustrated in Fig. 13(a) and (b), respectively. As shown in Fig. 13(a), a simultaneous OC fault in leg-2 of module-1 is detected in 250 μs and localized in additional 550 μs. Similarly, a simultaneous OC faults in leg-1 of module-3 is detected in 50 μs and localized in 3.4 ms, as shown in Fig. 13(b).

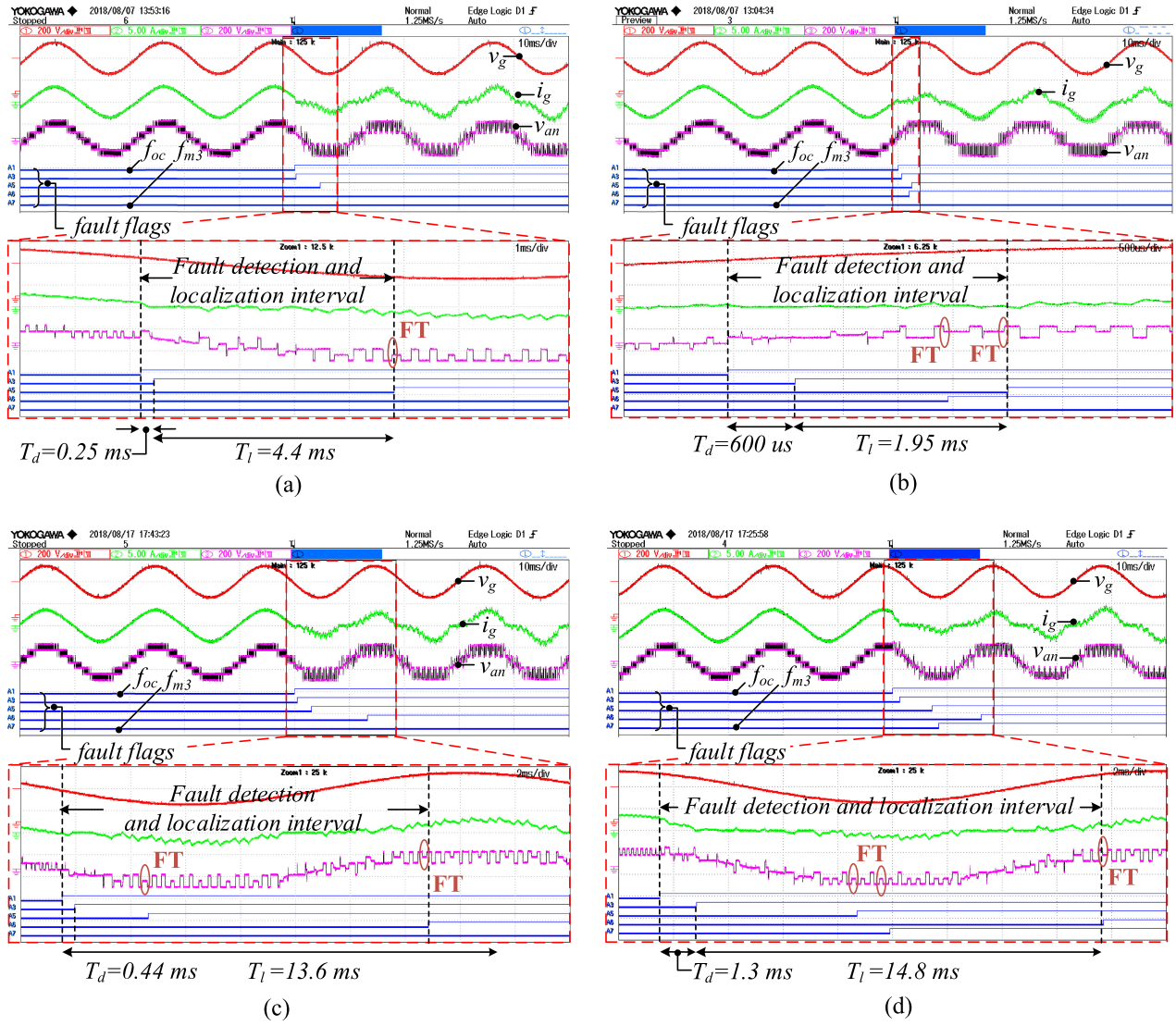

Fig. 14. Experimental results illustrating the performance of the proposed algorithm for simultaneous multiple switch failures in various modules. (a) Failure of multiple switches in a module. (b)–(d) Failure of multiple switches in multiple modules. f_{oc}: OC fault flag showing the instance at which fault occurred, f_d: fault flag depicting the instance at which fault is detected, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3. (a) Failures in switches S_1 and S_3 of module-1. (b) Failure in S_3 of module-1 and S_3 of module-2. (c) Failure in S_1 of module-1 and S_3 of module-2. (d) Failures in S_1, S_3, and S_1 of module-1, -2, and -3, respectively.

To illustrate the performance of the proposed algorithm for multiple OC faults in one module, the experimental results for simultaneous OC faults in switches S_1 and S_3 of module-1 are presented in Fig. 14(a). As shown in the figure, the simultaneous OC faults at the end of the positive half cycle of i_g is detected within 250 μs. Even though OC fault in S_1 is undetectable in the positive half cycle of i_g, OC fault in S_3 has caused the detection possible. The fault localization has completed within 4.4 ms, which is less than a quarter line cycle.

C. Multiple Faults in Multiple Modules Cases

To show the performance of the proposed algorithm for multiple faults in multiple modules cases, the experimental results for simultaneous OC faults in S_3 of module-1 and S_3 of module-2, S_1 of module-1 and S_3 of module-2, and S_1 of module-1, S_3 of module-2, and S_1 of module-3 are depicted in Fig. 14(b)–(d), respectively. Following are some of the inferences.

1) Two simultaneous OC faults in S_3 of module-1 and S_3 of module-2 at the beginning of the positive half cycle of i_g are detected within 600 μs, as shown in Fig. 14(b). After the fault is detected, the modulation scheme is switched from unipolar SPWM to bipolar SPWM to localize the fault. The localization is completed and the fault flags for module-1 and module-2 are set high in 1.95 ms. The detection and localization took less than a quarter line cycle as the fault happened in the detectable half cycle of i_g.
2) Two simultaneous OC faults in S_1 of module-1 and S_3 of module-2 at the end of the negative half cycle of i_g are detected within 440 μs, as shown in Fig. 14(c). OC fault

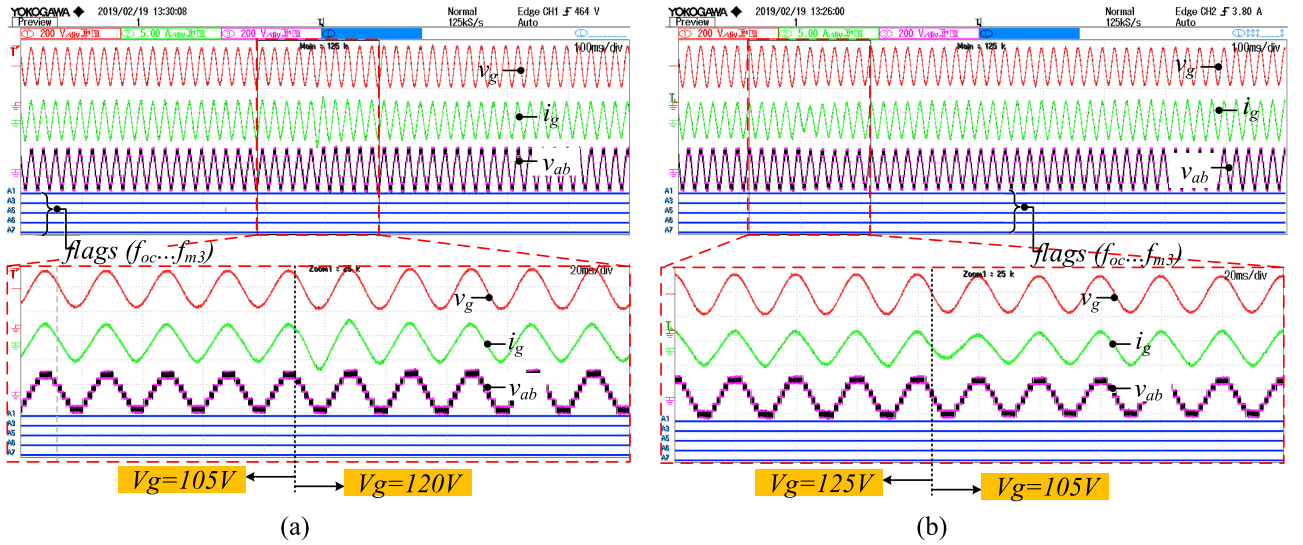

Fig. 15. Experimental results illustrating the robustness of the proposed algorithm for grid-side disturbances. (a) Step increase in grid voltage (v_g) from 105 to 120 V. (b) Step decrease in grid voltage (v_g) from 120 to 105 V. f_{oc}: OC fault flag showing the instance at which fault occurred, f_d: fault flag depicting the instance at which fault is detected, f_{m1}: fault flag for module-1, f_{m2}: fault flag for module-2, and f_{m3}: fault flag for module-3.

TABLE VII
COMPARISON OF THE PROPOSED FAULT DETECTION AND LOCALIZATION ALGORITHM WITH CONVENTIONAL METHODS PRESENTED IN THE LITERATURE

Algorithms from Literature	$(T_d + T_l)$ **for single switch faults**	$(T_d + T_l)$ **for multiple switch faults**	**Overview of method adopted & computational burden**
H. Sim et al [22], [35]	∼3 line cycles	Not possible	Slope calculations and comparison (Moderate)
K. Thantirige et al [21]	∼6 line cycles	Not possible	FFT calculation and comparison (High)
J. Lee et al [36]	∼4 line cycles	Not possible	Calculation and comparison (Moderate)
K. Thantirige et al [37]	∼5 line cycles	Not possible	Residual calculation and comparison (Moderate)
J. Lamb et al [1]	∼1.5 line cycles	Not possible	Two comparison (Low)
Proposed method	1 line cycle	1 line cycle	Two comparison (Low)

in S_1 of module-2 is localized immediately as the fault is detected in the negative half cycle of i_g itself. Since the OC fault in S_3 can be detected only in the positive half cycles, it took about 13.6 ms to localize all faults.

3) Three simultaneous OC faults in S_1 of module-1, S_3 of module-2, and S_1 of module-3 in the positive half cycle of i_g are detected in the same half cycle, as shown in Fig. 14(d). Faults in S_1 of module-1 and S_1 of module-3 are localized in the consecutive negative half cycle, and S_3 is localized in the subsequent positive half cycle.

D. Robustness of Proposed Control Scheme for Grid-Side Disturbances

To illustrate the robustness of the proposed fault detection and localization scheme, a 15% step change in the grid voltage (v_g) (both step increase and decrease) is introduced during the operation of the SST. The corresponding experimental results are illustrated in Fig. 15. It can be seen from these results that the proposed fault detection algorithm does not misstrigger an OC fault despite the external disturbances. This proves that the proposed scheme is not sensitive to the amplitude of grid voltage as the fault detection and fault localization depends only on the measured multilevel switching voltage (V_{an}) and dc bus voltages (V_{hf1}, V_{hf2}, and V_{hf3}).

E. Proposed Method Versus Conventional Methods

In this section, the proposed fault detection and localization method is compared with the conventional methods presented in the literature, and results are presented in Table VII.

The fault detection and localization time $(T_d + T_l)$ in the proposed method depend on switching frequency of the CHB stage as well as the number of modules in CHB stage. A higher switching frequency and less number of submodules result in faster fault detection and fault localization. This is in fact true in most of the computation-based FDLI schemes presented in the literature. Also, as the switching frequency of the CHB stage and number of submodules during experimentation are not standardized, various authors presented results with different switching frequencies and number of submodules in the literature. As a result, the fault detection time (T_d) and fault localization time (T_l) cannot be compared between various proposals. Therefore, the total fault detection and localization time $(T_d + T_l)$ for single and simultaneous multiple faults cases are analyzed for various algorithms presented in the literature and summarized in the Table VII.

Similarly, computational burden for various methods is compared by analyzing the fault detection and localization algorithms presented in the literature.

TABLE VIII
PERFORMANCE OF THE PROPOSED FAULT DETECTION AND LOCALIZATION TECHNIQUE FOR VARIOUS FAULTS

Fault Category	OC fault Location	Fault detection time (T_d (ms))	Fault localization time (T_l (ms))	Results	Comments
Single switch fault	S_3 of module-1	2.875	0.2	Fig. 10	Undetectable region: *2.725 ms*
	S_1 of module-2	0.2	0.65	Fig. 11	Undetectable region: *0.0 ms*
	S_3 of module-3	2.575	0.225	Fig. 12(a)	Undetectable region: *2.0 ms*
	S_3 of module-2	10.4	0.22	Fig. 12(b)	Undetectable region: *10 ms*
Multiple faults in one module	Leg-2 of module-1	0.25	0.55	Fig. 13(a)	Undetectable region: *0 ms*
	Leg-1 of module-3	0.05	3.4	Fig. 13(b)	Undetectable region: *0 ms*
	S_1, S_3 of module-1	0.6	1.95	Fig. 14(a)	Undetectable region: *0.0 ms*
Multiple faults in multiple modules	S_3 of module-1 & S_3 of module-2	0.25	4.4	Fig. 14(b)	Undetectable region: *0.0 ms*
	S_1 of module-1 & S_3 of module-2	0.44	13.6	Fig. 14(c)	Undetectable region: *0.0 ms*
	S_1 of module-1, S_3 of module-2 & S_1 of module-3	1.3	14.8	Fig. 14(d)	Undetectable region: *0.0 ms*

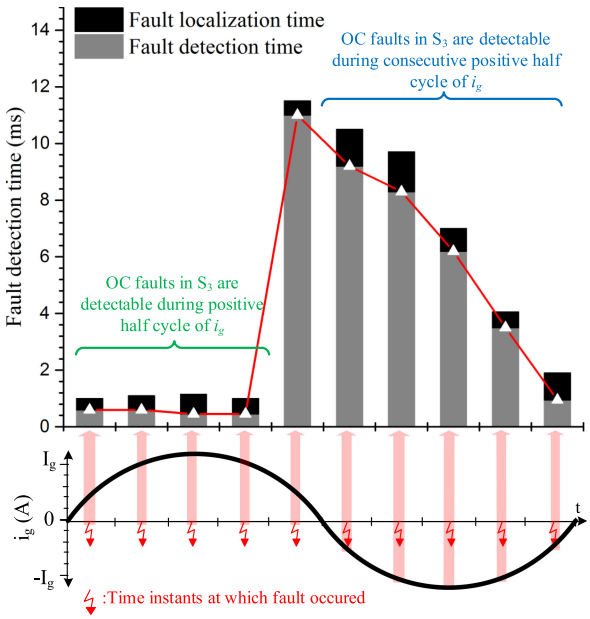

Fig. 16. Time taken for fault detection and localization for an OC fault in S_3 of module-1 at various instant of grid current (i_g). OC fault in S_3 is detectable during positive half cycle of i_g, which is evident from the detection time.

1) If the fault detection and localization is purely based on comparisons, then the computational burden is considered minimum.
2) If the fault detection and localization is based on residual calculations or rms calculations and comparisons, then the computational burden is considered moderate.
3) If the fault detection and localization is based on fast Fourier transform (FFT) or any other similar computationally intensive signal processing mechanisms, then the computational burden is considered high.

The fault detection and localization time at different instants of grid current (i_g) for an OC fault in S_3 of module-1 is shown in Fig. 16. The OC fault in S_3 is detectable during the positive half cycle of i_g. Therefore, the time taken to detect the fault in S_3 is very small in the positive half cycle of i_g compared to the negative half cycle. The maximum undetectable region in this case is 10 ms. Once the fault is detected, fault localization happens shortly. It can be seen from the presented experimental results that the proposed algorithm not only detected the single switch faults but also localized the multiple switch faults in multiple modules within a line cycle. The performance of the proposed algorithm is depicted in Table VIII. Once the faults are localized, the postfault restoration schemes discussed in [2] and [27] can be applied to isolate and restore the faulty modules. In fact, the postfault restoration scheme very specific to SSTs has been discussed in [2].

VI. CONCLUSION

A novel yet simple fault detection and localization algorithm is presented in this article to localize the OC faults in the CHB stage of an SST. Different from the single switch fault cases discussed in the literature, the results are presented for both single switch fault cases as well as simultaneous multiple switch faults in multiple modules cases to illustrate the performance of the proposed algorithm. The proposed method is designed such that it uses only one voltage sensor to measure the grid-side multilevel voltage of the CHB to detect and localize the fault. The estimated grid-side voltage of the CHB from switching signals and dc bus voltages is continuously compared with the measured voltage to detect the fault. Once the fault is detected, the modulation scheme is switched from phase-shifted unipolar SPWM to phase-shifted bipolar SPWM to localize the fault. In bipolar SPWM, the change in the grid-side voltage of CHB is always twice the dc bus voltage for every switching state change during healthy operating conditions and less than twice the dc bus voltage during FTs. Instances where only one module changes the state are identified for localizing the faults. The difference between the measured grid-side voltages of CHB before and after the module's state change is calculated and faults are localized. The experimental results from a 1-kVA SST prototype demonstrated the effectiveness of the proposed algorithm.

The main advantage of the proposed algorithm is that it requires only $2n$ comparisons to localize the faulty modules in a CHB with n H-bridges. Moreover, the fault detection and localization is completed in less than one line cycle irrespective

of the number of faults and failure modules. Also, the proposed method can be applied to both symmetric and asymmetric CHB MMCs in SST, STATCOMs, and medium-voltage motor drive applications.

REFERENCES

[1] J. Lamb and B. Mirafzal, "Open-circuit IGBT fault detection and location isolation for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4846–4856, Jun. 2017.

[2] J. Liu and N. Zhao, "Improved fault-tolerant method and control strategy based on reverse charging for the power electronic traction transformer," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2672–2682, Mar. 2018.

[3] N. B. Y. Gorla, S. Kolluri, P. J. Chauhan, and S. K. Panda, "A fault tolerant control approach for a three-stage cascaded multilevel solid state transformer," in *Proc. 18th Workshop IEEE Control Model. Power Electron.*, 2017, pp. 1–6.

[4] A. Ghazanfari and Y. A.-R. I. Mohamed, "A resilient framework for fault-tolerant operation of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2669–2678, May 2016.

[5] D. Zhou, S. Yang, and Y. Tang, "A voltage-based open-circuit fault detection and isolation approach for modular multilevel converters with model predictive control," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9866–9874, Nov. 2018.

[6] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015.

[7] B. Lu and S. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters," in *Proc. Ind. Appl. Soc. Annu. Meeting*, 2008, pp. 1–8.

[8] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters—An overview," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 507–513.

[9] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[10] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 256–263, Mar./Apr. 1995.

[11] R. Alwitt and R. Hills, "The chemistry of failure of aluminum electrolytic capacitors," *IEEE Trans. Parts, Mater., Packag.*, vol. PMP-1, no. 2, pp. 28–34, Sep. 1965.

[12] Z. Wang, X. Shi, L. M. Tolbert, F. F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[13] R. J. Patton, P. M. Frank, and R. N. Clarke, *Fault Diagnosis in Dynamic Systems: Theory and Application*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1989.

[14] L. Chen, F. Z. Peng, and D. Cao, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," in *Proc. 23rd Annu. Appl. Power Electron. Conf. Expo.*, 2018, pp. 1602–1607.

[15] D.-P. Sadik *et al.*, "Short-circuit protection circuits for silicon-carbide power transistors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, Apr. 2016.

[16] K. Mtepele, D. Campos-Delgado, A. Valdez-Fernandez, and J. Pecina-Sánchez, "Fault tolerant controller for a generalized n-level CHB multilevel converter," in *Proc. 13th Int. Conf. IEEE Power Electron.*, 2016, pp. 75–80.

[17] B. Gou, X. Ge, S. Wang, X. Feng, J. B. Kuo, and T. G. Habetler, "An open-switch fault diagnosis method for single-phase PWM rectifier using a model-based approach in high-speed railway electrical traction drive system," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3816–3826, May 2016.

[18] C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T. A. Meynard, "Fault management of multicell converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 988–997, Oct. 2002.

[19] F. Richardeau, P. Baudesson, and T. A. Meynard, "Failures-tolerance and remedial strategies of a PWM multicell inverter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 905–912, Nov. 2002.

[20] P. Lezana, R. Aguilera, and J. Rodríguez, "Fault detection on multicell converter based on output voltage frequency analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2275–2283, Jun. 2009.

[21] K. Thantirige, A. K. Rathore, S. K. Panda, S. Mukherjee, M. A. Zagrodnik, and A. K. Gupta, "An open-switch fault detection method for cascaded H-bridge multilevel inverter fed industrial drives," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 2159–2165.

[22] H.-W. Sim, J.-S. Lee, and K.-B. Lee, "Detecting open-switch faults: Using asymmetric zero-voltage switching states," *IEEE Ind. Appl. Mag.*, vol. 22, no. 2, pp. 27–37, Mar./Apr. 2016.

[23] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.

[24] S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013.

[25] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721–2732, May 2015.

[26] S. Pugliese, M. Andresen, R. Mastromauro, G. Buticchi, S. Stasi, and M. Liserre, "Voltage balancing of modular smart transformers based on dual active bridges," in *Proc. Energy Convers. Congr. Expo.*, 2017, pp. 1270–1275.

[27] A. Ghazanfari, "Control, modulation, and protection strategies for modular multilevel converters in smart ac and dc grids applications," *Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ.* Alberta, Edmonton, AB, Canada, 2017.

[28] J. Liu, J. Yang, J. Zhang, Z. Nan, and Q. Zheng, "Voltage balance control based on dual active bridge dc/dc converters in a power electronic traction transformer," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1696–1714, Feb. 2018.

[29] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1154–1166, Apr. 2011.

[30] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523–1532, Apr. 2013.

[31] B. Zhao, Q. Song, and W. Liu, "A practical solution of high-frequency-link bidirectional solid-state transformer based on advanced components in hybrid microgrid," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4587–4597, Jul. 2015.

[32] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[33] R. Poley and A. Shirsavar, "Digital peak current mode control with slope compensation using the TMS320F2803x," Texas Instruments, Dallas, TX, USA, Appl. Rep. SPRABE7A, Apr. 2012.

[34] B. Holdsworth and C. Woods, *Digital Logic Design*. Amsterdam, The Netherlands: Elsevier, 2002.

[35] H. Sim, J. Lee, and K. Lee, "A detection method for an open-switch fault in cascaded H-bridge multilevel inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 2101–2106.

[36] J. Lee, J. Lee, and K. Lee, "A fault detection method in cascaded H-bridge multilevel inverter," in *Proc. IEEE Int. Conf. Power Energy*, Nov. 2016 pp. 473–478.

[37] K. Thantirige, S. Mukherjee, M. A. Zagrodnik, C. Gajanayake, A. K. Gupta, and S. K. Panda, "Reliable detection of open-circuit faults in cascaded H-bridge multilevel inverter via current residual analysis," in *Proc. IEEE Transp. Electrific. Conf.*, Dec. 2017, pp. 1–6.

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