# A High-Efficiency Fast Transient COT Control DC–DC Buck Converter With Current Reused Current Sensor

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***Abstract*—This article presents a high-efficiency fast transient constant ON-time (COT) control dc–dc buck converter for the Internet of Things applications. The current reused current sensor is proposed to enhance the loop stability and improve the power conversion efficiency at light load. Input current is sensed and added to the feedback voltage of the dc–dc converter to increase the sensed output ripple voltage. Fast transient dc-offset cancelation technique is introduced to achieve a fast transient recovery time and to cancel the output dc offset. This chip is fabricated with a 0.13-$\mu$m CMOS process. A standard supply voltage of 7–15 V is applied to produce the output voltage of 5–5.33 V. The total die area is 2 mm $\times$ 1.5 mm. The settling time is 17 $\mu$s. The transient recovery time from light to heavy load and from heavy load to light load are 3 $\mu$s and 2.7 $\mu$s, respectively, with a maximum dc offset of 3.5 mV. The overshoot voltage is 85 mV and the undershoot voltage is 72 mV. The peak efficiency of the proposed design is 95.56% at 0.5 A and efficiency at the light load of 10 mA is 84.60%.**

***Index Terms*—Adaptive ON-time (AOT), constant ON-time (COT), current reused current sensor (CRCS), dc–dc buck converter, fast settling time, fast transient dc offset cancelation (FT-DCOC), power conversion efficiency (PCE), power management integrated circuits (PMICs).**

## I. Introduction

IN RECENT years, the Internet of Things (IoT) has emerged as a major phenomenon in portable electronics. Accordingly, power consumption has also increased rapidly in order to operate high-performance functions. Although battery time and charging technology have not followed the demand of the IoT. Power supply, battery life, and size play an important role in the efficient power management system. Due to the system demand, and the need to resolve the power necessity, the research is being carried out to improve the effective power management techniques are progressively expanding. Consequently, battery life and reduced size are essential desirabilities to increase the flexibility of the user's need [1]–[12]. Power management integrated circuits (PMICs) are not a new existence when it comes to their role to improve battery life, minimizing power consumption, and to deliver an exclusive power source to the system. The power conversion circuit is a major module of PMICs along with other switching and linear regulators. Because of the capability of high-efficiency attainment, dc–dc converters are considered as the most significant in power conversion circuits and PMICs [13]. Different kinds are used according to the users' demands, however, the primary aim is to get high efficiency, reduced size, and reduced power consumption. Likewise, different kinds of control schemes are used for different needed conditions and applications, such as current mode, voltage mode, and constant ON-time mode. Voltage mode and current mode control techniques are the earliest ones, however, they include loop compensation blocks to achieve stability which results in a large area of the fabrication chip [14]–[17].

A constant ON-time (COT) controller dc–dc buck converter has gained enormous attention in recent years because of its high light-load conversion efficiency benefits. It is very popular compared with its counterpart, i.e., current mode and voltage mode, due to its better efficiency, an easier design, a faster transient response, and a simple control mechanism. Moreover, to improve light-load efficiency issues, the constant ON-time control technique is majorly popular due to its capability to decrease the switching frequency and hence switching losses in discontinuous conduction mode (DCM). In addition to this, constant ON-time control also eliminates the necessity of the error amplifier in the circuitry and generates a pulsewidth modulation signal with a fixed ON time [12]–[19].

Fig. 1 shows the conventional COT dc–dc buck converter where Q1 and Q2 being power transistors are working as switches, $L_o$ as the output inductor, and $L_{ESL}$ is the equivalent

Manuscript received June 7, 2020; revised August 20, 2020, October 21, 2020, and December 19, 2020; accepted January 9, 2021. Date of publication January 15, 2021; date of current version May 5, 2021. This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MIST) (2020M3H2A1076786), and in part by Samsung Electronics. Recommended for publication by Associate Editor M. Chen. *(Corresponding author: Kang-Yoon Lee.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3052198.

Digital Object Identifier 10.1109/TPEL.2021.3052198

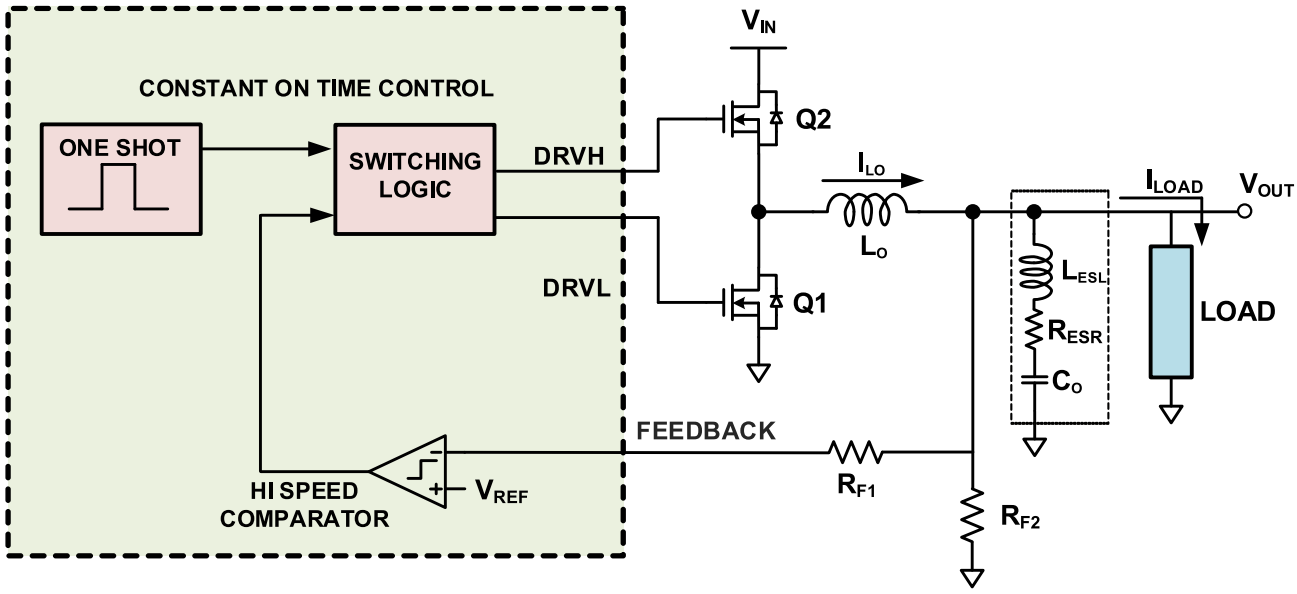


Fig. 1. Conventional COT dc–dc buck converter circuit diagram.

series inductance and $R_{\rm ESR}$ is the equivalent series resistance of the output capacitor $C_{\rm o}$. Fig. 1 indicates that inductor current ($I_{\rm LO}$) contains the information of the output voltage ripples. The current passing through the load is mentioned as $I_{\rm LOAD}$. The whole or partial feedback voltage $V_{\rm FB}$ is fed to the input of the high-speed comparator. Then, it is compared with reference voltage $V_{\rm REF}$ by the high-speed comparator. Switching logic, based on pass transistors or transmission gates will turn ON the gates of the high-side and low-side transistor switches nonsimultaneously. The constant ON-time control is very prevalent in dc–dc converters if there is a demand for high light-load efficiency due to its reduction in switching frequency and switching losses. Nonetheless, the transient response is also faster than traditional voltage mode control [2], [12]–[19].

In the conventional COT dc–dc buck converter, this control technique suffers from subharmonic oscillations and instability problems due to feedback ripple signalsthat are affected by the effective series resistance ($R_{\rm ESR}$) and effective series inductance ($L_{\rm ESL}$), in the output capacitor. The ripple of output voltage ($V_{\rm OUT}$) is changed by $L_{\rm ESL}$, $R_{\rm ESR}$, and $C_{\rm O}$. When $R_{\rm ESR}$ decreases, the $V_{\rm OUT}$ ripple voltage also decreases. If the ripple voltage is not large enough, the stability of the system will get worse. Hence, the system will be stable when $R_{\rm ESR}$ is large and will be unstable when $R_{\rm ESR}$ is small. To cater this problem, an optimum value of $R_{\rm ESR}$ should be used to get better results. Because small $R_{\rm ESR}$ led to the deterioration of sensing voltage, which in turn led to instability issues. When the ripple of voltage across resistor ESR ($V_{\rm ESR}$) decreases, the voltage across the output capacitor becomes dominant at the feedback voltage ($V_{\rm FB}$) ripple. Sub harmonics components are generated, and the COT buck converter enters into an unstable state [2], [12]–[16]. Moreover, the switching losses escalate with subharmonic oscillation as compared to without subharmonic oscillations. Although at a higher load of 20 A efficiency with and without subharmonics is equal due to conduction loss. [2], [6], [7], [12]–[16].

COT control with an additional current feedback path in conventional buck converters is proposed in [11]. The proposed techniques remove the need for large $R_{\rm ESR}$ at the output capacitor, but small $\rm R_{ESR}$ affects the output voltage accuracy, increases the recovery time, and decreases the transient response. Subsequently, stability will also be affected and will affect the operation of the processor. Different approaches have been proposed to solve the main instability problem with low-ESR capacitance for the buck converter. [11]–[16].

The usage of a virtual inductor current ripple is suggested in [2] and [10]. It improves the instability issue, but it also increases the voltage ripple effect of the ESR in the feedback. This structure improved stability, but the switching frequency is set as low as 55 kHz. An external ramp compensation design technique has been implemented in [6] to eliminate the ripple oscillation to overcome stability issues. To select the compensation ramp, proper adjustment is needed between the stability and the fast load transient response; although the drawback is the variation of the performance with a fixed compensation ramp due to widely varying input voltage and load transients.

To achieve stability, the switching frequency should be kept high. However, increasing the switching frequency increases the switching loss, hence also decreases efficiency. To ensure system stability and low cost, a technique is proposed in [13], which enhances the system stability when the multilayer ceramic capacitor (MLCC) is utilized. MLCC ensures the use of small $R_{\rm ESR}$, which reduces the output ripple and increases efficiency as compared to large $R_{\rm ESR}$. However, MLCC is large in size and has a small capacitance per volume. Moreover, its variety of quality at different temperatures is also not very optimum.

The circuit proposed in [14] is used in the feedback loop to improve stability by compensating the phase; although that

made fast transient recovery time to be challenging, which is around 25 $\mu$s. An additional current feedback loop is added to accommodate this problem where a small output voltage ripple is reduced and stability was improved with small $R_{\mathrm{ESR}}$, but then again its drawback is that the transient recovery time is degraded and offset voltage for the load is generated for current feedback [14].

Another major issue seen in the COT dc–dc converter is the fast transient recovery time. When the load shifts from the light load to heavy load, in conventional COT control technique, the feedback voltage $V_{\mathrm{FB}}$ is lower than the reference voltage $V_{\mathrm{REF}}$, due to which switching frequency increases and works only for minimum OFF time because of which $V_{\mathrm{OUT}}$ recovers quickly. In the COT control with the proposed scheme mentioned in [14], if the summation signal ($V_{\mathrm{SUM}}$), which is composed of sensed voltage ($V_{\mathrm{SEN}}$) and feedback voltage ($V_{\mathrm{FB}}$), was higher than the reference voltage ($V_{\mathrm{REF}}$) due to dc value of inductor current, the output voltage $V_{\mathrm{OUT}}$ dropped. Similarly, the response time of $V_{\mathrm{OUT}}$ is also increased. When the load shifts from heavy to light load, the situation deviates from the conventional COT control technique. Now, the feedback voltage $V_{\mathrm{FB}}$ is higher than the reference voltage $V_{\mathrm{REF}}$, due to which the switching frequency reduces and minimum OFF-time increases because of which $V_{\mathrm{OUT}}$ recovers quickly. The output voltage $V_{\mathrm{OUT}}$ is increased, but $V_{\mathrm{SUM}}$ is not in phase with $V_{\mathrm{OUT}}$ due to the dc value of the inductor current, and redundant ON-time occurs even if the load current is slightly changed.

Using the technique mentioned in [14], the difference between the inductor current and minimum dc component of the inductor current is injected into the feedback voltage. As soon as the load changes with the load detector, the inductor current is sent to the minimum dc component of the Inductor current signal, but the drawback is that feedback does not add inductor current and the valley clamper works correctly only by turning ON the switches in valley clamper when the load changes [14], [17]–[22].

The existing method adds the inductor current into the output voltage ripple, making ESR effective and large, but, it in return lead to the generation of dc and ac output voltage offsets. To avoid the output voltage offset, the waveform tracking circuit in [14] generates a difference between the inductor current and the minimum dc component of the inductor current so that only the ripple of the input current is injected into the feedback voltage. Moreover, current sensing is done through resistor and capacitor and their values must be changed according to changes in the inductor ($L$) and direct current resistance (DCR) values. In the conventional COT dc–dc converter, if the feedback voltage is lower than the reference voltage, when the load is changed from light to heavy load, OFF-time is reduced to the minimum, increasing switching frequency and making response time fast. However, the transient recovery time of the COT dc–dc converter can be increased when the load is changed from light to heavy load. [23]–[25].

Although the technique mentioned in the previous literature paper obtained by inductor current sensing increases the system stability, the output offset is reduced at the same time, but, consequently, these technique suffers from slow transient response because of the opposite trend among the inductor current and output voltage variation. Consequently, for COT buck converters, voltage-only feedback control relies on output filter capacitor ESR for stability and have subharmonic effects. With an additional current feedback path, traditionally the inductor current, the stability requirements can be relaxed, but avoiding load-dependent dc offset errors in the output voltage and achieving fast transient response are complicated.

Thus, these control techniques suffer from subharmonic oscillations and instability due to the feedback ripple signals. If the stability issues are addressed, the degradation in the performance of the fast transient response occurs. Similarly, offset of dc components is also generated by the circuits added to cater the stability issues. Thus, it is required to propose a system to cater these issues.

In the proposed design, a high efficiency fast settling COT control dc–dc buck converter with current reused current sensor (CRCS) for IoT and wide-range power applications is presented. A high-resolution CRCS is presented to sense current. The input current value is injected in the feedback voltage node to enhance the loop stability and to ensure the fast settling time. The CRCS reduces the output voltage ripple and power consumption thus increasing the power conversion efficiency (PCE). To overcome the complications of additional dc offset produced by the feedforward compensator and output voltage ripple, a fast transient dc offset cancelation block is introduced. The presented scheme increases the efficiency, has fast settling time, low dc offset value, and transient recovery time reduces the output voltage ripple, and the power consumption thus increasing the PCE.

The rest of this article is organized as follows. Section II presents the proposed architecture of the COT dc–dc buck converter. The main building blocks and their working principles are explained in Section III. The experimental results are shown and discussed in Section IV. Finally, the conclusion is summarized in Section V.

## II. Proposed Architecture of the COT DC–DC Buck Converter

Fig. 2 illustrates the top block diagram of the proposed COT dc–dc buck converter. The three main parts of the COT dc–dc buck converter are COT controller, PWR block, and power MOSFET. COT controller is composed of adaptive ON-time, minimum OFF-time, current sensor, and feedback generator with offset canceler. PWR block is composed of bandgap reference (BGR), undervoltage lock out (UVLO), low dropout voltage regulator (LDO50), high-side gate driver, and low-side gate driver, and finally the power MOSFET part is composed of two power transistors ($\mathrm{M_{NH}}$, $\mathrm{M_{NL}}$). The N-type MOS switching MOS in a synchronous buck converter structure can reduce die area compared to P-type MOS. Since the $V_{\mathrm{IN}}$ voltage can be supplied up to 5 V, the VLIMIT circuit is used to supply power to BGR and LDO by limiting the voltage above the breakdown voltage of the device. The BGR and LDO circuits supply the bias voltage to the COT dc–dc buck converter. Therefore, there is no need for an external power supply for BGR and LDO.

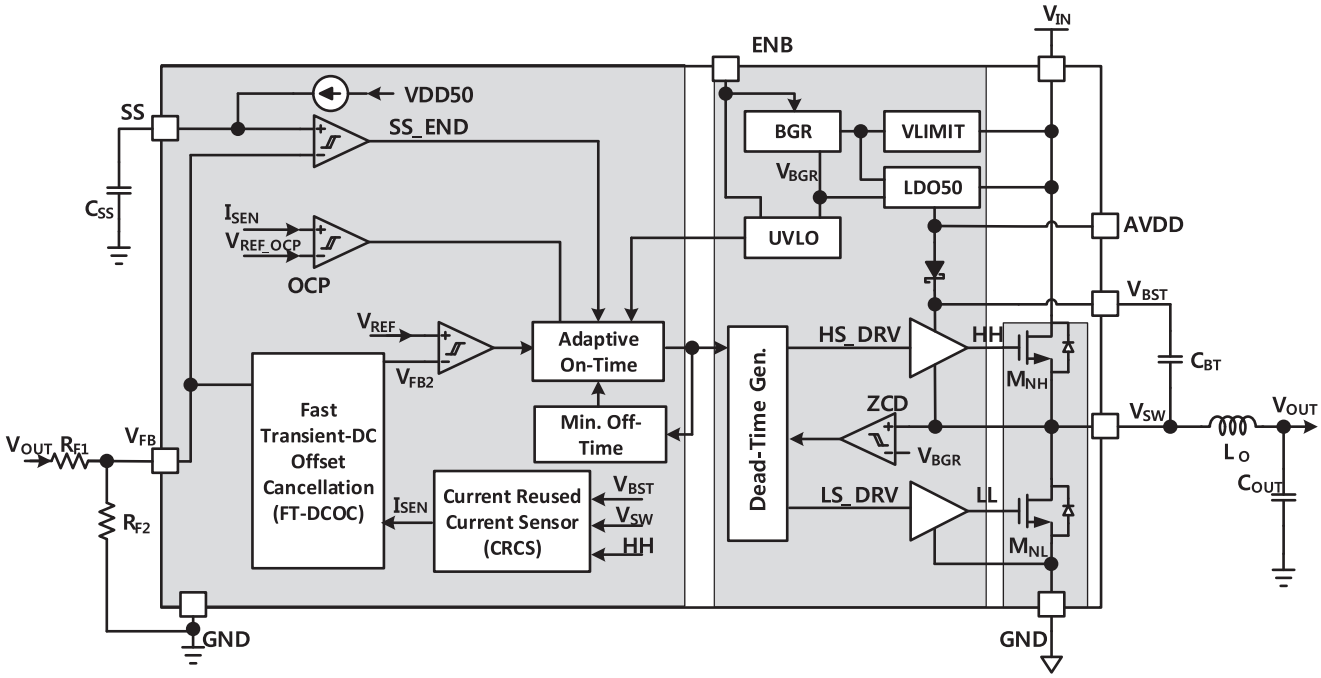


Fig. 2. Top block diagram of the proposed COT dc–dc buck converter.

In the COT control buck converter, the low-ripple output voltage $V_{\rm OUT}$ is fed back to the controller by voltage divider rule composed of $R_{\rm F1}$ and $R_{\rm F2}$. Accordingly, $V_{\rm FB}$ is smaller during the phase delay and the noise immunity is moderately lesser as compared to $V_{\rm OUT}$. The current sensor generates $I_{\rm SEN}$ based on boosted supply switch voltage ($V_{\rm BST}$), precharging switch node voltage ($V_{\rm SW}$), and high side driver (HH). Feedback Gen. with offset canceler takes $I_{\rm SEN}$ from the current sensor. $V_{\rm BST}$ is the boosted supply switch voltage. This boosted supply rail is referenced to the high side switch. The supply voltage is maintained by a bootstrap capacitor tied from the $V_{\rm BST}$ pin to the $V_{\rm SW}$ node. Minimum OFF-time operation assures that the boost capacitor is refreshed each switching cycle. COT period is generated by the comparator and adaptive ON-time (AOT) increasing the inductor current. Thus, the inductor current decreases until the updated feedback voltage ($V_{\rm FB2}$) falls below the reference voltage, $V_{\rm REF}$, or the $I_{\rm L}$ fall awaiting the OFF-time generated by the OFF-time occurs.

The CRCS is proposed to enhance the loop stability and improves the PCE at the light load. Input current ($I_{\rm IN}$) is sensed and added to the feedback voltage ($V_{\rm FB}$) of the dc–dc converter to increase the sensed output ripple voltage ($V_{\rm FB2}$). Thus, loop stability can be enhanced. It also minimizes the current consumed by the current sensor using the CRCS. Furthermore, the proposed CRCS can achieve a fast transient recovery time and cancel the output dc offset.

Meanwhile, not only the input current is detected through CRCS, but the dc value of the inductor current is also injected into the feedback voltage $V_{\rm FB}$. Consequently, there is no concern due to adding the additional current. The output dc offset value for the input current ac component occurs as much as the error between $V_{\rm FB}$ voltage and $V_{\rm REF}$.

## III. Circuit Implementation

The proposed COT dc–dc buck converter in Fig. 2 is composed of the CRCS circuit, fast transient dc offset cancelation (FT-DCOC) circuit, enhanced zero current detection (ZCD) circuit, and overcurrent protection (OCP) circuit.

### A. Current Reused Current Sensor (CRCS)

Higher power consumption is a major drawback of IoT devices with higher processing speed. To overcome this issue, current scaling becomes an effective solution to achieve improved efficiency. CRCS is used to minimize current consumption by the current sensor and thus increases efficiency with a light load. Efficiency is improved for all cases since the current is reused, especially at the high load where the sense current is a larger portion of the loss. The recycling of current has a larger impact compared to static loss sources but light load efficiency is also improved. It minimizes the current consumption by the current sensor, reuses the sense current, and scales it with the input current.

The sensed current scales with input current, which enables the recycling of less current at light load. CRCS enhances the loop stability, reduces switching frequency at light load which reduces the switching losses hence improves the PCE at light load. Likewise, the light load efficiency decreases due to switching losses, but in COT control, high efficiency at light loads can be achieved.

Fig. 3 shows the circuit diagram of the CRCS. The proposed current sensor mirrors the main current from the input voltage. When HH is low and LL is high, the input current is passed through R2 and R1. When HH is high and LL is low, the input current is passed through $M_{\rm NH}$ and then the current is discharged at precharging switch node voltage ($V_{\rm SW}$). The input current

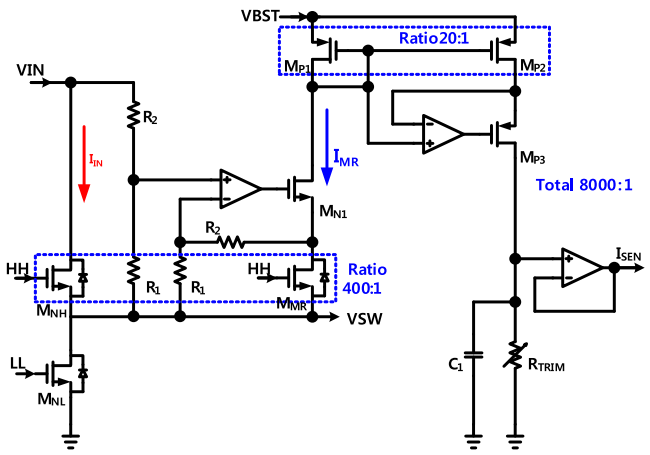


Fig. 3. Current reused current sensor (CRCS) circuit diagram.

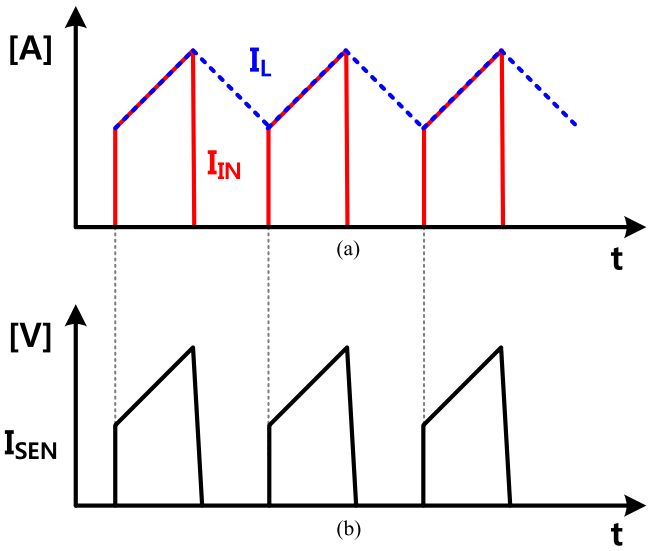


Fig. 4. Operation waveform of the CRCS circuit.

($I_{\mathrm{IN}}$) is sensed and copied to the internal current ($I_{\mathrm{MR}}$) by the current mirror composed of $\mathrm{M_{NH}}$ and $\mathrm{M_{NL}}$ with a current ratio of 400:1. The $I_{\mathrm{MR}}$ current is copied to the $I_{\mathrm{SEN}}$ current by the current mirror composed of $\mathrm{M_{P1}}$ and $\mathrm{M_{P2}}$ with a current ratio of 20:1. It is detected by mirroring $\mathrm{M_{NH}}$ (high side MOSFET) of the COT buck converter.

The $I_{\mathrm{MR}}$ current of the mirroring path is discharged at $V_{\mathrm{SW}}$ and is used again. The generated $I_{\mathrm{SEN}}$ signal is produced by detecting merely input current. The PCE of the proposed COT buck converter is improved under the light load due to the proposed CRCS since the mirroring current is reused for the output current. Conventionally, a small input current has a signal noise issue. In this condition, the resultant sense current is small, but the system does not suffer from signal noise issues due to the closely tracking of the input current. In experimental results, the wide range of input current from very low to high is used to check the limitation of the CRCS range. Moreover, the resultant sense current could become insignificant, but the current from the mirror is used again at the $V_{\mathrm{SW}}$ node. This current reusing phenomenon is a significant advantage of sensing input current.

The advantage of input current sensing over inductor current sensing is fast transient response. The inductor current sensor evaluates the ac and dc inductor current information, whereas the input current sensor estimates the ac and dc current information of the input current. The inductor current information is dependent on the DCR resistance of the inductor, which makes perfect pole–zero cancelation complicated in inductor current sensing. However, in input current sensing, reusing the current directly affects the performance of transient response and the output voltage ripple.

The improvement in efficiency is attained by the CRCS even though the output current of the buck is higher than the input current. However, the contribution seems low due to the current mirror ratio, but the current is recycled in a loop to achieve higher efficiency. For each switching cycle, the current is recycled and added to the feedback voltage of the dc–dc converter to increase the sensed output ripple voltage.

Fig. 4 shows the operation waveforms of the proposed CRCS. The sensing current $I_{\mathrm{SEN}}$ in Fig. 4(b) is following and copying the input current $I_{\mathrm{IN}}$ shown in Fig. 4(a).

### *B. Fast Transient DC Offset Cancelation*

In continuous conduction mode (CCM) the load current is positive for the whole period. In COT Control, during light load operation, the inductor current ($I_{\mathrm{L}}$) approaches zero when OFF time is sufficient enough to discharge the inductor. When the load current or inductor current falls below zero, the buck converter operates in DCM. In DCM, once the $I_{\mathrm{L}}$ reaches zero, the low side switch turns OFF while the high side switch is already OFF. Due to zero current in the inductor, the high side switch will remain OFF until output voltage reduces lower than $V_{\mathrm{REF}}$. During this stage, when both the switches are at an OFF state, the remaining charge in the output capacitor is discharged by the load current. The switching frequency will vary with load current in DCM. Due to which the output voltage ripple is composed of many different frequencies. An added dc offset is created due to the feed-forward compensator and output voltage ripple, which leads to undesirable voltage harmonics. Fast transient dc offset cancelation block is introduced to overcome the complications of additional dc offset produced by the output voltage ripple and feed-forward compensator.

The accuracy of voltage can be enhanced by eliminating the imprecise deviancy that occurred by the sensed inductor current. $V_{\mathrm{OFFSET}}$ is subtracted from $V_{\mathrm{SUM}}$ and the new feed feedback voltage $V_{\mathrm{FB2}}$ is free from any offset voltage. Fig. 5 shows the circuit diagram of the FT-DCOC block. The differential difference amplifier is modified to a differential adder. With the differential adder amplifier and two subtractors, this FT-DCOC block eliminates the dc offsets by adding components that can compensate the offset terms, thus getting the new feedback voltage $V_{\mathrm{FB2}}$, which is free of dc offsets. $V_{\mathrm{SUM}}$ voltage is obtained from the sensed voltage and feedback voltage. While $\mathrm{V_{OFFSET}}$ is generated from the feedback voltage and reference voltage. As a result, the resultant output voltage is the error due to the offset of voltage generated by $V_{\mathrm{SUM}}$ voltage. $V_{\mathrm{FB2}}$ voltage is compensated by $V_{\mathrm{SUM}}$ for error. The sensed inductor current ripple information $I_{\mathrm{SEN}}$ is inserted into the feedback to

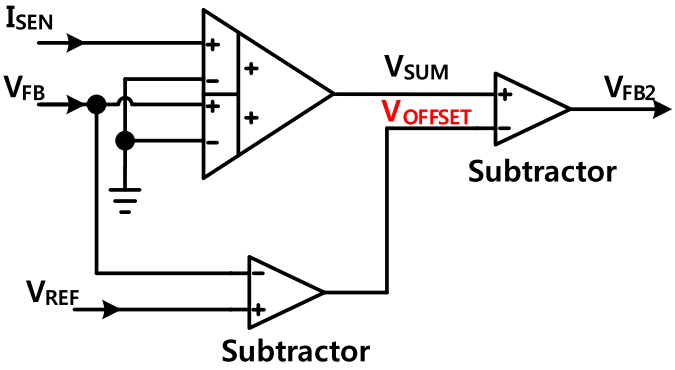


Fig. 5. Circuit diagram of the proposed FT-DCOC circuit.

overcome the stability limitations of large $R_{\mathrm{ESR}}$. Finally, the feedback voltage $V_{\mathrm{FB2}}$ is determined by comparing $V_{\mathrm{OFFSET}}$ with the summation signal voltage ($V_{\mathrm{SUM}}$) that is composed of $V_{\mathrm{FB}}$ and $I_{\mathrm{SEN}}$. As the negative pins of the four input differential adder amplifier are converted to ground, the output voltage is the sum of the positive pins input as

$$V_{SUM} = gm.Av(V_{FB} + I_{SEN}). \tag{1}$$

The resultant $V_{\mathrm{FB2}}$ signal is expressed as

$$V_{FB2} = gm.Av(V_{FB} + I_{SEN}) - V_{OFFSET} \tag{2}$$

$$V_{OFFSET} = (V_{REF} - V_{FB}). \tag{3}$$

The transient response is being slowed down by the sensed inductor current and output feedback voltage ($V_{\mathrm{FB}}$). $V_{\mathrm{FB}}$ is the feedback signal from the output voltage ($V_{\mathrm{OUT}}$) which is by the voltage divider rule is equal to

$$V_{FB} = \frac{R_{F2}}{(R_{F1} + R_{F2})} V_{OUT}. \tag{4}$$

Fig. 6 shows the operation waveforms of the FT-DCOC block for light load and heavy load. The output loads current and sensed inductor are different for light and heavy loads as shown in Fig. 6(a) and (b), respectively. After matching $V_{\mathrm{FB}}$ and $I_{\mathrm{SEN}}$, we get $V_{\mathrm{SUM}}$, which has dc offsets as shown in Fig. 6(c). Meanwhile, $V_{\mathrm{SUM}}$ is reliant on load, it results in load-dependent droop voltage. Due to the feedback voltage $V_{\mathrm{FB2}}$, the dc offset value is reduced to zero.

### C. Enhanced Zero Current Detection

Normally, for high load operation, dc–dc converters are intended to work in the CCM, but the circumstances vary when the output load current $I_{\mathrm{LOAD}}$ decreases below the inductor current $I_{\mathrm{L}}$. The reverse inductor current increases the power losses and thus DCM steps in. In DCM zero current detector (ZCD) is added for the smooth process of the light load operation. Moreover, to increase the PCE at light load and decrease the conduction loss, ZCD is majorly used in the dc–dc buck converter. The ZCD circuit delays the negative inductor current from going back to the source, which in turn reduces the rms current value. It switches OFF the low side MOSFET when the inductor current

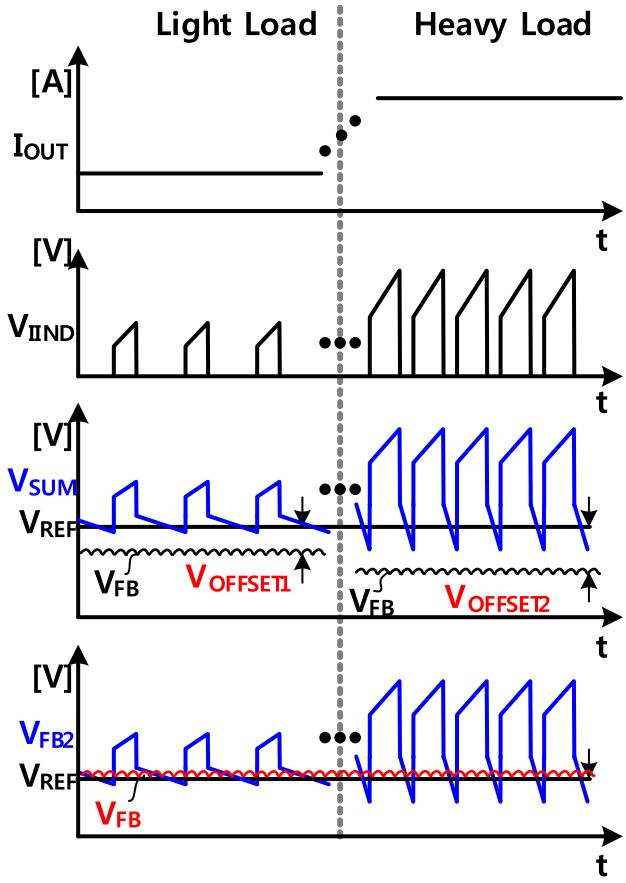


Fig. 6. Operation waveform of the proposed FT-DCOC circuit.

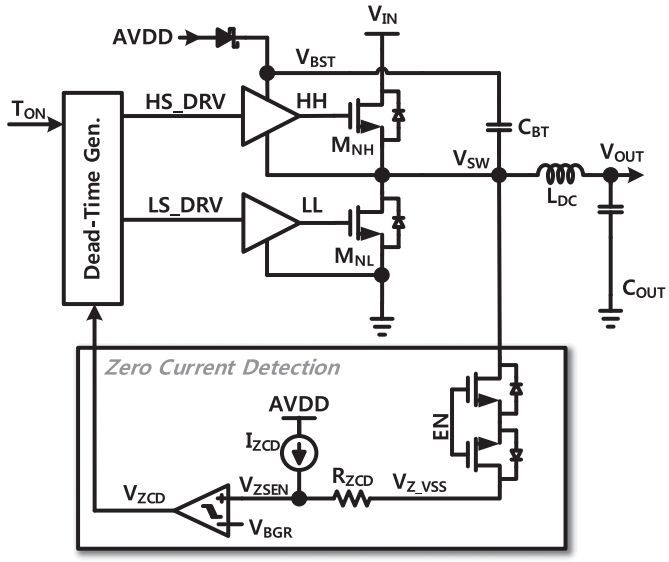


Fig. 7. Circuit diagram of the zero current detection circuit.

reverses. This stops excessive wastage of power and forces the converter into DCM.

A circuit diagram of enhanced ZCD is shown in Fig. 7. It is composed of a CMOS switch combination, $R_{\mathrm{ZCD}}$, and zero voltage comparator. The inductor current is detected at $V_{\mathrm{SW}}$. Since the inductor current is a continuous function, therefore

absolute negative current is still present in the inductor even when both power MOSFETs are turned OFF. Though, this negative inductor current is decreased by the parasitic capacitor of the power MOSFETs, this negative inductor current has to be reduced entirely from flowing back to the power source and increasing the losses. CMOS switch combination shuns the movement of the negative inductor. When the EN switch is turned ON, the switching node voltage is detected through comparator by level shifting without attenuation. As a result, the resulting expression is expressed as follows:

$$V_{ZSEN} = V_{Z\_VSS} + (I_{ZCD} * R_{ZCD}). \tag{5}$$

This zero current sensed voltage $V_{\mathrm{ZSEN}}$ is compared with reference voltage $\mathrm{V_{BGR}}$ to detect and reduce the absolute negative inductor current.

$I_{\mathrm{ZCD}}$ and $R_{\mathrm{ZCD}}$ are designed so that the bottom switch is turned OFF ahead of the zero-crossing instant by a dead-time generator. The power MOSFETs are driven by nonoverlapping gate signals generated by the dead-time generator to avoid the large shoot-through current through the power MOSFETs and short circuiting of the power source. The dead-time generator design is proposed to optimize the dead time and improve efficiency. The dead time generator block is designed by a series of inverters and capacitor bank.

The dead-time generator generated a dead time duration of 10 to 160 ns with a 10 ns step size achieved by tuning the capacitor bank through trimming bits. The inductor current ramp is detected at $V_{\mathrm{SW}}$, which produces $V_{\mathrm{ZSEN}}$ and later $V_{\mathrm{ZCD}}$. The dead time is generated from the output of the ZCD ($V_{\mathrm{ZCD}}$) and adaptive ON time. The duration of the dead time generator accuracy depends on the inductor current ramp and load current although the prediction ON dead time need not to be adaptive of input/output voltage circuit parameters due to the $T_{\mathrm{ON}}$ generated by the adaptive-ON time block.

Fig. 8 shows the operation waveforms of the proposed enhanced zero current detection circuit. The zero current is detected from $V_{\mathrm{ZSEN}}$, $V_{\mathrm{Z\cdot VSS,}}$ and $V_{\mathrm{SW}}$. Fig. 8(a) and (b) shows that the inductor has some residue current $I_{\mathrm{L}}$ even when the power MOSFET switch turns OFF. A positive voltage $V_{\mathrm{SW}}$ at the node is attained for the time period when the inductor current is increasing as revealed in Fig. 8(c). In Fig. 8(d), $V_{\mathrm{ZSEN}}$ is obtained from (3) and is following $V_{\mathrm{SW}}$. Finally, $V_{\mathrm{ZCD}}$ is detected by comparing the $V_{\mathrm{ZSEN}}$ voltage and a reference voltage $V_{\mathrm{BGR}}$ and is shown in Fig. 8(e). $V_{\mathrm{ZCD}}$ will deliver a high signal to turn OFF the power MOSFETs. ZCD circuits reduce the switching frequency and automatically adjust it in DCM according to the load and enhance the PCE at light loads.

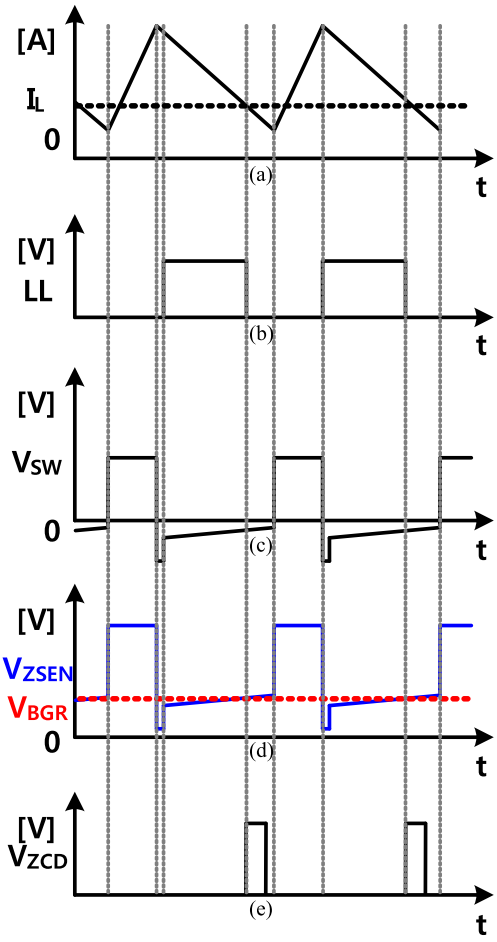


Fig. 8. Operation waveform of the zero current detection circuit.

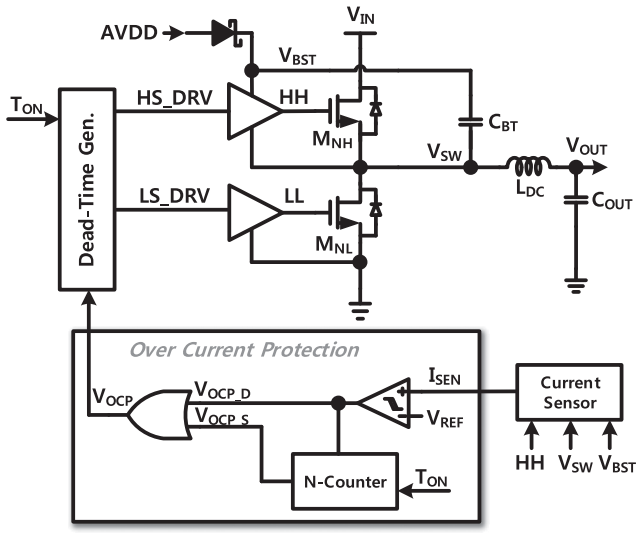


Fig. 9. Block diagram of OCP circuit.

## D. Overcurrent Protection (OCP)

High efficiency is a desirable entity of PMICs, but sometimes it led to the risk of short circuits at the load due to high current. This undesirable situation also led to huge power dissipation at the load. OCP circuit is used in such a state to get rid of the excess current problem. Fig. 9 shows the Block diagram of the OCP circuit. It will protect the output current from limiting off the range and blowing up the power supply unit. This circuit will function when the load draws a large amount of current than the specified limit. OCP is crucial to prevent the damage caused by large output current conditions. The output current is sensed by the comparator, and based on the results, the load is disconnected from the power supply.

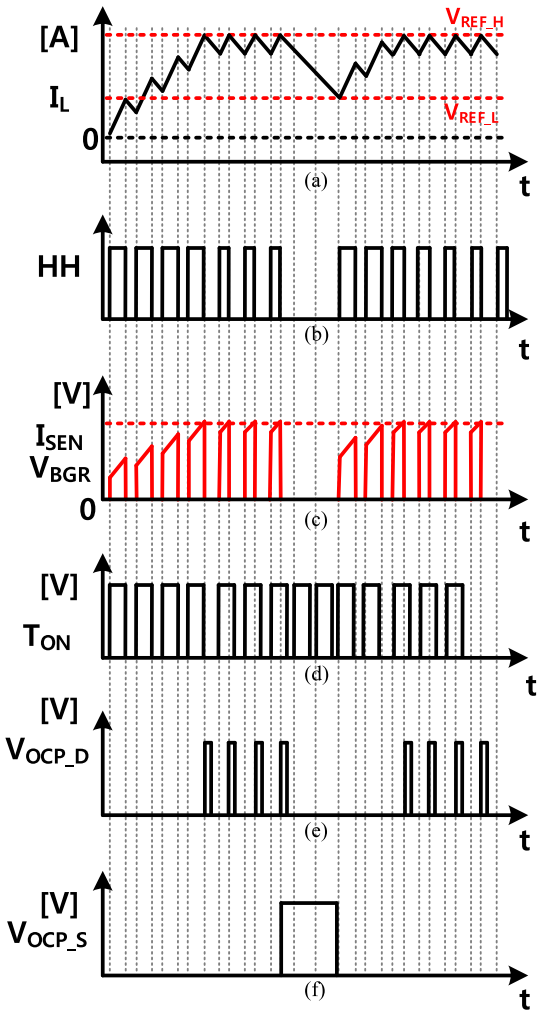


Fig. 10. Operation waveform of the overcurrent protection circuit.

TABLE I
SPECIFICATION TABLE

| | |
|---|---|
| Process | **0.13 µm** |
| Input Voltage ($V_{IN}$) | **7 ~ 15 V** |
| Output Voltage ($V_{OUT}$) | **5 ~ 5.33 V** |
| Switching Frequency ($F_{SW}$) | **2 MHz** |
| Load Current Range ($I_{LOAD}$) | **0 ~ 2 A** |
| Inductor (L) | **2.2 µH** |
| Effective Series Resistance ($R_{ESR}$) | **2 mΩ** |
| Transient (L→H, H→L) | **3 µs, 2.7 µs** |
| Offset DC | **3.5 mV** |
| Light Load Efficiency | **84.60 % @ 10 mA** |
| Peak Power Efficiency | **95.56 %** |

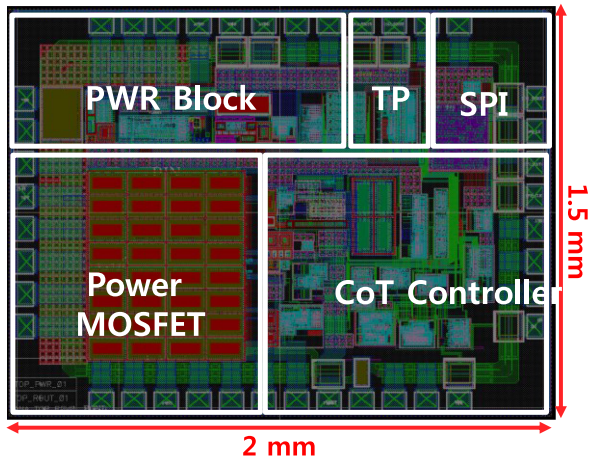


Fig. 11. Chip layout of the COT dc–dc buck converter.

In Fig. 9, the voltage at $V_{SW}$, $V_{BST}$, and HH is fed to the input of the current sensor. The current sensor detects the current and generates $I_{SEN}$, which is then compared with the reference voltage set for the overcurrent limit. If $I_{SEN}$ is less than $V_{REF}$, then the output of the op-amp will be negative. If $I_{SEN}$ is greater than $V_{REF}$, then the output of the op-amp will be positive. This positive or negative output voltage will be used to connect or disconnect the load from the power supply. If a certain number of times are repeated, then it operates in hiccup mode to perform the current limit. Fig. 10 shows the operation waveforms of the OCP circuit. Fig. 10(a) shows the inductor current $I_L$ with a higher and lower limit of reference voltage $V_{REF}$. In Fig. 10(b), high side driver voltage HH is plotted. Fig. 10(c) shows $I_{SEN}$, which is generated from the current sensor. $I_{SEN}$ is compared with $V_{REF}$ to generate $V_{OCP\_D}$. Finally, $V_{OCP}$ is generated from $V_{OCP\_S}$ and $V_{OCP\_D}$, where $V_{OCP\_D}$ and $V_{OCP\_S}$ are the outputs of the comparator and $N$ counters, respectively, as shown in Fig. 10(e) and (f). The overprotection voltage $V_{OCP}$ will be high even if one of them is high and will immediately shut OFF the high side gate disconnecting the load from the power supply.

## IV. EXPERIMENTAL RESULTS

The proposed COT dc–dc buck converter design is fabricated using a 130-nm CMOS process with a poly layer, four layers of metal, MIM capacitors, and poly resistors. The switching frequency is 2 MHz. The input voltage varies from 7 to 15 V, whereas the output generated varies from 5 to 7 V. The OFF-chip inductor and the capacitor value are set as 2.2 $\mu$H and 10 $\mu$F, respectively. Table I states the specifications of the proposed design. The performance is evaluated based on the results attained from the measurement. Fig. 11 shows the chip layout of the COT dc–dc buck converter in which the PWR block, test buffer, serial peripheral interface (SPI), power MOSFET, and COT controller blocks are shown. The active die area of the COT dc–dc buck converter is 2 mm $\times$ 1.5 mm.

Fig. 12 shows the chip microphotograph of the test board of the COT dc–dc buck converter. The 2.2-$\mu$H external inductor, resistive, and capacitive feedback components are used. SPI, supply voltage, input voltage, and output voltage pins are highlighted in the figure. The measurement setting of the COT dc–dc buck converter which consists of a test board, an SPI control PC, an oscilloscope, a power supply, and an electronic load is

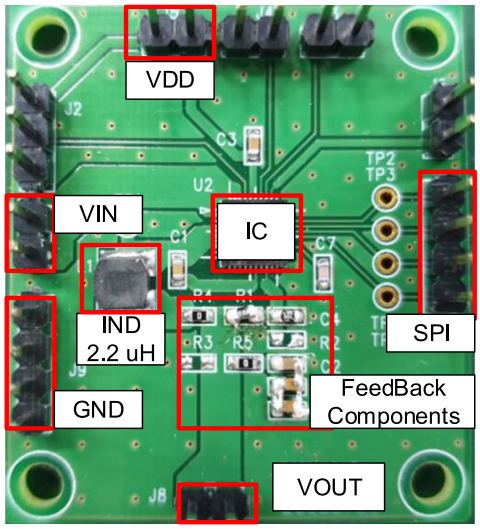


Fig. 12. Chip microphotograph of the test board of the COT dc–dc buck converter.

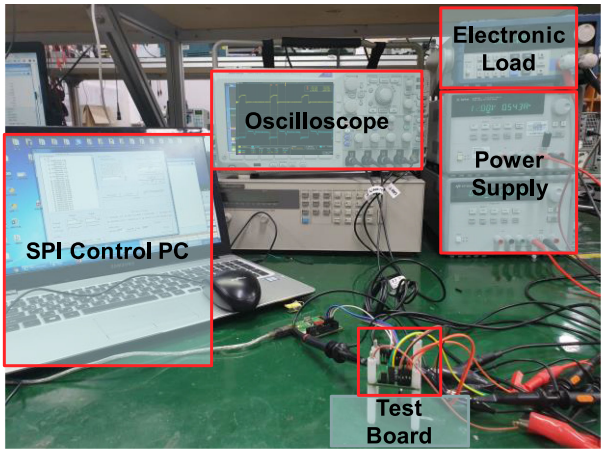


Fig. 13. Measurement environment of the COT dc–dc buck converter.

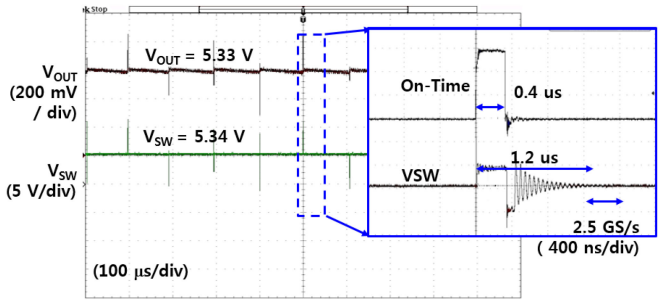


Fig. 14. Measurement results of the COT dc–dc buck converter at $I_{\mathrm{OUT}} =$ 1 mA.

demonstrated in Fig. 13. In the test board, the COT dc–dc buck converter process and regulation characteristics are measured by changing the load condition using electronic load after powering on the VIN. Likewise, the output voltage of the COT dc–dc buck converter is checked by applying a 7–15 V external power supply.

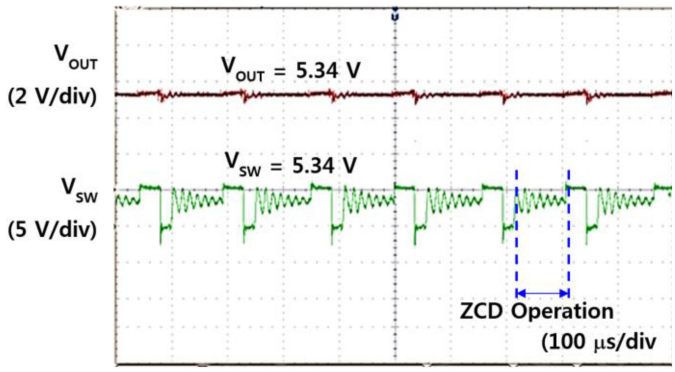


Fig. 15. Measurement results of the COT dc–dc buck converter at $I_{\mathrm{OUT}} =$ 100 mA.

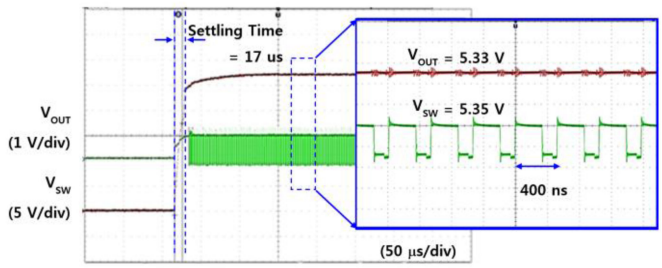


Fig. 16. Measurement results of the COT dc–dc buck converter at $I_{\mathrm{OUT}} = 1$ A.

Fig. 14 shows the experimental results for light load operation of the COT dc–dc buck converter. In Fig 14, the measured waveform has been shown for $V_{\mathrm{IN}} = 12$ V, $C_{\mathrm{OUT}} = 10$ $\mu$F, $R_{\mathrm{ESR}} = 2$ m$\Omega$, and $R_{\mathrm{LOAD}} = 5$ k$\Omega$. The output voltage of 5.33 V has been verified with $I_{\mathrm{OUT}} = 1$ mA. Conventionally, to get a stable dc–dc buck converter operation, the switching frequency should be around 10 MHz. Using the proposed COT dc–dc buck converter, the stability is attained with switching frequency as low as 2 MHz. Fig. 15 also shows the experimental results for the light load operation of the COT dc–dc buck converter. In Fig 15, the measured waveform is being shown for $V_{\mathrm{IN}} = 12$ V, $C_{\mathrm{OUT}} = 10$ $\mu$F, $R_{\mathrm{ESR}} = 2$ m$\Omega$, and $R_{\mathrm{LOAD}} = 50$ $\Omega$. The output voltage of 5.33 V has been verified with $I_{\mathrm{OUT}} = 100$ mA. Few ripples can be observed in $V_{\mathrm{OUT}}$ in Fig. 15.

The output voltage ripple occurs due to the high-frequency noise while turning ON/OFF the MOSFET switches. The output voltage ripple noise is induced due to inductor parasitic capacitance (CL) and equivalent series inductance (ESL). The inductor parasitic capacitance (CL) and equivalent series inductance (ESL) has the shortcomings of low driving capabilities and switching leakage problem. Hence, FT-DCOC block is used to remove the voltage ripple noise and distortion. Therefore, the signal from the FT-DCOC blocks the distortion from the output voltage due to which the ripples are improved. Moreover, an inductor of 2.2 $\mu$H is utilized to overcome the significant ripple in $V_{\mathrm{OUT}}$. At light loads, due to a decrease in switching frequency, high efficiency is attained. Fig. 16 shows the measured waveform results for heavy load operation of the COT dc–dc buck converter. In Fig 16, the measured waveform has been plotted for $V_{\mathrm{IN}} = 12$ V, $C_{\mathrm{OUT}} = 10$ $\mu$F, $R_{\mathrm{ESR}} = 2$ m$\Omega$, and $R_{\mathrm{LOAD}} =$

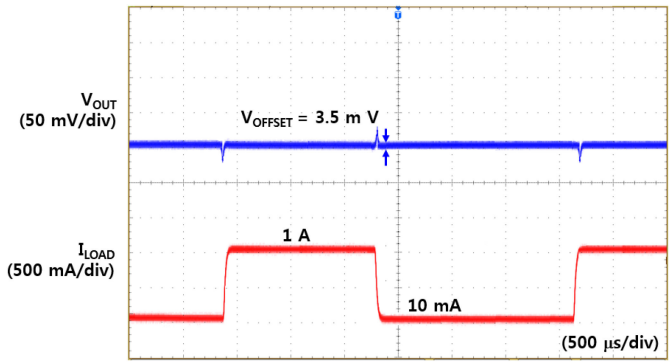


Fig. 17. Measurement waveform of the COT dc–dc buck converter with output current change with $V_{\rm IN} = 12$ V and from load current of 10 mA to 1 A and vice versa.

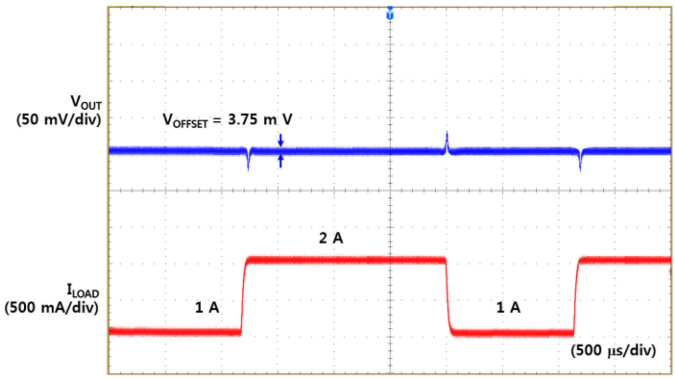


Fig. 18. Measurement waveform of the COT dc–dc buck converter with output current change with $V_{\rm IN} = 12$ V and from load current of 1 to 2 A and vice versa.

5 kΩ. The output voltage of 5 V has been verified with $I_{\rm OUT} = 1$ A. The settling time observed in measurement is 17 $\mu$s, which is attained by CRCS.

Fig. 17 shows the experimental results of COT dc–dc Buck Converter with the output load current change from high to low and low to high. $V_{\rm OFFSET}$ is observed as 3.5 mV when current is changed from 10 mA to 1 A and vice versa. In Fig. 17, the dc offset voltage of 3.5 mV is observed when the load current is increased till 1 A. Fig. 18 shows the experimental results of COT dc–dc buck converter when the output load current is changed from 1 to 2 A and vice versa. Due to the increment in load current, the dc offset voltage is dominated by sensed inductor current. Consequently, more $V_{\rm OFFSET}$ is induced in the output waveform. $V_{\rm OFFSET}$ is observed as 3.75 mV when the current is changed from 1 to 2 A and vice versa. The collective $V_{\rm OFFSET}$ from a light load of 10 mA to 2 A is 7.25 mV with a load current difference of 1.99 A.

In Fig. 19, the measured waveform has been plotted for light load of $I_{\rm OUT} = 10$ mA and $R_{\rm LOAD} = 0.5$ kΩ to heavy load of $I_{\rm OUT} = 1$ A and $R_{\rm LOAD} = 5\,\Omega$. It can be seen in the measurement results that the output of the COT dc–dc buck converter has remained stable when the load current is changed from light to heavy. During the transition of the load current from light to heavy, an undershoot voltage has been reduced to 72 mV and the transient recovery time is 3 $\mu$s in case of light to heavy load change, as shown in the figure. The undershoot voltage can be seen as a sharp peak but the output voltage is recovered within a recovery time of 3 $\mu$s. Moreover, to get a stable dc–dc buck converter operation, the switching frequency should be less than 10 MHz. The switching node voltage waveform, $V_{\rm SW} = 5.10$ V, reiterates that the stability is attained with switching frequency as low as 2 MHz using the proposed COT dc–dc buck converter. The CRCS reuses the input current and recovers the output swing. Moreover, the CRCS reduced the output voltage ripple.

Fig. 20 demonstrates the measured results of the COT dc–dc buck converter for heavy to light load. In Fig. 20, the measured waveform has been plotted for heavy load of $I_{\rm OUT} = 1$ A and $R_{\rm LOAD} = 5\ \Omega$ to the light load of $I_{\rm OUT} = 10$ mA and $R_{\rm LOAD} = 0.5$ kΩ. The overshoot voltage is 85 mV and the recovery time is 2.7 $\mu$s in case of heavy to light load change. The overshoot voltage can be seen as a sharp peak but the output voltage is recovered within a recovery time of 2.7 $\mu$s. The switching node voltage waveform, $V_{\rm SW} = 5$ V, is attained with a switching frequency of 2 MHz using the proposed COT dc–dc buck converter. The overall $V_{\rm SW}$ and $V_{\rm OUT}$ remain in the range although small peaks of few millivolts are observed during the switching node voltage. The proposed FT-DCOC technique reduces recovery time, undershoot voltage, overshoot voltage, and a dc offset value.

As this is a closed-loop system with $V_{\rm OUT}$ being fed back to the controller with feedback resistors to regulate the output voltage of the COT dc–dc buck converter for a wide range of input voltage. Subsequently, there is around +6.6% voltage regulation deviation from the nominal voltage 5 V. The voltage deviation occurs due to the slow change of input voltage and output load current. The feedback system improves the input/output impedance and bandwidth of the system hence improving the system stability. Furthermore, the COT controller parameters optimize the closed-loop system to achieve stability for the range of the input voltages. Moreover, the voltage deviation is within the range of +10% of the nominal voltage under the normal operating conditions.

Fig. 21 shows the measurement waveform of the output voltage regulation over the input voltage range. It demonstrates the wide input range regulation capability of the proposed design. The input voltage is varied from 7 to 16 V with 2-V step size in measurement. The results show that the output voltage varies from 5 to 5.33 V for a load current of 1 A. $V_{\rm OUT}$ steps up in a staircase as $V_{\rm IN}$ is changed in steps. For an input voltage change of 8 V, 330-mV change in output voltage has been observed with smooth regulation. The change in output voltage Versus input voltage is 41.25 mV/V for the wide range from $V_{\rm IN}$ 7 to 16 V. It is worth mentioning that the change in input voltage is nonuniform. Hence, the change in $V_{\rm OUT}$ increases a little as we increase the input voltages as can be seen in Fig. 20. Moreover, the change in $V_{\rm OUT}$ is gradual until $V_{\rm IN}$ approaches 14 V. An enormous change of 100 mV $V_{\rm OUT}$ is observed from $V_{\rm IN}$ 14 to 16 V due to the increase in voltage. Overall, the change in output voltage Versus input voltage is less than 50 mV/V for $V_{\rm IN}$ 7 to 14 V. Comparing it with previous work, this line regulation is

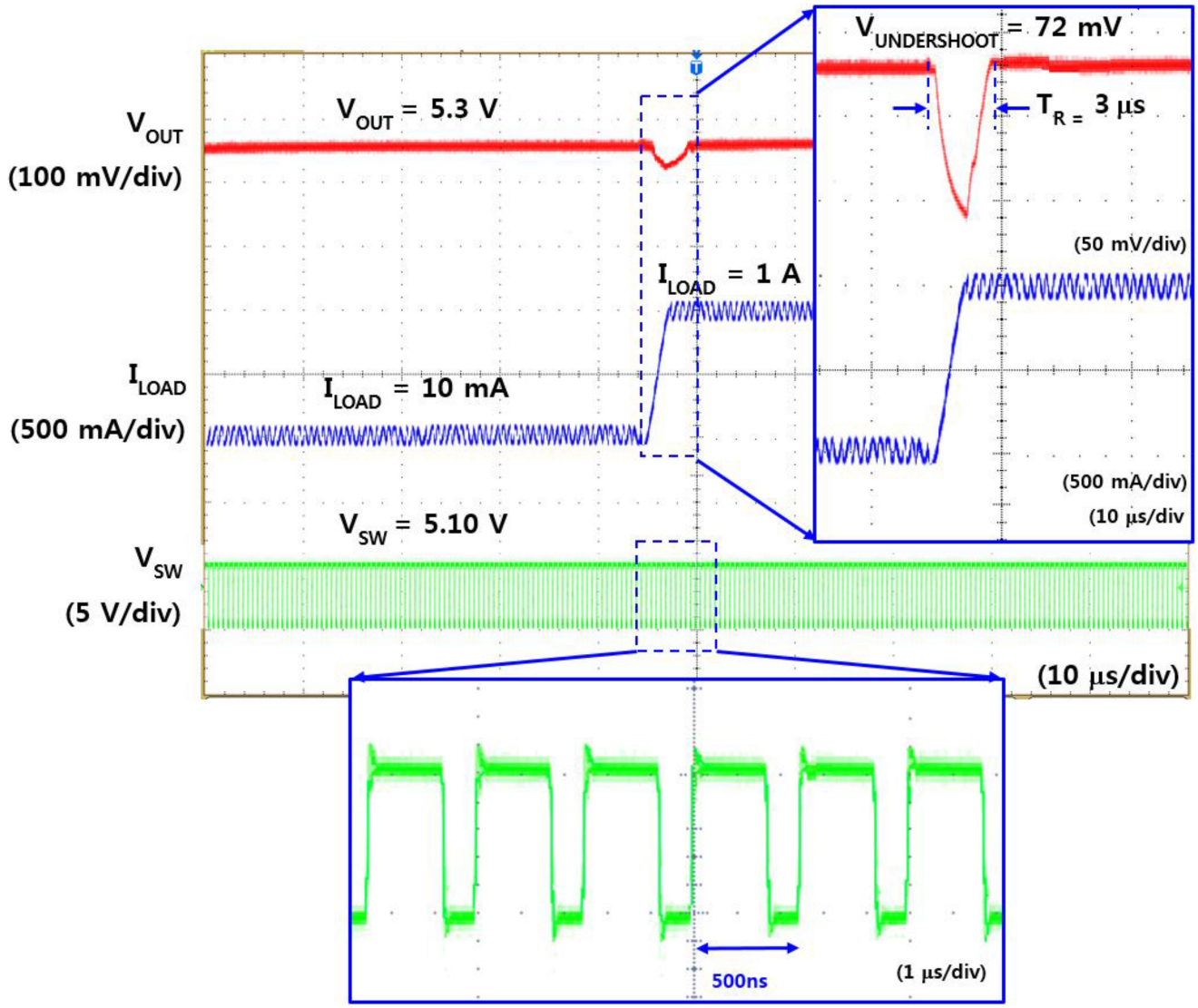


Fig. 19. Measured waveform of the COT dc–dc buck converter for light to heavy load with $V_{\mathrm{IN}} = 12$ V.

quite better and lower than the previous architectures. Moreover, the 0.33 V total output voltage change over the rated input range may seem to be concerning for some applications, but the 8 V input voltage range is wide enough to opt it for several IoT applications.

Fig. 22 shows the line regulation that is output voltage Versus input voltage between the wide range of 7–15 V at an input current of 100 mA, 500 mA, 1 A, 1.5 A, and 2 A. The measured value graph shows the output voltage to be between 5.26 and 5.398 V, 5.10 and 5.366 V, 5.02 and 5.33 V, 5.015 and 5.30 V, and 5.0 and 5.25 V for an output current of 100 mA, 500 mA, 1 A, 1.5 A, and 2 A respectively.

Fig. 23 shows the load regulation that is output voltage Versus input current between the wide ranges of 1 mA to 2 A at an input voltage of 7, 9, 12, and 15 V. The measured value graph shows the output voltage to be between 5.28 and 5, 5.331 and 5.25 V, 5.388 and 5.274 V, and 5.42 and 5.25 V for 7, 9, 12, and 15 V, respectively. It could be observed from the graph that as the input voltage is increased, the output voltage also shows some escalation as well. Though the overall output voltage range stays between the specified ranges.

The chip resistor tolerance of 0.1 to 0.2 kΩ raises the output voltage. Fig. 24 demonstrates the measured waveform of the efficiency versus load current of the COT dc–dc buck converter at the input voltage of 12 V and a switching frequency of 2 MHz. For the output voltage to be 5 V, the maximum efficiency achieved after the measurement is 95.56% at a load current of 500 mA. The light-load efficiency achieved at 10 mA is 84.6%. More than 90% of efficiency is achieved for the output load current range from 100 mA to 1.80 A

Finally, Table II demonstrates the performance comparison with previous works. This chip is fabricated with a 130-nm CMOS process. The input supply voltage range is 7–15 V and the generated output voltage is 5–5.33 V. The switching frequency is 2 MHz. The peak power efficiency is 95.56% and light load efficiency is 84.6% at 10 mA, which is attained by the CRCS. The measured efficiency of this work is highest compared with those of [10] and [13]–[16]. FT-DCOC allowed the COT control

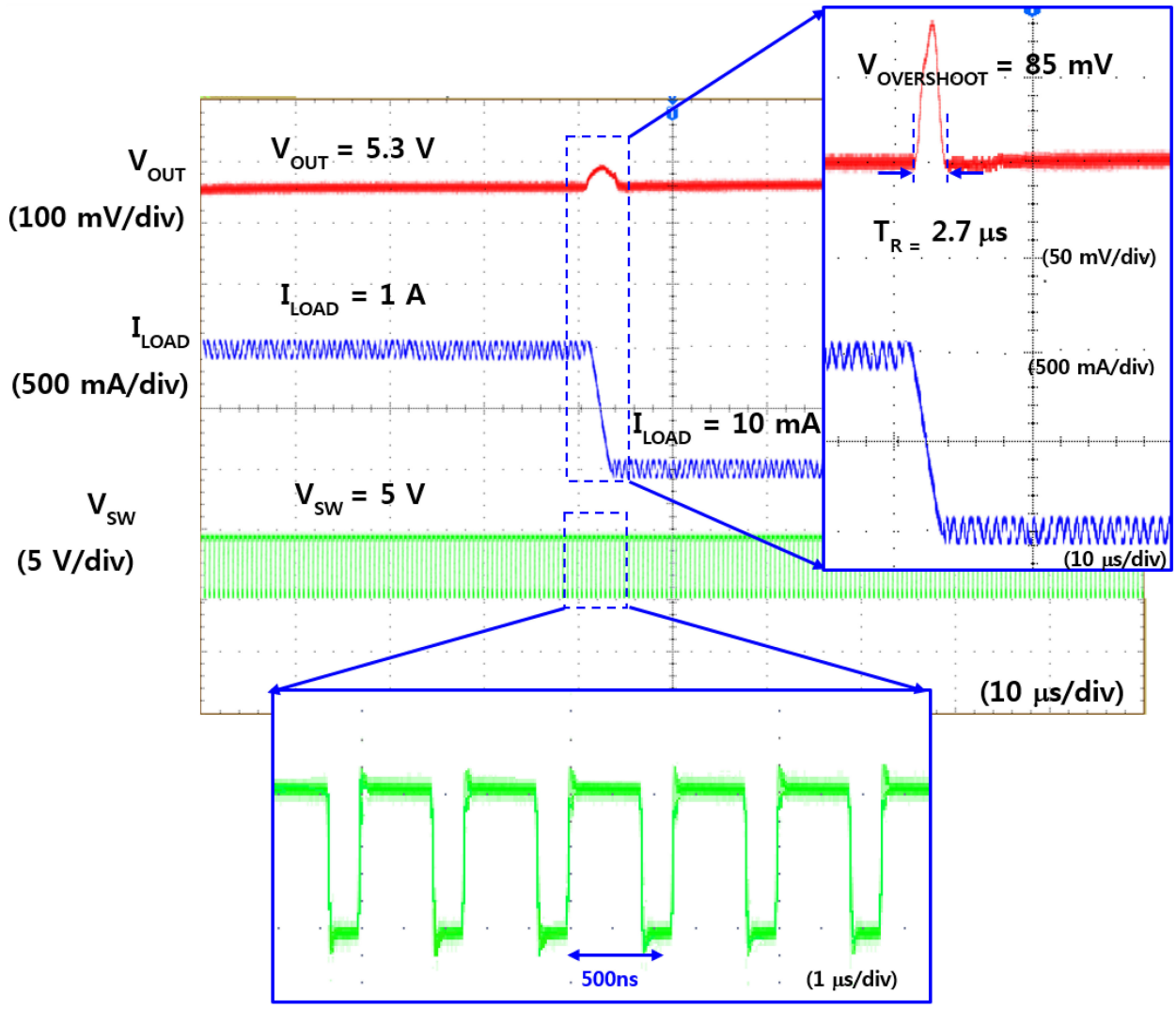


Fig. 20. Measured waveform of the COT dc–dc buck converter for heavy to light load with $V_{\mathrm{IN}} = 12$ V.

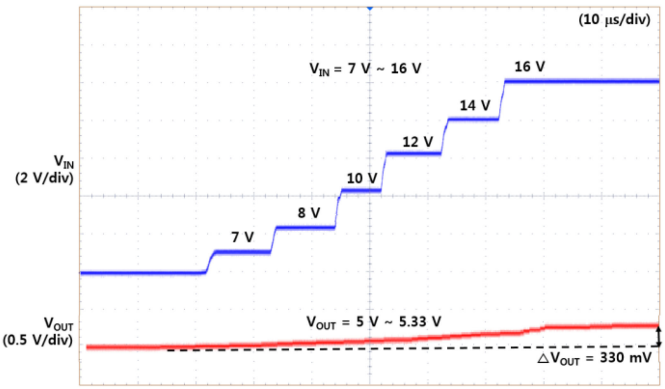


Fig. 21. Measurement waveform of the COT dc–dc buck converter output voltage regulation over input voltage range of 7–16 V with 2-V step size for load current of 1 A.

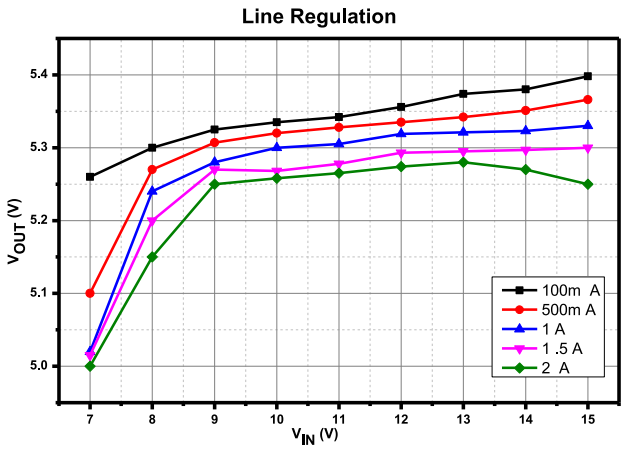


Fig. 22. Measured line regulation of the COT dc–dc buck converter at $I_{\mathrm{OUT}} = 100$ mA, 500 mA, 1 A, 1.5 A, and 2 A.

to attain fast recovery time, low undershoot/overshoot voltage, and a smaller dc offset value. Measured transient recovery time from light to full load and from full load to light load are 3 and 2.7 $\mu$s, respectively. The undershoot and overshoot voltage observed are 72 and 85 mV, respectively. The measured maximum dc

TABLE II
COMPARISON OF PREVIOUS PAPERS AND THIS ARTICLE

| Parameters | [10] TPE 2012 | [13] TPE 2013 | [14] TPE 2018 | [15] TPE 2016 | [16] TPE 2010 | This Work |
|---|---|---|---|---|---|---|
| **Control** | COT | COT | COT | AOT | Quadratic Differential & Integration (QDI) | **COT** |
| **Process** | 0.35 μm | 0.35 μm | 28 nm | 0.18 μm | 0.35μm | **0.13 μm** |
| **$V_{IN}$ [V]** | 9 | 15 | 3.3 | 2.7 ~ 3.6 | 3.3 | **7 ~ 15** |
| **$V_{OUT}$ [V]** | 4.5 | 1.5 | 1.05 | 1 ~ 1.2 | 2 | **5 ~ 7** |
| **$F_{SW}$ [MHz]** | 0.55 | 0.3 | 2.5 | 1 ~ 1.2 | 0.8 | **2** |
| **$I_{LOAD}$ [A]** | 2~7 | 0.1 ~ 8 | 0.3 ~ 1.7 | 1.1 | 0.01 ~ 0.5 | **0 ~ 2** |
| **L [uH]** | 90 | 1 | 1 | -- | 4.7 | **2.2** |
| **$R_{ESR}$ [Ω]** | 50 m | 1 m | 4 m | -- | 10 m | **2 m** |
| **Transient Recovery time (L→H, H→L)** | N/A | 25 μs , 20 μs | 4 μs, 5 μs | 7.8 μs, 10.7 μs, | 10 μs, 8 μs, | **3 μs, 2.7 μs** |
| **Offset DC [mV/%]** | N/A | 0.66 % | 4 mV | - | 50 mV | **3.5 mV** |
| **Light Load Efficiency [%]** | N/A | 70 @ 10 mA | 82 @ 300 mA | 82 @ 10 mA | -- | **84.60 @ 10 mA** |
| **Peak Power Efficiency [%]** | N/A | 91 | 94 | 88.2 | 93 | **95.56** |

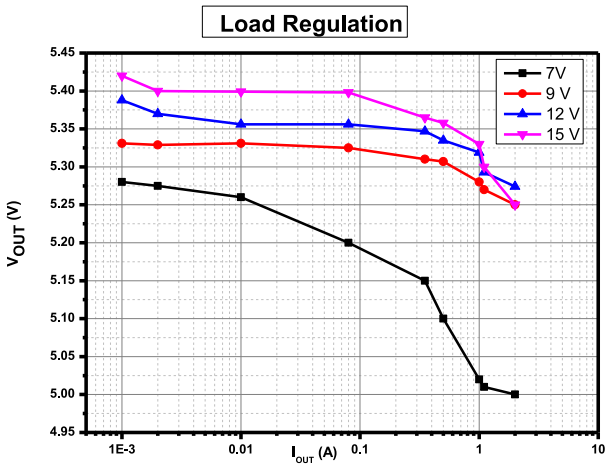


Fig. 23. Measured load regulation of the COT dc–dc buck converter at $V_{IN}$ = 7 V, 9 V, 12 V, and 15 V.

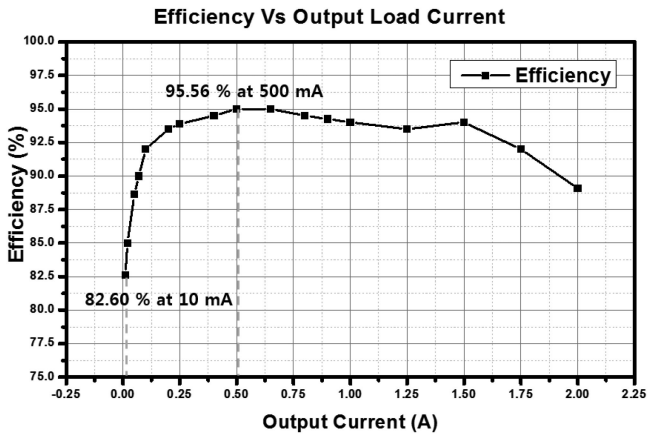


Fig. 24. Efficiency versus output load current COT dc–dc buck converter at $V_{IN}$ = 12 V.

offset is 3.5 mV. The proposed CRCS and FT-DCOC method achieves high efficiency, fast settling time, fast recovery time, and lower dc offset voltage.

## V. CONCLUSION

High-efficiency fast settling constant ON-time control dc–dc buck converter with CRCS is proposed for IoT applications. The CRCS is proposed to enhance the loop stability and improve the PCE at the light load. Input current sensed and added to the feedback voltage of the dc–dc converter to increase the sensed output ripple voltage. Furthermore, the FT-DCOC technique is introduced to achieve fast transient recovery time and cancel the output dc offset. Accordingly, the proposed technique removes the issue of a large recovery time. The effectiveness of the proposed architecture with the CRCS and FT-DCOC techniques has been verified with experimental results. This chip is fabricated with a 0.13-$\mu$m CMOS process, which enables high density and high speed. A standard supply voltage of 7–15 V is applied to

produce the output voltage of 5–5.33 V. The total die area is 2 mm × 1.5 mm. And, 17 $\mu$s of settling time is achieved from the proposed technique. Measured transient recovery time from light to heavy load and from heavy load to light load is 3 $\mu$s and 2.7 $\mu$s, respectively. The maximum dc offset for an output voltage of 5.3 V is 3.5 mV when the current is changed from 10 mA to 1 A and vice versa. The overshoot voltage is 85 mV and the undershoot voltage is 72 mV for an output of 5.3 V at the light to heavy and heavy to light load transition. The transient response of the circuit is accelerated and the efficiency is improved. The measured peak PCE of the proposed COT dc–dc buck converter is 95.56% at 0.5 A and PCE at the light load of 10 mA is 84.60%.

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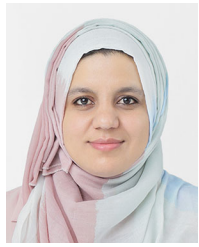

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