A Dual-Sided Control Strategy Based on Mode Switching for Efficiency Optimization in Wireless Power Transfer System

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***Abstract*—Transfer efficiency of a wireless power transfer (WPT) system is tightly related to the load, which varies greatly in a wide range during the charging process. Generally speaking, dual-sided control strategies are commonly applied to overcome the load variation and improve system efficiency. However, the system may suffer from hard switching, high control complexity, and auxiliary dc/dc converters. In this article, a dual-sided control strategy based on mode switching is proposed to approach an optimal load impedance, zero-voltage switching of all MOSFETs in WPT system, and a required output. In this control strategy, the output voltage of the inverter is adjusted in a wide range by switching the operation mode of the inverter to approach the optimal load impedance. The output current/voltage is regulated by the active rectifier control. Besides, a novel phase-locked method is proposed for the semi-bridgeless active rectifier control, which is simpler compared with the traditional phase-locked method. Finally, a 500-W prototype is built to verify the theoretical analysis, and the peak system efficiency of 93.9% is gained with $k = 0.23$.**

***Index Terms*—Mode switching, optimal load impedance, wireless power transfer (WPT), zero-voltage switching (ZVS).**

I. Introduction

WIRELESS power transfer (WPT) is becoming increasingly popular for its safety and convenience compared with the conventional plug-in charging method [1], [2]. It has attracted attention in these applications including biomedical implants, consumer electronics, underwater loads, and electric vehicles [EVs] [3]–[9]. Applying WPT to EVs for wireless charging is one of the most promising applications. The WPT system is desired to achieve high efficiency with constant voltage (CV) and constant current (CC) charging capability during the entire charging process.

For improving system efficiency, realizing the zero-voltage switching (ZVS) operation of converters in the WPT system and the load impedance matching are the commonly used technologies. An extra dc/dc converter is usually added on the secondary side for maintaining load impendence [10]. Constant output voltage and current of the system are achieved by adjusting the duty cycle of the output voltage of the inverter. However, the ZVS operation of the inverter cannot be achieved. In order to maintain the ZVS operation of the inverter, another dc/dc converter is usually added on the primary side [11]–[13]. Due to the existence of the extra dc/dc converter, not only the system cost and power loss increase but also the volume of the system increases. For sake of the extra dc/dc converters, some control strategies based on the active rectifier control are proposed. The output power of the system can be achieved by controlling the duty cycle or phase angle of the active rectifier [14], [15]. The duty cycle of the inverter always keeps the full duty cycle. But there will be a large amount of reactive power decreasing the system efficiency under the light load. Therefore, the dual phase shift control has been proposed to minimize the amount of reactive power for improving system efficiency [16]–[19]. The equivalent load impedance can be controlled by the duty cycle of the active rectifier for impedance matching. However, the converters lose the ZVS operation. In order to solve this problem, the triple phase shift control is proposed [20]. In order to realize the ZVS operation of the converter, a large enough phase compensated angle must be introduced. The value of phase-compensated angle is related to the parameters of the resonant network and load, which increases the control complexity. Recently, the pulse density modulation is adopted for the WPT system based on the SS compensation network, which can realize the ZVS operation of the converter and load impedance matching [21]–[23]. However, this strategy is commonly used in the SS compensated WPT system, which is not suitable for the high-order WPT system. Therefore, a control strategy for realizing the ZVS operation of converters and approaching the optimal load impedance of the system simultaneously is significant.

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On the other hand, all the control strategies based on the active rectifier can be implemented only if the secondary controller operates in synchronism with the primary side. It means that the voltage vector produced by the primary converter should be available to the secondary-side controller. By detecting the zero cross of resonant current on the secondary side, the synchronization signal can be gained for the driver signals generation of the active rectifier [24]–[26]. In some cases, there are a lot of harmonics in the current, which lead to the current distortion. It may have multiple zero-crossing points causing the false generation of driver pulse if the traditional zero-cross detection method is adopted. To avoid this problem, an auxiliary winding on the pickup side is used to sense the current in the primary main coil in [27], which produces a synchronizing signal for the active rectifier. But the signal sensed by the auxiliary winding is sensitive to the parameters of the detection circuit and should be compensated critically. A synchronization method based on the dedicated wireless communication interface between the primary and pickup sides is proposed in [28]. Such a solution increases the system complexity and decreases its robustness. Recently, a phase-locked method based on the detection of the active power and reactive power on the secondary side has been proposed [29]. The input current and voltage of the rectifier both need to be measured. In addition, the input current needs to be shifted by 90°. This phase-detected circuit is complex and costly. Therefore, a simple and reliable phase-locked method is meaningful.

Upon considering the aforementioned drawbacks, a novel dual-sided control strategy based on mode switching (DCS-MS) is proposed in this article. By adopting DCS-MS, the WPT system can achieve CC/voltage output, the ZVS operation of converters, and optimal load impedance simultaneously. The main contributions of this article are listed as follows.

1) A novel DSC-MS is proposed. In this control strategy, the inverter could switch among three different modes: full bridge, full-half bridge, and half bridge. The output voltage of the inverter can be adjusted in a wide range by mode switching to approach the optimal load impedance during the charging process combined with the limited output voltage range of PFC. Since the output voltage of the inverter always maintains a full duty cycle, the ZVS operation of the inverter can be realized with minimum reactive power in the system, which helps to improve the efficiency of the resonant network and reduce the control complexity.
2) A novel phase-locked method is proposed for the semi-bridgeless active rectifier control, saving the process of detecting the resonant current. This method is simpler and cheaper compared with the existing phase-locked method. Based on the proposed method, the active rectifier control is adopted to regulate the output voltage/current without relying on communication.

The rest of article is organized as follows. In Section II, the basic characteristics of the system are analyzed first. Then the loss model of the resonant network is built. The conditions for the optimal efficiency of the resonant network are given on the premise of realizing the ZVS operation of the rectifier.

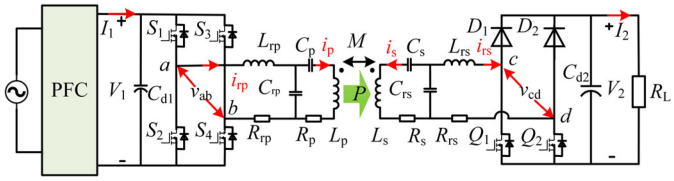


Fig. 1. WPT system with dual-sided LCC compensation network.

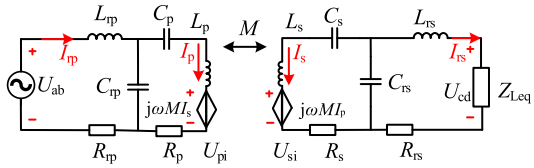


Fig. 2. Equivalent circuit of the resonant network.

In Section III, the mode switching of the inverter is proposed. Then, the parameters design requirements for realizing the ZVS operation of the converter are also given. Besides, the operation principle of the rectifier is analyzed. In Section IV, a novel phase-locked method is proposed for the semi-bridgeless active rectifier control first. Then, the DSC-MS is proposed, and the control diagram is also given. In Section V, the experiment results are given to verify the theoretical analysis and the proposed control strategy. Finally, Section VI concludes the article.

II. Theoretical Analysis of the WPT System

A. Equivalent Circuit Model

The WPT system adopted in this article is as shown in Fig. 1, which consists of a high-frequency inverter, a dual-sided LCC compensation network, and a high-frequency rectifier. S_1–S_4 and Q_1–Q_2 are the power switches of primary and secondary side converters, respectively. V_1 is the dc input voltage of the inverter, which is usually supplied by the PFC [30]–[32]. The output high-frequency voltage v_{ab} of the inverter excites the resonant network. L_p and L_s are the self-inductance of the main coils used for transferring energy from the primary side to the secondary side. L_{rp} and L_{rs} are the self-inductance of compensation inductor. C_{rp}, C_s, C_{rs}, and C_p are resonant capacitors. v_{cd} is the input voltage of the rectifier which is converted into dc voltage V_2 by the semi-bridgeless rectifier. R_L represents the load resistance.

The amount of active power transferred in the WPT system is mainly relevant to the amplitude of the fundamental component. The high-order harmonics have little contribution to active power transmission. Therefore, the fundamental harmonic approximation (FHA) method is usually adopted for simplifying the analysis.

The equivalent model is shown in Fig. 2. All the voltage and current in the model are fundamental harmonic of the corresponding voltage and current in the system. For example, U_{ab} is the fundamental harmonic of the voltage v_{ab}. Z_{Leq} is the fundamental equivalent input impedance of the rectifier. Neglecting the equivalent series resistances (ESR) in resonant

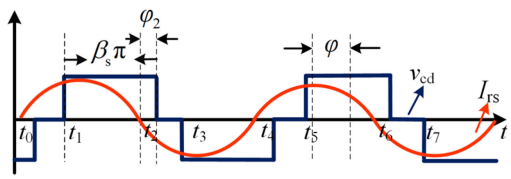


Fig. 3. Typical operation waveforms of the active rectifier.

network, the current of each branch in the resonant network can be derived by (1) shown at the bottom this page, where I_{rp}, I_{rp}, I_s, and I_{rs} are the fundamental harmonic of i_{rp}, i_p, i_s, and i_{rs}, respectively. M is the mutual inductance between the main coils L_p and $L_{s,}$ which is defined as

$$M = k\sqrt{L_p L_s} \tag{2}$$

where k is the coupling coefficient. To minimize the reactive component of the system, the operation frequency is usually set to the resonant frequency f_0, and the value of resonant elements satisfy

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_{rp}C_{rp}}} = \frac{1}{\sqrt{L_{rs}C_{rs}}} = \frac{1}{\sqrt{(L_p - L_{rp})C_p}} = \frac{1}{\sqrt{(L_s - L_{rs})C_s}}. \tag{3}$$

U_{cd} is the fundamental harmonic of v_{cd}, which can be gained by

$$\dot{U}_{cd} = \dot{I}_{rs}Z_{Leq} = \dot{I}_{rs}\left(R_{Leq} + \mathrm{j}X_{Leq}\right) = \left|\dot{U}_{cd}/\dot{I}_{rs}\right| e^{-\mathrm{j}\varphi} \tag{4}$$

where Z_{Leq} is the fundamental equivalent input impedance of the rectifier. The typical operation waveforms of semi-bridgeless active rectifier are depicted in Fig. 3. β_s is the duty cycle of the input voltage of the rectifier. φ is the phase difference between U_{cd} and I_{rs}. The value of U_{cd} and dc output voltage V_2 satisfy

$$U_{cd} = \frac{2\sqrt{2}V_2}{\pi}\sin\left[\frac{\beta_s\pi}{2}\right]. \tag{5}$$

The dc output current I_2 of the rectifier can be derived by

$$I_2 = I_{rs}\frac{2\sqrt{2}}{\pi}\sin\left[\frac{\beta_s\pi}{2}\right]\cos\left[\varphi\right]. \tag{6}$$

According to (5) and (6), Z_{Leq} can be given as

$$\begin{cases} Z_{Leq} = R_{Leq} + \mathrm{j}X_{Leq} = \left|\dot{U}_{cd}/\dot{I}_{rs}\right| e^{-\mathrm{j}\varphi} \\ X_{Leq} = \frac{8}{\pi^2}\sin^2[\frac{\beta_s\pi}{2}]\,|\cos[-\varphi]|\sin[-\varphi]R_L \\ R_{Leq} = \frac{8}{\pi^2}\sin^2[\frac{\beta_s\pi}{2}]\,|\cos[-\varphi]|\cos[-\varphi]R_L. \end{cases} \tag{7}$$

B. Maximum Efficiency Analysis of Resonant Network on the Premise of ZVS Operation of Rectifier

The system losses include loss in converters and resonant networks. In this section, only the losses in the resonant network are analyzed, containing the main coils loss and compensated inductor loss. The loss model of the resonant network is built as shown in Fig. 2(a). The R_{rp}, R_p, R_{rs}, and R_s are the equivalent series resistance of coils in the resonant network. And the losses and output power can be calculated by

$$\begin{cases} P_o = I_{rs}^2 R_{Leq} \\ P_{Loss} = I_{rp}^2 R_{rp} + I_p^2 R_p + I_s^2 R_s + I_{rs}^2 R_{rs}. \end{cases} \tag{8}$$

P_{Loss} represents the power loss in the system, and P_o represents the output power of the system. Therefore, the efficiency of the resonant network ηcan be given by

$$\eta = P_o/(P_{Loss} + P_o). \tag{9}$$

According to (1), (4), (7), (8), and (9), the efficiency η can be gained by

$$\eta = 8k^2 n_1 n_2 n_3^2 \pi^2 / \left[8k^2 n_1 n_2 (8R_L B \sin^2(\frac{\beta_s\pi}{2}) + n_3^2\pi^2) + \frac{n_3^2\pi^4 A}{R_L \sin^2(\frac{\beta_s\pi}{2})\sin(\frac{\beta_s\pi}{2} - \varphi_2)|\sin(\frac{\beta_s\pi}{2} - \varphi_2)|} \right] \tag{10}$$

where

$$\begin{cases} n_1 = L_p/L_{rp} \\ n_2 = L_s/L_{rs} \\ n_3 = L_{rs}/L_{rp} \end{cases} \tag{11}$$

$$\begin{cases} A = n_3 R_p + k^2 n_1 n_2 R_{rs} \\ B = (R_s + k^2 n_1 n_2 n_3 R_{rp})/(\omega_0^2 L_{rp}^2). \end{cases} \tag{12}$$

φ_2 is defined as the phase angle between the falling edge of v_{cd} and the zero cross of I_{rs} as shown in Fig. 3, which satisfies

$$\begin{cases} \varphi_2 = \varphi + \beta_s\pi/2 - \pi/2 \\ 0 \le \beta_s \le 1. \end{cases} \tag{13}$$

The resonant network efficiency against φ_2 and β_s is plotted in Fig. 4 according to (10). The parameters used for plotting the efficiency curve are listed in Table I. The load resistor R_L is 50 Ω. As can be seen from Fig. 4, the resonant network efficiency decreases to zero when the $\beta_s\varphi/2$ is equal to φ_2. Because there is no active output power of the system at this time. When the $\beta_s\varphi/2$ is smaller than the φ_2, the power is transferred from the secondary side to the primary side. This article only discusses the transmission of power from the primary side to the secondary side. In order to realize the ZVS operation of the active rectifier,

$$\begin{bmatrix} \dot{I}_{rp} \\ \dot{I}_p \\ \dot{I}_{rs} \\ \dot{I}_s \end{bmatrix} = \begin{bmatrix} \frac{1}{\mathrm{j}\omega C_{rp}} + \mathrm{j}\omega L_{rp} & \frac{-1}{\mathrm{j}\omega C_{rp}} & 0 & 0 \\ \frac{-1}{\mathrm{j}\omega C_{rp}} & \frac{1}{\mathrm{j}\omega}\left(\frac{1}{C_p} + \frac{1}{C_{rp}}\right) + \mathrm{j}\omega L_p & 0 & \mathrm{j}\omega M \\ 0 & \mathrm{j}\omega M & \frac{1}{\mathrm{j}\omega C_{rs}} & \frac{1}{\mathrm{j}\omega}\left(\frac{1}{C_s} + \frac{1}{C_{rs}}\right) + \mathrm{j}\omega L_s \\ 0 & 0 & -\left(\frac{1}{\mathrm{j}\omega C_{rs}} + \mathrm{j}\omega L_{rs}\right) & \frac{-1}{\mathrm{j}\omega C_{rs}} \end{bmatrix}^{-1} \begin{bmatrix} \dot{U}_{ab} \\ 0 \\ 0 \\ \dot{U}_{cd} \end{bmatrix} \tag{1}$$

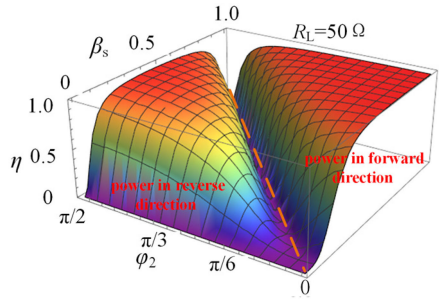


Fig. 4. Resonant network efficiency η against φ_2 and β_s.

TABLE I
RESONANT NETWORK PARAMETERS FOR CALCULATION

Symbol		Value
L_p	Main coil on the primary side	160uH
L_s	Main coil on the secondary side	160uH
L_{rp}	Primary Compensated inductor	37uH
L_{rs}	Secondary Compensated inductor	37uH
R_p, R_s	ESR of the main coil	214m
R_{rp}, R_{rs}	ESR of the compensate inductor	49mΩ
C_{rp}	Primary resonant capacitor	94.8nF
C_{rs}	Secondary resonant capacitor	94.8nF
C_p	Primary resonant capacitor	28nF
C_s	Secondary Resonant capacitor	29nF
k	Coupling coefficient	0.2
f_0	Resonant frequency	85kHz

the values of φ and φ_2 need to meet the following constraints in a unidirectional wireless charging system

$$\begin{cases} 0 \le \varphi \le \frac{\pi}{2} \\ \varphi_2 \ge 0. \end{cases} \tag{14}$$

According to Fig. 4 and (10), it can be obtained that the larger the value of φ_2 is, the lower the efficiency is. Therefore, the value of φ_2 should be set zero. The efficiency η can be rewritten as

$$\begin{aligned} \eta &= \frac{8k^2 n_1 n_2 n_3^2 \pi^2}{\frac{n_3^2 \pi^4 A}{R_L \sin^4(\frac{\beta_s \pi}{2})} + 8k^2 n_1 n_2 (8R_L B \sin^2(\frac{\beta_s \pi}{2}) + n_3^2 \pi^2)} \\ &= \frac{k^2 n_1 n_2 n_3^2}{2\pi^{-\frac{2}{3}} R_L^{\frac{1}{3}} (A n_3^2 |Z_{Leq}^{-\frac{4}{3}}| + B k^2 n_1 n_2 |Z_{Leq}^{\frac{2}{3}}|) + k^2 n_1 n_2 n_3^2}. \end{aligned} \tag{15}$$

According to (15), it exists an optimal impedance to achieve the highest efficiency of the resonant network

$$|Z_{opt}| = \frac{\sqrt{2} n_3}{k} \sqrt{\frac{A}{n_1 n_2 B}}. \tag{16}$$

$|Z_{opt}|$ is defined as the optimal equivalent impedance, which is decided by resonant network parameters and independent of the load.

For simplifying the design and analysis of the resonant network, only the case that parameters of the primary and secondary sides are the same is discussed in the rest of this article. It is assumed that the quality factors of the coils and inductors on the primary and secondary sides are the same respectively. That means

$$\begin{cases} L_p / L_s = L_{rp} / L_{rs} \\ R_p / R_s = R_{rp} / R_{rs} = 1. \end{cases} \tag{17}$$

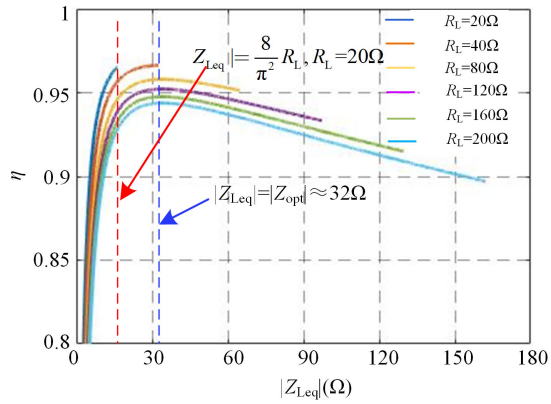


Fig. 5. Resonant network efficiency η against Z_{Leq} with the different load resistance R_L.

By substituting (17) into (16), the optimal impedance can be simplified as follows:

$$|Z_{opt}| = \sqrt{2} \omega_0 L_{rp} / (k n_1). \tag{18}$$

According to the parameters in Table I, the resonant network efficiency η against $|Z_{Leq}|$ is plotted as Fig. 5 with different load resistance R_L. It should be noted that the value of $|Z_{Leq}|$ is always smaller than R_L which satisfies

$$|Z_{Leq}| = \frac{8}{\pi^2} \sin^3 \left[\frac{\beta_s \pi}{2} \right] R_L \le \frac{8}{\pi^2} R_L. \tag{19}$$

Therefore, the value of $|Z_{Leq}|$ corresponding to the highest efficiency of the resonant network is equal to $8R_L/\pi^2$, when the value of load resistance R_L satisfies

$$R_L \le \frac{\pi^2 |Z_{opt}|}{8}. \tag{20}$$

The value of $|Z_{Leq}|$ corresponding to the highest efficiency point is equal to Z_{opt}, when the value of load resistance R_L satisfies

$$R_L > \frac{\pi^2 |Z_{opt}|}{8}. \tag{21}$$

The ratio of input fundamental harmonic voltage to output fundamental harmonic voltage of resonant network is defined as T, which can be represented by

$$T = U_{ab} / U_{cd}. \tag{22}$$

When the equivalent impendence Z_{Leq} is equal to Z_{opt} in (18), U_{cd} and U_{ab} satisfy

$$T_{opt} = \frac{U_{ab}}{U_{cd}} = \frac{U_{ab}}{|I_{rs} Z_{opt}|} = \frac{1}{|\sqrt{2}|}. \tag{23}$$

T_{opt} is defined as the optimal voltage ratio, which is independent of the load and coupling coefficient k. When the optimal ratio T_{opt} and $\varphi_2 = 0$ are maintained simultaneously, the optimal load impedance is achieved.

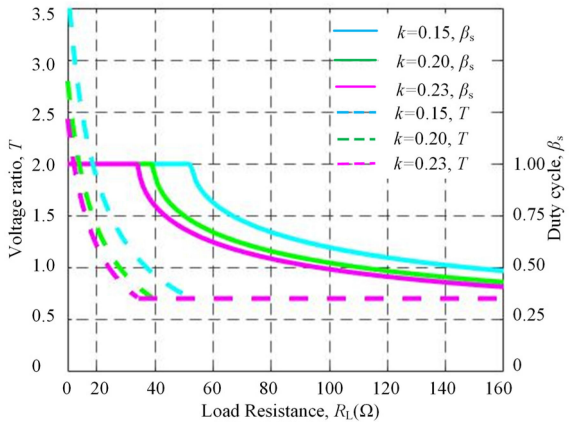


Fig. 6. Voltage ratio and duty cycle versus the load resistance.

For approaching the optimal load impedance, the curves of the voltage ratio T and the pulse width β_s with the load under different coupling coefficients are plotted as shown in Fig. 6 according to (7) and (18)–(23). The parameters used for plotting the curves are listed in Table I. When load resistance R_L is small, the duty cycle β_s is kept at 1 and the voltage ratio T is larger than T_{opt}. With the load resistance R_L increasing, the T gradually approaches the optimal voltage ratio T_{opt}. When the R_L satisfies (23), Z_{Leq} can achieve Z_{opt} and T is kept at T_{opt}.

III. Operation Principle of Converters

For optimizing the system efficiency, a DCS based on mode switching is proposed. In this control strategy, the inverter regulates output voltage v_{ab} by switching the operation mode and adjusting input voltage V_1 of the inverter without changing the duty cycle. The output voltage is adjusted to make the Z_{Leq} approach the optimal load. The semi-bridgeless active rectifier is adopted on the secondary side. The output current and voltage are controlled by the duty cycle of input voltage v_{cd} of the rectifier.

A. Operation Principle of Inverter With Mode Switching

For achieving the optimal load impedance, the voltage v_{ab} needs to be adjusted in a wide range. However, the input voltage V_1 is usually supplied by PFC, which has an adjustment range but is limited [33]–[35]. In this article, the mode switching of the inverter is proposed. The inverter operates among three modes: full-bridge, full-half bridge and, half-bridge, as shown in Fig. 7. In half-bridge mode, the MOSFET S_3 keeps OFF and MOSFET S_4 keeps ON during one switching cycle. In full-half bridge mode, the inverter works alternately in full-bridge and half-bridge modes. By Fourier decomposition, the amplitude of each frequency component in output voltage v_{ab} of the inverter with different operation modes is shown as in Table II. The f_0 in Table II is the resonant frequency.

In WPT system based on the dual-sided LCC compensation, the amount of active power transferred to the load is decided by the amplitude of the fundamental component of v_{ab}. In different mode, the fundamental harmonic component of the output voltage of the inverter is different. Therefore, a wide

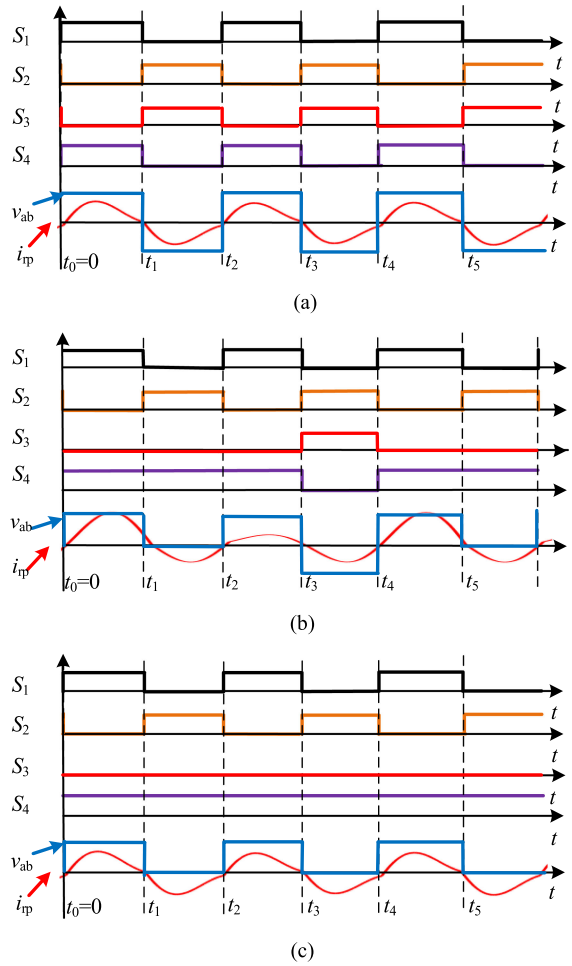


Fig. 7. Three operation modes of the inverter. (a) Full-bridge. (b) Full-half bridge. (c) Half-bridge.

TABLE II
EACH FREQUENCY COMPONENT IN THE OUTPUT VOLTAGE OF INVERTER

Frequency	(a) Full bridge	(b)Full-half bridge	(c)Half bridge
DC component	0	$V_1/4$	$V_1/2$
$0.5f_0$	0	$\sqrt{2}V_1/\pi$	0
f_0	$4V_1/\pi$	$3V_1/\pi$	$2V_1/\pi$
$1.5f_0$	0	$\sqrt{2}V_1/3\pi$	0
$2f_0$	0	0	0
$2.5f_0$	0	$\sqrt{2}V_1/5\pi$	0
$3f_0$	$4V_1/3\pi$	V_1/π	$2V_1/3\pi$
$5f_0$	$4V_1/5\pi$	$3V_1/5\pi$	$2V_1/5\pi$

range of the output voltage of the inverter can be obtained by mode switching with the limited output voltage range of PFC. Assuming that the output voltage V_1 of PFC can be adjusted from 320 to 500 V, the range of the fundamental component of output voltage v_{ab} can be extended to 144–450 V by the mode switching.

B. Conditions for ZVS Operation Realization of Inverter

In the full-bridge mode, the output voltage of the inverter always keeps the full duty cycle. There are rich high-order harmonics in the output current of the inverter, which will cause

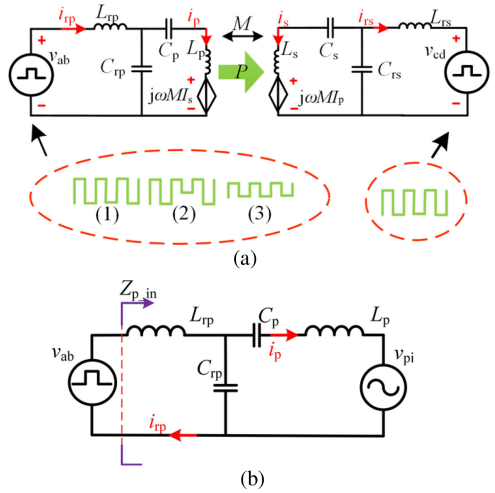


Fig. 8. (a) Equivalent circuit model of resonant network considering all frequency components. (b) Simplified equivalent circuit model.

the distortion of the current i_{rs}. In [36], the specific effect of high-order harmonics in the current i_{rs} has been analyzed. The existence of higher harmonics increases the MOSFET turn-OFF current, which is helpful to realize the ZVS operation of MOSFET in the same arm. The total increased value of the turn-OFF current can be obtained by the following equation:

$$\Delta i_{rp\_off} = \sqrt{2}\sum_{k=1}^{\infty}\frac{1}{\left((2k+1)^2-1\right)}\frac{U_{ab}}{\omega_0 L_{rp}} = \frac{\sqrt{2}U_{ab}}{4\omega_0 L_{rp}}. \quad (24)$$

The condition for realizing ZVS operation of inverter is analyzed in detail in [36]. In half-bridge mode, the condition to realize ZVS operation is the same as that of full bridge.

In full-half bridge mode, the inverter works alternately in half-bridge and full-bridge. Thus, there is an unneglected low-frequency component in the output current i_{rp}, which will affect the ZVS operation of the inverter.

For analyzing the effect of low frequency on the ZVS operation of the inverter in half-full bridge mode, the circuit model of the system is built as shown in Fig. 8(a) to obtain the time domain expression of current i_{rp}. Two square wave voltage sources are used to replace the inverter and rectifier, respectively. In a high-order system, it is difficult to directly solve the time-domain analytical expression of current. Therefore, the model needs to be simplified. Due to the filtering function of the circuit formed by L_{rs} and C_s, the main component of current i_s is the fundamental harmonic. The coil current i_s can be calculated by the FHA model for simplification. The voltage v_{pi} in the main coil on the primary side is induced by the current i_s. Therefore, the induced voltage v_{pi} is approximately a sinusoidal voltage. Therefore, a sinusoidal voltage source can be used to represent the circuit on the secondary side for simplifying the circuit further. The resonant network can be equivalent as shown in Fig. 8(b).

In full-half bridge mode, the voltage v_{ab} can be derived by Fourier series expansions as follows:

$$v_{ab}(t) = \frac{a_0}{2} + \sum_{n=1,2,\ldots}^{\infty}\left(a_n \sin\left(\frac{n\omega_0 t}{2}\right) + b_n \cos\left(\frac{n\omega_0 t}{2}\right)\right)$$
$$= \frac{V_1}{4} + \frac{\sqrt{2}V_1}{\pi}\sin\left(\frac{1}{2}\omega_0 t - \frac{\pi}{4}\right) + \frac{3V_1}{\pi}\sin(\omega_0 t) \ldots. \quad (25)$$

The v_{pi} in Fig. 8(b) is approximately a sinusoidal voltage, which can be presented by

$$\dot{v}_{pi} = j\omega_0 M\dot{I}_s = \frac{3V_1 k^2 n_1^2 |Z_{Leq}|}{\pi\omega_0 L_{rp}}\angle\left(-\varphi - \frac{\pi}{2}\right). \quad (26)$$

Equation (26) is calculated according to (1) and the model in Fig. 8. The phase of v_{pi} is gained by taking the fundamental harmonic voltage U_{ab} as a reference. By the superposition theorem, the individual current supplied by v_{ab} or v_{pi} is calculated with the other voltage source replaced by a short circuit. The steady-state time-domain expression of i_{rp} can be obtained by

$$i_{rp}(t) = \mathrm{Im}\left[\sum_{n=1/2,1,3/2}^{\infty}\left(\frac{\dot{U}_{ab}(n)}{Z_{p-in}(n)}\right) - \frac{\dot{v}_{pi}}{j\omega_0 L_{rp}}\right] \quad (27)$$

where $\dot{U}_{ab}(n)$is the n_{th} frequency nf_0 component in the phasor domain of voltage v_{ab}. When n is equal to 1/2, the $U_{ab}(n)$ means the $1/2f_0$ component of v_{ab}

$$\dot{U}_{ab}\left(\frac{1}{2}\right) = \frac{\sqrt{2}V_1}{\pi}\angle -\frac{\pi}{4}. \quad (28)$$

$Z_{p\text{-}in}(n)$ represents the equivalent input impedance of the resonant network at the n_{th} frequency nf_0, which is given by

$$\begin{cases} Z_{p-in}(n) = \frac{(-1+(-1+n^2)^2 n_1)j\omega_0 L_{rp}}{n(-1+n^2)n_1}(n \neq 1) \\ Z_{p-in}(n) = \infty(n = 1) \end{cases}. \quad (29)$$

Since the other frequency components are small enough to be ignored, only 0.5th, 1.5th, 2.5th, 3th, 5th, and the fundamental frequency components are analyzed. According to (27), the time-domain expression of current i_{rp} can be derived by where the coefficients in (30) shown at bottom of the next page, are given by

$$\begin{cases} A_{0.5} = 6\sqrt{2}V_1 n_1/((9n_1-16)\omega_0 L_{rp}\pi) \\ A_1 = 3|Z_{Leq}|V_1 k^2 n_1^2/(\omega_0^2 L_{rp}^2\pi) \\ A_{1.5} = 10\sqrt{2}V_1 n_1/((25n_1-16)\omega_0 L_{rp}\pi) \\ A_{2.5} = 42\sqrt{2}V_1 n_1/((441n_1-16)\omega_0 L_{rp}\pi) \\ A_3 = 24V_1 n_1/((64n_1-1)\omega_0 L_{rp}\pi) \\ A_5 = 72V_1 n_1/((576n_1-1)\omega_0 L_{rp}\pi). \end{cases} \quad (31)$$

σ is the phase difference of U_{ab} and I_{rp}, which can be controlled by the active rectifier. The vector diagram of the fundamental component in the resonant network is depicted in Fig. 9. The value of σ is just equal to φ according to Fig. 9. That means if I_{rs} leads U_{cd}, I_{rp} will lag U_{ab}.

According to Fig. 7(b), to achieve ZVS operation of the inverter, the following constraints should be satisfied:

$$i_{rp}(t_0) < 0, i_{rp}(t_1) > 0, i_{rp}(t_2) < 0, i_{rp}(t_3) > 0. \quad (32)$$

According to (30) and (31), it can be obtained

$$i_{rp}(t_0) + i_{rp}(t_1) = \sqrt{2}A_{0.5} - \sqrt{2}A_{1.5} - \sqrt{2}A_{2.5} \quad (33)$$

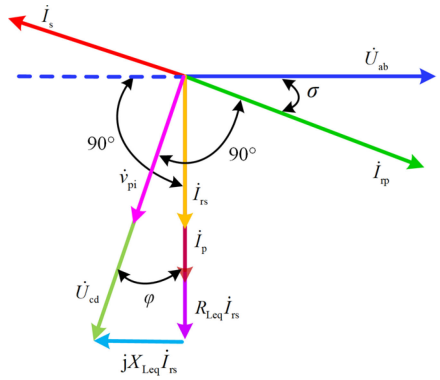


Fig. 9. Phasor representations of currents and voltages of the system.

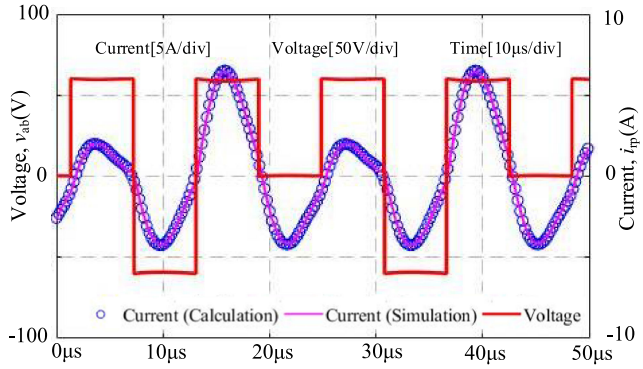


Fig. 10. Simulation and theoretical calculation waveforms of current i_{rp}.

where $t_1 = t_0 + 1/(2f_0)$. When n_1 is larger than 16/9, $i_{rp}(t_0) + i_{rp}(t_1) > 0$. Since $t_3 = t_0 + 3/(2f_0)$, $t_2 = t_1 + 1/(2f_0)$, it can be gained that

$$\begin{cases} i_{rp}(t_0) + i_{rp}(t_3) = 0 \\ i_{rp}(t_1) + i_{rp}(t_2) = 0. \end{cases} \tag{34}$$

Therefore, for realizing the ZVS operation of the inverter, it only needs to satisfy (35) without considering the parasitic capacitance of MOSFETs when $n_1 > 16/9$

$$i_{rp}(t_0) < 0. \tag{35}$$

By substituting (30), (31) into (35), the conditions for ZVS can be obtained as follows:

$$n_1 > a(a \approx 4.8), \varphi \geq 0. \tag{36}$$

That means the inductance of the main coil should be set more than 4.8 times that of the compensated inductor on the primary side for realizing the ZVS operation of the inverter. The equivalent input impedance of the rectifier needs to be resistive or inductive. When the n_1 is smaller than 4.8, the actual value of the primary series resonant capacitor can be set slightly smaller than the resonance value C_p for realizing the ZVS operation of the inverter. The specific analysis is similar to that in [36]

$$C_{p1} = C_p - \Delta C_p. \tag{37}$$

C_{p1} is the actual value of the primary series resonant capacitor. The closer n is to 4.8, the smaller the ΔC_p is. For verifying the accuracy of model and analytical method, the simulation and theoretical calculation waveforms are compared as shown in Fig. 10. The parameters used for simulation and calculation are given in Table I. In the simulation model, the rectifier is uncontrolled rectification, and the load resistor R_L is 60 Ω.

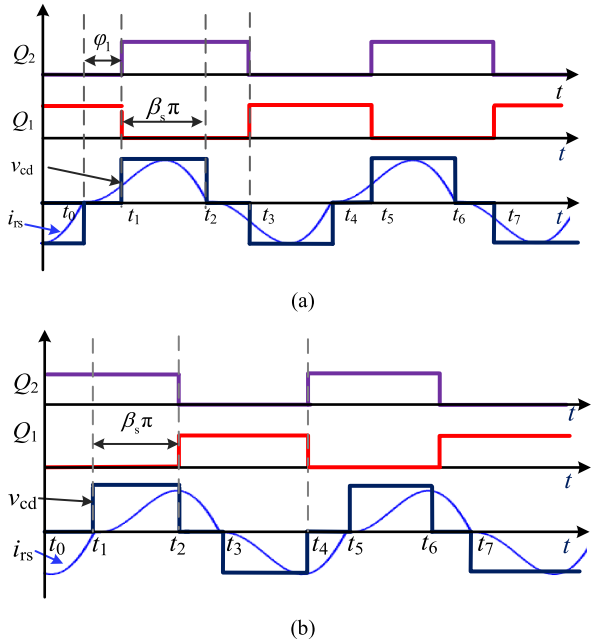


Fig. 11. Two cases: (a) current i_{rs} leads voltage v_{cd}; (b) current i_{rs} lags voltage v_{cd}.

C. Operation Principle of Semi-Bridgeless Active Rectifier

The semi-bridgeless active rectifier is composed of two diodes and two MOSFETs. The duty cycle of input voltage v_{cd} of the rectifier is controlled to achieve the required output. The steady-state operation waveforms of the semi-bridgeless have two cases as shown in Fig. 11. When it is the case(a), the rectifier has four common modes as depicted in Fig. 12.

Mode (a): During interval t_1–t_2, the MOSFET Q_2 is ON, and the MOSFET Q_1 is OFF. The current i_{rs} flows through the MOSFET Q_2 and D_1, and charges the load.

$$i_{rp}(t) \approx A_{0.5}\sin(\frac{1}{2}\omega_0 t + \frac{\pi}{4}) + A_1\sin(\omega_0 t - \sigma) + A_{1.5}\sin(\frac{3}{2}\omega_0 t - \frac{\pi}{4}) + A_{2.5}\sin(\frac{5}{2}\omega_0 t - \frac{3\pi}{4}) + A_3\sin(3\omega_0 t - \frac{\pi}{2}) + A_5\sin(5\omega_0 t - \frac{\pi}{2}) \tag{30}$$

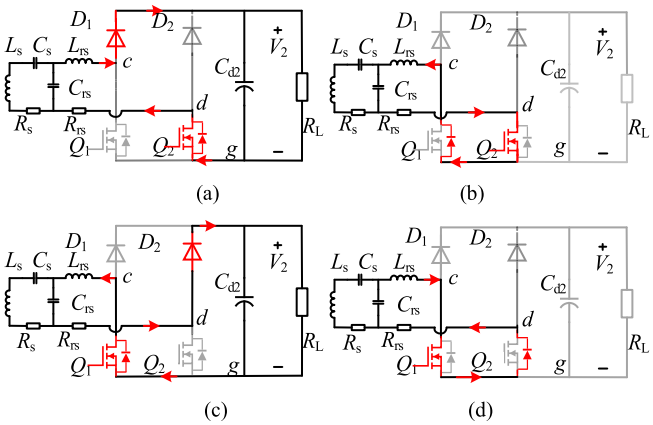


Fig. 12. Four operation modes of the rectifier when current i_{rs} leads voltage v_{cd}. (a) Interval t_1–t_2. (b) Interval t_2–t_3. (c) Interval t_3–t_4. (d) Interval t_4–t_5.

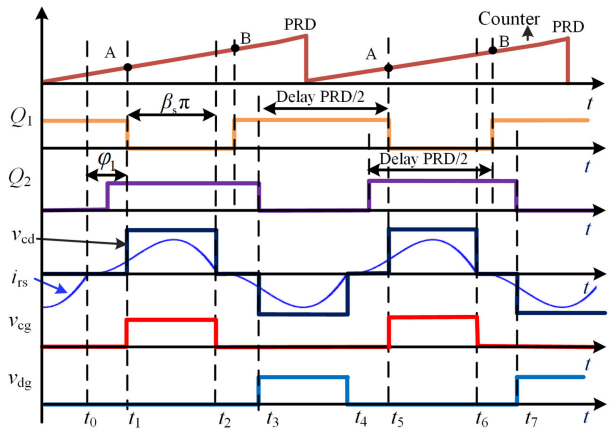


Fig. 13. Operation waveforms of the rectifier.

Mode (b): During interval t_2–t_3, the MOSFET Q_2 is ON, and the MOSFET Q_1 is OFF. The current i_{rs} flows through the MOSFET Q_2 and the antiparallel diode of the MOSFET Q_1.

Mode (c): During interval t_3–t_4, the mosfet Q_2 is OFF, and the MOSFET Q_1 is ON. The current i_{rs} flows through the MOSFET Q_1 and D_2, and charges the load.

Mode (d): During interval t_4–t_5, the MOSFET Q_2 is OFF, and the MOSFET Q_1 is ON. The current i_{rs} flows through MOSFET Q_1 and the antiparallel diode of the MOSFET Q_2.

When current i_{rs} leads voltage v_{cd}, both the two MOSFETs can achieve the ZVS operation. As shown in Fig. 12(b) and 12(d), the current flows through the antiparallel diode of the MOSFETs during the interval t_2–t_3 and t_4–t_5, which increases conduction loss. In this article, the MOSFET's ON time is extended as depicted in Fig. 13 to reduce the freewheeling time of the body-diode of the MOSFET. If the MOSFET is ON during t_0–t_1 and t_2–t_3, the current can flow through the channel of MOSFET as shown in Fig. 14. In this way, the loss caused by the antiparallel diode of the MOSFET can be decreased.

When it is the case as in Fig. 11(b), the rectifier also has four modes. Obviously, in this case, MOSFETs of the rectifier lose the ZVS operation. Therefore, it is necessary to control the rectifier

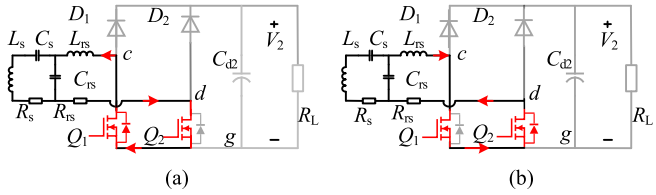


Fig. 14. Current path when the input voltage is zero level. (a) Interval t_0–t_1. (b) Interval t_2–t_3.

to avoid this case. The details of control will be described in the next section.

IV. Proposed Control Strategy

A. Phase-Locked Method for Semi-Bridgeless Active Rectifier

The implementation of active rectifier control depends on the reliable phase-locked technology. In this article, a new phase-locked method has been proposed, which gets rid of sensing the current in the resonant network.

When the rectifier operates in the case as in Fig. 11(a), the falling edge of voltage v_{cd} occurs at the same time as the current i_{rs} crosses zero point from positive to negative. The voltage rising edge corresponds to the time when the MOSFET Q_1 is turned OFF. φ_1 is defined as the phase angle between the rising edge of v_{cd} and the zero crossing of the i_{rs}. The duty cycle β_s and φ_1 satisfy

$$\varphi_1 = \pi - \beta_s \pi. \tag{38}$$

As long as β_s is measured, φ_1 can be obtained by (38). The pulse width of voltage v_{cg} and v_{dg} is exactly equal to the pulse width of the input voltage v_{cd} as shown in Fig. 13. A phase detection circuit is proposed as depicted in Fig. 15. The voltage v_{cg} is a high-frequency square wave voltage, which contains a rich higher harmonic. Therefore, the parasitic capacitance of the resistor cannot be neglected, which may cause the distortion of the sampling voltage. For eliminating the effect of parasitic capacitance, external capacitors must be connected in parallel with the resistors in Fig. 15, which satisfy

$$R_1 C_1 = R_2 C_2. \tag{39}$$

The output voltage v_{cg1} of the voltage divider is sent to the comparator. The square voltage v_{cg2} is the output signal of the comparator. The dc component of v_{cg2} is proportional to the duty cycle β_s of voltage v_{cd}, which can be obtained through the low-pass filter. In the secondary controller, the counter counts with a period equal to PRD as shown in Fig. 13. When the counter reaches value A, the driver pulse of Q_1 clears low. When the counter reaches the value B, the driver pulse of Q_1 sets high. As can be seen from Fig. 13, the duty cycle β_s can be controlled by adjusting the comparison value A. When the rectifier operates in case of Fig. 13(a), the later the counter reaches value A, the smaller the duty cycle is. While in case(b), the later the counter reaches value A, the larger the duty cycle is.

When the feedback value of β_s is smaller than the target value β_{sref}, the error between the β_{sref} and β_{sfb} is sent to the PI

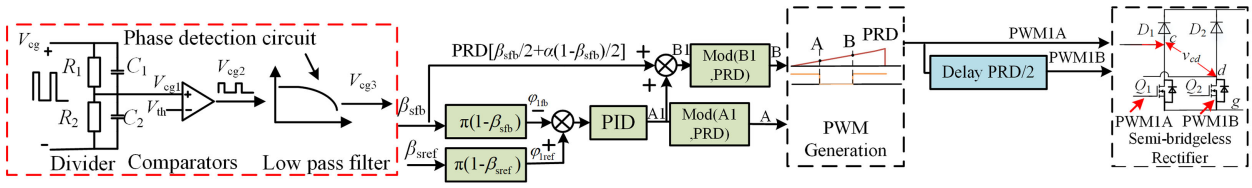


Fig. 15. Phase-locked method.

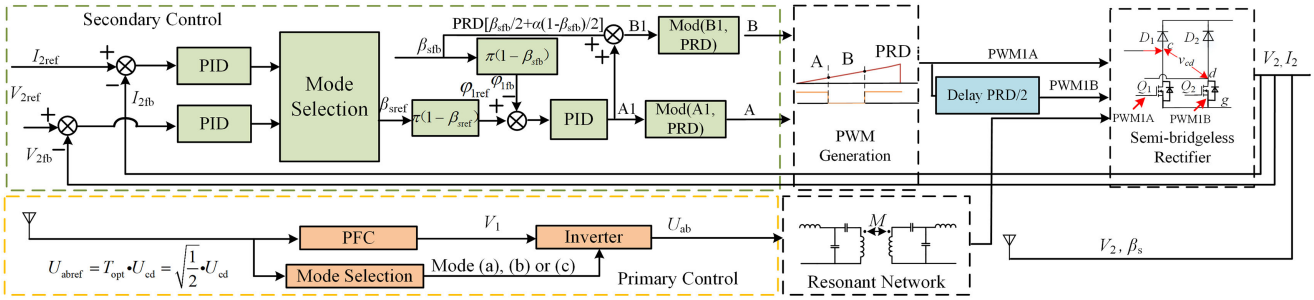


Fig. 16. System control strategy.

controller to decrease the value A as shown in Fig. 15. If the output value of the PI controller is greater than PRD, the output value is the remainder of PRD. Then the duty cycle will approach the target value, and the rectifier will operate in case(a). If the error between the β_{sref} and β_{sfb} is sent to the PI controller to increase the value A1, then the duty cycle will approach the target value, and the rectifier will operate in case(b). The value of B1 can be gained by

$$\mathrm{B1} = \mathrm{A1} + \left(\frac{\beta_{\mathrm{s}}}{2} + \left(\frac{(1-\beta_{\mathrm{s}})}{2}\right)\alpha\right) \times \mathrm{PRD}, \alpha \in (0,1]. \tag{40}$$

The freewheeling time of the body diode can be adjusted by adjusting α. The driver pulse of Q_2 can be obtained by delaying the driver pulse of Q_1 for a half period. By the phase-locked method in Fig. 15, the rectifier on the secondary side can operate in synchronization with the inverter on the primary side and the current leads the voltage. Although there will be oscillation on the edge of the drain-source voltage v_{cg} across the MOSFETs when the current i_{rs} is discontinuous, the output voltage v_{cg3} of low-pass filter is still smooth. The value of v_{cg3} is the feedback value of phase-locked loop. There is no direct detection of the current zero-crossing point or voltage zero-crossing point as the synchronization signal in the proposed phase-locked method. So even though the current is distorted seriously, the rectifier can still operate stably, synchronized with the inverter. If the influence of harmonic components on the zero cross of current i_{rs} is neglected, the φ_2 can be regarded as 0. If φ_2 equal to 0, it helps to optimize resonant efficiency according to the previous analysis.

B. System Control Strategy

The system control has three control goals: the constant output voltage/current, the ZVS operation of the converters, and approaching the optimal load impedance. The control objects

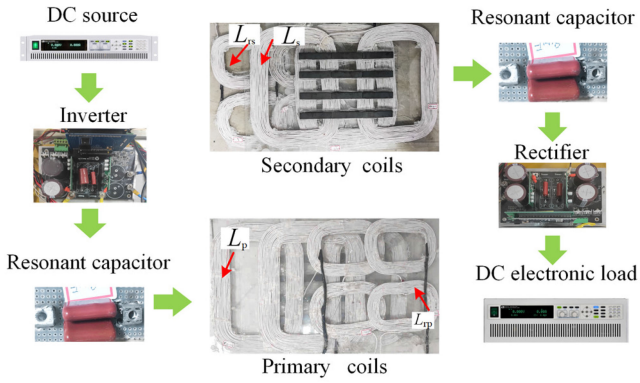


Fig. 17. Experimental prototype.

are the pulse width β_{s}, the operation mode of the inverter, and the input voltage of inverter V_1. A new DCS based on the mode switching for the WPT system has been proposed as depicted in Fig. 16. On the secondary side, the outer loop is the voltage/current loop, and the output control value of the outer loop is the duty cycle β_{sref}. Then $\varphi_{1\mathrm{ref}}$ is gained according to (38), which is used as the reference command of the inner phase-locked loop. By the secondary side control, the constant output and ZVS operation of the converter can be achieved. By the primary side control, the input voltage V_1 of the inverter and operation mode is adjusted to approach the optimal ratio T_{opt} for achieving optimal load impendence. The operation mode of the inverter is changed according to U_{abref}.

V. Experiment Verification

A. Experimental Prototype

For verifying the proposed control method, a 500-W prototype is built up, which is shown in Fig. 17. The system includes a

TABLE III
EXPERIMENT PARAMETERS

Symbol		Value
$L_{\rm p}$,	Main coil on the primary side	160.6uH,
$L_{\rm s}$	Main coil on the secondary side	161.3uH
$L_{\rm rp}$	Compensated inductor on the primary side	36.1uH
$L_{\rm rs}$	Compensated inductor on the secondary side	36.3uH
$C_{\rm rp}$	Resonant capacitor on the primary side	97nF
$C_{\rm rs}$	Resonant capacitor on the secondary side	97nF
$C_{\rm p}$	Resonant capacitor on the primary side	27nF
$C_{\rm s}$	Resonant capacitor on the secondary side	29nF
$f_{\rm s}$	Operation frequency	85kHz
$R_{\rm rp}$	ESR of inductor $L_{\rm rp}$	50mΩ
$R_{\rm rs}$	ESR of inductor $L_{\rm rp}$	51mΩ
$R_{\rm p}$	ESR of coil $L_{\rm p}$	228mΩ
$R_{\rm s}$	ESR of coil $L_{\rm s}$	231mΩ

dc source, a high-frequency inverter, a dual-sided LCC resonant network, a semi-bridgeless rectifier, and an electronic load. Usually, the three-phase PFC output voltage can be adjusted from 600 to 800 V. Therefore, the output voltage range of the dc source is set as 60–80 V, which replaces the output voltage of the PFC in this article. The converters on the primary side and secondary side are controlled by a DSP28335 controller, respectively. The MOSFET IXTQ96N20P is adopted in the downsized prototype in this article.

It should be noted that if high voltage MOSFEST with quite large drain-source ON-state resistance is used in the system, the conduction loss should be considered in the loss model of the system. In this case, the optimal voltage ratio $T_{\rm opt}$ may need to be recalculated. All the coils in the resonant network are made by the Litz wire with three hundred strands. The main coils and compensated inductors in the resonant network adopt a DD structure. The compensated inductor is integrated into the main coil and shares the same magnetic core with the main coil. The ratio n_1 of the inductance of main coil $L_{\rm p}$ to the inductance of the compensated inductor $L_{\rm rp}$ is slightly smaller than 4.8 in this article. Therefore, the actual value of capacitor $C_{\rm p}$ is set to 27 nF, smaller than the theoretical value. The other detail parameters in the WPT system are listed in Table III.

B. Experimental Results

In the proposed control strategy, the load voltage and current are regulated by active rectifier control on the secondary side. The phase-locked loop is critical to the secondary side control. The steady-state performance and dynamic performance of the proposed phase-locked method are tested, respectively.

The phase-locked circuit board is shown Fig. 18(a), which just contains two parts: the high-frequency square wave voltage detection circuit and low-pass filter circuit. Compared with a traditional phase-locked circuits for the active rectifier, it is simpler and cheaper. The drain-source voltage $v_{\rm cd}$ of MOSFET Q_1 is converted to the voltage signal $v_{\rm cg1}$, which is sent to the comparator TL3116. Fig. 18(c) shows the sample signal $v_{\rm cg}$ and the drain-source voltage of the MOSFET Q_1. It can be seen that the sampled signal $v_{\rm cg2}$ has almost no phase delay

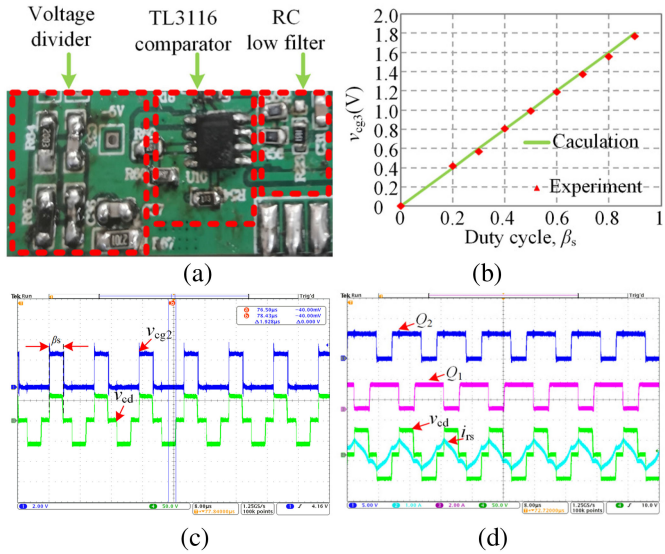


Fig. 18. (a) Phase-locked circuit. (b) Theoretical value and actual value of duty cycle. (c) Input voltage $v_{\rm cd}$ and signals $v_{\rm cg2}$. (d) Driver signals, voltage $v_{\rm cd}$, and current $i_{\rm rs}$ with $V_1 = 60$ V, $k = 0.2$.

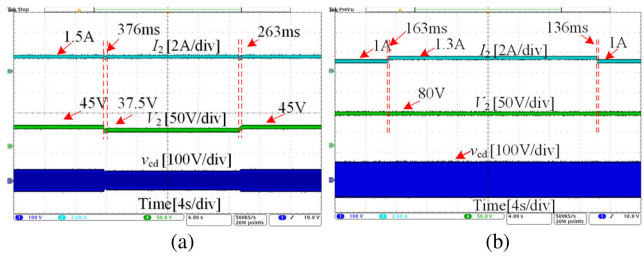
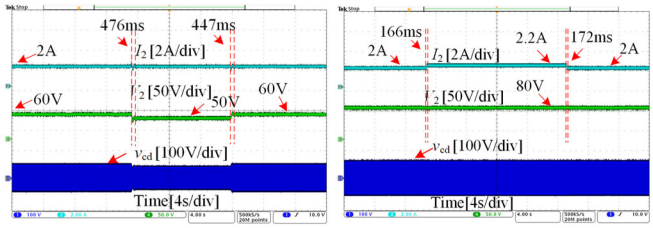


Fig. 19. Inverter in half-bridge mode. (a) CC mode, changing $R_{\rm L}$ from 30 to 25 Ω and vice versa. (b) CV mode, changing $R_{\rm L}$ from 80 to 62 Ω and vice versa.

and distortion, the pulse width of which is exactly equal to the width of the input voltage $v_{\rm cd}$. Fig. 18(b) shows the comparison between the theoretical calculation dc component value and the experimental detection value of $v_{\rm cg3}$ versus different duty cycles $\beta_{\rm s}$. It can be seen that $v_{\rm cg3}$, the output voltage of the low-pass filter, can represent the duty cycle of the input voltage $v_{\rm cd}$. When the system operates stably, the driver signals, the voltage $v_{\rm cd,}$ and current $i_{\rm rs}$ are as shown in Fig. 18(d). As shown in Fig. 18(d), the current $i_{\rm rs}$ leads to the voltage $v_{\rm cd}$. It means the rectifier can realize the ZVS operation by the proposed phase-locked method.

In order to verify the dynamic performance of phase-locked method, the time-domain response experiments are carried out under different operation modes of the inverter. The input voltage V_1 is kept at 80 V, and the coefficient is $k = 0.2$. In Figs. 19–21, the inverter operates in half-bridge mode, half-full bridge mode, and full-bridge mode, respectively. In Fig. 19 (a), the inverter operates in half-bridge mode. The output current is kept at 1.5 A in CC mode, and the load resistance is changed from 30 to 25 Ω first. Then the load resistance is changed from 25 to 30 Ω. In CV mode as shown in Fig. 19 (b), the output voltage V_2 is kept at 80 V. The load resistance is changed from 80 to 62 Ω first. Then, the load resistance is changed from 62 to 80 Ω. Similarly, the



(a) (b)

Fig. 20. Inverter in full-half bridge mode. (a) CC mode, changing R_L from 30 to 25 Ω and vice versa. (b) CV mode, changing R_L from 40 to 36 Ω and vice versa.

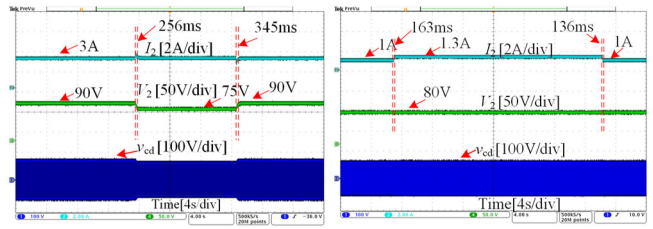


Fig. 21. Inverter in full bridge mode. (a) CC mode, changing R_L from 30 to 25 Ω and vice versa. (b) CV mode, changing R_L from 32 to 27 Ω and vice versa.

dynamic test is also done in the half-full bridge and full bridge mode. In each operation mode, the constant output current and voltage can be guaranteed through the load resistance changes suddenly.

As shown in Fig. 22, the steady-state voltage and current waveforms of the inverter and rectifier are provided with the different operation modes of the inverter when k is 0.2. When it is a heavy load, the inverter operates in full mode. When it is half load, the inverter operates in half-full bridge mode. When it is a light load, the inverter operates in half-bridge mode. All MOSFETs of the inverter and rectifier can realize the ZVS operation over a wide power range. It can be seen that the system can operate stably under different loads. Even the current distortion is very serious under light load or the load resistor has a step, the rectifier can still operate stably, synchronized with the primary side.

To verify the accuracy of the model used for analyzing the conditions for realizing ZVS operation of inverter in half-full bridge mode, the open-loop test is conducted. On the secondary side, it is uncontrolled and the rectifier serves as a passive rectifier. The theoretically calculated and experimental waveforms of currents i_{rp} are shown in Fig. 23 with the different load resistance. The input voltage V_1 is kept at 60 V, and the coefficient k is 0.2. The load resistor R_L is 40 Ω in Fig. 23(a) and 60 Ω in Fig. 23 (b).

As can be seen from Fig. 23, the theoretically calculated curves of the current i_{rp} basically coincide with the experimental curves. Therefore, the model in Fig. 8 is accurate enough for analyzing the conditions of realizing ZVS operation of the inverter. In order to evaluate the influence of harmonic components on system loss in half-full bridge mode, the power loss distribution caused by each harmonic component in the resonant network current is shown in Fig. 24 with $k = 0.2$, $R_L = 40\ \Omega$. The rectifier is uncontrolled. The power loss caused by the n_{th} harmonic

TABLE IV
PER-UNIT VALUE OF THE HARMONIC COMPONENT IN CURRENT I_{RP}

Frequency	i_{rp_pu}	i_{p_pu}	i_{s_pu}	i_{rs_pu}
$0.5f_0$	0.40	0.12	≈ 0	≈ 0
$1f_0$	1	0.75	1.13	0.67
$1.5\,f_0$	0.17	0.015	≈ 0	≈ 0
$2.5\,f_0$	0.034	≈ 0	≈ 0	≈ 0
$3\,f_0$	0.09	≈ 0	≈ 0	0.14
...				

component of current in the system is defined as

$$P_{\mathrm{Loss}}(n) = I_{\mathrm{rp}}^2(n)(R_{\mathrm{rp}} + 2R_{\mathrm{ds}}) + I_{\mathrm{p}}^2(n)R_{\mathrm{p1}} + I_{\mathrm{s}}^2(n)R_{\mathrm{s1}} + I_{\mathrm{rs}}^2(n)R_{\mathrm{rs}} \tag{41}$$

where $I(n)$ represents the nth harmonic component of the current. The per-unit value of each frequency component in the resonant current is calculated as shown in the following Table IV. The value of I_{rp} is used as the reference value for the per-unit value calculation. If the turn-OFF loss of the inverter, the loss on the parallel resonant capacitor, and the loss on the dc bus capacitors are ignored, the total loss of the system can be gained by

$$P_{\mathrm{Loss}} = \sum_{\mathrm{n}=0.5,1,1.5\ldots}^{\infty} (I_{\mathrm{rp}}^2(n)(R_{\mathrm{rp}} + 2R_{\mathrm{ds}}) + I_{\mathrm{p}}^2(n)R_{\mathrm{p1}} + I_{\mathrm{s}}^2(n)R_{\mathrm{s1}} + I_{\mathrm{rs}}^2(n)R_{\mathrm{rs}}) + 2\int_0^T |i_{\mathrm{rs}}(t)|v_{\mathrm{ds\_on}}\mathrm{d}t \tag{42}$$

where R_{p1} is the sum of ESR of the main coil L_p and the series resonant capacitor C_p on the primary side. The R_{s1} is the sum of ESR of the main coil L_s and the series resonant capacitor on the secondary side. R_{ds} represents the ON-state resistance of the MOSFETs. v_{ds_on} is the conduction voltage drop of the diode in the rectifier. All the values of ESRs are measured by the LCR meter. The ON-state resistance of the MOSFET and the conduction voltage drop of the anti-parallel diode are gained from the datasheet of the MOSFET IXTQ96N20P.

Fig. 24(a) shows that the fundamental harmonic loss dominates the total system loss. On the one hand, the loss in the main coil is the main part of the total loss of the system, while the proportion of harmonics in current through the main coil is so small that it can be ignored. On the other hand, the fundamental harmonic component still dominates the current i_{rp} and i_{rs}, although i_{rp} and i_{rs} are distorted. Therefore, the harmonic does increase the loss of the system, but the amount is very limited. The loss distribution of the system is plotted as shown in Fig. 24(b). The two graphs are gained according to the theoretical current value and the measured ESR value, rather than directly measured. It can be known from Fig. 23 that the theoretical value of current is consistent with the actual value. Therefore, the loss distribution shown in Fig. 24 can basically represent the actual loss distribution of the system.

According to the proposed control strategy, curves of T and β_s changing with the load resistance are shown in Fig. 25. The overall system efficiency curves are plotted in Fig. 26.

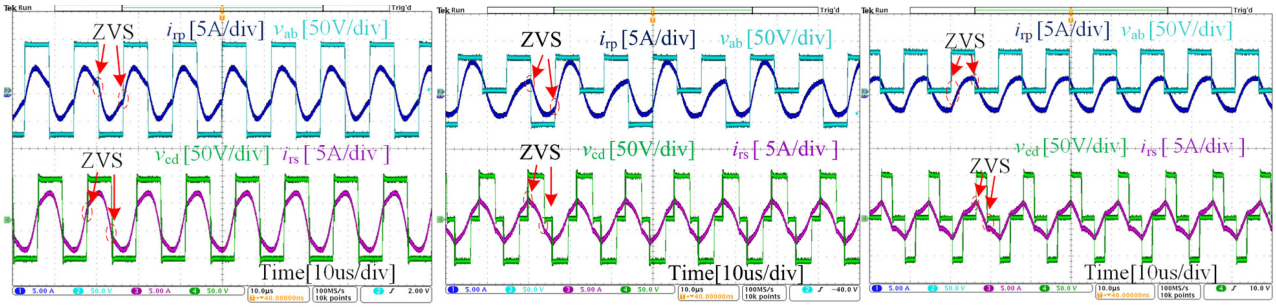


Fig. 22. Characteristic waveforms of the inverter and rectifier with $k = 0.2$. (a) Heavy load with output power $P = 239$ W, $R_L = 26\ \Omega$. (b) Half load with output power $P = 91.32$ W, $R_L = 70\ \Omega$. (c) Light load with output power $P = 42.34$ W, $R_L = 150\ \Omega$.

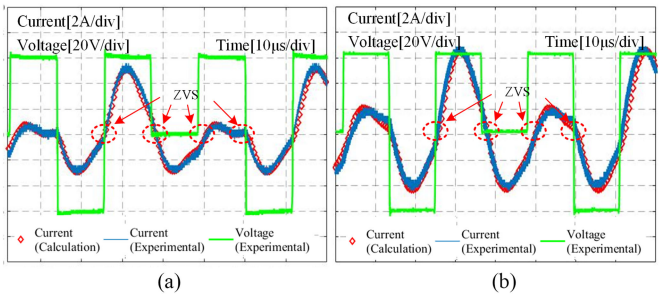


Fig. 23. Output voltage and current waveforms of inverter with $V_1 = 60$ V. (a) Load resistance $R_L = 40\ \Omega$. (b) Load resistance $R_L = 60\ \Omega$.

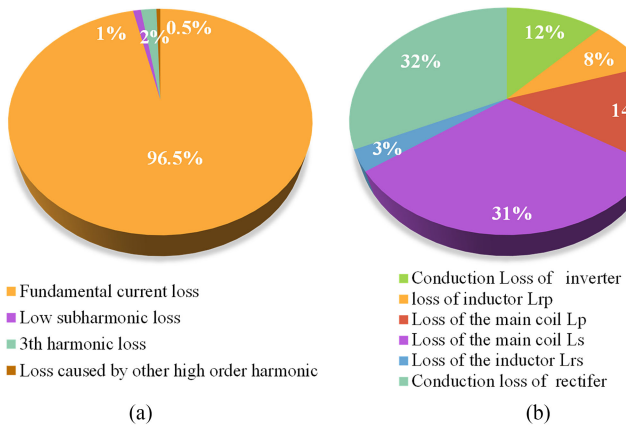


Fig. 24. Power loss distribution when it is half-full bridge mode with $R_L = 40\ \Omega$ and $k = 0.2$. (a) Proportion of the loss of each harmonic component. (b) Loss distribution of the system.

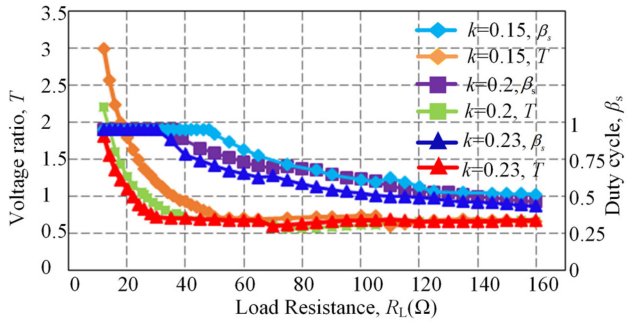


Fig. 25. Voltage ratio and duty cycle versus the load resistance.

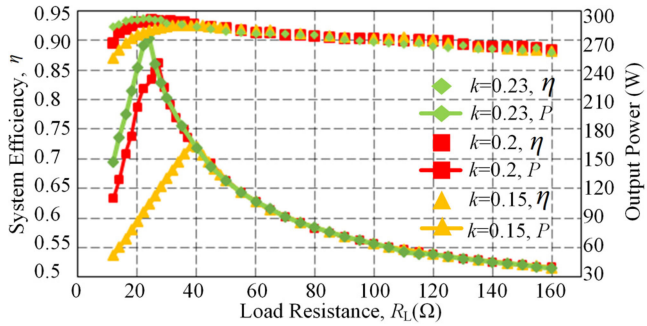


Fig. 26. System efficiency and output power versus load resistor R_L with a different coefficient.

The entire charging process of the battery is simulated by adjusting the load resistance. The electric load (IT8814C) serves as the adjustable resistor. When the load resistance is small, the system is in CC mode. The output current I_o is set 3.5, 3, and 2.1 A, respectively, when k is 0.23, 0.2, and 0.15. With the load resistance increasing, the output voltage becomes larger. When the output voltage reaches 80 V, it changes to the CV charging mode, and the voltage is kept at 80 V. The peak efficiency 93.9% is gained at 270 W with $k = 0.23$, $R_L = 22\ \Omega$. When it is light load, the system efficiency still achieves 88.07% at 40 W with $k = 0.15$, $R_L = 160\ \Omega$.

VI. Conclusion

In this article, the conditions for the optimal efficiency of the resonant network are analyzed on the premise of realizing ZVS operation of the rectifier. Then a DCS based on mode switching is proposed for optimizing the system efficiency. In this control strategy, the output voltage of the inverter can be adjusted by switching inverter operation mode to make the Z_{leq} approach the optimal load impedance during the charging process combined with the limited adjustable range of the input dc-bus voltage of the inverter. Moreover, a time-domain model is built to analyze

the conditions for realizing the ZVS operation of the inverter in different modes. The resonant network parameters design requirements are also given. Besides, a novel phase-locked method is proposed for the semi-bridgeless active rectifier control, which is simpler than the traditional phase-locked method. The output voltage or current is regulated by the active rectifier control. Through the proposed control strategy, the ZVS operation of all MOSFETs in the WPT system and the required CC/CV output can be achieved. The optimal value of load impedance can be approached simultaneously. The peak efficiency 93.9% of the WPT system is gained at 270 W with $k = 0.23$, $R_{\mathrm{L}} = 22\ \Omega$. When it is light load, the system efficiency can still achieve 88.07% at 40 W with $k = 0.15$, $R_{\mathrm{L}} = 160\ \Omega$.

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