Three-Phase Step-Up Multilevel Inverter With Self-Balanced Switched-Capacitor

Yuanmao Ye, *Member, IEEE*, Shikai Chen, Ruijie Sun, Xiaolin Wang, and Yong Yi

***Abstract*—This article presents a new three-phase multilevel inverter with boosting capability for low-voltage applications like electric vehicles and renewable energy sources. This inverter is fed by a single dc voltage source and each phase involves two low-voltage transistors, two high-voltage transistors, two diodes, and two capacitors. Except that the two high-voltage transistors withstand twice the dc input voltage, all other components are rated to the dc input voltage. With phase-disposition pulsewidth modulation, the two types of high- and low-voltage transistors operate in low and high switching frequencies, respectively. This is very beneficial for reducing switching losses and selecting semiconductor switches. The two capacitors are connected in parallel and series alternately with the dc source resulting in high ac output voltage with multiple levels, self-balanced capacitor voltages as well as low voltage ripples. The topology, operation principle, capacitors' voltage ripples and power loss are analyzed in detail. Both simulation and experimental results are provided to demonstrate the feasibility of the proposed inverter.**

***Index Terms*—Multilevel inverter (MLI), pulsewidth modulation (PWM), switched-capacitor.**

I. Introduction

AS THE inherent advantages of reduced switching stresses *dv/dt*, near-sinusoidal output voltage waveforms and operation with lower switching frequency, etc., multilevel inverters (MLIs) have attracted the wide attention of industrial and research communities [1], [2]. Since Nabae *et al.* [3], [4] invented the neutral-point-clamped (NPC) inverter in 1979, Meynard and Foch invented the flying capacitor (FC) inverter in 1992, both NPC and FC inverters have caused a substantial attention for researchers globally and they have already been put into commercial use. However, the two types of MLIs suffer from the problems of unbalanced capacitor voltages and complex clamping circuits. In 1995, Peng *et al.* [5] presented cascaded H-bridge (CHB) inverter for static var generation, and Hammond [6] promoted it successfully for medium-voltage high-power motor driver. As each H-bridge is fed by a dc source, the CHB inverter requires multiple isolated dc sources. In recent years, the modular multilevel converter (MMC) presented by Marquardt [7] in 2003 is also very popular and it has been applied in HVdc applications.

A common feature for these classic MLIs is that none of them have the voltage-boosting capability. For instance, the amplitude of ac output line voltages for NPC, FC, and MMC is equal to the dc input voltage, whereas the amplitude of ac output phase voltages for CHB is equal to the sum voltage of all isolated dc sources used to feed H-bridges in each phase. This makes these classic MLIs very suitable for high- and medium-voltage applications.

Nowadays, with the rapid development of electric vehicles (EVs) and renewable energy source (RES) like solar panels and fuel cells, boosting-type inverters play a critical role in these low-voltage applications where the dc source's low voltage needs to be boosted and then inverted to a high ac voltage to drive a motor or connect to the grid. The commercialized solution for this type of inverters is to cascade boosting-type dc–dc converter with a conventional two-level inverter. In this system, all transistors employed in the two-level inverter have to withstand high voltage and operate in high switching frequency resulting in more switching loss and serious EMI problem [8], [9]. To overcome this issue, a new type of MLIs based on switched capacitor (SC) technology has been proposed in recent years [10]–[21].

Different from NPC, FC, CHB, and MMC that have been commercialized in medium- and high-voltage applications, SC-based MLIs (SCMLIs) are mainly developed for low-voltage application as they have the advantages of voltage-boosting capability and self-balanced capacitors' voltages. For instance, the series/parallel SCMLI presented by Hinago and Koizumi in [10] is capable of generating $2n+3$ levels of ac output voltage and each level is equal to the dc input voltage, here n is the number of SC cells. In addition, all capacitors' voltages of this SCMLI are balanced automatically without the use of auxiliary balancing circuits and control algorithms.

So far, various SCMLIs are mainly introduced as single-phase structures and the most popular type of SCMLIs is developed by cascading an SC-based dc–dc multilevel conversion circuit with an inverting H-bridge. Different dc levels are generated by the front-side circuit, while ac output voltage is achieved by the end-side H-bridge. Specifically, a general series/parallel SC dc–dc multilevel circuit and its simplified version as well as an improved structure are used to feed H-bridges in [10]–[12]. In [13] and [14], SC-based voltage doubler is used as the front-side of five-level inverting units. In [15], the front-side of a

Manuscript received June 15, 2020; revised August 21, 2020 and October 19, 2020; accepted December 18, 2020. Date of publication December 24, 2020; date of current version March 5, 2021. This work was supported by the National Natural Science Foundation of China under Grant 51907033. Recommended for publication by Associate Editor Y. Li. *(Corresponding author: Xiaolin Wang.)*

The authors are with the School of Automation, Guangdong University of Technology, Guangzhou 510006, China (e-mail: eeyeym@gdut.edu.cn; 199031391@qq.com; 1129209335@qq.com; xiaolinwang@gdut.edu.cn; yiyongshanxi@126.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2020.3047198.

Digital Object Identifier 10.1109/TPEL.2020.3047198

seven-level inverter is implemented by an SC-based voltage tripler. In [16] and [17], a bridge modular SC network and a cross-switched SC circuit are developed as front-side circuits to feed H-bridges. Another popular type of SCMLIs is developed by inserting an SC-based dc–dc multilevel conversion circuit between two half-bridges [18]–[21]. In this type of SCMLIs, different voltage levels are also generated by the SC dc–dc conversion circuit while the two half-bridges are responsible for alternating polarity. Compared with the former type of SCMLIs, only two high-voltage semiconductor switches are required while another inverting half-bridge withstands low voltage stress. The both types of SCMLIs are developed specifically for single-phase applications. Because the voltages across the inverting H-bridge and/or half-bridges are varied, it is difficult to extend these single-phase SCMLIs to three-phase configurations directly by increasing the number of inverting legs. In contract, the classic MLIs like NPC, FC, and MMC use a stable dc bus voltage provided by a single dc source to feed phase-leg, the number of phases can be changed very flexible by changing the number of phase-legs. Of course, three-phase SCMLI configurations can be easily implemented by connecting three single-phase circuits in "Y" structure. Taking the conventional series/parallel SCMLI [10], the boost SCMLI [19], the quadruple boost SCMLI [21], the FC-clamped SCMLI [28], [29] and the cross-switched SCMLI [17] as examples, their three-phase topologies configured in "Y" structure are illustrated in Fig. 1(a) to (e), respectively. It indicates that each phase needs at least one dc source and the "Y" structure comes at the cost of complex structure and more components.

Otherwise, more effort is needed to reconstruct these SCMLIs for three-phase applications, and the corresponding new modulation logic and analysis need to be developed as well. For instance, Fig. 2(a) illustrated a new single-source three-phase SCMLI derived from the conventional series/parallel structure [10]. Compared with Fig. 1(a) of which each phase voltage has seven different levels, the new three-phase SCMLI has different output levels and other features as well, so that new modulation logic and design philosophy also need to be developed accordingly. Similarly, Fig. 2(b) shows another new three-phase SCMLI derived from the boost structure [19]. It is obvious that it has different features from Fig. 1(b). Hence, the modulation logic and analysis given in [19] cannot be applied in this three-phase SCMLI directly.

In this article, a new SCMLI is developed to convert a single dc source's low voltage to three-phase high ac voltages with four levels per phase. As each phase has two transistors withstanding twice the input voltage, the proposed three-phase SCMLI is actually not suitable for high-voltage applications. However, it has the advantages of voltage-boosting capability, simple circuit configuration, and self-balanced capacitors' voltages. These features make the proposed inverter expected to be a new member of three-phase MLIs, mainly used for low-voltage applications such as EV, solar panels, and fuel cells, rather than a competitor of the conventional MLIs. With phase-disposition pulsewidth modulation (PD-PWM), two types of high- and low-voltage transistors employed in the proposed SCMLI operate in low and high switching frequencies, respectively, so that the switching loss is reduced. Moreover, capacitor's voltage ripples and the harmonics of output voltages are reduced as well. Both simulation and experimental results are provided to demonstrate the effectiveness of the three-phase SCMLI.

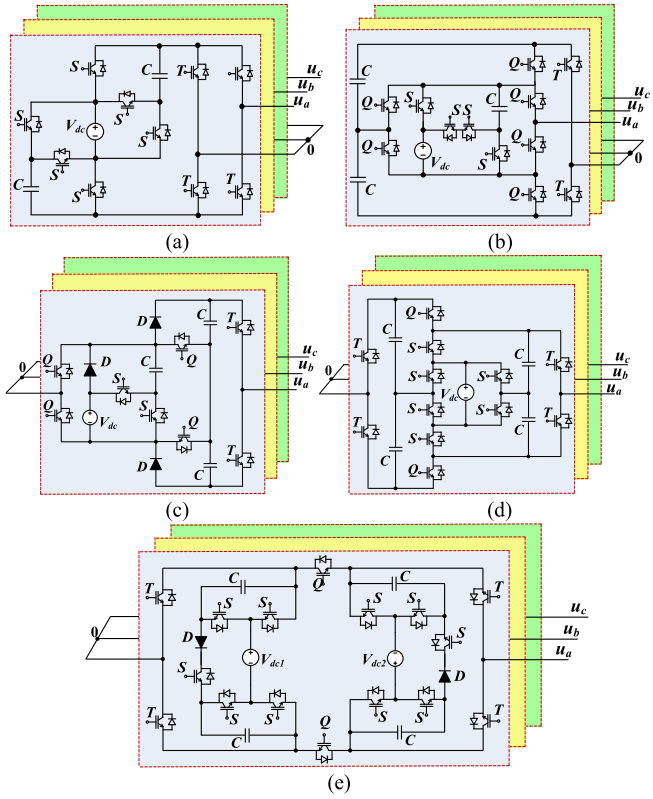


Fig. 1. Three-phase topologies configured in "Y" structure for the existing SCMLIs. (a) Series/parallel SCMLI [10]. (b) Boost SCMLI [19]. (c) Quadruple boost SCMLI [21]. (d) FC-clamped SCMLI [28], [29]. (e) Cross-switched SCMLI [17].

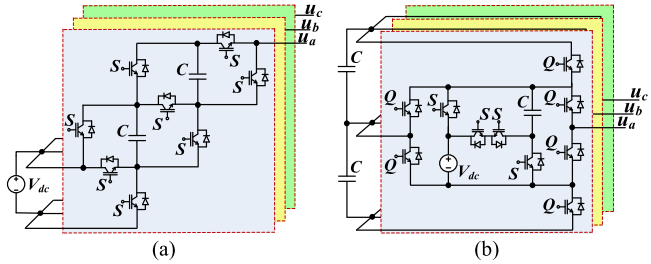


Fig. 2. Three-phase topologies derived from the existing SCMLIs. (a) Series/parallel SCMLI [10]. (b) Boost SCMLI [19].

II. Topology of the Proposed SCMLI

A. Circuit Description

The proposed three-phase SCMLI is shown in Fig. 3. Its three phases have the same circuit configuration and they are powered by a dc voltage source V_{dc}. Its neutral point is provided by two dc-link capacitors C_1 and C_2 withstanding the same voltage stress of 0.5 V_{dc}. Compared with the conventional two-level half-bridge inverter, each phase of the proposed inverter has one

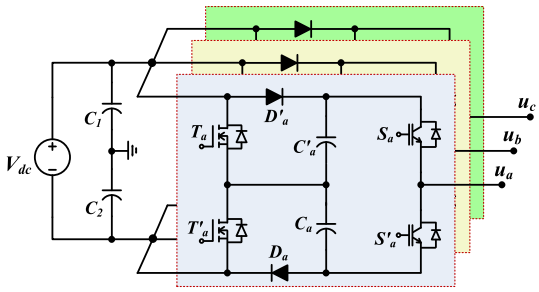


Fig. 3. Circuit configuration of the proposed three-phase SCMLI.

TABLE I
SWITCHING STATES OF THE PROPOSED SCMLI, $X = A$, B, AND C

Switching states	Switches				Capacitors		Output
	T_x	T'_x	S_x	S'_x	C_x	C'_x	u_x
1	1	0	1	0	C	D	$+1.5V_{dc}$
2	0	1	1	0	—	C	$+0.5V_{dc}$
3	1	0	0	1	C	—	$-0.5V_{dc}$
4	0	1	0	1	D	C	$-1.5V_{dc}$

more SC unit inserted between the dc source and the inverting half-bridge. The SC unit consists of one half-bridge, two diodes, and two capacitors. Hence, two half-bridges are employed in each phase of the proposed SCMLI and each half-bridge is made up of two complementary operating transistors.

When the transistor T_x is turned ON while T'_x is OFF, the capacitor C_x is charged by the dc source through the diode D_x, where $x = a$, b, and c. This makes the capacitor voltage V_{Cx} equal to V_{dc}. Similarly, C'_x is charged to V_{dc} through D'_x when T'_x is turned ON while T_x is OFF. All components employed in this SC unit are rated to the dc input voltage V_{dc}.

In addition, the inverting half-bridge is connected in parallel with the series-connection of C_x and C'_x. The voltage stress of S_x and S'_x is therefore $2V_{dc}$. Each of them can also be implemented by two series-connected transistors so that all components employed in the SCMLI are rated to V_{dc}.

B. Operation Principle

To facilitate the following analysis, all components employed in the proposed SCMLI are seen as ideal and the capacitors C_1, C_2, C_x, and C'_x are so large that their voltages are constant at $0.5V_{dc}$ and V_{dc}, respectively.

As each half-bridge is controlled by a pair of complementary signals and there are two half-bridges in each phase, there are a total of four switching states as illustrated in Table I. Note that 1 and 0 represent ON and OFF states of the related transistor, respectively. Capacitors' states are indicated by "C," "D," and "—" which are indicative of charging, discharging, and idle states, respectively. As a result, the proposed inverter is capable of generating four different output levels that are $\pm 0.5V_{dc}$ and $\pm 1.5V_{dc}$. Compared with the traditional two-level inverter of which each phase is capable of generating the levels of $\pm 0.5V_{dc}$, the proposed inverter not only has the boosting ability, but also can generate more ac voltage levels.

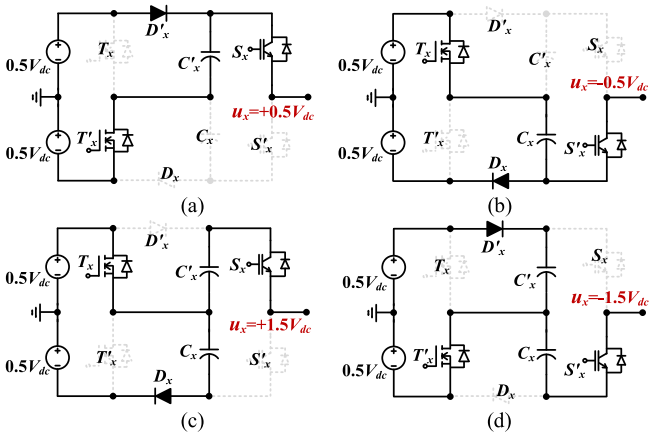


Fig. 4. State circuits for one phase of the proposed SCMLI, $x = a$, b, and c. (a) $u_x = +0.5V_{dc}$. (b) $u_x = -0.5V_{dc}$. (c) $u_x = +1.5V_{dc}$. (d) $u_x = -1.5V_{dc}$.

1) $u_x = +0.5V_{dc}$: When the switches S_x and T'_x are turned ON while T_x and S'_x are OFF, the output level $+0.5V_{dc}$ is directly provided by the capacitor C_1 through the diode D'_x and the switch S_x, as shown in Fig. 4(a). The same output level can also be provided by the reverse series connection of C'_x and C_2 for inductive loads. In this state, C'_x is charged by the dc source while C_x is idle.
2) $u_x = -0.5V_{dc}$: When the switches T_x and S'_x are turned ON while S_x and T'_x are OFF, the output level $-0.5V_{dc}$ is directly provided by C_2 through the diode D_x and the switch S'_x, as shown in Fig. 4(b). The same output level can also be provided by the reverse series connection of C_1 and C_x for inductive loads. In this state, C_x is charged by the dc source while C'_x is idle.
3) $u_x = +1.5V_{dc}$: When the switches S_x and T_x are turned ON while S'_x and T'_x are OFF, the output level $+1.5V_{dc}$ is provided by the series connection of C_1 and C'_x, as shown in Fig. 4(c). In this state, C_x is charged by the dc source while C'_x discharges to loads.
4) $u_x = -1.5V_{dc}$: When the switches S'_x and T'_x are turned ON while S_x and T_x are OFF, the output level $-1.5V_{dc}$ is provided by the series connection of C_2 and C_x, as shown in Fig. 4(d). In this state, C'_x is charged by the dc source while C_x discharges to loads.

C. Self-Balance of Capacitor Voltages

As analyzed before, the transistors T_x and T'_x operate in a complementary manner, the capacitors C_x and C'_x are alternately charged by the dc source through the diode D_x and D'_x, respectively. Their voltages can therefore be balanced to the dc input voltage V_{dc} automatically.

III. MODULATION OF THE PROPOSED SCMLI

For the proposed SCMLI, various modulation strategies like multicarrier PWM and space vector modulation can be applied to control its output voltage. In this section, only PD-PWM strategy is adopted to illustrate the operation of the proposed SCMLI.

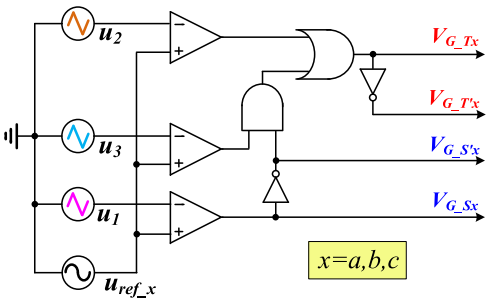


Fig. 5. Modulation logic of the proposed SCMLI with PD-PWM.

Figs. 5 and 6 show the modulation logic and typical waveforms of the proposed three-phase SCMLI with the PD-PWM strategy. There are three carrier signals u_1, u_2, and u_3, which are compared with the reference signals u_{ref_a}, u_{ref_b}, and u_{ref_c} to generate the gating signals $V_{G\_Sa,b,c}$ and $V_{G\_Ta,b,c}$. Specifically, the gating signals V_{G_Sx} is generated by comparing the reference signal u_{ref_x} with the bipolar carrier signal u_1, where again $x = a$, b, and c. According to Table I, the transistor T_x is turned ON when $u_{ref\_x}>u_2$ or $u_1>u_{ref\_x}>u_3$. Its gating signal V_{G_Tx} is therefore the comparing result of the reference signal with the three carriers as illustrated in Fig. 5.

The waveforms of Fig. 6 shows that the high-voltage transistors $S_{a,b,c}$ and $S'_{a,b,c}$ operate in lower switching frequency while the low-voltage transistors $T_{a,b,c}$ and $T'_{a,b,c}$ operate in higher switching frequency. This is very beneficial for either the selection of transistors or the reduction of switching losses. For instance, MOSFETs with low ON-resistance and fast turn-ON/OFF speed can be used as the low-voltage transistors while IGBTs can be used as the high-voltage transistors.

As a result, there are seven different levels for the line voltages u_{ab}, u_{bc}, and u_{ca} of the proposed SCMLI as illustrated in the bottom of Fig. 6. And the amplitude of the line voltages is three times the dc input voltage, i.e., $3V_{dc}$. This makes the line voltages closer to sinusoidal waveforms than the conventional two-level inverter and a low dc voltage source can be used to power the three-phase inverter.

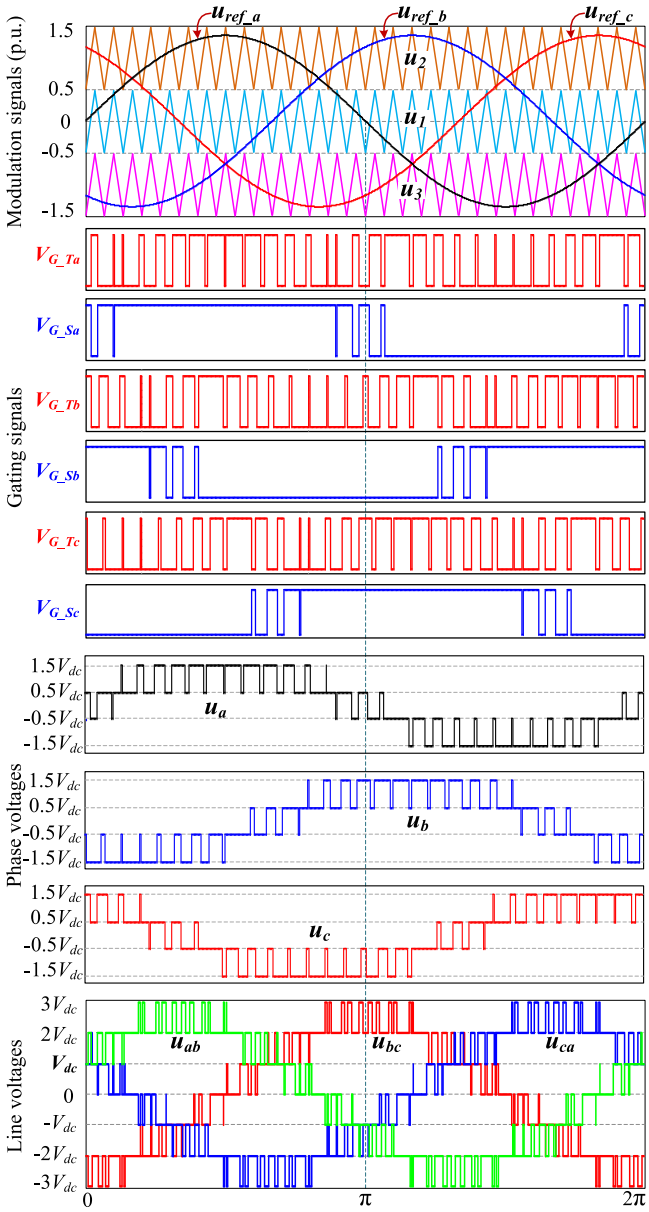


Fig. 6. Typical waveforms of the proposed SCMLI with PD-PWM.

IV. Capacitance Determination

A. Switched Capacitors

In the proposed SCMLI, the SCs C_x and C'_x are used as dc voltage sources to generate different output levels. Their voltages will drop when they discharge to loads.

With the PD-PWM, the capacitors operate alternately between charging and discharging modes at the carriers' frequency. As the effect of the total parasitic resistance r_{Cr} including the ESR of capacitors, on-resistance of switches as well as the internal-impedance of the dc source, voltage ripples of C_x and C'_x in three different cases are illustrated in Fig. 7.

The best case is that r_{Cr} is so small that the capacitors can be fully charged to V_{dc} every time, as illustrated in Fig. 7(a). It means that the time constant of the charging loops is smaller than a quarter of the shortest charging duration when the reference signal u_{ref_x} reaches to its amplitude A_{ref}, i.e., $r_{Cr}C_x<(1.5\text{-}A_{ref})/(4f_C)$, wherein f_C is the carriers' frequency. Under the premise that the carriers' frequency is far higher than the reference signals' frequency, the load current i_x can be seen as constant in each period of carrier frequency, the capacitors' voltage ripples are determined by the integral of the load current i_x and the duty ratio d for each charging interval as well as the capacitance, i.e.,

$$\Delta V_{Cx} = \frac{Q_x}{C_x} = \frac{i_x(t) \times d(t)}{C_x f_C} = \frac{I_O \sin(\omega t - \varphi)}{C_x f_C}\left[A_{ref}\sin(\omega t) - 0.5\right] \quad (1)$$

where I_O and ω are, respectively, the amplitude and angular frequency of the output current, φ is the phase difference between the output voltage and the output current.

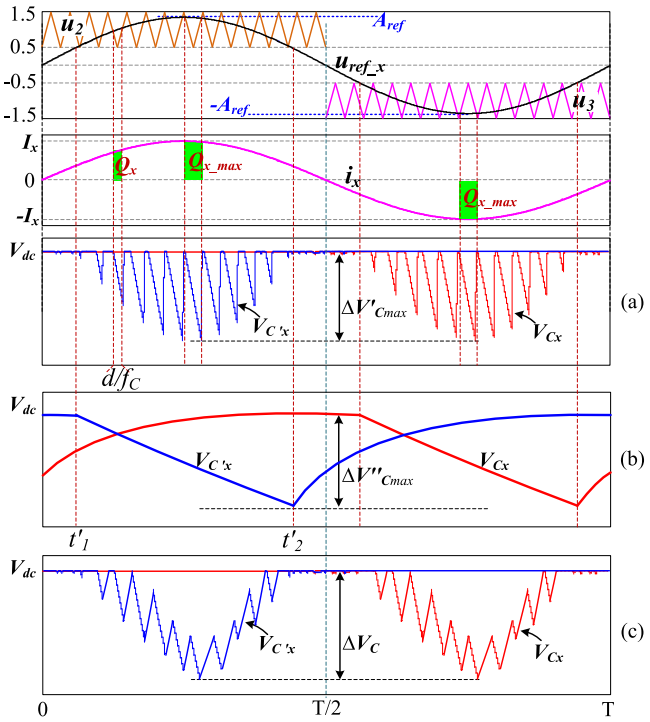


Fig. 7. Capacitors' voltage ripples of the proposed SCMLI. (a) Best case. (b) Worst case. (c) In practice.

For loads with a power factor of 1, the maximum voltage ripple $\Delta V'_{Cmax}$ is found in the interval when u_{ref_x} reaches to its amplitude A_{ref}. The output current also reaches to I_O in this discharging interval. As a result, the maximum voltage ripple is calculated by

$$\Delta V'_{Cmax} = \frac{Q_{x\_max}}{C_x} = \frac{A_{ref} - 0.5}{C_x f_C} I_O. \tag{2}$$

The worst case is that r_{Cr} is too large to effectively charge the related capacitor when $|u_{ref\_x}|>0.5$, as illustrated in Fig. 7(b). It means that $r_{Cr}C_x$ is far greater than the longest charging duration when u_{ref_x} is just above 0.5, i.e., $r_{Cr}C_x >> 1/f_C$. In this case, the maximum voltage ripple is estimated by

$$\Delta V''_{Cmax} = \frac{Q'_x}{C_x} = \frac{1}{C_x}\int_{t'_1}^{t'_2} i_x dt = \frac{I_O}{\pi f_{ref} C_x A_{ref}} \sqrt{A_{ref}^2 - 0.25} \tag{3}$$

where $t'_1 = [\sin^{-1}(0.5/A_{ref})]/(\pi f_{ref})$, $t'_2 = 1/(2f_{ref}) - t'_1$.

In practice, the parasitic resistance should be as small as possible but it cannot be infinitely small. The maximum capacitors' voltage ripple is therefore between above two cases, i.e., $\Delta V'_{Cmax} < \Delta V_{Cmax} < \Delta V''_{Cmax}$ as illustrated in Fig. 7(c). As a result, the capacitance C_x can be estimated by

$$\frac{1.5M - 0.5}{f_C \Delta V_{Cmax}} I_O \leq C_x < \frac{I_O}{1.5M\pi f_{ref} \Delta V_{Cmax}} \sqrt{2.25M^2 - 0.25} \tag{4}$$

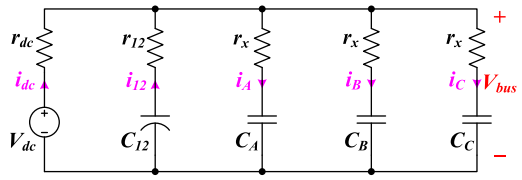


Fig. 8. Charging network for capacitors of three-phase operation.

where $M = A_{ref}/1.5$ is the modulation ratio. The voltage ripple ratio $\Delta V_{Cmax}/V_{dc}$ is usually set to 5% or 10%.

B. DC-Link Capacitors

As shown in Fig. 4, in each phase, there is always one SC, which is connected in parallel with the dc source to charge at any time. For three-phase operation, there are therefore three SCs connected in parallel with the dc source and the dc-link capacitors, as shown in Fig. 8, wherein C_A, C_B, and C_C represent C_a or C'_a, C_b or C'_b, and C_c or C'_c, $C_{12} = C_1/2 = C_2/2$, r_{12} is the ESR of the dc-link capacitors C_{12}, r_{dc} is the internal impedance of the dc source, r_x is the sum of ESR for each of C_x and C'_x, and ON-resistance for each of T_x and T'_x.

By setting $r_{dc} = k \times r_{12}$ and applying the Kirchhoff's voltage law to Fig. 8, the virtual bus voltage V_{bus} can be derived as

$$V_{bus}(t) = \frac{r_x [V_{dc} + kV_{C12}(t)] + kr_{12} \sum V_{Cx}(t)}{3kr_{12} + (1+k) r_x} \tag{5}$$

where x in ΣV_{Cx} represents A, B, and C. The currents flowing output of the dc source and the dc-link capacitors are therefore given by

$$i_{dc}(t) = \frac{r_{12} [3V_{dc} - \sum V_{Cx}(t)] + r_x [V_{dc} - V_{C12}(t)]}{[3kr_{12} + (1+k) r_x] r_{12}} \tag{6}$$

$$i_{12}(t) = \frac{kr_{12} [3V_{C12}(t) - \sum V_{Cx}(t)] + r_x [V_{C12}(t) - V_{dc}]}{[3kr_{12} + (1+k) r_x] r_{12}}. \tag{7}$$

And, the total charging current $\Sigma i_x = i_A + i_B + i_C = i_{dc} + i_{12}$ is

$$\sum i_x(t) = \frac{[3V_{dc} - \sum V_{Cx}(t)] + k[3V_{C12}(t) - \sum V_{Cx}(t)]}{3kr_{12} + (1+k) r_x}. \tag{8}$$

When the internal impedance of the dc source is far smaller than the ESR of C_{12}, i.e., $k<<1$, almost all charging current is provided by the dc source and the dc-link capacitor is idle. In this case, the inrush current is totally limited by the parasitic resistance r_x, and it is independent of the values of the dc-link capacitors.

Otherwise, the dc-link capacitors can be used to absorb the inrush charging current partially. Considering the initial voltage of the dc-link capacitors is same as the dc input voltage V_{dc}, the initial values of the currents are given by

$$\begin{cases} i_{dc}(0) = \frac{\sum \Delta V_{Cx}}{3kr_{12} + (1+k) r_x} \\ i_{12}(0) = \frac{k \sum \Delta V_{Cx}}{3kr_{12} + (1+k) r_x} \\ \sum i_x(0) = \frac{(1+k) \sum \Delta V_{Cx}}{3kr_{12} + (1+k) r_x} \end{cases} \tag{9}$$

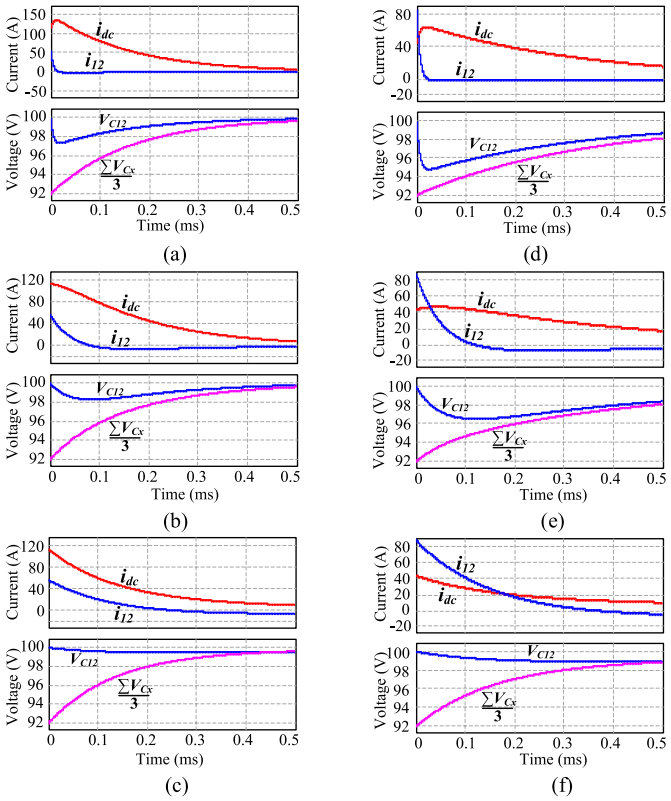


Fig. 9 Variations of the charging currents and capacitor voltages. (a) $k = 0.5$, $C_{12} = 100$ μF. (b) $k = 0.5$, $C_{12} = 1000$ μF. (c) $k = 0.5$, $C_{12} = 10000$ μF. (d) $k = 2$, $C_{12} = 100$ μF. (e) $k = 2$, $C_{12} = 1000$ μF. (f) $k = 2$, $C_{12} = 10000$ μF.

where ΔV_{Cx} is the voltage ripple of SCs.

Considering that the currents i_{C12} and i_x have opposite reference directions in Fig. 8, the rate of change for the current i_{dc} is derived from (6), i.e.,

$$\frac{di_{dc}(t)}{dt} = \frac{r_x C_x i_{12}(t) - r_{12} C_{12} \sum i_x(t)}{C_x C_{12} [3kr_{12} + (1+k) r_x] r_{12}}. \quad (10)$$

According to the above analysis, variations of the inrush charging currents and the capacitor voltages are determined by the resistance r_{dc}, r_{12}, r_x, the capacitance C_{12}, C_x, and the voltage ripple of capacitors together. For instance, with the parameters of $r_{12} = 0.04\ \Omega$, $r_x = 0.1\ \Omega$, $C_x = 1000\ \mu$F, $V_{dc} = V_{C12}(0) = 100$ V, $V_{CA}(0) = 90$ V, $V_{CB}(0) = 91$ V, and $V_{CA}(0) = 95$ V, the simulation results with different values of C_{12} and $k = r_{dc}/r_{12}$ are shown in Fig. 9. The results are consistent with (9), i.e., the initial values of the charging currents are determined by the resistance and the voltage ripple of capacitors, and the ratio $i_{dc}(0)$:$i_{12}(0) = r_{12}$:$r_{dc} = 1$:k. Moreover, the variation trend of the current i_{dc} is related to the capacitance C_{12} and C_x, as described by (10). Specifically, when the dc-link capacitor C_{12} is so small that the numerator on the right side of (10) is positive, the current r_{dc} will rise first and then fall, as depicted in Fig. 9(a) and (d). In the rise stage, the maximum changing rate is found at the start moment. In order to suppress the inrush charging current of the dc source effectively, the numerator on the right side of (10) should be negative at the start moment. As a result,

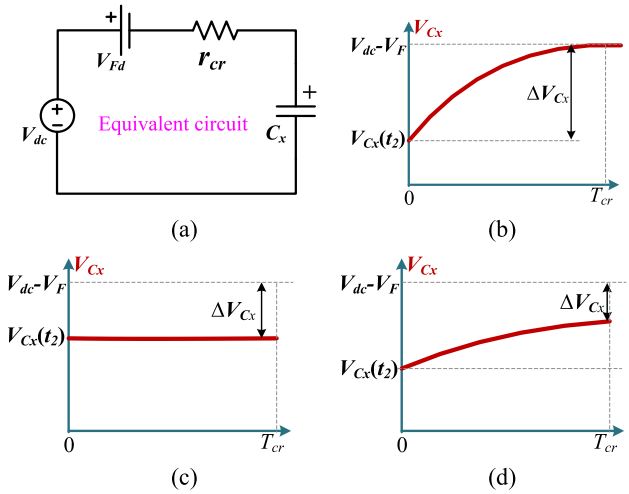


Fig. 10. Charging circuit and voltage variation for individual SC. (a) Equivalent charging circuit. (b) Full charge. (c) No effective charge. (d) Partial charge.

the value of the dc-link capacitors is derived as

$$C_1 = C_2 = 2C_{12} > \frac{2r_x i_{12}(0)}{r_{12} \sum i_x(0)} C_x = \frac{2kr_x}{(1+k) r_{12}} C_x \quad (11)$$

where again r_{12} is the total ESR for C_1 and C_2, k is the ratio of the internal impedance of the dc source to r_{12}, r_x is the sum of the ESR for each of C_x and C'_x, and ON-resistance for each of T_x and T'_x.

V. Power Loss Analysis

The proposed SCMLI operates alternately in charging and discharging processes of capacitors. In a charging process, the power loss is determined by the difference of charging voltage and capacitors' initial voltage, and it is absorbed by parasitic resistors of switches and capacitors in the charging loop. In a discharging process, the power loss is mainly determined by the load current which is provided by the capacitors. This loss is also absorbed by parasitic resistors of the discharging loop. Hence, all power loss of the SCMLI can be classified into three categories of charging loss of capacitors, conduction loss caused by the load current, and switching loss of transistors.

A. Charging Loss of Capacitors

As shown in Fig. 4(b) and (c), the capacitor C_x is charged by the dc source through the transistor T_x and the diode D_x. The charging loop can be equivalent to the circuit of Fig. 10(a) by ignoring the influence of the dc-link capacitors, where V_{Fd} is the forward voltage drop of D_x, r_{cr} is the charging loop's impedance including on-resistance of T_x and ESR of C_x. As the charging loss is absorbed by parasitic resistors of the charging loop, it also analyzed according to the three cases shown in Fig. 7.

For the best case when $r_{cr}C_x$ is so small that the capacitor can be fully charged to V_{dc}–V_F every time, as illustrated in

Fig. 10(b), energy loss in one charging process is given by

$$\Delta E_{cr} = V_{Fd}\, C_x \Delta V_{Cx} + \frac{1}{2} C_x \Delta V_{Cx}^2 \tag{12}$$

where ΔV_{Cx} is the voltage difference of the capacitor at start and end moments of the charging process.

As illustrated in Table I, when the phase voltage u_x is switched between $-0.5V_{dc}$ and $-1.5V_{dc}$, the capacitors C_x operates alternately in charging and discharging modes at the carriers' frequency f_C. During one cycle of the output voltage, the number of charging/discharging cycles for the capacitor C_x can therefore be expressed by

$$n_{Cx} = \frac{f_C}{f_{ref}} \left(\frac{1}{2} - \frac{1}{\pi} \arcsin \frac{1}{2A_{ref}} \right) \tag{13}$$

where again A_{ref} and f_{ref} are, respectively, the amplitude and frequency of the reference signal, and f_C is the carriers' frequency.

As a result, the charging loss of the capacitor C_x for the best case is given by

$$P_{Cx\_min} = f_{ref} C_x \sum_{k=1}^{n_{Cx}} \left(V_{Fd} \Delta V_{Cx\_k} + \frac{1}{2} \Delta V_{Cx\_k}^2 \right) \tag{14}$$

where ΔV_{Cx_k} is a voltage ripple occurred in the kth charging process of the capacitor C_x.

For the worst case, r_{Cr} is too large so that there is little current charged into the capacitors in each pulse charging duration, as shown in Fig. 10(c). C_x and C'_x can only be replenished in the positive and negative half-cycles of the output voltage, respectively, as illustrated in Fig. 7(b). In this case, the charging loss of the capacitor C_x is given by

$$P_{Cx\_max} = f_{ref} C_x \left(V_{Fd} \Delta V''_{Cmax} + \frac{1}{2} \Delta V''^2_{Cmax} \right). \tag{15}$$

As analyzed before, as r_{Cr} cannot be infinitely small and the pulse charging duration is varied, the capacitors are charged partially in many cases, as illustrated in Fig. 10(d). Hence, the charging loss in practice should be between (14) and (15).

B. Conduction Loss Caused by Load Currents

At any time, one of the two IGBTs S_x and S'_x is turned ON to provide path for the load current i_x. Conduction loss caused by the three inverting half-bridges is therefore given by

$$P_{Con\_S} = 3 I_{AV} V_{Fs} \tag{16}$$

where I_{AV} is the average value of phase currents in half-cycle and V_{Fs} is the voltage drop of one IGBT.

In one cycle of the output voltage, the amount of charge flowing into a capacitor is equal to that flowing out of it. This means that all output current has to flow through the diodes. Conduction losses caused by the diodes is therefore given by

$$P_{Con\_D} = 3 I_{AV} V_{Fd} \tag{17}$$

where V_{Fd} is the voltage drop of one diode.

For the phase voltage $u_x = \pm 1.5V_{dc}$, the load current i_x flows through one of the MOSFETs T_x and T'_x. Conduction loss caused by the MOSFETs is therefore given as

$$P_{con\_T} = \begin{cases} 0, & u_x = \pm 0.5V_{dc} \\ 3 r_T i_x^2, & u_x = \pm 1.5V_{dc} \end{cases} \tag{18}$$

where r_T is ON-resistance of one MOSFET.

C. Switching Loss of Transistors

Usually, the switching loss of a transistor can be estimated by two ways. One way is based on the overlap of the transistor's current and voltage at switching instants [22]. Another way is based on the transistor's parasitic capacitance C_{OSS} and its voltage stress V_{DS} as well as the switching frequency f_S [23], i.e.,

$$P_S = C_{oss} {V_{DS}}^2 f_S \tag{19}$$

For the proposed SCMLI, two types of transistors with the voltage stresses of $2V_{dc}$ and V_{dc} are employed. As shown in Figs. 5 and 6, the gating signals for the low-voltage transistors T_x and T'_x are the comparison result of the reference signals and the three carriers. Their switching frequency is therefore the same as the carriers' frequency f_C. In one cycle of the output voltage, the number of state switching for each of the high-voltage transistors S_x and S'_x is given by

$$n_{Sx} = \frac{2 f_C}{\pi f_{ref}} \arcsin \frac{0.5}{A_{ref}}. \tag{20}$$

As a result, the total switching loss of all transistors employed in the proposed SCMLI is expressed as

$$P_{sw} = 6 \left(f_C C_{oss\_T} + n_{Sx} f_{ref} C_{oss\_S} \right) {V_{dc}}^2 \tag{21}$$

where C_{OSS_T} and C_{OSS_S} are the parasitic capacitances for one MOSFET and one IGBT, respectively.

VI. Comparison With Other Three-Phase MLIs

As analyzed before, the boost capability of this inverter makes it possible to convert low dc input voltage to high ac output voltage. In contrast, the classic MLIs like NPC and FC do not have boost capability, but they have been commercialized in medium-voltage high-power ac motor drivers. Hence, it is actually difficult to fairly compare the proposed inverter with the traditional four-level MLIs. Nevertheless, this section still attempts to compare their differences and their advantages by designing a 660V/1140V-55 kW motor driver.

First, the NPC and FC as well as their derivation topologies like the nested NPC (NNPC) [24], the hybrid-clamped (HC) [25] and the active NPC (ANPC) [26], [27] have the same boosting factor of 0.5. Their dc input voltage is therefore required to be about 1612 V. For the proposed inverter, as it has a boosting factor of 1.5, its dc input voltage is about 537 V.

In order to realize this motor driver with four-level output voltage, all components in the NPC (18 transistors, 18 diodes, and 3 capacitors), in the FC (18 transistors and 9 capacitors), in the NNPC (18 transistors, 6 diodes, and 6 capacitors), and in the HC (24 transistors and 6 capacitors) withstand the same voltage stress of 537 V. In the ANPC, 12 low-voltage transistors and 3 capacitors have the same voltage stress of 537 V while other 6

TABLE II
COMPARISON OF 660 V-55 kW MOTOR DRIVER WITH DIFFERENT TOPOLOGIES

4-level MLIs	NPC	FC	NNPC [24]	HC [25]	ANPC [26, 27]	SCMLI
No. of transistors	18	18	18	24	24	18
No. of diodes	18	0	6	0	0	6
No. of cap.	3	9	6	6	3	6
Total components	39	27	30	30	27	30
DC voltage (V)	1612	1612	1612	1612	1612	537
Boosting factor	0.5	0.5	0.5	0.5	0.5	1.5
DC-link cap. (μF)	3000	---	---	3000	3000	1333
Flying cap. (μF)	---	2214	2214	2214	---	---
Switched cap. (μF)	---	---	---	---	---	6000
Energy of cap. (J)	432	319	319	751	432	1057
Cost/size	High	Low	Med.	Med.	Low	Med.
Efficiency	High	High	Med.	Low	Low	Med.

high-voltage transistors withstand the voltage stress of 1074 V. Similarly, in the proposed inverter, 6 low-voltage transistors and 6 capacitors as well as 6 diodes have the same voltage stress of 537 V, while other 6 high-voltage transistors withstand the blocking voltage of 1074 V. As analyzed in [27], each high-voltage transistor aforementioned can be replaced with a series connection of two low-voltage transistors so that all components in these compared four-level inverters have the same voltage stress of 537 V. As a result, the numbers of transistors required in the ANPC and the proposed MLI are 24 and 18, respectively. If the cost and volume of the motor driver are roughly judged based on the total number of components, both of the FC and ANPC have the lowest cost and the smallest size, while the highest cost and the greatest size are found in the NPC. The proposed inverter has the same cost/size as the NNPC and HC. In addition, as the NPC and FC have been commercialized, the specialized components and design processes are very mature, there is no doubt that they have very high efficiency. If only the power loss caused by the switching components is considered, the NNPC and the proposed MLI should have higher efficiency than the HC and ANPC as they have fewer active switches which consume conduction loss, switching loss, and driving loss.

In the FC, NNPC, and HC, the numbers of FCs are 9, 6, and 3, respectively, while there are 6 SCs employed in the proposed inverter. Based on the assumptions of 1 kHz carrier frequency and 10% voltage ripple ratio of capacitors, the total capacitance of all FCs in each MLI is calculated by the [28, (7)]. According to (4), the value of each SC should be between 732 μF and 3.1 mF. The total capacitance of 6 mF is therefore used in the proposed inverter. And according to (11), the dc-link capacitor C_{12} is estimated as 1333 μF by setting $r_x = 0.1\ \Omega$, $r_{12} = 0.05\ \Omega$, and $k = 0.5$. In the NPC, HC, and ANPC, three dc-link capacitors are required and each of them is set to 1000 μF. As a result, energy stored in all capacitors of each MLI is estimated by ignoring their voltage ripple.

All compared items aforementioned are listed in Table II. It indicates that the proposed four-level SCMLI has the advantages of simple structure and boosting capability, while its main drawback is the use of large capacitors. Overall, it is a competitive circuit to implement this motor driver. Especially, its boosting ability make it very suitable for EV motor drivers of which dc input voltage is provided by series-connected batteries. On the other hand, the use of two high-voltage transistors in each phase makes this inverter very difficult in medium- and high-voltage applications. In contrast, as multiple semiconductors are connected in series to withstand the dc input voltage, the NPC and FC are considered as a very attractive solution for medium-voltage applications. Hence, the proposed SCMLI will not actually become a competitor of the existing MLIs, but as a new member mainly used for low-voltage applications such as EV, PV, and fuel cells.

TABLE III
COMPARISON OF THE PROPOSED INVERTER WITH OTHER WORKS

Inverters	DC sources	Transistors	Diodes	Cap.	Boost factor
[8]	1	21	3	3	1
[17]	6	27.9	1.7	3.5	3
[19]	3	31.3	0	6.5	4
[28] [29]	3	28.7	0	7.8	4
[10]	3	31.3	0	3.5	3
SCMLI	1	18	6	6	1.5

A brief comparison between the proposed four-level inverter and the SC-based boost inverter of [8] is also made by designing the 660 V/1140 V-55 kW motor driver. To get the line voltage of 1140 V, the dc bus voltage V_{PN} of the boost inverter in [8] is need to be about 1612 V and its dc input voltage is therefore 806 V which is higher than the proposed inverter's input voltage 537 V. Although both inverters have six high-voltage transistors, the voltage stress of each high-voltage transistor in [8] is 1612 V while that in the proposed inverter is 1074 V. The six high-voltage transistor's switching frequency in [8] is the same as carriers' frequency while that in the proposed inverter is much lower as illustrated in Fig. 6. Of course, the boost inverter of [8] requires only two low-voltage transistors, two capacitors, and two diodes, and their voltage stress is 806 V. In contrast, the proposed inverter requires six low-voltage transistors, six capacitors, and six diodes, but their voltage stress is 537 V. If we calculate an equivalent number of transistors by dividing the total voltage of transistors by a reference voltage of 537 V, the equivalent number is 21 for [8] and is 18 for the proposed inverter. Similarly, the equivalent numbers of diodes and capacitors are also calculated as given in Table III. Overall, although the proposed inverter requires more components, it has higher boost factor and provides four-level output voltage making it has better output voltage quality than the two-level inverter of [8]. And the lower switching frequency of the six high-voltage transistors contributes to lower switching loss than [8]. In addition, the equivalent numbers of components for multiple existing SCMLIs configured in "Y" structure are also listed in Table III. Specifically, the third column of Table III is for the three-phase 13-level inverter shown in Fig. 1(e) which has been verified by simulation and experiment in [17]. There are six isolated dc sources with the same voltage of 156 V employed to meet the phase voltage of 660 V. The fourth column is for the three-phase inverter of Fig. 1(b), and components for the three-phase inverter of Fig. 1(d) are given in the fifth column, wherein three isolated dc sources with the same voltage of 234 V are employed in the two structures to meet the phase peak voltage of 934 V. The sixth column of Table III is for the three-phase series/parallel seven-level inverter of Fig. 1(a) and there are three isolated dc sources with the same voltage of 312 V. As all these SCMLIs

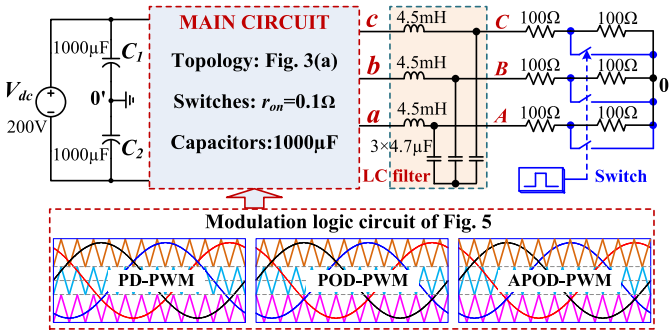


Fig. 11. Diagram and parameters for the simulation model.

require dc-link capacitors, there is no comparison of this item in Table III. Overall, the three-phase SCMLIs configured by the existing SCMLIs in "Y" structure are capable of providing higher boost factor, but this is at the cost of more dc sources and complex circuit structures.

VII. Simulation and Experiment

A. Simulation Results

In order to verify the feasibility of the proposed three-phase SCMLI, a simulation model was built in PSIM9.0. As shown in the diagram of Fig. 11, the main circuit is built by referring the circuit configuration of Fig. 3. The dc input voltage is 200 V, all capacitors used in the simulation model are 1000 μF, and the on-resistance of each switch is 0.1 Ω which represents the total parasitic resistance of capacitors' charging loops. An *LC* filter (4.5 mH+4.7 μF) is added to suppress the higher harmonics of the output voltage. In order to test the dynamic response of the inverter, the load *R* is switched between 100 and 200 Ω. The PWM modulation circuit is built by referring the logic circuit of Fig. 5. Three types of PD-PWM, POD-PWM, and APOD-PWM are applied to control the simulation model, wherein the carriers' frequency $f_C = 5$ kHz and the reference signal's frequency $f_{ref} = 50$ Hz, the modulation index $M = A_{ref}/1.5 = 1.4/1.5 = 0.933$. Simulation results are shown in Figs. 12 and 13.

With the PD-PWM modulation strategy, simulation waveforms of the output voltages $u_{a0'}$, $u_{b0'}$, $u_{c0'}$, u_{ab}, u_{bc}, u_{ca} and the load voltages u_{A0}, u_{B0}, u_{C0}, u_{AB}, u_{BC}, u_{CA}, the capacitor voltages V_{Ca}, $V_{C'a}$, V_{Cb}, $V_{C'b}$, V_{Cc}, $V_{C'c}$, the load currents, and the transistors' currents are illustrated in Fig. 12. The rms values of the four types of output and load voltages are 213.7, 352, 198.1, 342.9 V when $R = 200$ Ω, and are 213.3, 351.2, 197.5, 342 V when $R = 100$ Ω. It indicates that the output voltages and the load voltages are very stable when the load currents i_A, i_B, i_C change dynamically. Although the ripples of capacitor voltages increase along with the load currents, they are also very stable and are balanced automatically. As more power is required to replenish larger voltage ripples of capacitors, the capacitor's charging currents flowing through the transistors T_x and T'_x also rise along with the load currents.

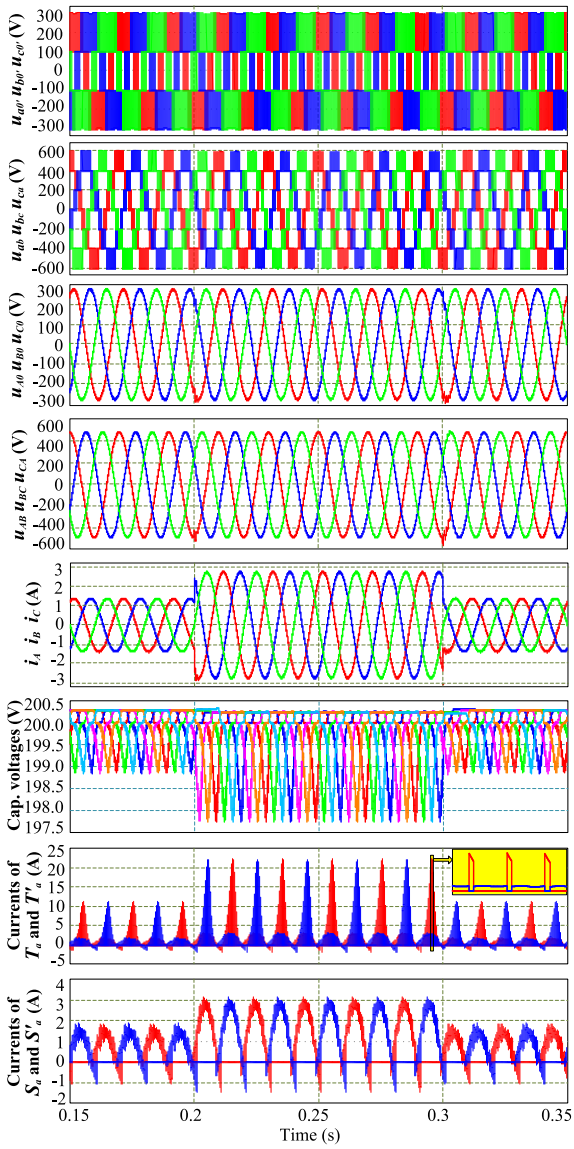


Fig. 12. Simulation waveforms of the three-phase four-level inverter with PD-PWM and dynamic loads.

With the three different types of SPWM modulation strategies, FFT analysis results of the output voltage and load voltages are given in Fig. 13. It indicates that there is the same output phase voltage for the three types of SPWM. However, the PD-PWM is much better than the POD-PWM and APOD-PWM in the aspects of waveform shape and THD of the output line voltages. As the higher harmonics of the output voltages have been suppressed by the *LC* filter, the load voltage waveforms are almost purely sinusoidal and there are only a few lower harmonics. Especially, the THDs for both load phase voltage and line voltage of PD-PWM are only 0.6%. Overall, the three types of SPWM can be used to modulate the proposed inverter, but the PD-PWM has better performance than POD-PWM and APOD-PWM.

Fig. 14 shows the results when a three-phase inductive load 100 Ω-50 mH is used to replace the *LC* filter and the pure resistive

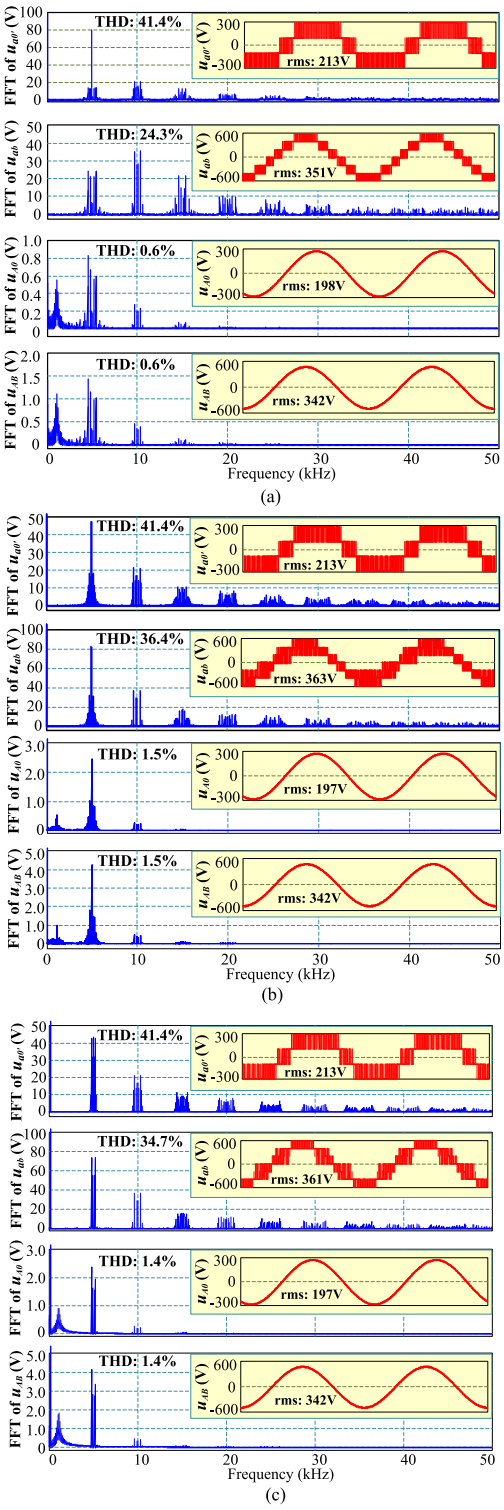


Fig. 13. FFT analysis of output and load voltages of the three-phase four-level inverter. (a) With PD-PWM. (b) With POD-PWM. (c) With APOD-PWM.

load in the simulation model of Fig. 11. It indicates that both phase-voltage and line-voltage are the same as that for pure resistive loads, and the load currents are almost pure sinusoidal waveforms. As capacitors absorb reactive power of the inductive load, their voltages are above 200 V sometimes but the ripples are very limited.

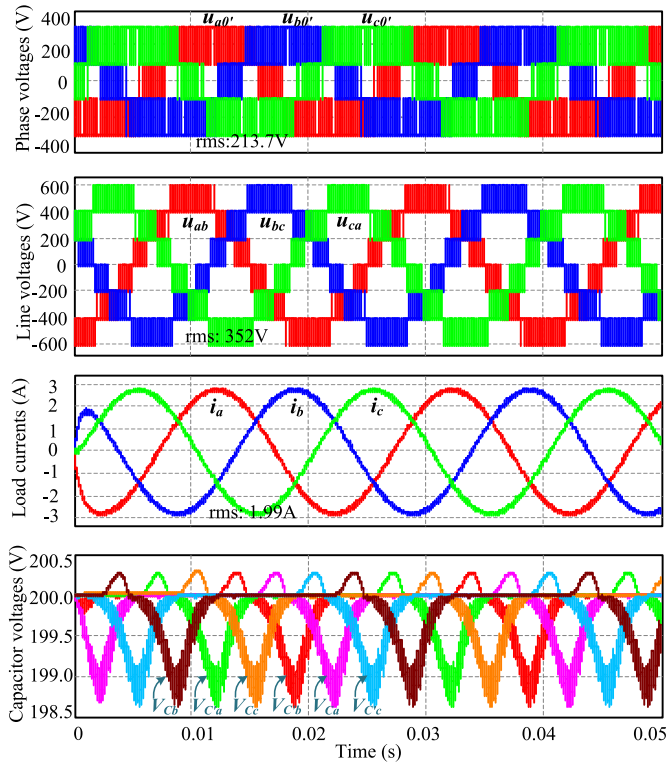


Fig. 14. Simulation waveforms for an inductive load 100 Ω-50 mH.

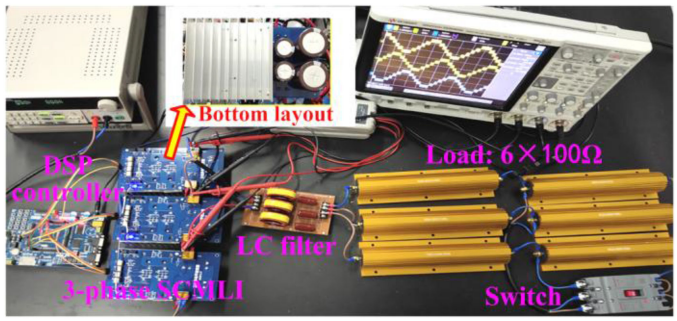


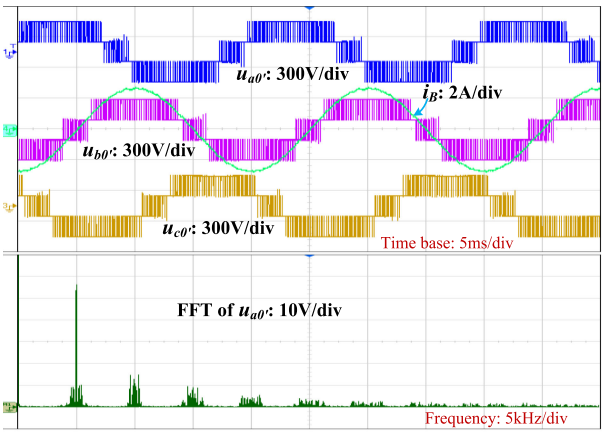
Fig. 15. Experimental bench for the three-phase SCMLI.

TABLE IV
SPECIFICATION AND COMPONENTS OF THE THREE-PHASE PROTOTYPE

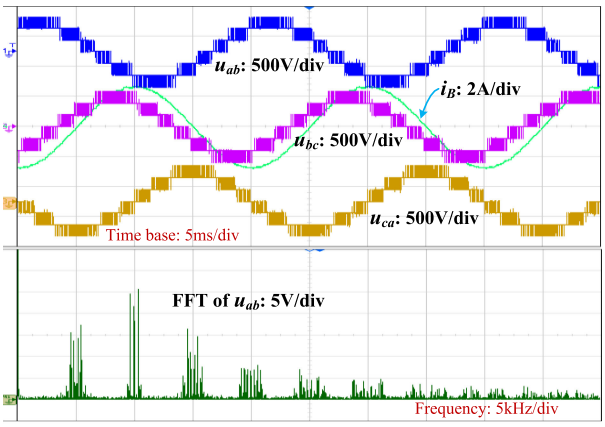
Input voltage (V_{dc})	200VDC
Frequency of output voltage f_{ref}	50 Hz
Frequency of carriers f_C	5 kHz
C_a, C_b, C_c, C'_a, C'_b, C'_c	1000μF
S_a, S_b, S_c, S'_a, S'_b,S'_c (IGBT)	IRG4PC40S
T_a, T_b, T_c, T'_a, T'_b, T'_c (MOSFET)	IRFP4868PBF
D_a, D_b, D_c, D'_a, D'_b, D'_c (Diode)	SBR40U300CT
LC filter	3×(4.5mH+4.7μF)

B. Experimental Results

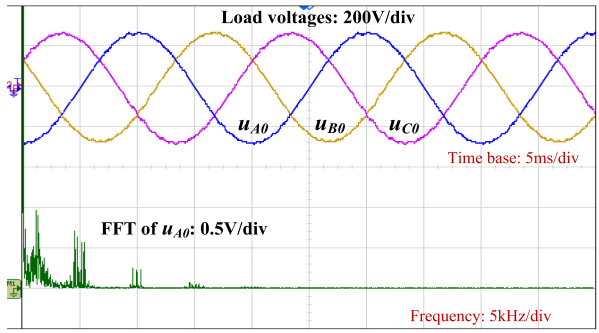
By referring the configuration of the upper part of Fig. 11, a prototype of the proposed three-phase SCMLI was also built in the laboratory. Fig. 15 shows the experimental bench, wherein the main power circuit was designed with the specification and



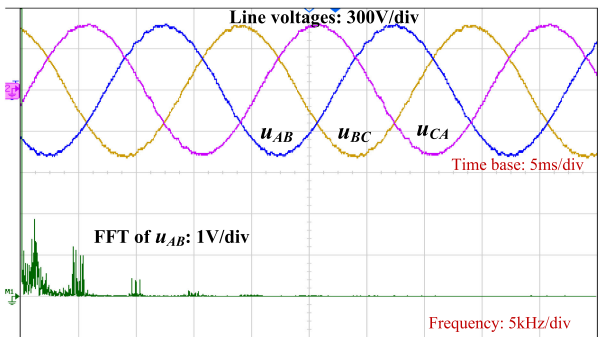
(a)



(b)

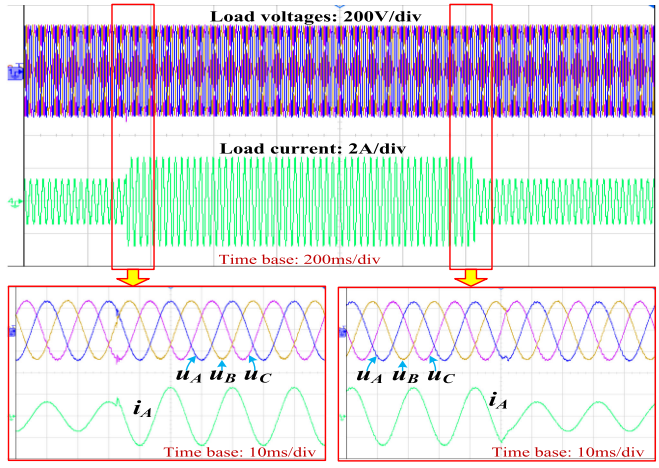


(c)

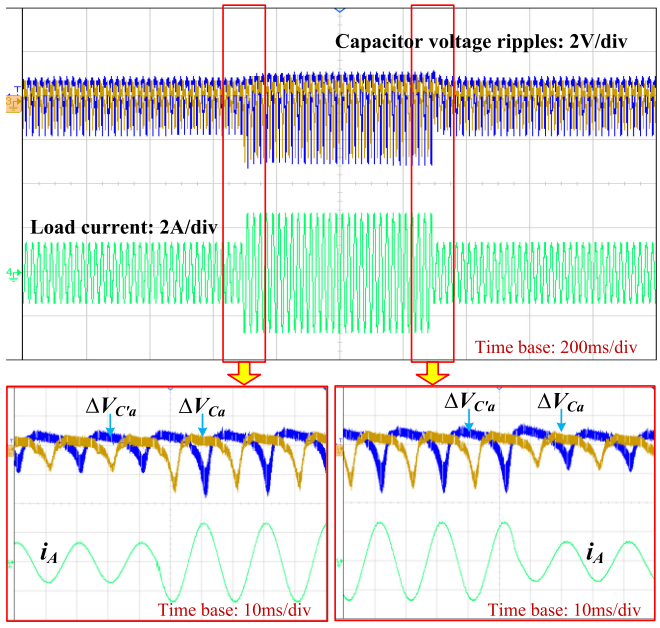


(d)

Fig. 16. Experimental results of the three-phase SCMLI. (a) Output phase voltages. (b) Output line voltages. (c) Load phase voltages. (d) Load line voltages.



(a)



(b)

Fig. 17. Experimental results with dynamic loads. (a) Load voltages. (b) Capacitors' voltages.

components given in Table IV. The value of the capacitors was calculated by (4), wherein $M = 0.93$, $I_O = 2.79$ A, and $\Delta V_C = 10$ V. According to the simulation result, the PD-PWM has better performance than other two SPWM algorithms. It was therefore adopted to modulate the proposed inverter and it was implemented in TMS320F28335.

Fig. 16 shows the experimental results of the three-phase SCMLI when $R = 100\ \Omega$ and the modulation index is set to 0.933. Specifically, the output phase voltages $u_{a0'}$, $u_{b0'}$, $u_{c0'}$ and the corresponding FFT analysis are illustrated in Fig. 16(a). The rms value is about 209 V and the harmonics are mainly distributed around the carrier frequency 5 kHz and its integer multiple. This is consistent with the simulation results given in Fig. 13(a). Fig. 16(b) shows the output line voltages u_{ab}, u_{bc}, u_{ca} and the corresponding FFT analysis. The rms value is about

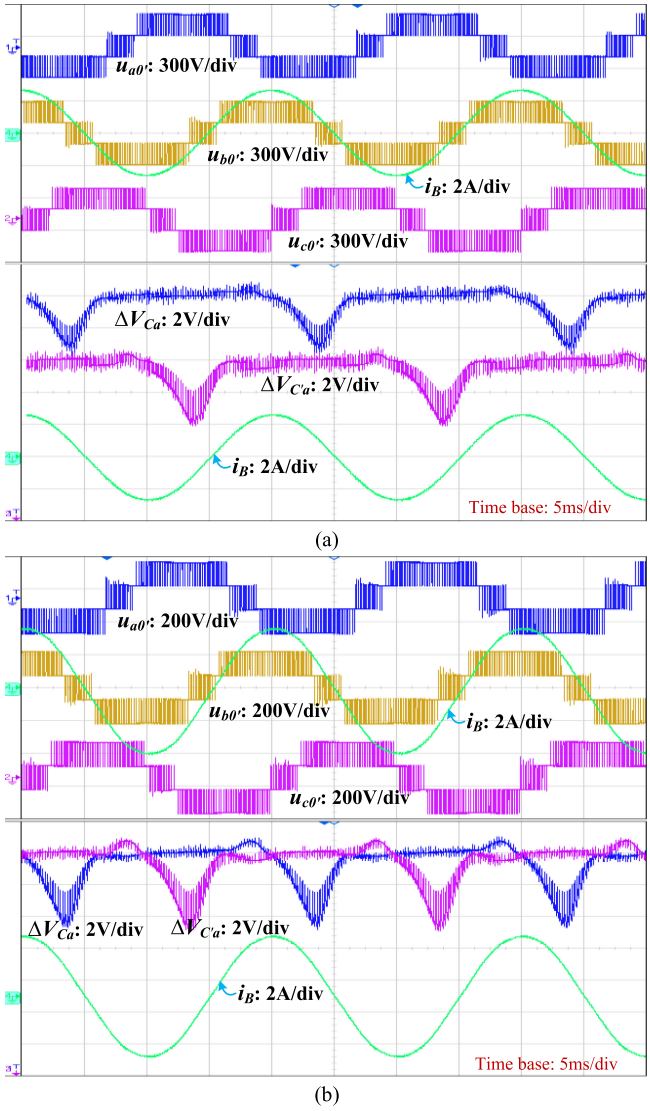


Fig. 18. Experimental results with *RL* loads. (a) $V_{dc} = 200$ V, *RL* = 100 Ω−50 mH. (b) $V_{dc} = 150$ V, *RL* = 50 Ω-50 mH.

340 V and the distribution of the harmonics is the same as the simulation result.

The load phase voltages u_{A0}, u_{B0}, u_{C0} and the line voltages u_{AB}, u_{BC}, u_{CA} as well as their FFT analysis are shown in Fig. 16(c) and (d). Their rms values are about 190 V and 330 V, respectively. The same as the simulation, all load voltages are sinusoidal and there are only a few lower harmonics. This is benefited from the new topology and the PD-PWM strategy which eliminates the main lower harmonics, as well as the *LC* filter which suppresses the higher harmonics.

When the load is changed between 100 and 200 Ω, the load voltages u_{A0}, u_{B0}, u_{C0} and the capacitors' voltages V_{Ca}, $V_{C'a}$ are illustrated in Fig. 17(a) and (b), respectively. It indicates that the load voltages are very stable when the load current changes dynamically. Similar to the simulation result of Fig. 12, the ripples of capacitors' voltages increase along with the rise of the load current, but they are also very stable and are balanced automatically.

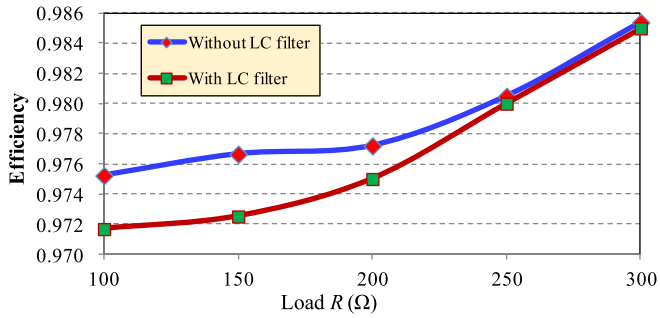


Fig. 19. Measured efficiency of the prototype with varied loads.

Fig. 18(a) shows the output phase voltages $u_{a0'}$, $u_{b0'}$, $u_{c0'}$ and the capacitor voltages V_{Ca}, $V_{C'a}$ when the prototype without *LC* filter is used to power a three-phase inductive load 100 Ω-50 mH. When the load is changed to 50 Ω-50 mH and the dc input voltage drops to 150 V, the experimental waveforms are shown in Fig. 18(b). The results indicate that the load current is almost pure sinusoidal and the output voltage is normal PWM waveform. The same as the simulation result given in Fig. 14, capacitor voltages are slightly higher than their rated value sometimes as they absorb reactive power of the inductive load.

Finally, when the pure resistive load was changed from 100 to 300 Ω, in 50 Ω increments, the efficiency of the three-phase prototype was tested as given in Fig. 19. As the test is based on the load's power and the source's power, the efficiency of the prototype with an *LC* filter is slightly lower than that without the filter. However, when the output power is changed from 384 to 1176 W, the efficiency in both cases is always higher than 0.97, and the peak value is up to 0.985. The high efficiency is first due to the low voltage ripple of capacitors, and second the low-frequency operation of the high-voltage switches.

VIII. Conclusion

A switched-capacitor-based three-phase four-level inverter is introduced in this article. Capacitors employed in this inverter operate alternately in charging and discharging modes resulting in self-balanced voltages and low voltage ripples. And they are connected in parallel and series alternately with a dc voltage source to generate high ac output voltage with multiple levels. Different from the classic MLIs which have been commercialized in medium- and high-voltage applications, both simulation and experimental results verified that the proposed inverter has boosting capability and self-balanced capacitors' voltages. It is therefore more suitable for low-voltage applications like motor drivers in EVs and grid-connected interfaces for RESs. Simulation and experimental results also prove its high efficiency and excellent performance under dynamic loads.

References

[1] H. Akagi, "Multilevel converters: Fundamental circuits and systems," in *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
[4] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Specialists Conf.*, Jun./Jul. 1992, pp. 397–403.
[5] F. Z. Peng, J. S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," in *Proc. IEEE/IAS Annu. Meeting*, Orlando, FL, USA, Oct. 1995, pp. 2541–2548.
[6] P. W. Hammond, "A new approach to enhance power quality for medium voltage drives," in *Proc. Ind. Appl. Soc. 42nd Annu. Petroleum Chem. Ind. Conf.*, Sep. 1995, pp. 231–235.
[7] R. Marquardt, "Modular multilevel converters: State of the art and future progress," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 24–31, Dec. 2018.
[8] T. Tran, M. Nguyen, T. Duong, J. Choi, Y. Lim, and F. Zare, "A switched-capacitor-voltage-doubler based boost inverter for common-mode voltage reduction," *IEEE Access*, vol. 7, pp. 98618–98629, 2019.
[9] Y. Zhou and W. Huang, "Single-stage boost inverter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1885–1893, Apr. 2012.
[10] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.
[11] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.
[12] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series-parallel conversion with less number of components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016.
[13] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.
[14] J. Liu, K. W. E. Cheng, and Y. Ye, "A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4219–4230, Aug. 2014.
[15] W. Peng, Q. Ni, X. Qiu, and Y. Ye, "Seven-Level inverter with self-balanced switched-capacitor and its cascaded extension," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11889–11896, Dec. 2019.
[16] L. He and C. Cheng, "A bridge modular switched-capacitor-based multilevel inverter with optimized SPWM control method and enhanced power-decoupling ability," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6140–6149, Aug. 2018.
[17] T. Roy, P. K. Sadhu, and A. Dasgupta, "Cross-switched multilevel inverter using novel switched capacitor converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8521–8532, Nov. 2019.
[18] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi, and E. Pouresmaeil, "A novel step-up single source multilevel inverter: Topology, operating principle, and modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, Apr. 2019.
[19] Y. Nakagawa and H. Koizumi, "A boost type nine-level switched capacitor inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6522–6532, Jul. 2019.
[20] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.
[21] J. Liu, W. Lin, J. Wu, and J. Zeng, "A novel nine-level quadruple boost inverter with inductive-load ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4014–4018, May 2019.
[22] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.
[23] M. K. Kazimierczuk, "Switching losses with linear MOSFET output capacitance," in *Pulse-Width Modulated DC–DC Power Converters*, 1st ed. West Sussex, U.K.: Wiley, 2008, pp. 37–38, ch. 2, sec. 2.2.9.
[24] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec. 2014.
[25] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A Four-level hybrid-clamped converter with natural capacitor voltage balancing ability," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1152–1162, Mar. 2014.
[26] X. Yuan, "Derivation of voltage source multilevel converter topologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 966–976, Feb. 2017.
[27] K. Wang, Z. Zheng, and Y. Li, "Topology and control of a four-level ANPC inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2342–2352, Mar. 2020.
[28] L. He and C. Cheng, "A flying-capacitor-clamped five-level inverter based on bridge modular switched-capacitor topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, Sep. 2016.
[29] C. Cheng and L. He, "Flying-capacitor-clamped five-level inverter based on switched-capacitor topology," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–5.

Yuanmao Ye (Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Jinan, Jinan, China, in 2007, the M.Sc. degree in control science and engineering from the South China University of Technology, Guangzhou, China, in 2010, and the Ph.D. degree in electrical engineering from the Hong Kong Polytechnic University, Hong Kong, in 2016.

From September 2010 to January 2014, he was with the Department of Electrical Engineering, the Hong Kong Polytechnic University, as a Research Assistant. He is currently a Full Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China. His research interests include multilevel inverters, switched-capacitor technique and its applications, and battery management systems.

Shikai Chen was born in Shanwei, China, in 1996. He received the B.Sc. degree in electrical engineering from the Guangdong Polytechnic Normal University, Guangzhou, China, in 2018. He is currently working toward the M.Sc. degree with the Guangdong University of Technology, Guangzhou, China.

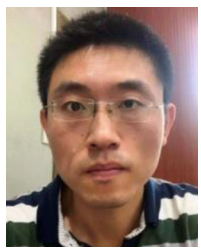
His research interests include multilevel inverters, dc–dc power converters and intelligent control for renewable energy power generation.

Ruijie Sun was born in Jieyang, China, in 1997. He received the B.Sc. degree in electrical engineering and automation in 2020 from the Guangdong University of Technology, Guangzhou, China, where he is currently working toward the M.Sc. degree with the School of Automation.

His research interests include multilevel inverters and switched-capacitor technique.

Xiaolin Wang received the B.Sc. degree in electrical engineering and automation from Three Gorges University, Yichang, China, in 2012, the M.Sc. and Ph.D. degrees from The Hong Kong Polytechnic University, Hong Kong, in 2013 and 2018, respectively.

She is currently an Assistant Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China. Her research interests include battery management systems, multilevel inverters, distribution system planning and vehicle to grid (V2G).



Yong Yi received the B.Sc. degree from the University of Jinan, Jinan, China, in 2007, the M.Sc. degree from the University of Shanghai for Science and Technology, Shanghai, China, in 2010, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2017, all in electrical engineering.

He is currently an Associate Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China. His research interests include electromagnetic environment, corona discharges, and multilevel inverters.