Temperature Influence on the Accuracy of the Transient Dual Interface Method for the Junction-to-Case Thermal Resistance Measurement

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***Abstract*—The transient dual interface method (TDIM), proposed by the JEDEC 51-14 standard [1], determines the junction-to-case thermal resistance of power electronics with the separate point of two transient thermal impedance curves under different contact conditions. However, the influence of the junction temperature is not considered and this underestimates the actual value with earlier separation point. This phenomenon is presented first with experimental results at different junction temperatures. Electro-thermal finite element simulations and simulation with semiconductor physical behavior in the devices simulations are performed to explain the root reason. After that, the improved TDIM with the junction temperature compensation is proposed to improve the accuracy. The experimental results show that the improved TDIM improves the accuracy of about 9.5% for 600-V discrete IGBT devices.**

***Index Terms*—Junction-to-case thermal resistance, simulation, temperature compensation, transient dual interface method (TDIM).**

I. Introduction

THE accurate measurement of the junction-to-case thermal resistance of power electronics becomes more critical for power modules with increased power density, such as new generations of power insulated gate bipolar transistors (IGBTs) modules [2]. It is important not only for manufacturers to improve the internal structure to decrease the junction temperature but also for users to optimize the performance without exceeding the allowed temperature range [3].

There are two most commonly used methods: traditional thermocouple method (also called the steady-state *method*) and transient dual interface method (also called the transient method), shortened TDIM in this article [1], [4]. The steady-state method was recommended by the IEC, MIL standards [5], and JEDEC51-1 standard [6]. With the power dissipation P [W] of the device under test (DUT), the junction temperature T_j [°C] and case temperature T_c [°C], the steady-state junction-to-case thermal resistance R_{thjc} [K/W] can be obtained by (1) [7]. The junction temperature is determined by the $V_{\mathrm{CE}}(T)$ method [8] according to the standard. The case temperature is obtained by the thermocouple located directly below the DUT case surface, which is also clearly specified in the AGQ324 standard [9]. However, the case temperature determination causes some errors from the thermocouple, such as the clamping force for a fixture, thermal grease, mounting conditions, etc., [10]

$$R_{\mathrm{thjc}} = \frac{T_j - T_c}{P}. \tag{1}$$

In 2010, the JEDEC51-14 standard [1] specified the TDIM without thermocouple to overcome those disadvantages for the reproducible measurement of the junction-to-case thermal resistance of semiconductor devices with a 1-D conductive heat flow path. The brief review of this method, before it was classified in the JEDEC51-14, is presented. The junction cooling temperature curve was first proposed in 2001 as an alternative method of junction-to-case thermal resistance measurement to overcome the disadvantages mentioned above of thermocouple [11], because the thermal path can be reflected by the junction cooling temperature. However, it was not easy to determine the thermal interface resistance between the DUT and heatsink at that time. Therefore, the junction cooling temperatures measured at different interface layers are converted to its structure functions to obtain this thermal resistance in 2005 [12], [13]. However, this method was found to be prone of blurring and spurious peaks in 2008 [14]. In the same year, the separation point of two transient thermal impedances at two different interface conditions was proposed and the method of how to identify this separation point is presented in [15]. It is difficult for the devices with an internal thermal barrier, and the separation point of structure functions is again used in this case in 2009 [16]. More details about the TDIM are discussed in [16], which is the foundation of the JEDEC51-14.

The key point of the standard TDIM is that two transient thermal impedances under two different contact conditions, for cooling between the DUT case surface and heatsink to make a separation point at the contact interface, must be measured

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accurately. Then, the corresponding thermal impedance (also the cumulative thermal resistance from junction to case) at the separation point is considered as the junction-to-case thermal resistance [1]. This method considerably improves the reproducibility and has been successfully applied in many kinds of power electronics, for example, the discrete power devices [13], [17], [18] and high-power devices like press pack IGBTs [19]. The measured transient thermal impedance can be also used to monitor the ageing process [20]. However, all these publications are focused on the application of the TDIM but not the method itself, as well as its accuracy.

According to the test procedure of JEDEC51-14, the worse contact condition, for example, without thermal grease, must induce a higher junction temperature due to the increased thermal contact resistance at the interface. This finally leads to an underestimation with an early separation point. The influence of temperature nonlinearities of packaging materials is analyzed by the finite element thermal simulation [21] with a constant power loss. However, the root reason is not only the material thermal conductivity temperature dependence but mainly the junction temperature determination by the $V_{\mathrm{CE}}(T)$ method with the voltage drop at small sense current. The reason is that the higher junction temperature and temperature gradient inside the device, especially the IGBT chip, change the "determined thermal path" by the measured voltage drop even though the real physical thermal path only depends on thermal-related material parameters and the geometry size. And, this is not possible to reveal in the finite element method (FEM) simulation, because no semiconductor physical model is included.

Delay time t_{MD} is inevitable for the junction temperature measurement with the $V_{\mathrm{CE}}(T)$ method, and the $V_{\mathrm{GE(th)}}$ method is not recommended in the standard [1]. The delay-time-induced maximum junction temperature offset for IGBT devices is discussed in [22]. However, the authors in [22] do not consider the *TDIM*.

In this article, the temperature influence on the measurement of the transient thermal impedance and accurate determination of the junction-to-case thermal resistance with TDIM is first discussed with experimental results. The root reason how the temperature affects the measured transient thermal impedance and finally the resulting junction-to-case thermal resistance is then tried to explain with the FEM simulation. However, no big difference is found between the two simulated transient thermal impedances under two different temperature conditions because the modeling of the IGBT chip with semiconductor physical is not possible in ANSYS FEM. The semiconductor physics-based technology computer-aided design (TCAD) simulation is, therefore, performed for further explanation of the root cause. The FEM and TCAD simulation models are experimentally verified, and the TCAD simulation results for the root reason explanation are also proven by the experimental results of 1200 V IGBT and diode. Finally, the improved TDIM with the junction temperature compensation by the coolant temperature adjustment is proposed to obtain accurate junction-to-case thermal resistance. The temperature distribution and gradient within the device, as well as the thermal path from the junction to case, can, therefore, be controlled in the same way as in the measurement for the tests with two different conditions.

II. Experimental Results

A. Methodology

The main issue for standard TDIM is to record the transient thermal impedance during the cooling phase with the junction temperature determination by the $V_{\mathrm{CE}}(T)$ method, as shown in (2). Then, the transient thermal impedance during the heating phase can be transferred from the cooling phase shown in (3). t_{MD} is the inevitable delay time to determine the junction temperature during the cooling phase because a recombination time for the space charge region is needed [1] after the load current is switched OFF. More details about the basic principle of transient thermal impedance measurement can be found in [1] and [4]

$$Z_{th,\mathrm{cooling}}\ (t) = \frac{T_j\ (t) - T_j\ (t=0)}{P} \text{ for } t\ >\ t_{\mathrm{MD}} \tag{2}$$

$$\begin{aligned} Z_{th,\mathrm{heating}}\ (t) &= Z_{th,\mathrm{cooling}}\ (t\ =\ 0) - Z_{th,\mathrm{cooling}}\ (t) \\ &= \frac{T_j\ (t=0) - T_j\ (t)}{P} \text{ for } t\ > t_{\mathrm{MD}} \end{aligned} \tag{3}$$

Details on the effect of t_{MD} are discussed in [22]. The transient thermal impedance of IGBT devices represents the ability to resist the heat dissipation from the p-n junction to case/heatsink/air (depends on the measurement point), and the thermal path inside the devices can be determined by this value. From its determination formula in (3), it can be seen that the transient thermal impedance, which means the "measured thermal path," depends on the measured junction temperature and power loss. The measured junction temperature depends on the measured p-n junction voltage drop. While the real physical thermal path only depends on its thermal-related material and geometry parameters as defined in (4). Several material parameters are temperature dependent, such as the thermal conductivity, but the effect is relatively small if the temperature is in the allowed maximum operating temperature range, normally smaller than 150 °C.

$$Z_{th}\ (t) = \sum_{i=1}^{n} R_i * \left(1 - e^{-t/\tau_i}\right) \quad \text{with} \quad \tau_i = R_i\ * C_i. \tag{4}$$

Other test conditions for the standard *TDIM*, such as the heating current, must not change for the two tests because the thermal path within the DUT cannot change. And, the device must be mounted on a temperature-controlled heat-sink, which should be very efficient to approximate the ideal cooling [1]. Water cooling is recommended to control the temperature to be stable. However, the test with worse contact condition, for example, without thermal grease, must lead to higher junction temperature and also larger temperature gradient. The measured p-n junction voltage drop of the IGBT chip at the sense current to obtain the junction temperature also changes at this condition. This changes the "determined thermal path" via the $V_{\mathrm{CE}}(T)$ method, which is presented by the transient thermal impedance

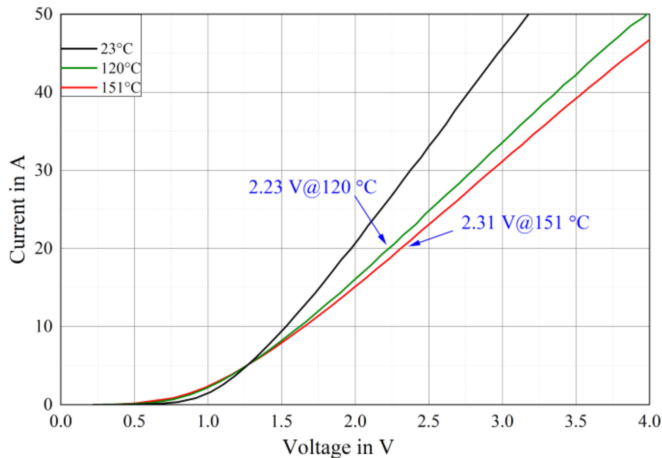


Fig. 1. Measured output characteristics at different temperatures of a 600-V 20-A discrete IGBT device.

$Z_{\mathrm{th}}(t)$ with the formula in (3). Finally, the resulting junction-to-case thermal resistance $Z_{\mathrm{thjc}}(t_{\mathrm{s}})$, which should be close to the steady-state thermal resistance R_{thjc} [1], is changed.

Another issue is that the voltage drop of IGBT devices is also temperature-dependent, and it finally changes the calculated transient thermal impedance with the changed power loss by (3). Fig. 1 shows the measured output characteristic of a 600 V–20 A discrete IGBT devices with different temperatures. The voltage drop at rated current (20 A) is 2.23 V with junction temperature of 120 °C and 2.31 V at 151 °C, respectively. This increases the power loss about 1.6 W with the heating current of 20 A, which is not considered in the FEM thermal simulation as constant power is applied [21].

The measured transient thermal impedance by (3) is, therefore, affected by the measured voltage drop at sense current to determine the junction temperature and also by the power loss. The thermal path of the DUT from junction to case, determined by the transient thermal impedance, at two tests changes at two different junction temperatures caused by two different contact conditions. This leads to an early separation and underestimates the actual value.

B. Test Setup

The power cycling test bench integrated with the transient thermal impedance measurement function is used and the delay time for all tests is controlled to be the same with 650 μs. The reason for longer delay time is that an inductance L is series-connected in the main loop to control the heating current stable during the heating phase. Three IGBT devices (IKW20N60H3), mounted on the separated copper adapter plates to reduce the thermal coupling effect, with 600 V blocking voltage from Infineon (#14, #15, and #16) are connected in series and tested simultaneously to avoid accidental behavior. A water-cooling system cools down the device and the coolant temperature T_{inlet} can be easily controlled. The sense current for the junction temperature determination is set as 100 mA and the load current I_{L} is 20 A identical to the rated current. The heating time is set as $t_{\mathrm{on}} = 20$ s and cooling time is $t_{\mathrm{off}} = 40$ s.

TABLE I
TEST SETUP FOR EXPERIMENTS OF #16 AS AN EXAMPLE

No.	t_{on} (s)	t_{off} (s)	I_{L} (A)	T_{vjmax} (°C)	T_{inlet} (°C)	Contact condition
1	20	40	20	123	50	One thermal foil
2	20	40	20	153	50	Two thermal foils
3	20	40	20	147	45	
4	20	40	20	142	40	
5	20	40	20	138	35	
6	20	40	20	133	32	
7	20	40	20	128	28	
8	20	40	20	124	24	
9	20	40	20	123	23	

The thermal foil of SB-HIS from DETAKTA with thermal conductivity of 1.0 W/(m∗K) and thickness of 0.15 mm is used to conduct the heat and also for electrical insulation. For the test with better contact condition, one thermal foil is used and the coolant temperature is set to 50 °C. The maximum junction temperature is intended to reach roughly 123 °C. Another test with worse contact condition, two thermal foils are used and the maximum junction temperature is desired to reach 153 °C with the same test conditions. The tests with one/two thermal foils are desired based on the JEDEC51-14 standard [1]. The coolant temperature is adjusted for other tests according to the desired junction temperature, as listed in Table I, to investigate the temperature influence. The reason why the coolant temperature is adjusted rather than the load current to achieve the desired junction temperature is that the load current changes the power density with the same device and finally the temperature distribution; even the junction temperature is the same. This leads to an influence on the thermal path. Device #16 is used as an example as the test results of all three devices are almost the same. Test No. 1 is the benchmark; Nos. 2–9 are designed to evaluate the temperature influence on the determination of transient thermal impedance and resulting junction-to-case thermal resistance.

C. Temperature Influence

1) Influence on the Measured Z_{thjs}*:* Fig. 2 shows the transient thermal impedances measured at different junction temperatures realized with different coolant temperatures. The experimental results show that the thermal impedance difference at the steady state (accumulative thermal resistance) between one thermal foil and two thermal foils with the same coolant temperature comes from the attribution from one additional thermal foil. The thermal time constant is also changed due to the insertion of an additional thermal foil and the heat needs more time to go through this interface. Additionally, for the measurement with higher junction temperature needs more time to reach the steady state when we compared the results of 123 °C and 153 °C with two thermal foils and leads to higher thermal resistance. This also implies that the junction temperature changes the “determined thermal path” by (3) from the junction to the heatsink. The temperature indeed changes the measured

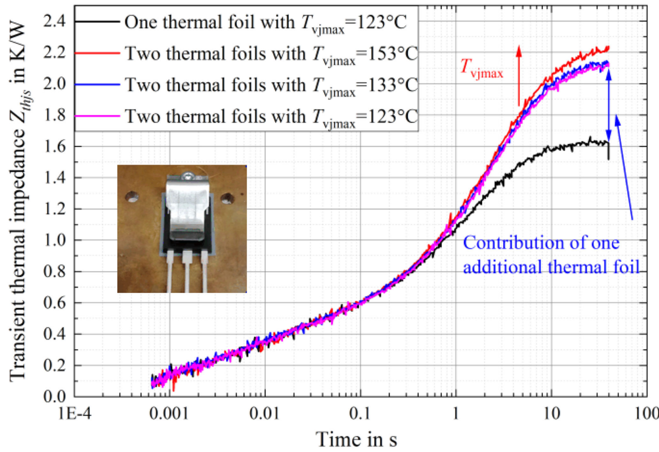


Fig. 2. Transient thermal impedances measured at different junction temperatures of #16 with test No.1, 2, 6, and 9 for example.

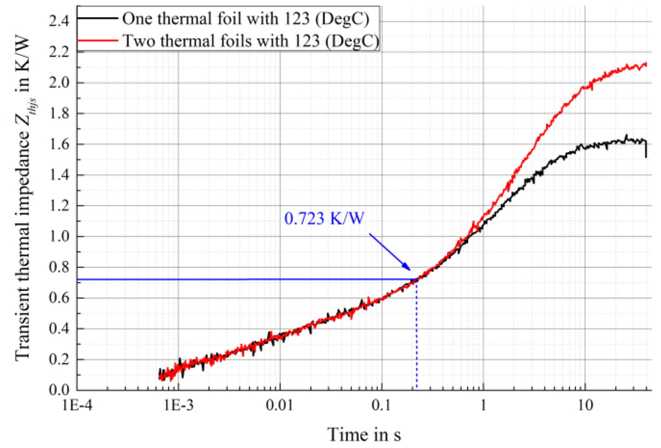


Fig. 4. Two transient thermal impedances comparison, determined junction-to-case thermal resistance is 0.723 K/W with two thermal foils measured at a junction temperature of 123 °C and one thermal foil at 123 °C.

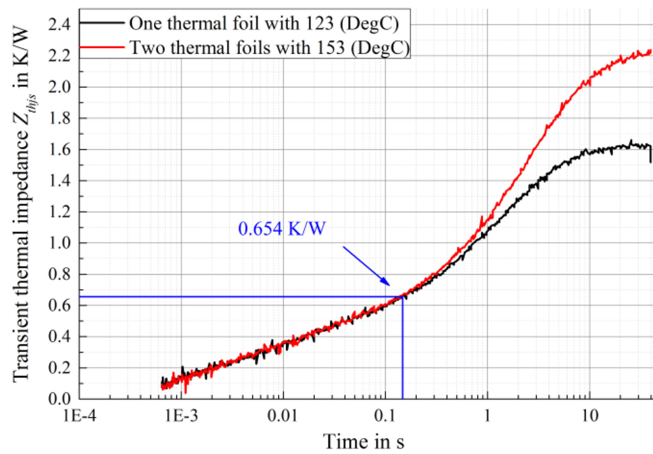


Fig. 3. Two transient thermal impedances comparison, determined junction-to-case thermal resistance is 0.654 K/W with two thermal foils measured at junction temperature of 153 °C and one thermal foil at 123 °C.

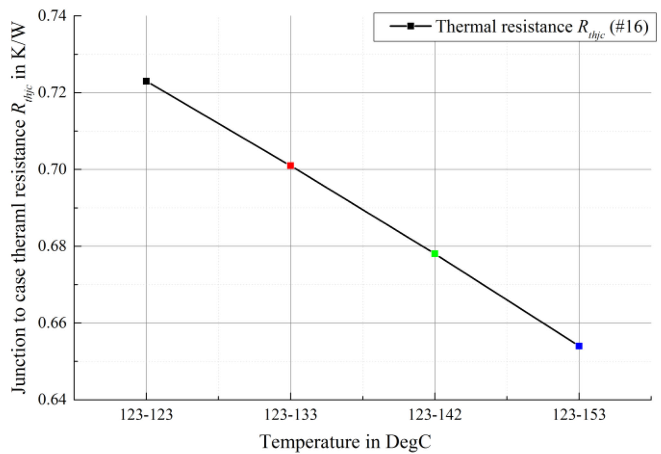


Fig. 5. Determined junction-to-case thermal resistance with different transient thermal impedances measured at different junction temperature for the second transient thermal impedance.

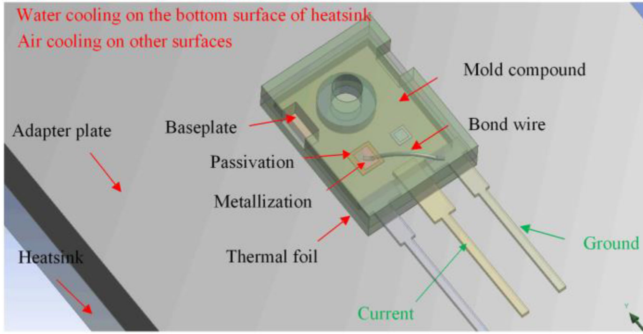
transient thermal impedance and the thermal path within the DUT.

2) Influence on the Determination of $Z_{thjc}(t_s)$: The temperature gradient and thermal path within the device at high junction temperature are modified as mentioned above, and this leads to an earlier separation point, as shown in Figs. 3 and 4. Fig. 4 shows the experimental results with the standard TDIM according to [1] and the determined junction-to-case thermal resistance is 0.654 K/W, which is much lower than the value (0.88 K/W) given in the datasheet. This agrees with the statement in [1] that the determined $Z_{\mathrm{thjc}}(t_s)$ is normally smaller than the steady-state thermal resistance R_{thjc}, especially for the device with an internal barrier to the heat flow. The details of separation point determination to obtain the junction-to-case thermal resistance is described in [1] and [4]. The determined value increases to 0.723 K/W after the junction temperature of two thermal foils is adjusted to the same with one thermal foil through coolant temperature.

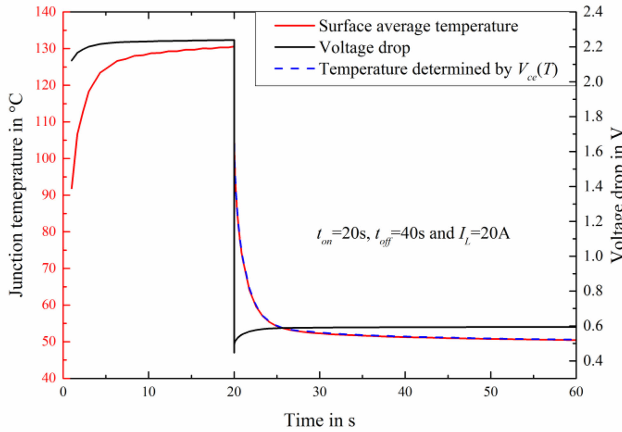
The determined junction-to-case thermal resistance based on different transient thermal impedances measured at different junction temperature is shown in Fig. 5, and we can see that the junction temperature has a big influence on the determination of the $Z_{\mathrm{thjc}}(t_s)$. The error is around -9.5% with 30 K temperature difference to the reference value of 0.723 K/W.

III. Simulation Results and Analysis

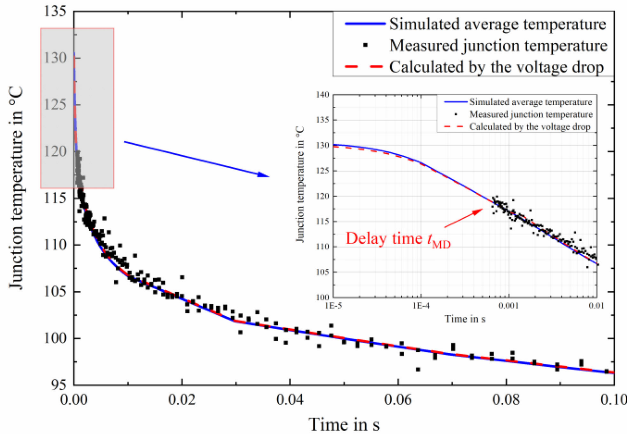
From the experimental results and discussion mentioned above, it can be seen that the junction temperature indeed changes the measured transient thermal impedance and the resulting junction-to-case thermal resistance. However, the temperature nonlinearities influence of packaging materials should not be that big, and the root reason is tried to be explained first by the FEM simulation with the consideration of electro-thermal behavior and temperature-dependent package materials in ANSYS Workbench. Then, the TCAD simulation with the semiconductor physical behavior of IGBT chip is performed for further explanation of experimental verification. The chip surface average temperature in the FEM and TCAD simulations



(a)



(b)



(c)

Fig. 6. Boundary conditions and simulation results.(a) Electrothermal simulation model and boundary conditions. (b) Simulated voltage drop and surface average junction temperature. (c) Simulation results fit quite well with experimental results.

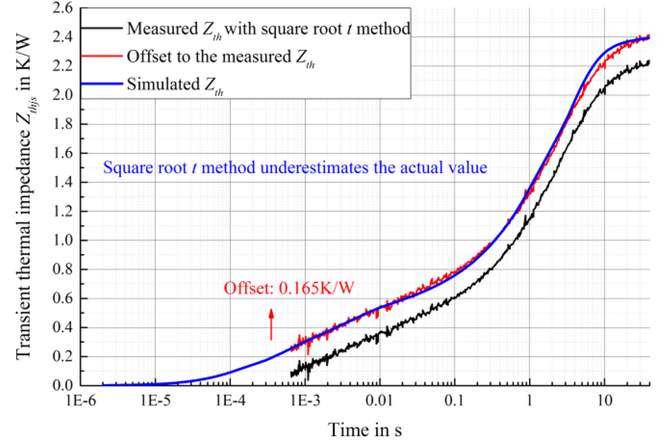


Fig. 7. Comparison of the simulated and measured $Z_{\mathrm{thj}s}$ curves, square root t method underestimates the actual value and makes an offset to the Z_{thjs}, figure from [23].

is defined as the junction temperature with the $V_{\mathrm{CE}}(T)$ method [8] and [24].

A. FEM Simulation

First, the FEM simulation model should be verified by the experimental results, as shown in Fig. 6(c). As the devices used in this article are the same type (IKW20N60H3) as in [22], they shared the same geometry size and simulation model. In the simulation, only the effective thickness of the thermal foil and the effective thermal convection coefficient of the heatsink to coolant are considered [8], which are far away from the chip and not important. Other parameters are based on the physical geometry structure, material parameters, and actual test conditions. The thermal-related material parameters, for example, thermal conductivity, are considered as temperature-independent to consider the temperature influence on the package. The electrothermal coupling analysis is selected to include the temperature influence on the voltage drop and power loss. The active area of the IGBT chip is modeled as a temperature-related resistor to obtain the voltage drops at both the load and sense currents. The electrical resistivity is calculated with the measured forward characteristic at different temperatures. A thickness of 5 μm aluminum metallization is also modeled on the IGBT chip surface, and the surface average temperature is selected as the junction temperature and voltage drop at sense current [$V_{\mathrm{CE}}(T)$ method temperature] as well. Fig. 6 shows the boundary conditions and simulation results of $t_{\mathrm{on}} = 20$ s, $t_{\mathrm{off}} = 40$ s, $I_{\mathrm{L}} = 20$ A, $T_{\mathrm{inlet}} = 23$ °C, and two thermal foils.

The junction temperature determined by the voltage drop at 100-mA sense current fits with the chip surface average temperature and measured values from Fig. 6(c). Meanwhile, we can see that the measured junction temperature determined by the square root t method [24] underestimates the actual value and this makes an offset for the measured Z_{thjs}, as shown in Fig. 7 [22]. More details about this offset in the measured Z_{thjs} can be found in [22]. But it can be seen that the simulated Z_{thjs} fits quite well with the measured Z_{thjs}, except for the offset from the square root t method. This error should be considered for IGBT with high power density experiments and applications [25].

The simulated Z_{thjs} with three different conditions according to the experimental results in Section II are shown in Fig. 8. No big difference exists for different coolant temperatures, which conflicts with the experimental results presented in Fig. 2, even

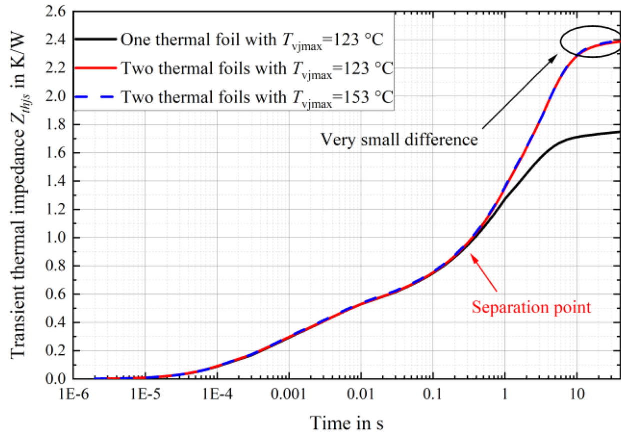


Fig. 8. Simulated transient thermal impedances with three different conditions according to the experimental results.

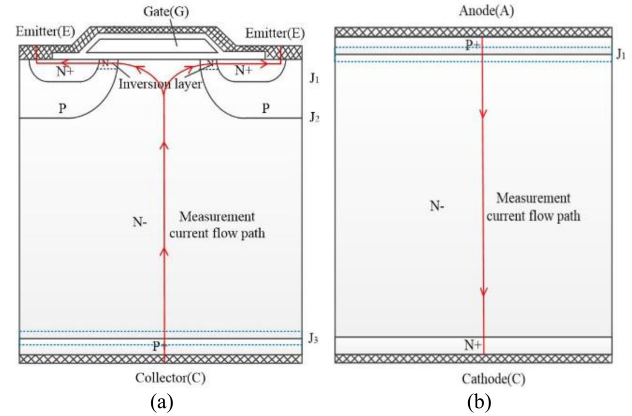


Fig. 9. Schematic diagram of IGBT and diode cells. (a) Voltage drop of p-n junction for junction temperature determination locates at the bottom of chip in J_3 for IGBT, figure from [23]. (b) Voltage drop of p-n junction for junction temperature determination locates at the top of chip in J_1 for diode.

the temperature nonlinearities of package materials are considered and IGBT chip is modeled as a temperature-related resistor. The very small difference between two different temperatures with two thermal foils is contributed from the temperature influence on the package materials and temperature gradient inside the DUT. That means the higher temperature and temperature gradient lead to higher thermal resistance, but it is very small as it can be seen from the results. Therefore, there must be another very important factor to affect the measured Z_{thjs}. From (3), it can be seen that the measured Z_{thjs} depends on the measured junction temperature and power loss. The power loss is calculated with the voltage drop and current, which is the same in the experiment.

The only difference between the measurement and the FEM simulation is the IGBT chip because the semiconductor-physical behavior cannot be modeled. The IGBT chip can be only modeled as a temperature-related resistor in the FEM simulation, and the junction temperature is extracted by the chip surface average temperature. However, the junction temperature is measured with the p-n junction voltage drop at the sense current for the transient thermal impedance measurement. In other words, the thermal path, determined by the junction temperature, as shown in (3), depends on the measured voltage drop. The root reason for the difference in the measured Z_{thjs} is from the V_{CE}(T) method with p-n junction voltage drop, which must be reflected in the TCAD simulation with the semiconductor physical.

Fig. 9 shows the schematic diagram of IGBT and diode cell structures with the sense current path to determine the junction temperature. For IGBT, the p-n junction J_3 used to determine the junction temperature locates at the bottom of the chip [23], but the heat generated at load current is in the whole volume and then transferred to the bottom and finally to heatsink. Therefore, the junction temperature determined by the V_{CE}(T) method is closer to the bottom surface average temperature rather than the top surface average temperature, which is determined in the FEM simulation. For IGBTs with high blocking voltage, more heat will be generated at the base region N^{-} and the load current also introduces voltage drop and power loss at this region with a thicker layer [26]. The difference between the measured junction temperature by p-n junction J_3 and the top surface average temperature in the FEM simulation should be even bigger. But, the situation in the diode is changed. Only one p-n junction exists in the diode and locates close to the top surface. There should be no difference in the determination of junction temperature for diodes. The temperature, therefore, should have no influence on the transient thermal impedance and the junction-to-case thermal resistance determination of diodes, which is experimentally verified in the following section.

B. TCAD Simulation

After the discussion with the FEM simulation results, the temperature influence on the measured Z_{thjs} of the IGBT devices and also why the FEM simulation cannot reveal this difference are mainly from the $V_{\mathrm{CE}}(T)$ method for the junction temperature determination, as shown in Fig. 9. The Sentaurus TCAD is an effective tool for simulating semiconductor devices, the internal physical behavior can be investigated. The chip is designed in one cell or some cells in parallel commonly. By multiplying the area factor, chip behavior can be presented. A simulation model with a complete IGBT chip, real packaging, and cooling system is not possible for Sentaurus. The TCAD simulation is dedicated to the semiconductor physical of chips rather than the thermal simulation for the whole package. Only the difference caused by the p-n junction J_3 to determine the junction temperature cooling curve is, therefore, presented in this section to support the explanation in Section III-A. And, the results of an additional real diode are presented to further verify the conclusion.

As shown in Fig. 9, the IGBT has a more complex structure than the diode, especially the gate structure. The gate structure of one IGBT cell should have a fine mesh at p-n junctions, channels as well as at material junctions, and there are millions of cells in parallel. Restricted by the number of elements, 2-D-Sentaursus simulation with real size IGBT-chip is not possible. However, the diode has a very simple structure compared to IGBT, the real size TCAD simulation with the thermal transfer path and thermal boundary condition is possible [27]. A simplified equivalent

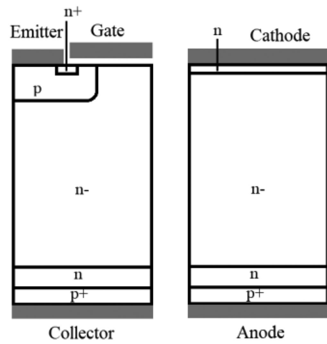


Fig. 10. Schematic of TCAD Simulation model. IGBT (left) and simplified IGBT chip model (right).

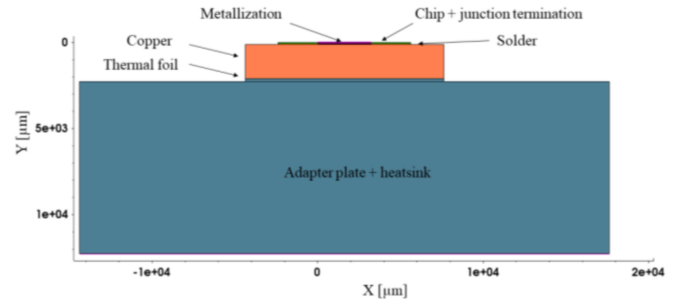


Fig. 11. TCAD simulation model of 650-V IGBT in discrete package with the layers and thermal path.

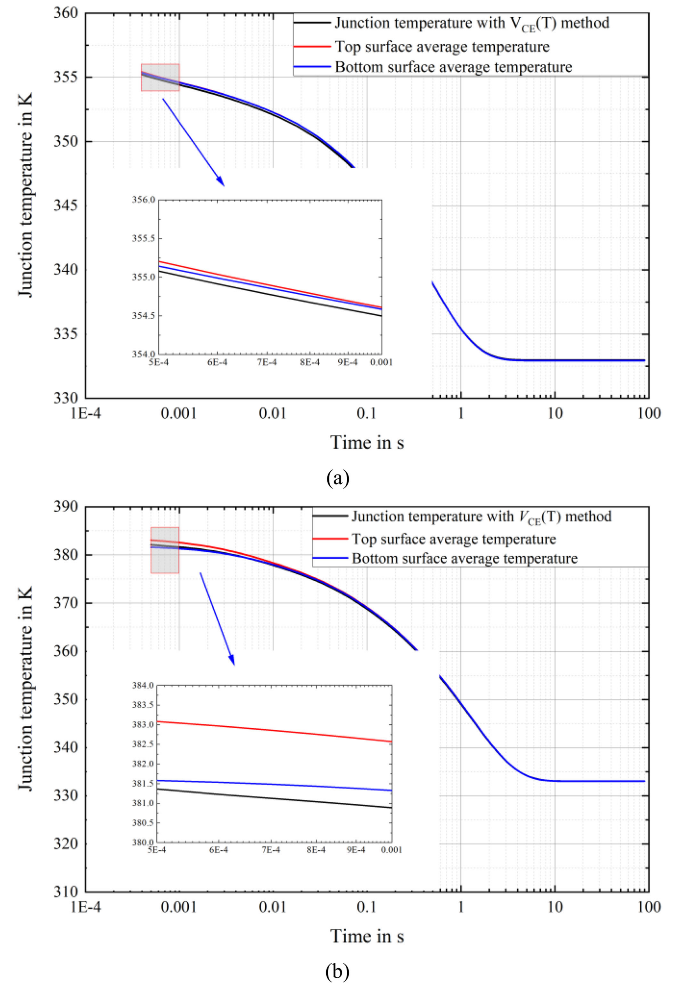


Fig. 12. Junction temperature at cooling phase. (a) 600-V diode model with discrete packaging. (b) 4500-V diode model with module packaging.

diode model with real packaging and cooling system is, therefore, performed. Fig. 10 shows the schematic of the simplified TCAD simulation model. In the equivalent diode model, active region, thickness of the chip, p^+ region, n buffer region, and the doping in n^- region are completely identical as in the IGBT with the exception of the gate structure, which is not important in this case. The n region on the cathode side of the equivalent diode model is selected to match the electric field distribution of the IGBT during isothermal forward bias simulation. The simulation results of this simplified equivalent diode model can, therefore, represent the results of IGBT devices as also presented in [27].

The TCAD simulation idea with the semiconductor physical and simplification of IGBT chip is from [27] but the simulation model, package structure, doping profile, chip parameters, and the topic in this article are different. In [27], the position-caused temperature difference between the top and bottom surfaces is revealed, which is caused by the thickness of the IGBT chip. For example, the temperature difference in the 4500-V IGBT (470 μm) is larger than the 600-V IGBT (70 μm) because the IGBT chip with a thicker base region n^- to withstand higher blocking voltage. But, the reason why the junction temperature determined by the $V_{\rm CE}(T)$ method closed to the surface average temperature and to which surface is not presented, as well as the results of the diode. Furthermore, the results of only one time set are not enough to represent the change tendency in this article.

The TCAD simulation of 650 and 4500 V IGBT is, therefore, performed again with the temperature cooling curve to explain the difference caused by the p-n junction J_3 shown in Fig. 9. The models are built with a corresponding thermal transfer path, which means, 650 V IGBT in discrete package and 4500-V IGBT in module, totally different simulation models compared to the previous one used in [27]. The TCAD simulation model of 650-V IGBT in discrete with the package and thermal path used in this article is shown in Fig. 11 as an example. Furthermore, the diode simulation is also performed to verify the explanation in Fig. 9 that there should be no difference in the diode. Because only one p-n junction is existing, the junction temperature determined by the $V_{\rm CE}(T)$ method should be always close to the top surface average temperature and should not depend on the voltage class and junction temperature. The electrical behavior of the models is well verified with the datasheet.

The simulation model is heated up with rated current for 10 s and then cooling down for 90 s. The coolant temperature is set as $T_{\rm inlet} = 60$ °C. Fig. 12 shows the changing trend of junction temperature determined by the $V_{\rm CE}(T)$ method (equals to the measurement value) as well as the top and bottom surface average temperature during the cooling phase. The transient thermal impedance is shown not only because the TCAD simulation is mainly dedicated to the semiconductor physical but

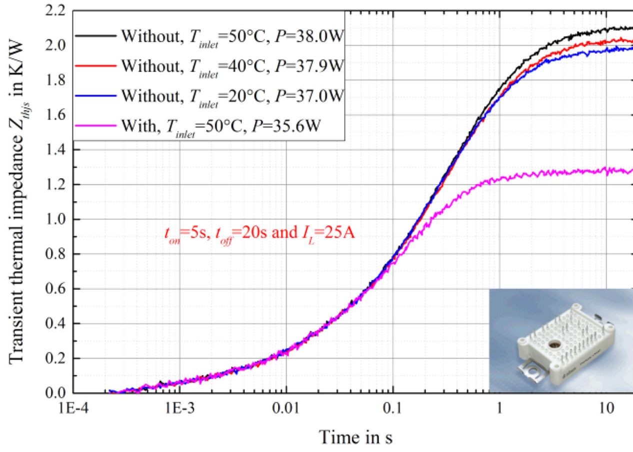
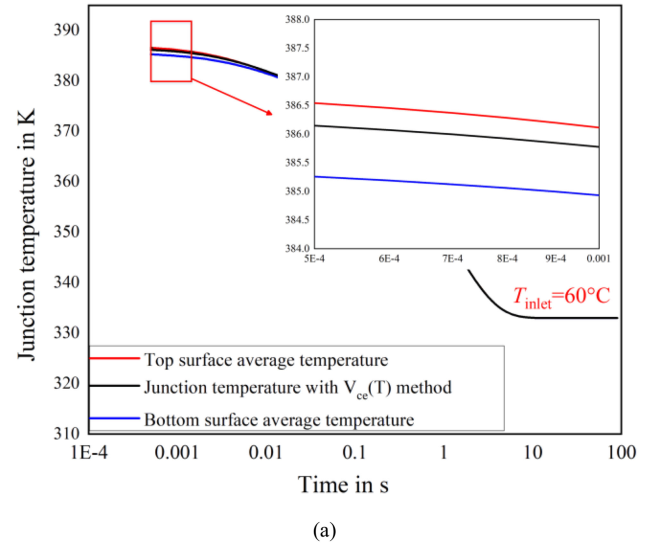


Fig. 13. Measured Z_{thjs} curves with different contact conditions and coolant temperature for 1200-V IGBT in easypack (FS25R120W1T4), "without/with" means without/with thermal grease at the contact interface.

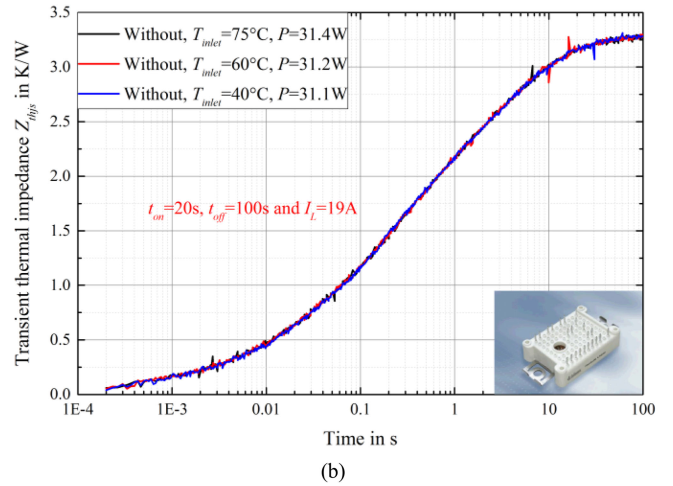
also the accurate thermal path cannot be presented with the 2-D simulation.

From the results, we can see that three temperatures [average temperature of the top surface and bottom surface, the junction temperature determined by the $V_{\mathrm{CE}}(T)$ method] show a small difference at the beginning and then they come to the same with longer cooling time. This difference at the beginning, however, affects the transient thermal impedance and the power loss can enlarge or reduce this difference depending on its amplitude when applying (2) and (3). The junction temperature determined by the $V_{\mathrm{CE}}(T)$ method is lower but closer to the bottom surface average temperature in both cases. This confirms the explanation in Fig. 9(a) that the p-n junction for the junction temperature of IGBT is located close to the bottom surface and the difference should increase with higher voltage classes. The measured transient thermal impedances of a 1200-V IGBT device in the easypack at different coolant temperatures to lead different junction temperatures are shown in Fig. 13. It can be seen that the difference in the measured Z_{thjs} also exists for 1200-V IGBT devices like the 600-V IGBTs shown in Fig. 2.

However, for the diode with only one p-n junction J_1, as shown in Fig. 9(b), the junction temperature measured by the $V_{\mathrm{CE}}(T)$ method should be close to the top surface average temperature and the temperature should have no influence on the measured Z_{thjs}. Fig. 14 shows the TCAD simulation results of a 4500-V diode model and experimental results of a 1200-V diode in the easypack. The simulation results of the 4500-V diode model are selected because the difference is bigger and readable. The only difference between the diode model here and the simplified equivalent diode model for IGBT device in Fig. 11 is the cell structure and doping profile. The packaging and cooling are the same. It can be seen that the junction temperature determined by the $V_{\mathrm{CE}}(T)$ method is lower but closer to the top surface average temperature rather than the bottom value. Furthermore, no difference in the measured Z_{thjs} shown in Fig. 14(b) is found in the 1200-V diode devices, which confirms the explanation in Fig. 11(b) and also the root reason of the temperature influence



(a)



(b)

Fig. 14. TCAD simulation results and experimental results for diode. (a) TCAD simulation results for 4500-V diode model, (b) Measured Z_{thjs} curves for 1200-V diode in easypack (FS25R120W1T4).

on the measured transient thermal impedance and resulting junction-to-case thermal resistance.

IV. Improved TDIM

From the electro-thermal FEM simulation results and TCAD simulation results with the consideration of semiconductor physics, it can be seen that the influence of the junction temperature on the measured thermal path from junction to case is not possible to be reflected in the FEM simulation. Because the root reason is the p-n junction location in IGBT used for the junction temperature determination, which is not possible to be implemented in the FEM simulation. This difference is also related to the voltage class for IGBT devices. For the diode, the temperature has no influence on the measured Z_{thjs}. The temperature influence on the accuracy of the standard *TDIM*, therefore, must be considered for IGBT devices.

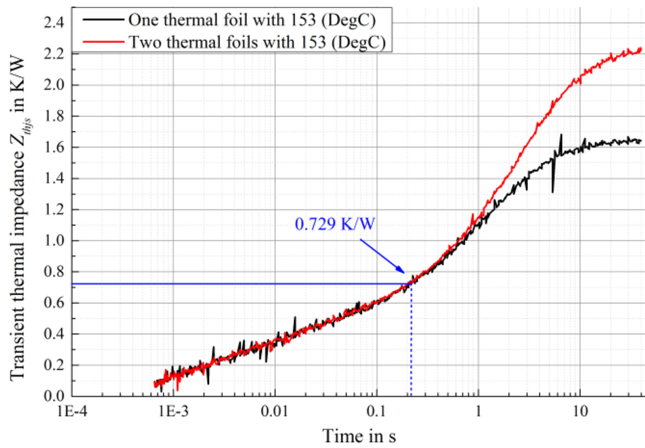


Fig. 15. Two transient thermal impedances comparison, determined junction-to-case thermal resistance is 0.729 K/W with two thermal foils measured at junction temperature of 153 °C and one thermal foil at 153 °C.

The improved TDIM is, therefore, proposed to improve the measurement accuracy with the adjustment of the coolant temperature to keep the junction temperature the same for two tests. Only in this case, the junction temperature and the temperature gradient within the DUT can be controlled to be the same. Then the measured transient thermal impedance from the junction to case will be the same for two tests and only differs at the contact interface for a separation point. The adjustment of any other parameters to control the junction temperature to be the same, like the load current, is not recommended because the temperature gradient will also change. This will also lead to an early separation point and underestimation.

Additional one test is performed to reach the same junction temperature of 153 °C with one thermal foil through increasing the coolant water temperature to verify the effectiveness of the *improved TDIM*. Fig. 15 shows that the determined junction-to-case thermal resistance is about 0.729 K/W, which is slightly higher but very close to the value (around 0.723 K/W) obtained at 123 °C. This difference can be explained by the temperature-dependent thermal conductivity of packaging materials, because the higher temperature leads to lower thermal conductivity. The final junction-to-case thermal resistance of the 600-V IGBT is around 0.888 K/W, which is very close to the value of 0.88 K/W specified in the datasheet, after the offset caused by the square root t method of 0.165 K/W is included, as shown in Fig. 8. The improved TDIM improves the accuracy by 9.5% for the 600-V IGBT compared to the standard TDIM even the offset is not considered.

V. Conclusion

The temperature influence on the accuracy of the TDIM for the junction-to-case thermal resistance measurement is experimentally researched and the root reason is also explained with the FEM and TCAD simulations. The improved TDIM is then proposed and verified to improve the measurement accuracy.

1) The junction-to-case thermal resistance of IGBT devices will be underestimated using the standard JEDEC-51-14 because the junction temperature with worse contact condition increases, finally it leads to the early separation point.
2) The square root t method underestimates the actual value of the 600 V IGBT device in this article and makes an offset for the measured Z_{thjs} of IGBT, and finally the determined junction-to-case thermal resistance. This also should be considered.
3) The main reason for this error in IGBT devices when applying the standard TDIM is the location difference of heat generation and p-n junction, which is used to determine the junction temperature with the $V_{\mathrm{CE}}(T)$ method. The junction temperature affects the measured transient thermal impedance and the resulting junction-to-case thermal resistance.
4) The standard TDIM is suitable for diodes because the p-n junction used for the junction temperature determination with the $V_{\mathrm{CE}}(T)$ method is close to the top surface. The temperature has no influence on the measured Z_{thjs}.
5) The FEM simulation is not possible to reveal the influence of the temperature on the measured Z_{thjs} even the electro-thermal models of the package layers are included because the semiconductor-physical models are not possible to be considered.

Nevertheless, the influence of the junction temperature on the measured Z_{thjs} must be considered. The standard TDIM is exact enough for diodes; however, it leads to a systematic error for IGBTs. With the proposed improved TDIM, it is possible to eliminate the error for IGBT without additional high experimental effort.

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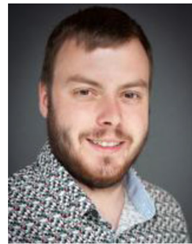

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