

Letters

Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count

Atif Iqbal , Senior Member, IEEE, Marif Daula Siddique , Member, IEEE, B. Prathap Reddy , Member, IEEE, and Pandav Kiran Maroti , Member, IEEE

Abstract—Multilevel inverter concepts (MLIs) with switched capacitor (SC) are emerging due to their scope in sustainable energy systems as well as high-voltage applications. In the SC technique, required voltage levels can be achieved with the lesser number of dc sources in combination with the capacitor voltage. In this perspective, the design of high-gain MLI with reduced sources as well as switch count is a challenging task. This letter proposes a single-source-driven quadruple boost multilevel inverter topology (QB-MLI) with lesser order of resources over the other SC MLIs. The proposed QB-MLI is capable to produce nine levels of voltage in output by effectively balancing the two capacitor's voltage with the associated control logic. The different SC MLIs are compared to verify the pros and cons with respect to the contribution of the proposed QB-MLI topology. Detailed experimental results at various test conditions of a laboratory set-up have been presented to validate the performance of the proposed QB-MLI.

Index Terms—Boost capability, multilevel inverter (MLI), reduced switch count, quadruple topology.

I. INTRODUCTION

ONE of the most prevalent approaches for the power conversion from dc to ac, which is involved in the photovoltaic (PV) cells and fuel cell types renewable energy system (RES), is multilevel inverters (MLIs). Higher voltage operation with low-voltage stress on switches, reduced dv/dt , and improved harmonic profile of the output voltage constitute key advantages of MLIs. The three conventional types of MLIs, i.e., cascaded H -bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC) have been proposed over the last few decades. The number of isolated dc sources in CHB, capacitors in FC, and clamping diodes in NPC are accumulative for the increase in output levels. In addition, the topologies with FC and NPC configurations necessitate external circuits and complex

control algorithms in order to assert the balance of the voltage of capacitors. With the RES, the boosting of the voltage is required for the higher voltage applications. In order to achieve a higher magnitude or boosted output voltage, a dc–dc boost converter after input or transformer is required on the load side. All these lead to complicated, voluminous, and expensive inverter systems [1], [2].

A new practice to overcome the abovementioned shortcomings, multilevel inverters based on the switched-capacitor concept has been reported in [3]–[11]. The switched-capacitor (SC) MLI can efficiently increase the voltage levels at the output along with boosting the input voltage. In [3], a single dc source topology was proposed without the use of a backend H -bridge. The topology in [3] has lower voltage stress on the individual switches, but the number of capacitors and power switches also increases as the voltage levels increase. In [4] and [5], two 9-level SC-MLI with single source configuration have been proposed, in which the balancing of capacitor voltage is achieved without using auxiliary circuits and complicated control. However, their voltage boosting factor is only 2. The inverter was recommended in [6] with a voltage boost increase of 4 using a lower count of capacitors and switches, but in this topology, two switches are rated for higher voltage blocking. In [7], a single source SCMLI was introduced with a quadruple voltage gain, where the inverter requires the higher order of switches and that is rated for ≤ 2 times of input dc voltage.

Many topologies with an appropriate agreement for a diversity of applications with the higher voltage gain are reported in [8]–[11]. In [9]–[11], backend H -bridge is used to generate a negative voltage level. The four switches of H -bridge must maintain the peak load voltage stress and are, therefore, not suitable for the applications requiring high voltage. To improve the abovementioned disadvantages, a new quadruple boost multilevel inverter topology (QB-MLI) has been proposed with a reduction in the number of switches and capacitors. The proposed MLI is suitable for low-voltage involved renewable energy sources such as photovoltaics, fuel cell-driven electric vehicles, and other applications with the involvement of low to high voltage requirements. The performance validation of the proposed QB-MLI has been done with the experimental prototype. The comparative analysis of the proposed QB-MLI over other SC-based MLIs in the literature with respect to the

Manuscript received October 2, 2020; revised November 9, 2020 and December 7, 2020; accepted December 10, 2020. Date of publication December 14, 2020; date of current version March 5, 2021. This work was supported by the Qatar University-Marubeni Concept to Prototype Development Research Grant M-CTP CENG-2020-2 from the Qatar University. The statements made herein are solely the responsibility of the authors. (Corresponding author: Marif Daula Siddique.)

The authors are with the Department of Electrical Engineering, Qatar University, Doha 2713, Qatar (e-mail: atif.iqbal@qu.edu.qa; marifdaula1@gmail.com; prathap.bhimireddy@gmail.com; kiranpandav88@yahoo.co.in).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2020.3044628>.

Digital Object Identifier 10.1109/TPEL.2020.3044628

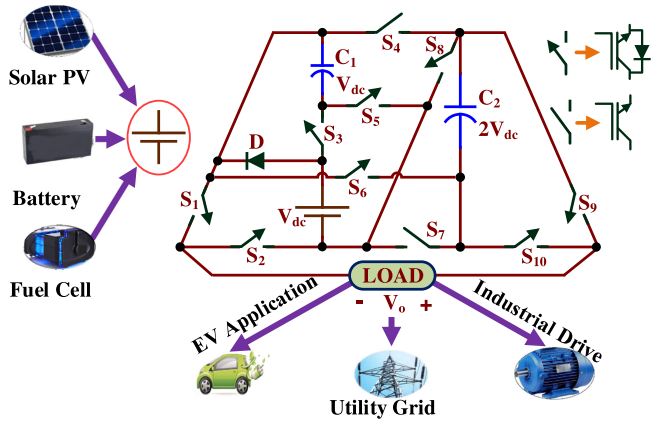


Fig. 1. Proposed quadruple boost topology.

 TABLE I
 SWITCHING STATES FOR THE PROPOSED QB-MLI

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	$V_o(\times V_{dc})$	C_1	C_2
0	1	1	0	0	1	0	0	1	0	4	D	D
0	1	0	0	1	1	0	0	1	0	3	C	D
0	1	1	1	0	0	1	0	1	0	2	D	C
0	1	0	0	1	1	0	0	0	1	1	C	—
1	0	0	0	1	1	0	0	0	1	zero	C	—
0	1	0	0	1	0	0	1	1	0			
1	0	0	0	1	0	0	1	1	0	-1	C	—
1	0	1	1	0	0	1	0	0	1	-2	D	C
1	0	0	0	1	0	0	1	0	1	-3	C	D
1	0	1	0	0	0	0	1	0	1	-4	D	D

Notations: 0 = OFF state of the switch, 1 = ON state of the switch, — = no change in capacitor voltage, C/D = charging and discharging of capacitor.”

switching devices, passive elements, and other performance indices is presented.

II. PROPOSED TOPOLOGY

A. Description of the Proposed QB-MLI

The circuit configuration of the proposed inverter is shown in Fig. 1. With the utilization of 11 switches and one diode as power semiconductor devices, the proposed topology generates 9-level waveform with a quadruple voltage gain. Out of 11 switches, the switches S_4 and S_7 are configured as reverse blocking (RB) switches, i.e., a switch without its antiparallel diode, and the remaining other switches are configured as a switch with its antiparallel diode. The quadruple voltage gain is achieved with two capacitors having a voltage rating of V_{dc} and $2V_{dc}$ with V_{dc} being the magnitude of the source voltage. The proposed inverter can be suitable for the applications like, solar PV, fuel cell, battery power applications, industrial drives, etc., as shown in Fig. 1. The equivalent switching circuit with the current flow for the positive voltage levels is shown in Fig. 2. The negative voltage levels can be visualized from the switching logic given in Table I.

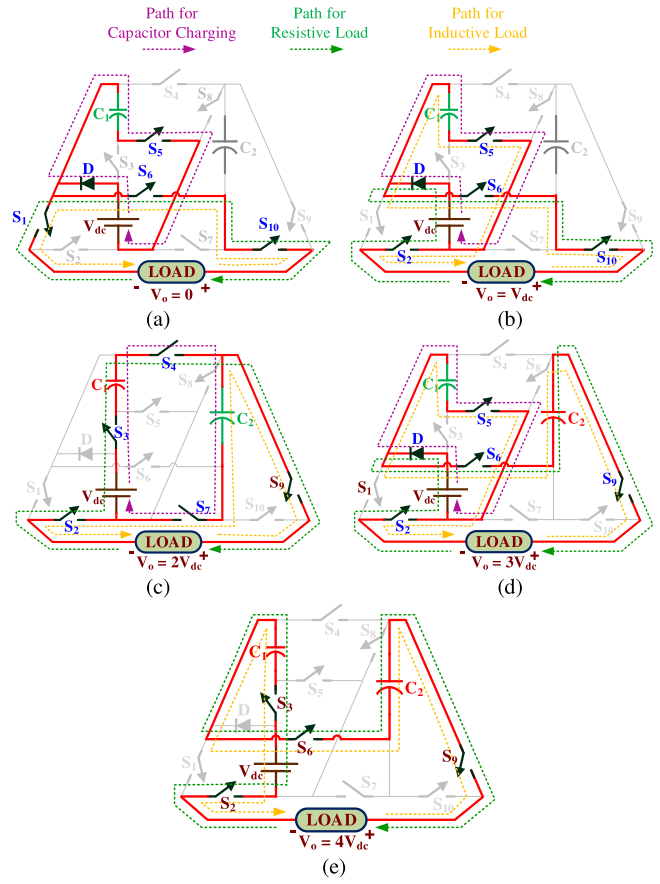


Fig. 2. Current flow for all positive voltage levels of the proposed QB-MLI.

B. Self-Voltage Balancing of Capacitors C_1 and C_2

As the voltage/current sensor(s) are absent, self-voltage balance is one of the most desirable characteristics of SC-based converters. Capacitors C_1 and C_2 attend self-balanced using a technique based on the series-parallel connection in the proposed QB-MLI. As given in Table I, the capacitor C_1 and dc source are in parallel connection at the output voltage levels of zero, $\pm V_{dc}$, and $\pm 3V_{dc}$. The C_1 , therefore, charges up to the voltage level V_{dc} . During the voltage level of $\pm 2V_{dc}$, the series connection of the capacitor C_1 and dc source is parallel with the load and capacitor C_2 , it helps to charge C_2 to voltage level $2V_{dc}$. For the $\pm 3V_{dc}$ output voltage, both C_1 and C_2 are charged and discharged, respectively. Finally, both capacitors are discharged at the $\pm 4V_{dc}$ level. Fig. 3 shows the pattern of charging and discharging of capacitors C_1 and C_2 for the positive voltage levels. The overall charge path time constant (due to parasitic elements) is relatively lesser than the time interval of each voltage level and, thus, guarantees rapid charging of the capacitors C_1 and C_2 . However, the voltage of C_1 and C_2 begins to decrease from their nominal value during the discharge period to the next charge period. Therefore, taking into account the corresponding maximum discharge time of C_1 and C_2 , the minimum capacitance value required to allow for an adequate voltage ripple (ΔV) for the peak load current ($I_{o,peak}$) with f

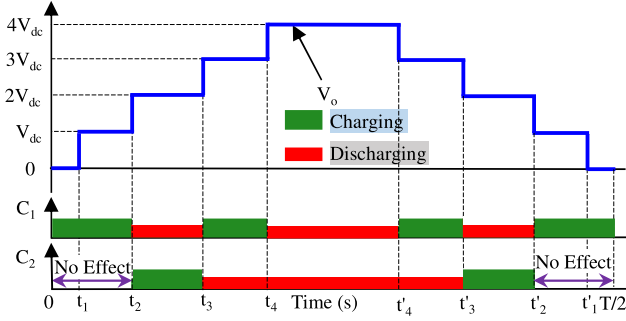


Fig. 3. Staircase output voltage with pattern of capacitor voltage.

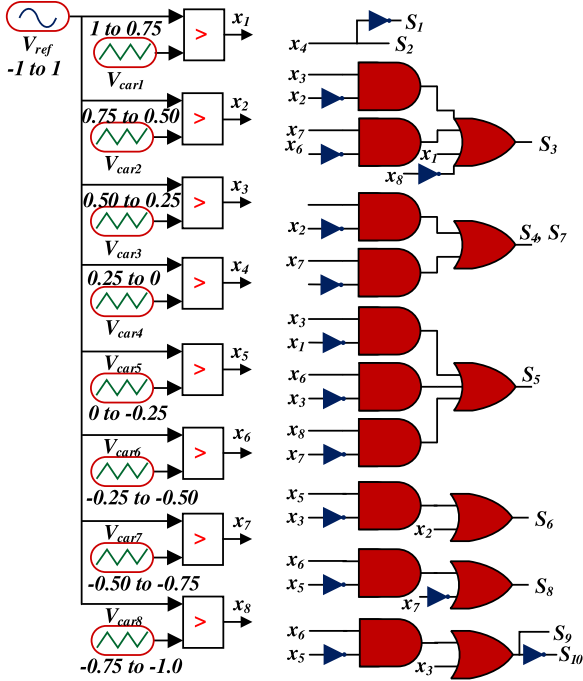


Fig. 4. Switching logic for gate pulse generation.

being the frequency of the output voltage is as follows:

$$\left. \begin{aligned} C_1 &= \frac{I_{o, \text{peak}}}{\pi \times f \times \Delta V} \times \Delta T_1 \\ C_2 &= \frac{I_{o, \text{peak}}}{\pi \times f \times \Delta V} \times \Delta T_2 \end{aligned} \right\} \quad (1)$$

where $\Delta T_1 = t'_4 - t_4$ is the duration of the voltage level of $4V_{dc}$ and $\Delta T_2 = t'_3 - t_3$ is the duration of the voltage levels of $3V_{dc}$ and $4V_{dc}$.

C. Modulation Technique

The inverter is modulated with the sinusoidal pulsewidth modulation, where one sine reference (V_{ref}) having a peak magnitude of one and eight level-shifted carrier waves equally distributed between -1.0 to 1.0 have been used. Fig. 4 shows the switching logic for the proposed QB-MLI. For varying the output voltage magnitude, the magnitude of reference is varied to change the modulation index. With this arrangement, the modulation index is the same as the peak magnitude of the reference signal.

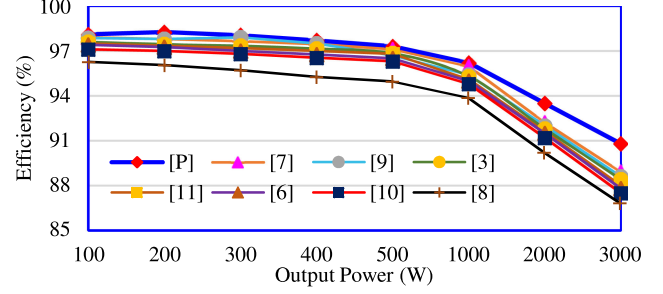


Fig. 5. Efficiency comparison.

III. COMPARATIVE ASSESSMENT

For a fair comparison, the proposed MLI is compared with the other MLI having the same number of levels with the quadruple voltage gain and is presented in Table II. The main objective of the proposed topology is to generate a high-quality output voltage waveform using a lower number of components. In the proposed topology, ten switches have been used to generate the nine-level output voltage waveform with a voltage gain of 4. The topologies presented in [6] and [10] require a lower number of controlled devices; however, the number of diodes in the topology presented in [6] and [10] are higher compared to the proposed topology. For attaining the quadruple voltage gain, the proposed topology requires two capacitors of the voltage rating V_{dc} and $2V_{dc}$ each, whereas the topology in [6] requires three capacitors out of which two capacitors need to be of $2V_{dc}$ and one of V_{dc} voltage rating. An additional capacitor of higher rating results in the higher cost, losses, and complexity to control their charging/discharging. In the proposed QB-MLI, only two capacitors are used, which is the same as the topology of [7]; however, the number of switches in [7] is 12, whereas only 10 switches have been used in the proposed QB-MLI.

The number of conducting devices in the charging loop of the capacitors, i.e., N_{SC} is another important parameter for the SC-based topologies. The devices in the charging loop need to be of higher current rating to handle the capacitor's charging current. For the proposed topology, only four devices of higher current ratings are required, whereas for the other topologies presented in [3], [6]–[11], a higher number of devices is required in the charging loop. The higher number of N_{SC} leads to higher costs and losses.

The total number of conducting devices during each voltage level is indicated by total conducting devices (TCD). From Table II, it can be concluded that the proposed QB-MLI has the minimum number of conducting devices during each level. However, the total standing voltage per unit (TSV_{pu}) is also less as compared to other MLI except [3], [7], and [8]; however, these topologies require a higher number of components.

To further assess the proposed QB-MLI, a cost function (CF) has been defined as described by [4] the following:

$$\begin{aligned} CF &= N_{sw} + N_d + N_c(1 \times N_{C, V_{dc}} + 2 \times N_{C, 2V_{dc}}) \\ &\quad + N_{sc} + \alpha TSV_{pu} + \beta TCD_{avg} \end{aligned} \quad (2)$$

TABLE II
COMPARISON TABLE FOR DIFFERENT NINE-LEVEL TOPOLOGIES WITH QUADRUPLE VOLTAGE GAIN

Top	N_{sw}	N_{gd}	N_d	N_{com}	N_c	VRC		N_{sc}	TSV _{p.u.}	TCD					CF (with value of α and β)			
						V_{dc}	$2V_{dc}$			$\pm 1^{st}$	$\pm 2^{nd}$	$\pm 3^{rd}$	$\pm 4^{th}$	TCD _{avg}	0.5, 0.5	1.0, 1.0	1.5, 0.5	0.5, 1.5
[3]	17	17	0	17	3	3	0	9	5.5	8	8	8	8	8	35.75	42.5	41.25	43.75
[6]	8	8	3	11	3	1	2	6	5.75	5	5	5	5	5	27.375	32.75	33.125	32.375
[7]	12	12	0	12	2	1	1	6	5.25	6	7	7	6	6.5	26.875	32.75	32.125	33.375
[8]	17	17	5	22	4	4	0	12	5.5	10	9.5	8	8.5	9	45.25	52.5	50.75	54.25
[9]	13	13	0	13	3	3	0	6	6.25	8	7	6	5	6.5	28.375	34.75	34.625	34.875
[10]	8	8	6	14	3	3	0	6	8	8	4	5	5	5.5	29.75	36.5	37.75	35.25
[11]	10	10	3	13	3	3	0	6	6.25	8	5	5	5	5.75	28	34	34.25	33.75
[P]	10	10	1	11	2	1	1	4	5.75	5	5	5	4	4.75	23.25	28.5	29	28

$N_{sw}/N_{gd}/N_d/N_{com}/N_c/VRC$ = Number of switches/number of gate driver circuit/number of diodes/total number of components ($N_{sw}+N_d$)/number of capacitor/voltage rating of capacitors, N_{sc} = number of devices in charging loop, TSV_{p.u.} = total standing voltage in per unit, TCD = total conducting device.

where α and β represent the weight coefficients of TSV_{p.u.} and TCD_{avg}, respectively. The values of α and β are not equal, and if both values selected are more than 1, then TSV_{p.u.} and TCD_{avg} are considered dominant for the comparison; otherwise, the cost of the switch, capacitor, and gate driver circuit has dominance for the CF if the values of α and β are less than 1. The estimated cost of the proposed MLI is calculated with different combinations of the α and β value and the same is tabulated in Table II. It is observed that the CF value for the proposed QB-MLI is lower as compared to other discussed MLI.

Furthermore, efficiency plots of different topologies used for the comparison have been provided in Fig. 5. The efficiency for different topologies has been computed using PLECS software in which the topologies are thermally modeled for the power loss analysis. For all topologies, the same parameters have been used for the efficiency estimation, i.e., $V_{dc} = 50$ V, $C = 2200$ μ F, and carrier frequency = 5 kHz. From Fig. 5, the peak efficiency of the proposed topology is 98.2%. Furthermore, the efficiency of the proposed QB-MLI is higher than all other topologies due to the lower component count of lower voltage ratings as well as lower conduction losses. Therefore, from Table II and Fig. 5, the performance of the proposed QB-MLI is better than the other topologies used for the comparison.

IV. RESULTS AND DISCUSSION

To validate the effectiveness of the proposed quadruple boost multilevel inverter, a PCB-designed circuit is implemented in the laboratory with discrete components like switches, capacitors, diodes, etc., and is shown in Fig. 6. The proposed topology has been tested for a rating of 500 W. The key components as well as parameters used for performing the experiment are given in Table III. The experimental results for a modulation index (MI) of 1.0, with RL load are shown in Fig. 7(a), where the results are shown for an open-circuited load, RL load (80 Ω –80 mH), and step change in RL load (two parallel-connected RL loads, 80 Ω –80 mH). From this figure, it is seen that the output voltage (V_o) has nine-levels, the voltage of capacitors C_1 and C_2 , i.e., V_{C1} and V_{C2} , are balanced, with their voltages being 50 and 100 V, respectively. The peak voltage/current (I_o) is 200 V/2.5 A and 200 V/5 A for the loads 80 Ω –80 mH and 40 Ω –40 mH, respectively. The experimental results for a change in load type

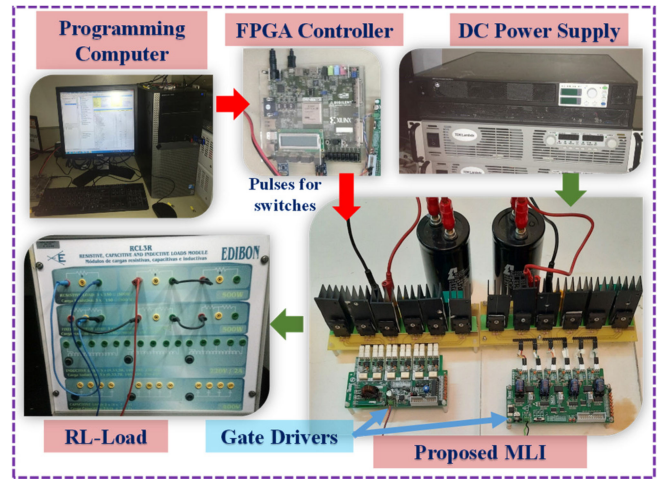


Fig. 6. Experimental prototype of proposed QB-MLI topology.

TABLE III
EXPERIMENTAL PROTOTYPE DETAILS

Key Components	
Switches	G60N100 IGBT
Capacitor	PG6DI (450V and 2200 μ F)
Controller	FPGA Vertix-5 (XC5VLX50T)
Gate Driver	GDA-2A4S1
dc power supply	TDK Lambda GEN300-11
Key Parameters	
Resistive + Inductive loads	Two sets of 80 Ω -80mH
Input dc Link Voltage	50V
Output Voltage	200V (peak)
Fundamental/Switching Frequency	50Hz/5kHz

from R load to RL load with MI = 1.0 are shown in Fig. 7(b), where the results are given for loads 80 Ω and 80 Ω –80 mH, respectively. From this figure, it can be seen that with the R load the voltage and currents are in-phase and with the RL load the currents lag the voltage.

The proposed nine-level QB-MLI has also been experimentally validated for RL load (40 Ω –40 mH) with various modulation indices (i.e., 1.0, 0.75, 0.50, and 0.25, respectively) as shown in Fig. 8(a). In this figure, it can be seen that the diminution in the MI reflects in the number of levels of output voltage, i.e.,

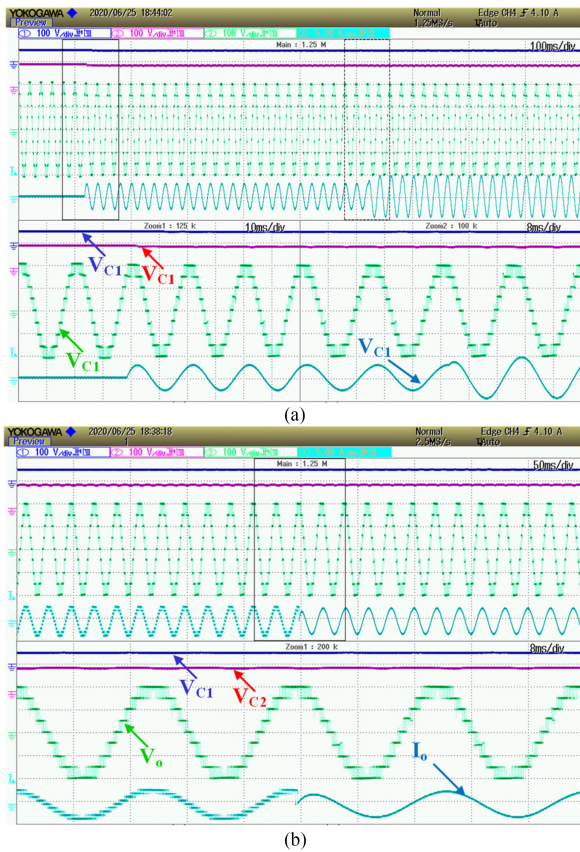


Fig. 7. Experimental results of a proposed nine-level inverter with change in (a) RL load, (b) load type [$V_o = 100$ V/div, $V_{C1} = 100$ V/div, $V_{C2} = 100$ V/div, and $I_o = 5$ A/div].

nine-levels, seven-levels, five-levels and three-levels for MI = 1.0, 0.75, 0.50, and 0.25, respectively. The current magnitude will come down with a reduction in MI since the load remains the same. The experimental results of a proposed inverter for an RL load with the MI = 1.0 and change in frequency from 50 to 100 Hz are shown in Fig. 8(b). The results shown in Figs. 7 and 8 are the evidence that the proposed 9-level QB-MLI is capable to operate effectively under various operating conditions like a step change in load, change in load type, a step-change in MI, and change in the frequency. Moreover, at these test conditions, the capacitor voltages are balanced with the proposed control logic.

The experimental prototype efficiency study for 100–500 W output power has given in Fig. 9, where the efficiency and power loss curve has been shown with respect to output power. From Fig. 9, it can be observed that the efficiency is inversely proportional to power loss of the proposed converter. The experimental efficiency of the proposed topology is 96.25% at an output power of 100 W, and an efficiency of 94.3% was measured at an output power of 500 W. The experimental efficiency (shown in Fig. 9) is slightly lesser than the simulation efficiency (shown in Fig. 5), because of the, first, ideal active and passive components in the simulation, second, mismatch of effective internal resistance of semiconductor devices (internal as well as parasitic elements) in simulation as well as experimental.

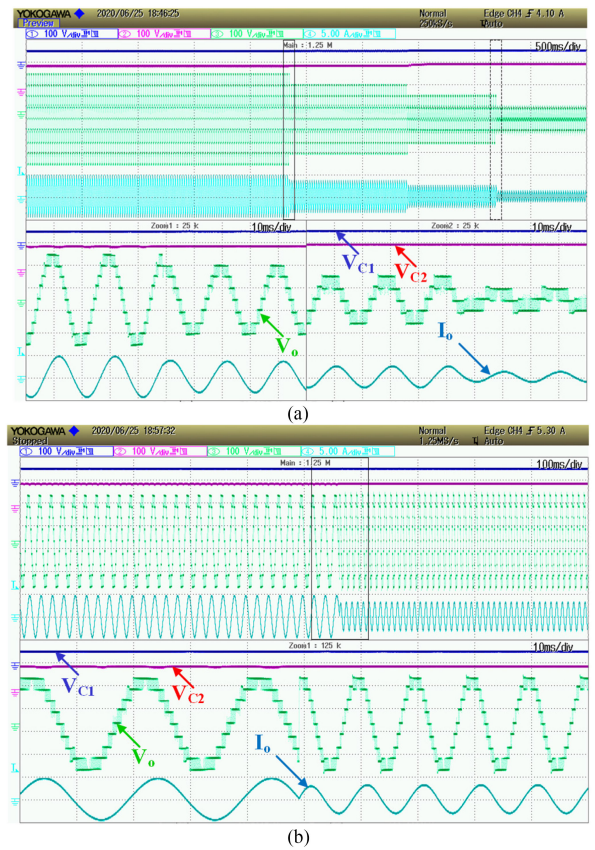


Fig. 8. Experimental results of a proposed nine-level inverter with a change in (a) step change in MI and (b) frequency [$V_o = 100$ V/div, $V_{C1} = 100$ V/div, $V_{C2} = 100$ V/div, and $I_o = 5$ A/div].

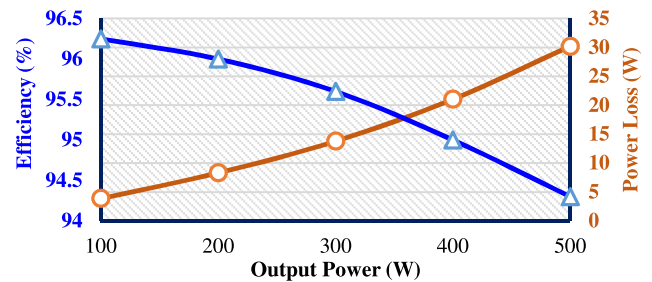


Fig. 9. Experimental efficiency and power loss curve.

V. CONCLUSION

In this letter, an improved circuitry of a single dc source-based SC multilevel inverter topology was proposed to attain higher voltage gain. The proposed QB-MLI was comprised of a lesser number of switching components with lower voltage ratings. The proposed QB-MLI gave a quadruple gain in output voltage by effectively utilizing the two capacitors and one low-voltage dc source. The inherent balancing of capacitors was done according to the switching logic of the proposed MLI. The comparison study in terms of the component count, cost function, and efficiency have shown the merits of the proposed QB-MLI over other SC-based MLIs. The experimental test results at various operating conditions demonstrated the effectiveness of the proposed circuit operation.

REFERENCES

- [1] B. P. Reddy, M. Rao A, M. Sahoo, and S. Keerthipati, "A fault-tolerant multilevel inverter for improving the performance of a pole-phase modulated nine-phase induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1107–1116, Feb. 2018.
- [2] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019.
- [3] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.
- [4] M. D. Siddique, S. Mekhilef, S. Padmanaban, M. A. Memon, and C. Kumar, "Single phase step-up switched-capacitor based multilevel inverter topology with SHEPWM," *IEEE Trans. Ind. Appl.*, to be published.
- [5] J. S. Mohamed Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019.
- [6] J. Liu, W. Lin, J. Wu, and J. Zeng, "A novel nine-level quadruple boost inverter with inductive-load ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4014–4018, May 2019.
- [7] N. Sandeep, J. Sathik, U. Yaragatti, and V. Krishnasamy, "Switched-capacitor based quadruple boost nine-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7147–7150, Aug. 2019.
- [8] H. K. Jahan, M. Abapour, and K. Zare, "Switched-capacitor based single source cascaded h-bridge multilevel inverter featuring boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019.
- [9] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.
- [10] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.
- [11] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.