Implementation of a Novel Very Low Frequency Cosine-Rectangular Voltage Generator for Insulation Testing of Power Cables

Saike Yang, Li Wang, Xiaokai Guo, Tingxi Sun, Yuxin Lu, Yuan Yan, and Hongjie Li

***Abstract*—As an important part of asset maintenance strategy, power utilities carry out insulation testing of power cables to diagnose and assure their health condition. Among various testing methods, very low frequency cosine-rectangular voltage (VLF-CRV) testing is a relatively new approach that has been recently proposed because of its significant advantages of high efficiency, multifunctionality, and easy transportability. This article shows the design, implementation, and confirmation of the topology of a novel VLF-CRV generator based on voltage multiplier that avoids separately using HVdc sources and high voltage switches, thus accordingly strengthening its scalability. Note that the mathematical modes of the generator are presented for comprehensive analysis and optimization of the VLF-CRV generator. Simulation in MATLAB/Simulink is performed to validate the generator's feasibility and implementation of a laboratory prototype is also detailed. Moreover, experiments on a capacitor and a medium voltage power cable were performed to confirm the effectiveness of our implementation.**

***Index Terms*—Cable testing, on-site testing, very low frequency.**

I. Introduction

GIVEN the rapid development of urban power networks, overhead lines are being replaced with underground cables. Potential defects in power cables always cause power failures, which result in considerable personal and property losses. Over the past several decades, as an important part of asset management strategy, in order to assure cables are in healthy condition for reliable power delivery, power utilities have been carrying out various tests to diagnose cable condition, including partial discharge (PD) detection, voltage withstand test, and dielectric loss measurement [1]–[3]. A voltage generator is the key functional unit comprising of a complete cable insulation testing system. So far, three types of ac testing voltage generators have been put forward successively and applied in practice, namely, power frequency ac, variable frequency ac and very low frequency (VLF) voltages [4], [5]. Of these voltage generation techniques, VLF is the most promising technique for the on-site testing of power distribution cables and can be used to conveniently solve difficult problems in the on-site charging of high-capacitance cable loads [6]. However, at the end of the last century, most of the commercially available generators had the major limitations of large size and heavy weight because of the use of mechanical switches, causing much inconvenience for on-site mobility and application [6]–[9].

With progress in power electronic devices that has been achieved since 1990, a door has been opened for the enhancement of power cable testing technology. Attempts have been made to introduce power diodes or analog devices to VLF generators [10]–[12]. In 1998, considerable progress was made by Gulski who developed a novel damped ac (DAC) voltage generator for 35 kV cable PD testing by replacing mechanical switches with insulated gate bipolar transistor (IGBT) devices [13]. This pioneering study resulted in a significant decrease in the weight and size of conventional variable frequency ac generators. In the following years, Gulski continued to perform many industrial application studies of the DAC technique [14]–[17].

After the beginning of the 21st century, an increasing number of studies have been performed on the improvement of cable testing technology using power electronic devices and new circuit topology. In [18] and [19], a new design and construction of a VLF high voltage generator were presented. A cascaded circuit technology and power diodes were used to produce a sinusoidal VLF voltage. In [20], Cao *et al.* presented a VLF sinus voltage generator based on a zero-voltage switching series–parallel resonant converter and a three-stage voltage multiplier (VM) rectifier. In [21], Hou *et al.* proposed techniques to connect discrete IGBT chips in series to generate a 20-kV DAC voltage for the PD detection of medium voltage power cables. In [22], a novel DAC PD testing system based on the frequency-tuned resonant technique was presented using two couples of IGBTs. In [23], Lei *et al.* proposed a 28-kV high-voltage (HV) multilevel arbitrary waveform generator for insulation testing that is based on a cascade connected multilevel modular converter. In [24], a 230-kV DAC testing system was implemented and applied for the on-site PD testing of transmission power cables. In [25], Eberharter *et al.* proposed a new type of very low

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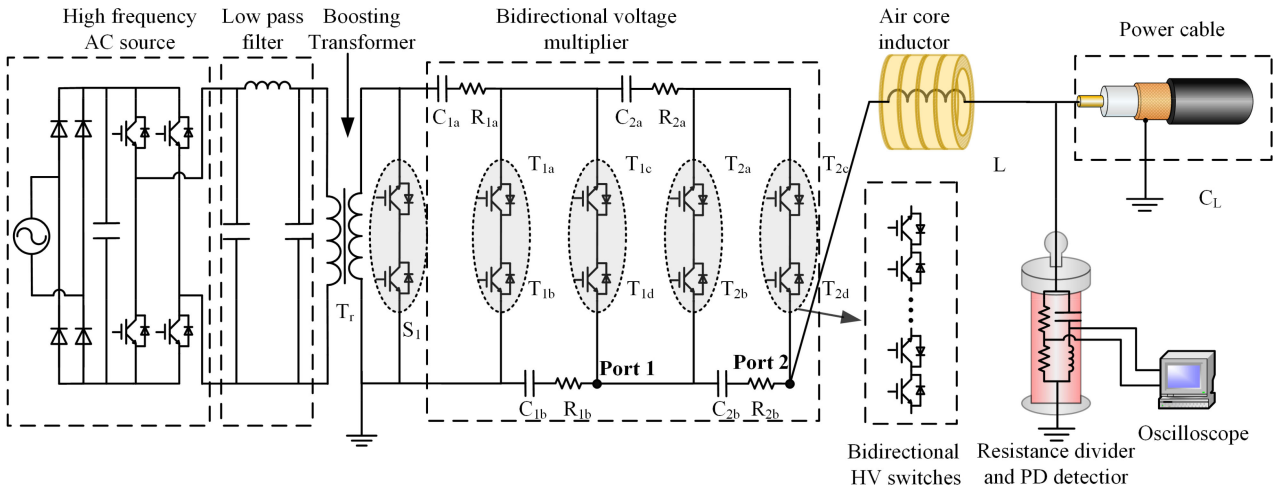

Fig. 1. Circuit topology of the proposed very low frequency cosine-rectangular voltage (VLF-CRV) generator.

frequency sinusoidal HV test system for on-site cable testing up to a root-mean-square voltage of 200 kV. Based on differential resonance technology, a VLF test system was constructed using a large amount of power electronics devices. However, the circuit cannot be applied for PD detection because of the heavy noise. In [26], Salathe proposed a very low frequency cosine-rectangular voltage (VLF-CRV) generator comprising two HVdc sources responsible for voltages of different polarity and four HV switches for polarity reversing and cable charging. However, unfortunately, two of the four switches were still mechanical, and in [27], this limitation was overcome. The proposed VLF-CR test is a multifunctional method that combines the withstand voltage testing and PD testing of power cables such that the on-site testing efficiency of power cables can be significantly enhanced. With its remarkable advantages, it can be anticipated that the VLF-CR generator will be extensively applied in the power industry.

In this article, a novel topology evolving from the VM is proposed and used to construct a VLF-CR generator. The VM concept is to charge the capacitors stage by stage to generate HVdc using relatively low ac voltages [28], [29]. The current advances in solid-state switches have extended modern VMs to many applications such as plasma science [30] and voltage equalizers [31]. The traditional VM is composed of charging capacitors and diodes. Because of the existence of diodes, the traditional circuit is limited to one polarity charging. In this article, several IGBT couples were connected back-to-back in series to construct bidirectional HV switches to replace the diodes in the VM circuit. The replacement of diodes makes bipolar charging possible. Moreover, resistors were connected in series with the charging capacitors to prevent negative influences of the surge current and the oscillating voltage with reversals in polarity. The topology positively affects both device cost and complexity compared to [27]. Moreover, with the specific advantages of the topology in terms of modularity and miniaturization, the VLF-CRV generator is convenient for easy extension to higher voltage levels.

In Sections II and III, this article describes the operational strategy and circuit analyses, respectively, of the proposed topology. Furthermore, a simulation model for the proposed topology is built to confirm the presented analysis in Section IV. Then, Section V presents the implementation of a prototype that adapts to the testing requirements of 8.7/10 kV power cables. The maximum voltage rated up to 35 kV is sufficient in accordance with [5]. Finally, Section VI concludes the article.

II. Overview and Operational Strategy

Fig. 1 shows the new topology of VLF-CRG based on VM. The primary components of the circuit are the power module, VM module, reactor, and capacitive load. The power module is composed of a high-frequency ac source, a low-pass filter, and a boosting transformer. The VM module comprises several bidirectional HV switches, charging capacitors, and blocking resistors.

A. Overview

In this article, the diodes of the classical VM circuit are replaced with bidirectional HV switches, as shown in Fig. 1. Using the topology, the circuit could work as a bipolar HVdc source. The use of semiconductor devices enables the realization of bidirectional HV switches. The bidirectional HV switches comprise IGBT couples connected back-to-back. While T_{ia} (T_{1a}, T_{2a}) and T_{id} (T_{1d}, T_{2d}) are turned OFF, and T_{ib} (T_{1b}, T_{2b}) and T_{ic} (T_{1c}, T_{2c}) are turned ON, the circuit can generate positive HVdc. A negative output voltage can be achieved if the polarities of the bidirectional HV switches are reversed.

To generate VLF-CRV, a capacitive specimen, such as a medium-voltage (MV) cable and an inductor L are connected in the circuit as loads. After the capacitor is charged by the proposed circuit through L for a specific time interval, the polarities of the bidirectional HV switches are reversed to reverse the voltage polarity of C_L. As shown in Fig. 2, because of the resonance of L and C_L, the voltage on C_L reverses in a cosinoidal voltage shape.

The maximum voltages on the charging capacitors, blocking resistors, and bidirectional HV switches are twice as large the output peak voltage of T_r while charging the load. If we neglect the leakage current of the load, the maximum output voltage of the circuit can reach $2n$ times the peak voltage of T_r, where n

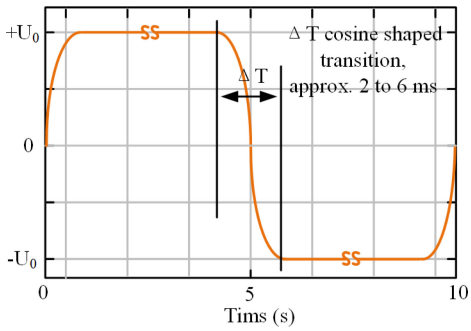

Fig. 2. Typical waveform of 0.1-Hz VLF-CRV.

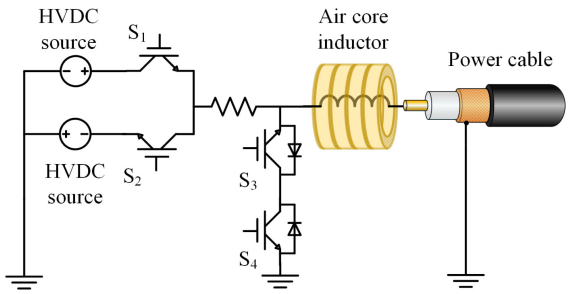

Fig. 3. Topology of the conventional VLF-CRG.

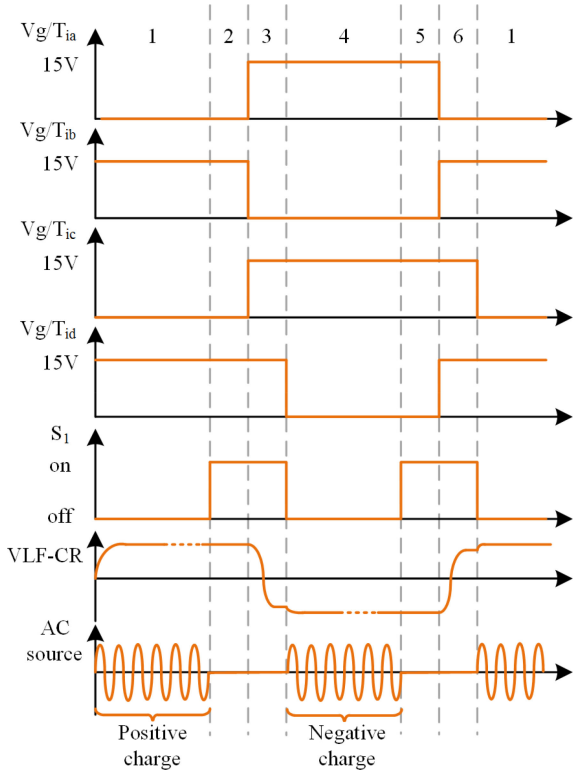

Fig. 4. Operating strategy of VLF-CR generator.

is the stage of the circuit. In the rest of this article, a VLF-CRV generator based on a two-stage VM topology is presented and analyzed.

In the reversing process, electrons in the charging capacitors C_{ia} (C_{1a}, C_{2a}) and C_{ib} (C_{1b}, C_{2b}) are released via the bidirectional HV switches. The bidirectional HV switches guarantee that the voltage applied on the load is nearly zero during the polarity reversing process. However, while the polarity reversing of CL is completed, the voltages on the charging capacitors are still zero, which results in the recharge of the charging capacitors until the voltages on the charging capacitors and C_L are the same. The recharging process would lead to an overvoltage on the bidirectional HV switches. To solve this limitation, blocking resistors are connected in series with the charging capacitors, and the IGBT groups T_{ic} and T_{id} are simultaneously triggered while the polarity reversed. Furthermore, a bidirectional HV switch S_1 is connected in parallel with the secondary coil of the transformer T_r. The HV switch is turned ON while the specimen was being charged, and the switch is turned OFF while the polarity reverses.

The output voltage of the high-frequency ac source is a pulsewidth-modulated signal generated by an inverter bridge. Traditionally, the charging speed increases with an increase in the frequency of the ac source. However, if the frequency of ac source is extremely high, the charging speed would not increase because of the proposed blocking resistors. By suitably optimizing the charging frequency and the passive devices, the capacitive load can be charged to 90% of the predetermined voltage in <3 s while the capacitance load is <1 μF.

Fig. 3 shows the conventional topology of the VLF-CRG [27]. The circuit includes two HVdc sources with different polarities and four HV switches. During the charging process, switches S_3 and S_4 are turned OFF and the specimen is charged by two HVdc sources through S_1 and S_2, respectively. During the polarity reversing process, switches S_1 and S_2 are turned OFF and the voltage on the specimen reverses through switch S_3 or S_4. The maximum withstand voltages of switches S_1 and S_2 are $2U_0$, where U_0 is the maximum output voltage of VLF-CRG. The maximum withstand voltages of switches S_3 and S_4 are U_0. Therefore, the summed withstand voltage of the four switches reaches 6 U_0. As proposed before, the withstand voltage of every bidirectional HV switch of the two-stage novel topology is 0.5 U_0. Moreover, the withstand voltage of the bidirectional HV switch connected in parallel with the secondary coil of T_r is 0.25 U_0. Therefore, the summed withstand voltage of the bidirectional HV switches of the novel topology is 2.25 U_0. Every bidirectional HV switch is composed of two unipolar HV switches. In conclusion, the summed withstand voltage of the switches of the novel topology is 4.5 U_0. Compared with the conventional VLF-CRG, in the novel topology, 25% of HV switches are saved and HVdc sources are not required. Moreover, the novel topology of VLF-CRG is easy to expand by increasing the stages of VM circuits.

B. Operating Strategy

As described in Section I, the polarity reversing of the bidirectional HV switches leads to the polarity reversing of the load. The capacitor C_L is sequentially charged by the positive and negative sources to maintain the absolute value of the voltage. Fig. 4 shows the operating strategy of the proposed VLF-CRV generator, which can be generalized using the following six steps.

Step 1. Positive Charging: In the beginning, the specimen C_L is positively charged. The switches T_{ia} and T_{id} are turned ON, and the switches T_{ib} and T_{ic} are turned OFF. To connect the ac power to the system, S_1 is turned OFF. This step is maintained for $\sim$5 s. By neglecting the leakage current of IGBTs and capacitors, the C_L voltage can be charged to nearly four times as much as the peak voltage of the ac source.

Step 2. Polarity Reversing Preparation: This step is a preparatory step for polarity reversing. In this step, all the devices based on the principle of inverters required to be stopped for the PD detection to reduce interference during commutation. To ensure the same parameter of every stage while the polarity is reversed, the switch S_1 is turned ON to cut off the transformer T_r. This step could only be maintained for several milliseconds.

Step 3. Polarity Reversing: Polarity reversing occurs in this step. The switches T_{ib}, T_{ic}, and T_{id} are turned ON, and the switches T_{ia} are turned OFF. To ensure the reliable activation of switches, dead time is necessary. Switches T_{ib} are turned OFF and switches T_{ia} and T_{ic} are turned ON in succession. The dead time, that is sufficient for T_{ib} to turn OFF, is 2 μs. In this step, the electrons in the capacitors C_{ia} and C_{ib} are discharged through the switches and blocking resistors in $<$100 μs. To ensure the equivalence of the PD detection with 50/60-Hz operating condition, the reversing time depending on the L–C resonance needed to be maintained within 2–6 ms. Hence, this step could be maintained for 10 ms. After polarity reversing, the charging capacitors are recharged. The oscillating voltage on the recharging process is evenly distributed on the switches T_{ia}. T_{ia} are not triggered ON; therefore, the voltage on the load could not be reversed again.

Step 4. Negative Charging: After polarity reversing from the positive, the absolute peak voltage slightly decreased because of the energy loss on the internal resistance of L and the recharge process of the charging capacitors. In this step, the specimen C_L is negatively charged until the absolute peak voltage is the same as the condition before polarity reversing. Unlike Step 1, the switches T_{ib} and T_{ic} are turned ON, and the switches T_{ia} and T_{id} are turned OFF. This step is continued for $\sim$5 s.

Step 5. Polarity Reversing Preparation: This is a preparatory step for the polarity reversing and is the same as Step 2.

Step 6. Polarity Reversing: The polarity reverses from negative to positive in this step. The switches T_{ia}, T_{ic}, and T_{id} are turned ON, and the switch T_{ib} is turned OFF. The details of this step are similar to Step *C*. The dead time setting corresponds with step 3. Switches T_{ia} are turned OFF and switches T_{ib} and T_{id} are turned ON in succession. Step 1 runs after this step until the test procedure is finished.

At the start of the VLF-CR test, the initial voltage on the specimen is zero. In ideal conditions, the specimen would be charged to the predetermined voltage in the first positive charging step. However, if the capacitance of the sample is large and the insulation resistance is small, the charging process will be completed in several cycles.

After completing the VLF-CR test, the device should stop operation and the electrons on the tested sample should be released. By natural discharge itself, the process is relatively slow. In the shut-down process, all of the switches are simultaneously turned ON and the electrons are released through the air-core inductor and the HV switches. Benefitting from the existence of the inductor, surge current does not occur and damped ac voltage is generated on the specimen. In this process, the electrons on the specimen can be released in hundreds of milliseconds.

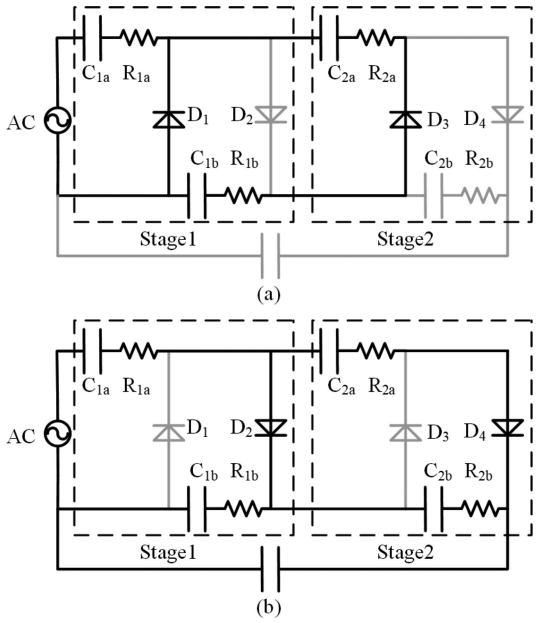

Fig. 5. Equivalent circuit of the two-stage VM neglecting the inductor and conductance of the specimen: (a) negative half cycle; (b) positive half cycle.

Furthermore, to ensure the generation of VLF–CRV with the desired specifications, we present the circuit analysis and parameter optimization in Section III.

III. Circuit Analysis and Parameter Optimization

Circuit analysis is the basis for parameter optimization and implementation. The proposed circuit is analyzed in four steps referred to in the VLF–CR waveform. First, we analyze the charging process to confirm the charging speed. Second, the polarity reversing process of the specimen is modeled. To limit the oscillating voltage, the recharging process is analyzed in this section. Third, the influence of the stray capacitances of IGBTs is analyzed. Finally, the strategy of parameter optimization is introduced based on the preset analyses.

A. Charging Process

In this section, the charging speed is the primary parameter that we want to obtain. The charging process can be analyzed as a traditional VM circuit. The positive and negative charging processes of the topology are entirely symmetrical. In this section, only the positive charging process will be analyzed.

Fig. 5 shows the equivalent circuit for the proposed topology, which neglects the conductance of the specimen at negative and positive half cycles of the ac source. In the negative half cycle of the ac source, the top charging capacitors are charged through D1 and D3. In the positive half cycle of the ac source, the bottom

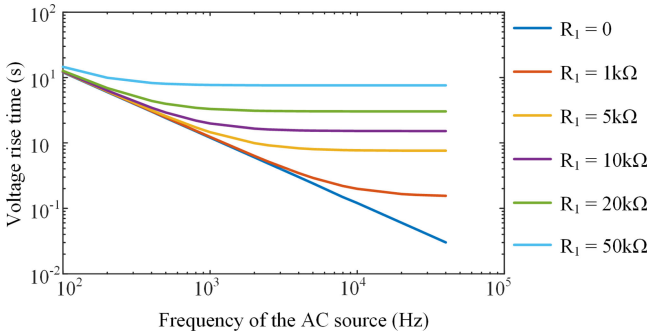

Fig. 6. Relationship between the rise time from 0% to 90% and the blocking resistor.

charging capacitors and the specimen are charged via D2 and D4.

However, because the topology has several nonlinear components, it is hard to obtain the exact expression. Thus, we obtain the charging speed of different parameters with the help of MATLAB/Simulink. Traditionally, a high ac frequency produces a fast charging speed. However, the existence of the blocking resistors considerably affects the charging speed. Then, the polarity of the ac source reverses; however, the charging capacitors cannot be fully charged or discharged because of the time constant $\tau = \mathrm{RC}$.

The model is built using MATLAB/Simulink to analyze relationships among charging speed, frequency of ac source and the blocking resistors. In the process, the charging capacitors are selected to be 10 nF and the load is selected to be 1 μF. Fig. 6 shows the rise time from 0% to 90% of the full output voltage. With the improvement of the blocking resistance $\mathrm{R_1}$, the charging speed significantly reduces at high frequencies. However, at a low frequency, the blocking resistors have little effect on the charging speed. As per the simulation results, while the passive components are determined, the charging frequency should be selected at the plateau part.

B. Polarity Reversing Process

Polarity reversing occurs while the specimen is being charged for a specific interval. In this process, the electrons in the charging capacitors are discharged through the adjacent HV switches that would not affect the polarity reversing process. In this process, the specimen discharges through the inductor, and the HV switches forming an *L–C* series resonance circuit. As per the operating strategy, Fig. 7(a) shows what happens when the polarity reverses from positive to negative. Neglecting the voltage drops of IGBTs, the voltage on the capacitance load follows a damped cosinoidal waveform as follows:

$$U_{CL}(t) = \frac{U_0}{A} e^{-\delta(t-t_0)} \cos[\omega(t-t_0)+\beta] \tag{1}$$

where U_0 and $\mathrm{t_0}$ are the initial voltage and initial time, respectively, when the voltage reverses, and

$$A = \sqrt{1 - \frac{R_L^2 C_L}{4L}} \tag{2}$$

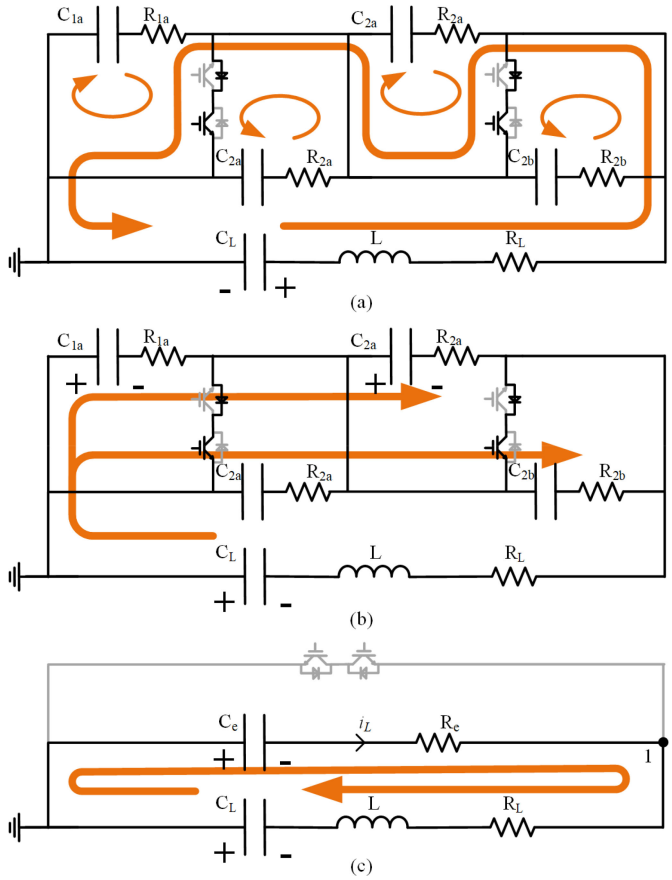

Fig. 7. Equivalent circuits of the reversing process and the recharging process. (a) Schematic diagram of polarity reversing. (b) Schematic diagram of the recharging process. (c) Simplified schematic diagram of the recharging process.

$$\omega = \sqrt{\frac{1}{LC_L} - \left(\frac{R_L}{2L}\right)^2} \tag{3}$$

$$\beta = \arccos A \tag{4}$$

$$\delta = \frac{R_L}{2L} \tag{5}$$

where L is the inductance of the reactor; $\mathrm{R_L}$ is the internal resistance of the reactor; and C_L is the capacitance of the specimen. Depending on the derivation, the voltage on the specimen slightly attenuates after polarity reversing

$$U_{CL}(t_1) = -KU_0 \tag{6}$$

where $\mathrm{t_1}$ is the end time of polarity reversing and

$$K = e^{-\pi \tan\theta} \tag{7}$$

After polarity reversing, the proposed voltage oscillation occurs on account of recharging the charging capacitors. Fig. 7(b) shows the schematic of the recharging process. HV oscillation always leads to high blocking voltage of IGBTs that considerably increases the complexity and cost of the system. To assess the effect of the oscillating voltage on the charging capacitors and IGBTs, the recharging process is mathematically modeled and the passive components are optimized.

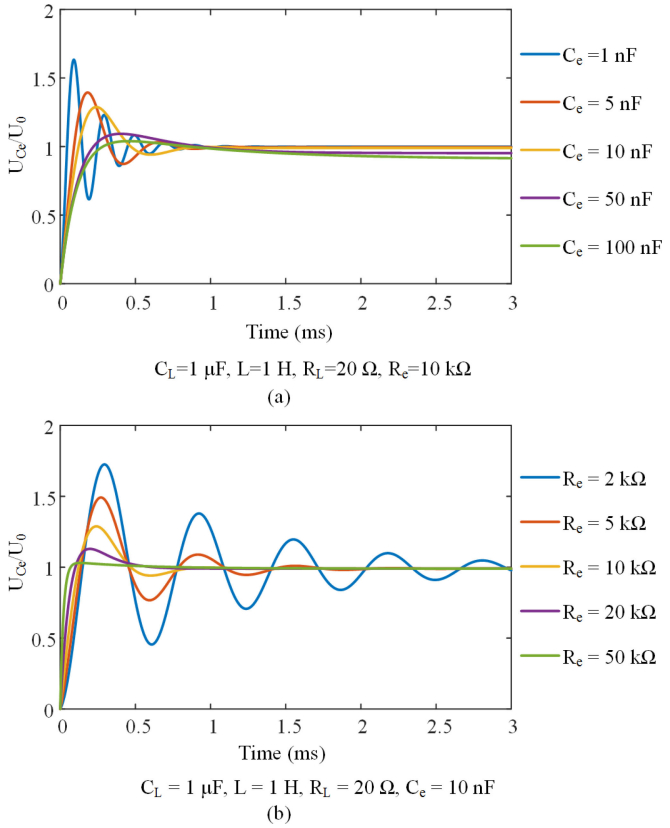

Fig. 8. Voltage on the HV switch while the charging capacitors are recharged.

Fig. 7(c) shows the equivalent circuit of the recharging process can be simplified into a dynamic circuit with three orders. C_e is the equivalent capacitance of the charging circuit, and R_e is the equivalent resistance of the charging circuit. In the two-stage system, C_e equals the value of the charging capacitors, and R_e equals the value of the blocking resistors. The state equations are written as follows:

$$\frac{dU_{CL}}{dt} = -\frac{i_L}{C_L} \tag{8}$$

$$\frac{dU_{Ce}}{dt} = \frac{i_L}{C_L} \tag{9}$$

$$\frac{di_L}{dt} = \frac{U_{CL}}{L} - \frac{U_{Ce}}{L} - \frac{R_e + R_L}{L} i_L \tag{10}$$

where U_{CL} denotes the voltage on the specimen; U_{Ce} denotes the voltage on the capacitor C_e; and i_L denotes the current of the inductor. The initial value of U_{CL} is $U_{CL}(t_1)$, and both U_{Ce} and i_L have the initial value of zero.

To obtain the maximum value of the oscillating voltage, we used recursive numerical computation to solve the third-order system. The total voltage that the HV IGBTs can withstand is as follows:

$$U_s = U_{Ce} + R_e i_L \tag{11}$$

The inductor was selected to be 1 H, and the internal resistance of the inductor was 20 Ω. The capacitance of the specimen was 1 μF. Fig. 8 shows the voltages on the HV switch U_0. While the resistance of R_e is fixed, the peak value of the oscillating voltage

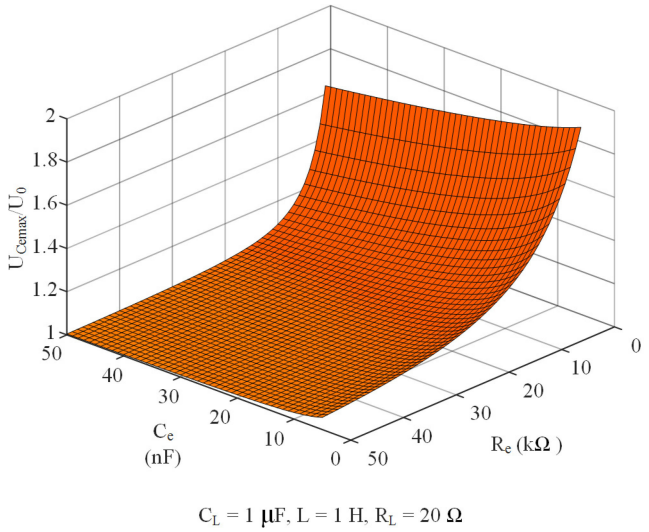

Fig. 9. Relationships among Re, Ce, and the ratio of the maximum value of U_s to $U_{Ce}(t_1)$.

decreases with increase in the capacitance of C_e. Furthermore, while the capacitance of C_e was fixed, the peak value of the oscillating voltage decreases with increase in the resistance of R_e. Moreover, Fig. 9 shows the relationships among R_e, C_e, and the ratio of the maximum value of U_s to $U_{Ce}(t_1)$ when the loads are fixed. The rule we obtain from Fig. 9 corresponds with that shown in Fig. 8. With increase in R_e and C_e, the voltage oscillation is adequately suppressed. Nevertheless, as the capacitance of C_e increases, its volume will increase, and as the resistance of R_e increases, the charging speed will be limited. Therefore, the values of R_e and C_e cannot be as large as possible.

Moreover, the recharging process also leads to a voltage drop in C_L because of the redistribution of the electrons on C_L. Finally, the voltage of C_L was maintained at U_1 as follows:

$$U_1 = -\frac{C_L}{C_e + C_L} K U_0 \tag{12}$$

Depending on the analysis, the high resistance of R_e and high capacitance of C_e led to lower peak values of the oscillating voltage. However, the high capacitance of C_e led to a HV loss of C_L and a high resistance of R_e, which led to low charging speed.

C. Analysis of the Influence of Stray Capacitances of IGBTs

The stray parameters have an obvious influence on the circuit. During the charging process, whether positive or negative, the states of IGBTs are fixed, and thus the HV switches can be considered as diodes. During the polarity-reversing process, the current mutation flowing through the HV switches does not happen due to the presence of the air-core inductor. Therefore, the stray inductance has no effect on the circuit.

The proposed VLF-CRV generator uses bidirectional HV switches composed of several IGBTs connected back-to-back in series; these switches replace the diodes in the traditional VM circuits. Because of the special structure of IGBTs, stray capacitances exist between the emitters and the collectors of

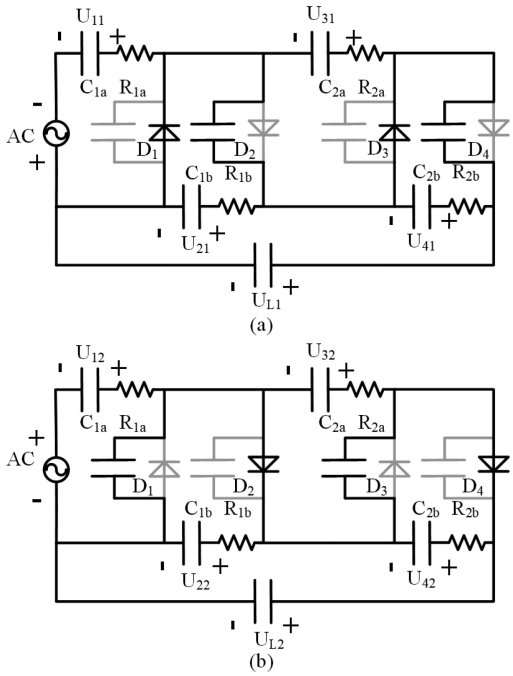

Fig. 10. Equivalent circuits of the positive charging process in (a) the negative half cycle of the ac source and (b) the positive half cycle of the ac source.

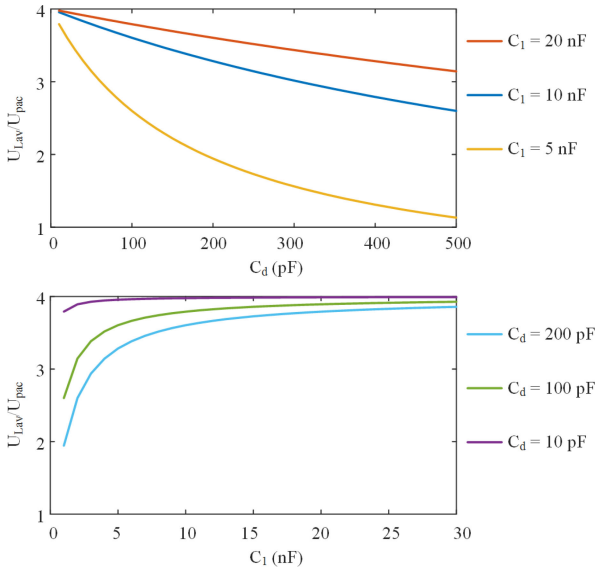

Fig. 11. Variations in the average voltage of C_L, the charging capacitors, and the stray capacitances.

IGBTs that can reach tens or hundreds of picofarads, which cannot be neglected.

While positively charging the capacitance C_L, the equivalent circuit of the charging circuit (considering the stray capacitances of IGBTs) is corrected as shown in Fig. 10. In the negative half cycle of the ac source, the charging capacitors C_{ia} (C_{1a}, C_{2a}) are charged through D_1 and D_3. Nevertheless, in this period, the diodes D_2 and D_4 withstand the reverse voltage, which results in charging the stray capacitances of diodes. In the positive half cycle of the ac source, the charging capacitors C_{ib} (C_{1b}, C_{2b}) are charged through D_2 and D_4, and the electrons in the stray capacitances D_2 and D_4 are released. Moreover, the diodes D_1 and D_3 withstand the reverse voltage, which resulted in charging the stray capacitances of D_1 and D_3 in this period. In the next half cycle of the ac source, the electrons in the stray capacitances of D_1 and D_3 are released. In every period of the ac source, the stray capacitances of the semiconductor devices are charged and discharged once, which directly leads to power loss.

As per the laws of conservation of voltage and current, in the interval from the negative peak moment of the ac voltage to the positive peak moment of the ac voltage, we can obtain the following equations by neglecting the blocking resistors:

$$(U_{12}-U_{11})C_1+U_{22}C_d+(U_{22}-U_{21})C_1 = (U_{32}-U_{31})C_1+U_{42}C_d+(U_{42}-U_{41})C_1 \quad (13)$$

$$(U_{32}-U_{31})C_1+(U_{42}-U_{41})C_1+U_{42}C_d+(U_{L2}-U_{L1})C_L=0 \quad (14)$$

$$U_{22}-U_{12}=U_{\mathrm{pac}} \quad (15)$$

$$U_{42}+U_{22}=U_{L2} \quad (16)$$

$$U_{32}=U_{42} \quad (17)$$

where U_{11}, U_{21}, U_{31}, and U_{41} are the voltages of the charging capacitors at the negative peak moment of the ac voltage. U_{L1} is the voltage of C_L at the negative peak moment of ac voltage. U_{12}, U_{22}, U_{32}, and U_{42} are the voltages of the charging capacitors at the positive peak moment of the ac voltage. U_{L2} is the voltage of C_L at the positive peak moment of the ac voltage. C_1 and C_{d} are the capacitances of the charging capacitors and stray capacitance, respectively, and U_{pac} is the peak value of the ac voltage.

In the interval from the positive peak moment of the ac voltage to the negative peak moment of ac voltage, we obtained the following equations by neglecting the blocking resistors:

$$(U_{21}-U_{22})C_1+(U_{31}-U_{32})C_1+(U_{L1}-U_{L2})C_L+U_{21}C_d=0 \quad (18)$$

$$(U_{21}-U_{22})C_1+(U_{31}-U_{32})C_1+U_{21}C_d-(U_{41}-U_{42})C_1-U_{41}C_d=0 \quad (19)$$

$$U_{11}=U_{\mathrm{pac}} \quad (20)$$

$$U_{21}+U_{41}=U_{L1} \quad (21)$$

$$U_{31}=U_{21} \quad (22)$$

Fig. 11 shows the variations in the average voltage of C_L, charging capacitors, and stray capacitances. The voltage on C_L increases as the stray capacitances decrease. The average voltage of C_L can be expressed as U_{Lav} and can be derived as follows:

$$U_{\mathrm{Lav}}=\frac{U_{L1}+U_{L2}}{2} \quad (23)$$

Fig. 12 shows the charging processes with different stray capacitances obtained by neglecting the blocking resistors and considering the blocking resistors. To obtain the waveforms, a model was built in MATLAB/Simulink. The frequency of the ac source was 1 kHz, and the stray capacitances were set to 50 pF.

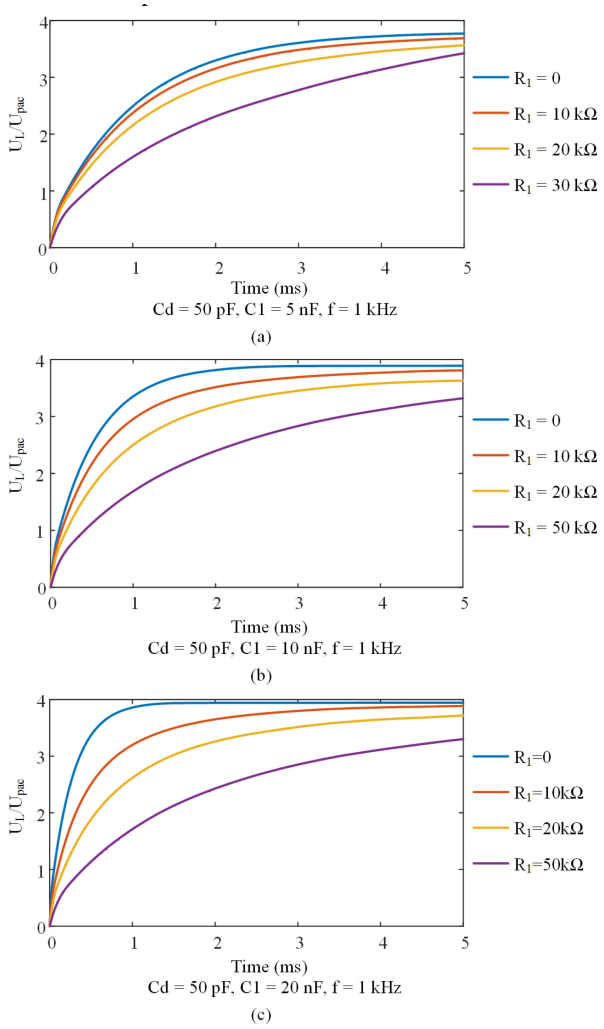

Fig. 12. Waveforms of the charging process with different parameters of passive components. R1 denotes the resistance of the blocking resistors and *f* denotes the frequency of the ac source.

The existence of the blocking resistors resulted in a decrease in the charging speed. This result corresponds with the conclusions presented in Section A.

D. Optimization of the Parameters

In the proposed circuit, several parameters, including blocking resistors, charging capacitors, and the frequency of the ac source, need to be optimized. The following rules required to be followed for this:

1) The cooperation of the blocking resistors and the charging capacitors can effectively avoid the influence of the voltage oscillation while the polarity is reversed. It can reduce the withstand voltage of the selected IGBTs.
2) The capacitance of the charging capacitors should be much higher than the stray capacitances of the IGBTs.
3) Considering the charging speed, the value of the blocking resistors cannot be too high.
4) To minimize the energy loss during polarity reversing, the value of the charging capacitors should be as small as possible.

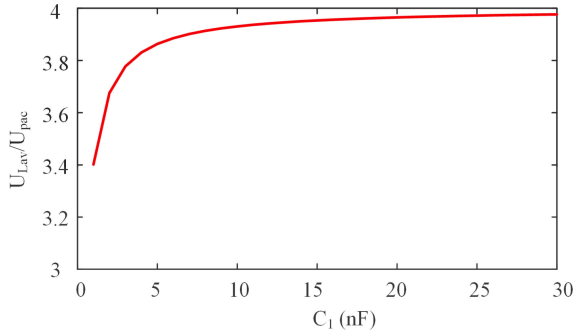

Fig. 13. Variation in the average voltage of C_L and the charging capacitors C_1 while Cd is equal to 32.2 pF.

5) The passive components should be as compact as possible.

We started by determining the model of IGBTs. To ensure maximum power per device, minimum number of devices, and minimum device size, we selected the IGBT chips IXYS^{TM} IXBL60N360 as the cell of the HV switches. The bidirectional HV switch comprises six couples of IXBL60N360 connected back-to-back in series. The stray capacitance of every IGBT chip is 193 pF as per the datasheet, and the stray capacitance of the bidirectional HV switch is ∼32.2 pF. The variation in the average voltage of C_L and the charging capacitors C_1 while the stray capacitance is 32.2 pF is shown in Fig. 13. Considering the general commercial model of the passive devices, the charging capacitors were determined to be 10 nF. In this situation, the voltage loss created by stray capacitance is <3%.

Moreover, the blocking resistors were determined to be 20 kΩ, and the frequency of the ac source was determined to be 10 kHz. In this configuration, the oscillating voltage is limited to less than 1.1 times the initial voltage. Moreover, the stable voltage of the test sample could reach 3.9 times the pack value of the ac source. When the load is 1 μF, the circuit could complete 90% of the charging process in 3 s, which is sufficient for the on-site test.

IV. Simulation

To validate the presented analysis, we built a simulation model in MATLAB/Simulink based on the proposed topology and parameters. A 10-kV ac source with a frequency of 10 kHz was selected to be the energy support. The periodic time of VLF–CSV was 10 s. *L* was selected to be a 1 H inductor whose internal resistance was 20 Ω. The different values of C_L were simulated to assess the capacity of carrying loads. The charging capacitors C_{ia} and C_{ib} were selected to be 10 nF. The block resistors were selected to be 20 kΩ based on the results of the circuit analysis.

Fig. 14 shows the waveforms of the voltages on the specimens with different capacitances. Even when the load capacitance was as high as 2 μF, the voltage on C_L could still be charged to ∼40 kV in two cycles. Table I lists the voltage loss during polarity reversing.

The reversing process shows that there will be a slight voltage drop after the voltage reversing on C_L is completed because of the redistribution of electrons during the recharging of charging

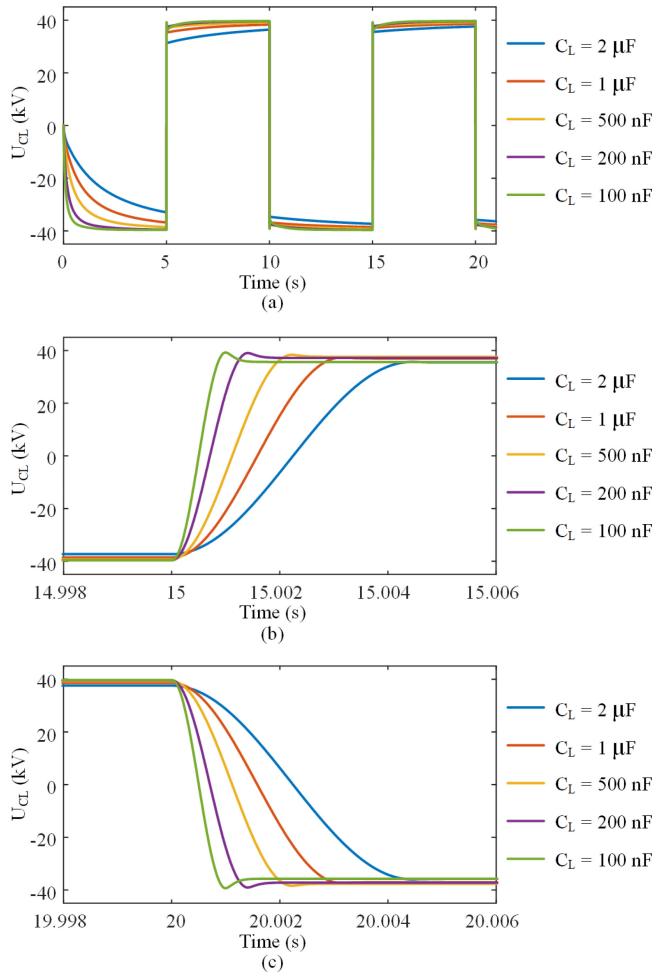

Fig. 14. Simulation results for the proposed VLF–CRV generator.

TABLE I
VOLTAGE LOSS DURING POLARITY REVERSING

Capacitance of C_L	Voltage on C_L before reversing (kV)	Voltage on C_L after reversing (kV)	Voltage loss(%)
2 μF	37.59	−35.77	4.84
1 μF	38.62	−37.06	4.04
500 nF	39.26	−37.64	4.13
200 nF	39.60	−37.18	6.11
100 nF	39.71	−35.72	10.5

capacitors. The lower the load capacitance, the more the voltage drops. Moreover, the period of the reversing process is in accordance with (3).

The voltage oscillation that occurs while the charging capacitors are recharged after the polarity reversing causes overvoltage on the IGBTs. Fig. 15 shows the details of the voltages on the IGBTs while the polarity is reversed. Fig. 16 shows the huge overvoltage on the IGBTs without considering the cooperation of the charging capacitors and the blocking resistors. It shows the effect of parameter optimization. Table II shows the oscillating voltage on the IGBTs during polarity reversing. The oscillation voltage is always less than 1.1 times the voltage before the voltage reversing.

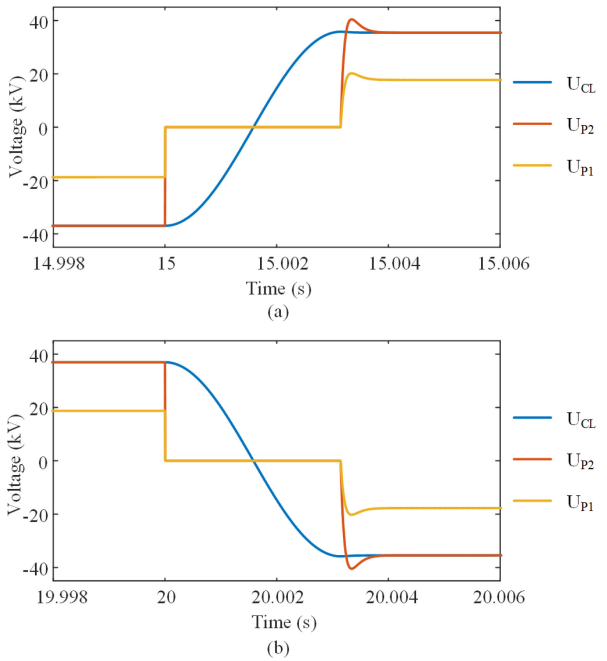

Fig. 15. Details of polarity reversal. UP2 is the voltage on port 2, as shown in Fig. 1, and UP1 is the voltage on port 1, as shown in Fig. 1.

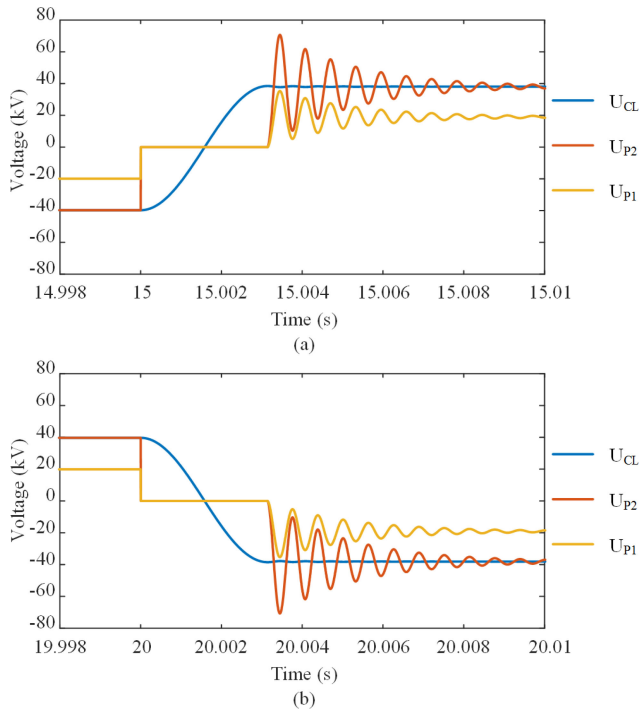

Fig. 16. Polarity reversal without considering the influence of voltage oscillation. UP2 is the voltage on port 2, as shown in Fig. 1, and UP1 is the voltage on port 1, as shown in Fig. 1.

The simulation results prove the feasibility of the proposed topology. VLF-CRV can be obtained and the requirement for restraining the oscillating voltage can be fulfilled. The results provide a reliable principle to support the implementation of the VLF-CRV generator.

TABLE II
VOLTAGE OSCILLATION DURING REVERSING

C_L	Voltage on IGBTs before reversing(kV)	Maximum Voltage on IGBTs during reversing(kV)	Rate of overvoltage (%)
2 μF	37.59	−40.69	108.25
1 μF	38.62	−42.28	109.48
500 nF	39.26	−43.18	109.98
200 nF	39.60	−43.35	109.47
100 nF	39.71	−42.83	107.86

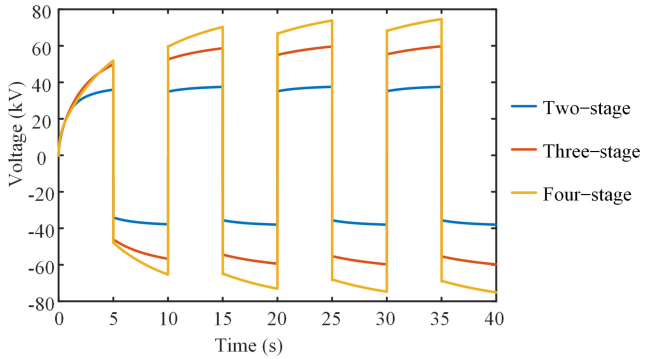

Fig. 17. Output voltages of different stages of the presented circuit.

Modularity is a superiority of the presented VLF-CRG compared with the conventional topology. In this article, a two-stage VLF-CRG is developed and implemented. In the simulation environment, a three-stage topology and a four-stage topology are simulated. Fig. 17 shows the output voltages of the three-stage and four-stage topologies. It is obvious that the output voltage linearly increases with the stage of the circuit; however, it takes longer to charge to a higher voltage.

V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

We implemented a prototype to validate the proposed VLF-CRG. The prototype was composed of a 10 kHz ac source, a boosting transformer, a control system, IGBT stacks, and power supply modules for IGBT stacks. Several experiments were performed to confirm the feasibility and stability of implementation. A detailed illustration of the implementation is presented in the following sections. Furthermore, we included certain results of an assembled setup testing.

A. Implementation

1) HV Switch: To integrate the proposed circuit as compactly as possible, we designed IGBT stacks, as shown in Fig. 18. For ease of integration, we selected the IGBT chip IXYS IXBL60N360 as the cell of the HV switches. Charging capacitors, block resistors, bidirectional HV switches, and auxiliary circuits were integrated as the IGBT stacks. To fit the voltage blocking requirement, six couples of series back-to-back connected IGBTs were assembled to form a 21.6-kV bidirectional HV switch. The IGBT couples and their auxiliary circuits were then integrated as a switch unit. The IGBTs were triggered by optical fibers that were connected with the control system. In our integration, the static voltage balancing resistors connected

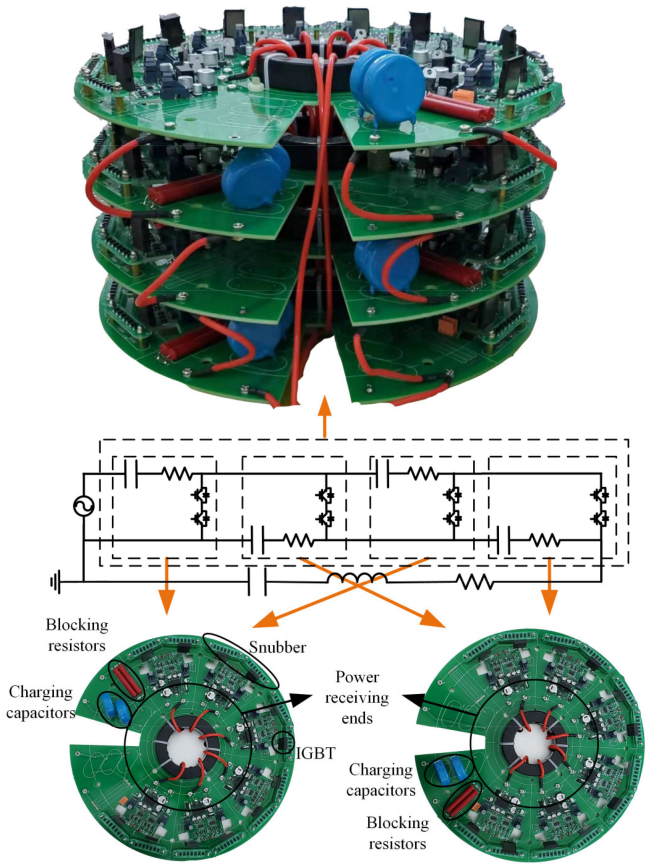

Fig. 18. View of IGBT stacks.

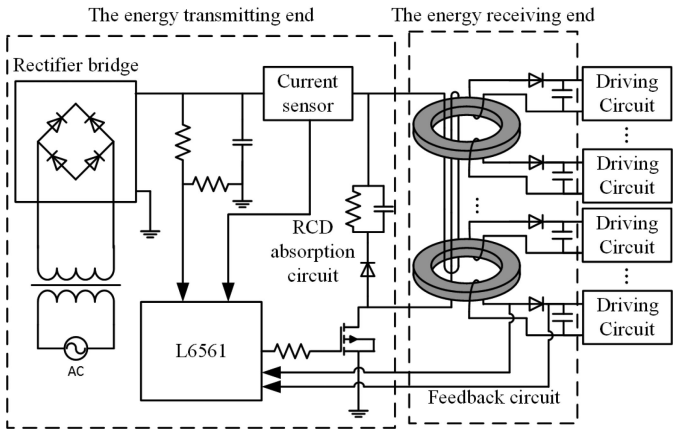

Fig. 19. Schematic diagram of the power supply module of the IGBT stacks.

in parallel with the IGBTs were set at 24 MΩ. The selection of the static voltage balancing resistors R_s should meet the following requirement:

$$R_s << \frac{U_{CES}}{I_{\text{leakage}}} \tag{24}$$

where U_{CES} is the rated voltage and I_{leakage} is the leakage current in the OFF-state of the IGBT. The total resistance of each bidirectional HV switch was ∼144 MΩ, and its leakage current was negligible. Snubber circuits are connected with IGBTs in

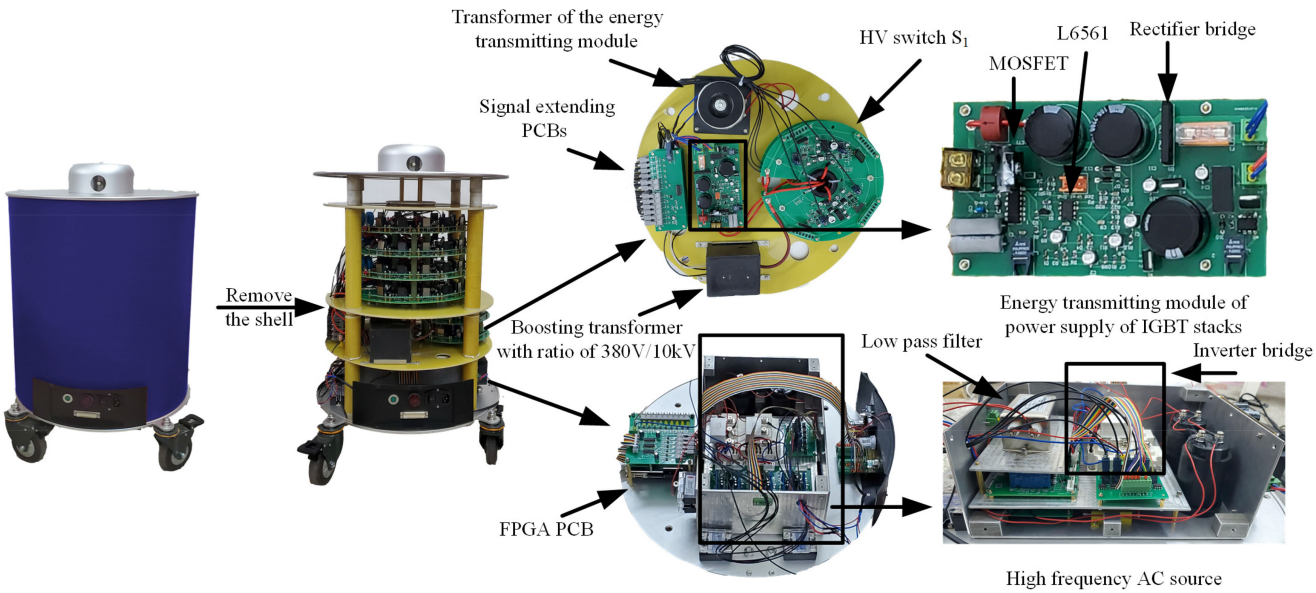

Fig. 20. Structure of the proposed VLF-CRV generator.

parallel. The snubber circuit is composed of six transient voltage suppressors (TVS) with a reverse voltage of 550 V connected in series. The charging capacitors and the block resistors were assembled with the bidirectional HV switches. Moreover, as shown in Fig. 20, the HV switch S_1 was constructed by four couples of IGBTs connected back-to-back in series.

2) Power Supply of IGBT Stacks: The IGBT stacks needed to fit the requirement of isolated power supply. In our prototype, the power supply module was composed of two parts: the energy receiving end and the energy transmitting end. It was designed based on the flyback circuit, as shown in Fig. 19.

The core of the energy transmitting module is a chip L6561 having the functions of power factor correction that controls the activation of the semiconductor switch. The ON-resistance of the semiconductor switch was approximately tens of milliohms, which reduced the switching energy loss. Moreover, to reduce the voltage spike caused by the leakage inductance, an RCD absorption circuit was connected in parallel with the primary winding.

As shown in Fig. 18, the energy receiving ends were integrated in the IGBT stacks. It comprised magnetic cores, secondary windings, and rectifying circuits. An electrolytic capacitor with a large capacitance of 3300 μF was connected in parallel with the power supply module of each unit. This capacitor acted both as a filter and an energystorage element and ensured that the IGBTs activated normally while the power supply module was stopped during the polarity reversing process. The module could support 17 V, which was sufficient for IGBT drivers.

3) High-Frequency AC Source: As shown in Fig. 20, the high-frequency ac voltage can be obtained from an inverter. Two Al electrolytic capacitors with large capacitances were charged using a full-bridge rectifier. The IGBT FF200R12KS4 modules produced by Infineon were selected to be the cells of the inverter bridge. The maximum dc forward current of the module can reach 200 A at 65 °C, which is sufficient for our application. To suppress the influence of stray inductance, two absorb capacitors with a value of 0.1 μF are connected to the IGBT modules in parallel. The inverter signals were given by the FPGA board. To suppress harmonics, an *LC* filter was connected with the inverter. A booster transformer with a transformer ratio of 380 V/10 kV was used to improve the voltage rate. To decrease interference while detecting the PD signals, the ac source was turned OFF by the control system for polarity reversing.

4) Control System: The control system comprised two parts, as shown in Fig. 20. One part was a printed circuit board (PCB) with an FPGA chip ALTERA EP4CE6, which provided the control signal of IGBTs and the inverter bridge of the ac source. The other part was structured by five PCBs used for extending the activation signals of IGBTs. The extension of the control signal could extend every IGBT activation signal to trigger 12 optical signals using 12 fiber optic transmitters.

Fig. 20 shows the prototype that we built. To avoid magnetic saturation, we selected an air-core inductor having a value of 1 H. However, without the iron core, the number of turns increased, which meant that the inductance was large. The internal resistance of the inductor was 20 Ω. For the convenience of application and experiment, the inductor and the PD coupler were integrated into a shell, as shown in Fig. 21.

B. Experimental Results

Case 1. Test on a Capacitor: First, the tested object was chosen to be a 250-nF film capacitor, which was a reasonable substitute for several hundred meters of power cables. The voltages on the key nodes were measured by three HV probes Pinktech P4069A. The data were collected using a Picoscope 5444B.

The experiment results are shown in Fig. 22. From Fig. 22(a), a perfect VLF-CRV was generated on the specimen. The voltages on the charging capacitors C_{ib} during the polarity reversing process are shown in Fig. 22(b). After cutting off the transformer,

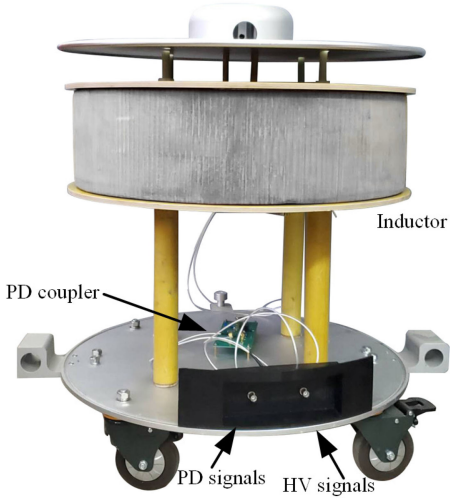

Fig. 21. Inductor and PD coupler.

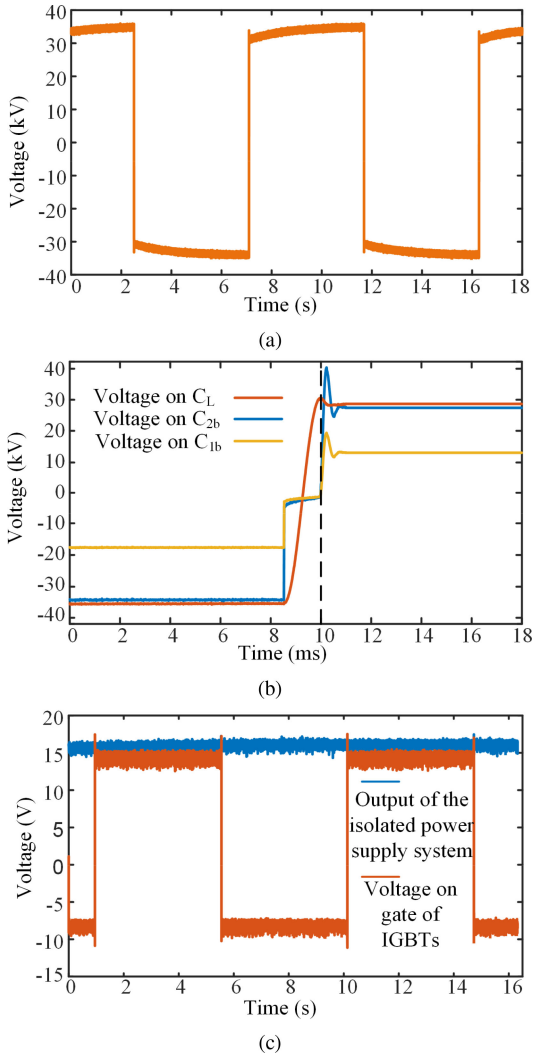

Fig. 22. Measurements of VLF-CRV generated on the capacitor. (a) VLF-CRV on the capacitor. (b) Voltage on the secondary coil of transformer and the charging capacitors. (c) Voltage supplied by the isolated power supply module and the voltage on the gate of an IGBT.

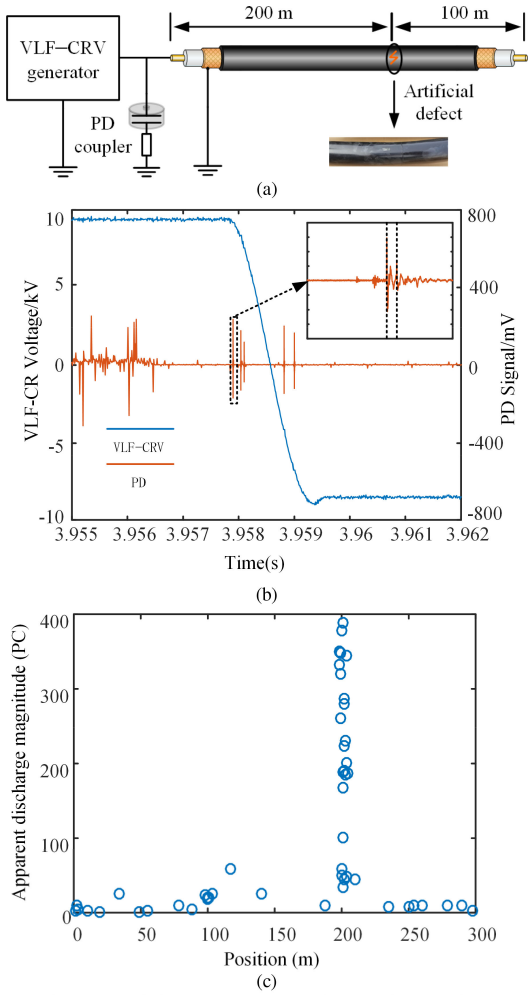

Fig. 23. Schematic and the experimental results on cable. (a) Diagram of the experiment. (b) Waveform of polarity reversing process. (c) PD positions.

the voltage was evenly distributed on C_{ib}. During the polarity reversing, the electrons on C_{ib} immediately discharged. The block resistors with the value of 20 kΩ decreased the influence on the discharge of the capacitors. After polarity reversing, the charging capacitors were recharged by the specimen, which resulted in a voltage drop on the specimen. Note that the voltage oscillations on the charging capacitors and on the bidirectional switches were effectively limited. The voltage on the specimen dropped by ∼15% compared with the initial situation before the polarity was reversed, and it was recharged to the initial value in <2 s. The VLF-CRV could attain a peak value of 35 kV, which was sufficient for the on-site test. Fig. 22(c) shows the voltage on the isolated power supply module. We can see that the voltages on the gates of IGBTs activate normally, and these voltages are not affected by power loss while the polarity is reversed.

Case 2. Test on a Cable: We performed another experiment to assess the PD detection function and background noise of the out prototype. A 300 m single-phase 8.7/10 kV XLPE power cable was selected as the sample. An artificial defect was added on the tested cable at a location 200 m from the near end that directly

connected with the VLF-CRV generator, as shown in Fig. 23(a). A PD detector was connected to the end. The PD detector was composed of a coupling capacitor and a coupling inductance, which acted as a high-pass filter. The polarity reversal details were obtained from the PD detector and the HV probe shown in Fig. 23(b).

The noise dropped to several millivolts because of quitting the isolated power supply module and the high-frequency ac source, which effectively improved the sensitivity of measurement. The time-domain reflectometry (TDR) method is widely accepted as a PD location algorithm for power cables. PD locating results obtained using the TDR method is shown in Fig. 23(c). Most of the PDs occur at a location 200 m from the near end, which is consistent with the anticipated results.

VI. Conclusion

A novel topology of the VLF-CRV generator based on VM is presented in this article. The special topology makes the HVdc source dispensable. The voltage source was replaced with a high-frequency ac source comprising a converter, a low-pass filter, and a boosting transformer. The characteristic of full control of IGBT enables the bidirectional controllable switches. Circuit analyses of the charging speed, the polarity reversing process, and the influence of stray capacitances provide powerful guidance for parameter optimization. The operation has been confirmed by simulation using MATLAB/Simulink. We designed and implemented a prototype for 8.7/10 kV VM cables. Our experiment results prove the reliability and feasibility of the prototype.

VLF-CRV detection is a multifunction method for cable testing. It is both a withstand voltage test method and a PD detect means. Realizing the withstand voltage test and PD detection simultaneously can prevent cable breakdown that will provide technical support for timely repair and will prevent more serious damage. Thus, the proposed topology and the cable test method may be considered as a promising alternative for the high-efficiency testing of power cables.

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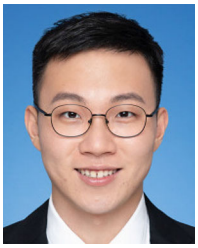

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