High-Efficiency *LLC* Resonant Converter With Reconfigurable Voltage Multiplying Rectifier for Wide Output Voltage Applications

Jaeil Baek, *Member, IEEE*, Keon-Woo Kim, *Student Member, IEEE*, Han-Shin Youn, *Member, IEEE*, and Chong-Eun Kim, *Member, IEEE*

***Abstract*—This article presents a reconfigurable voltage multiplying rectifier (RVMR) to improve the performance of an *LLC* resonant converter for wide output voltage applications. The RVMR can operate as voltage-doubler mode or voltage-quadrupler mode according to the primary switching strategy. Two operation modes split a wide output voltage range into two narrow ranges. Therefore, the RVMR enables the *LLC* resonant tank to be designed in a narrow output voltage range, which results in a narrow switching frequency range, high efficiency, and high power density. A smooth mode transition can be achieved by adopting a phase-shift control to general pulse frequency modulation control without any additional switch. The proposed RVMR *LLC* converter can improve its efficiency by 2.9% and reduce component volume by 26% compared to the conventional full-bridge *LLC* resonant converter. A 750-W prototype with 400 V input, 100–300 V output voltage, and 2.5 A max output current has been built and tested to verify the effectiveness of the proposed converter.**

***Index Terms*—*LLC* resonant converter, phase-shift (PS) control, reconfigurable voltage multiplying rectifier (RVMR), wide output voltage range.**

I. Introduction

GLOBAL power consumption has significantly increased due to high growth of electronic devices. Many developing countries will accelerate this trend, making the global energy crisis and global warming much worse. Accordingly, many efficiency regulations and guidelines have been introduced to reduce power consumption of power supplies [2]–[4]. Power supply manufacturers have a significant challenge of improving the efficiencies of their products.

Manuscript received March 20, 2020; revised September 5, 2020; accepted December 10, 2020. Date of publication December 25, 2020; date of current version March 5, 2021. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) under Grant 2020R1AC2C1005737. Recommended for publication by Associate Editor D. Costinett. *(Corresponding author: Chong-Eun Kim.)*

Jaeil Baek is with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08540 USA (e-mail: jaeil.baek@princeton.edu).

Keon-Woo Kim is with the Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea (e-mail: rainbowdot@kaist.ac.kr).

Han-Shin Youn is with the Department of Electrical Engineering, Incheon National University, Incheon 406840, South Korea (e-mail: hsyoun@inu.ac.kr).

Chong-Eun Kim is with the Department of Control and Instrumentation Engineering, Gyeongsang National University, Jinju 52828, South Korea (e-mail: bliss55178@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2020.3047005.

Digital Object Identifier 10.1109/TPEL.2020.3047005

In general, grid interface ac–dc power supplies over 70 W typically consist of a power factor correction (PFC) stage and a dc–dc stage. The PFC stage is usually implemented as a boost converter [5], [6], which provides high power quality and regulates the bus voltage. The dc–dc stage generates the well-regulated output voltage with the bus voltage. Many isolated dc–dc topologies such as *LLC* converter, phase-shifted full-bridge (FB) converter, active-clamp forward converter, and dual-active-bridge converter can be used. These days, *LLC* resonant converters have been adopted in many applications due to their efficient power conversion. *LLC* resonant converters can achieve a zero-voltage switching (ZVS) operation for the primary switches and zero-current switching operation for the secondary switches. The voltage stresses on both the primary and secondary switches are clamped to the input and output voltage, respectively, which eliminates snubbing loss and leverages high-performance devices. However, *LLC* resonant converters have critical challenges in wide output voltage applications such as LED driver, battery charger, and renewable power system because its switching frequency has to swing in a wide range and deviates from the resonant frequency, which causes higher conduction loss, core loss, and switching loss [7]–[17]. Therefore, *LLC* resonant converters have low efficiency and low power density in wide output voltage applications.

Many approaches have been researched to realize a wide voltage regulation range of the *LLC* resonant converter while maintaining high efficiency [7]–[17]. In [7] and [8], improved design methodologies were presented to optimize the *LLC* resonant converter. Thus, they can improve efficiency and power density by drawing the full capabilities of the *LLC* resonant converter. However, they still have low efficiency once the switching frequency is far away from the resonant frequency. In [9], a variable resonant tank was implemented with one additional resonant capacitor and an auxiliary switch to extend the voltage regulation range. However, this method still has a narrow operating range. In [10]–[12], hybrid FB and half-bridge (HB) operation schemes were studied. The configuration of the primary switches can be an FB or HB according to the input voltage range, which enables the *LLC* resonant converter to cover a wide input voltage range over two times while maintaining a narrow switching frequency range and high efficiency. However, these primary-side reconfigurable topologies are not suitable for applications with a wide output voltage range. When the

output voltage increases, the flux and magnetizing current of the transformer also increase regardless of the primary-side configuration, which results in large transformer core loss and primary conduction loss.

Reconfiguring a secondary rectifier structure can allow *LLC* resonant converters to achieve higher efficiency with an optimized transformer design for wide output voltage applications. In [13], a variable–inverter–rectifier–transformer was proposed to cover a wide operating voltage range with fractional and reconfigurable effective turns ratio. However, it requires many switches on the secondary side, which may increase the volume and cost of systems. In [14], a semiactive variable structure rectifier was proposed, which operates as a voltage doubler or a voltage quadrupler according to the control strategy of two additional floating MOSFETs of the rectifier. Thus, it can cover a wide output voltage range with a narrow switching frequency range. However, it requires additional MOSFETs and driving circuits. To reduce the number of additional MOSFET, a pulsewidth-modulated (PWM) *LLC* resonant converter was proposed in [15] and [16]. The primary switches are controlled with a fixed switching frequency and duty ratio. Instead, one additional floating MOSFET of the rectifier regulates the output voltage with a PWM control signal. However, the converter presented in [15] and [16] still uses one floating MOSFET requiring a complex driving circuit. Moreover, the PWM control causes not only high conduction losses with triangular current shape, but also high turn-OFF switching loss of the secondary switches and reverse recovery loss of the secondary diodes. In [17], an *LLC* resonant converter with a hybrid voltage multiplier was proposed. This method can change its rectifier structure by changing the control strategy of MOSFETs replacing low-side diodes of an FB rectifier. However, asymmetric operation among transformers causes an asymmetric design of transformers. The secondary capacitor should be sufficiently larger than the primary resonant capacitor, which limits the design flexibility of the converter. Moreover, it has low utilization of components in the rectifier.

This article introduces a high-efficiency *LLC* resonant converter with a reconfigurable voltage multiplying rectifier (RVMR) for wide output voltage applications. The RVMR enables the proposed converter to cover a wide output voltage range with a narrow switching frequency range, which results in high efficiency and high power density. Instead of adopting additional secondary MOSFETs as in previous papers, the proposed RVMR is only composed of diodes, and the phase-shift (PS) control of the primary switches reconfigures the structure of the RVMR with a smooth mode transition. Therefore, the proposed RVMR *LLC* converter can achieve high efficiency and high power density without any additional switch and abrupt mode transition in wide output voltage applications.

This article is an improved version of the conference publication [1]. In this article, a smooth mode transition control is proposed and verified with experimental results. The overall contents have been improved. Especially, design consideration, control strategy, more experimental results, and analysis of the mismatch of resonant tank parameters are newly added.

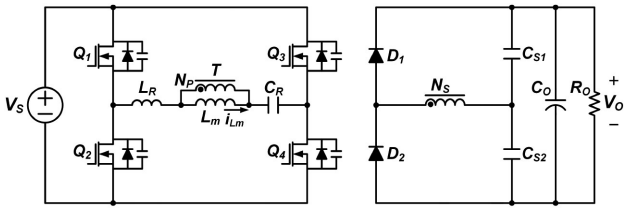


Fig. 1. Circuit diagram of conventional FB *LLC* resonant converter with a VDR.

II. Description of the Proposed RVMR *LLC* Converter

A. Key Concept

In the *LLC* resonant converter, peak flux density (B_{peak}) and peak magnetizing inductor current ($i_{Lm-\text{peak}}$) of a transformer (T) have a relationship with the output voltage (V_O) and minimum switching frequency ($f_{S-\text{Min}}$) as follows:

$$B_{\text{peak}} \propto i_{Lm-\text{peak}} \propto \frac{V_O}{f_{S-\text{Min}}}. \tag{1}$$

Fig. 1 shows the conventional FB *LLC* resonant converter circuit diagram with a voltage-doubler rectifier (VDR). Provided that it is designed in the below-resonant region under the constant input voltage and wide output voltage conditions, B_{peak} and $i_{Lm-\text{peak}}$ of the conventional FB *LLC* converter are minimum at the lowest output voltage condition, and they continue to increase as the output voltage increases. Moreover, since the switching frequency becomes lower and lower from the resonant frequency (f_R) to regulate higher output voltage, B_{peak} and $i_{Lm-\text{peak}}$ of the conventional FB *LLC* converter significantly increase under higher output voltage conditions. Therefore, the conventional FB *LLC* converter has lower efficiency as the output voltage increases due to large conduction loss, transformer core loss, and turn-OFF switching loss. A primary reconfiguration scheme in [11] can be applied to the conventional FB *LLC* converter to reduce the switching frequency variation range, i.e., higher $f_{S-\text{Min}}$. However, this scheme still has large B_{peak} and $i_{Lm-\text{peak}}$ because of the wide output voltage range, which limits the conversion efficiency and power density.

Fig. 2 shows the concept of the proposed converter with a RVMR. An HB *LLC* resonant converter with a single-ended VDR, shown in Fig. 2(a), is a block of the proposed RVMR *LLC* converter. In a low output voltage range where the RVMR operates as a VDR, the proposed RVMR *LLC* converter connects two blocks in parallel, as illustrated in Fig. 2(b). Thus, each block has half of the total input and output current, which results in small conduction loss. In a high output voltage range where the RVRM operates as a voltage-quadrupler rectifier (VQR), the proposed converter reconfigures two blocks with input in parallel and output in series, as illustrated in Fig. 2(c), which makes each block only cover half of the high output voltage. With a reconfigurable structure, the proposed RVMR *LLC* converter is able to reduce the output voltage range of each block as well as the switching frequency variation. As a result, the proposed RVMR *LLC* converter can have much smaller B_{peak} and $i_{Lm-\text{peak}}$ than the conventional converter, which results in higher efficiency and higher power density in wide output voltage applications.

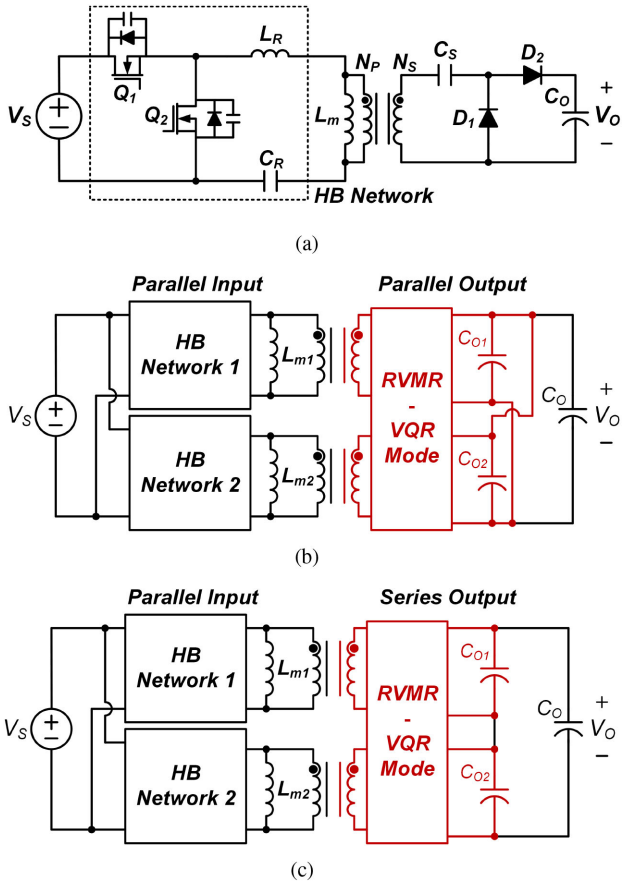


Fig. 2. Concept of the proposed RVMR *LLC* resonant converter. (a) HB *LLC* resonant converter with a single-ended VDR. (b) VDR mode in the low output voltage range. (c) VQR mode in the high output voltage range. In the proposed RVMR *LLC* converter, two HB networks are connected in parallel, and outputs are connected in series or in parallel to cover wide output voltage range.

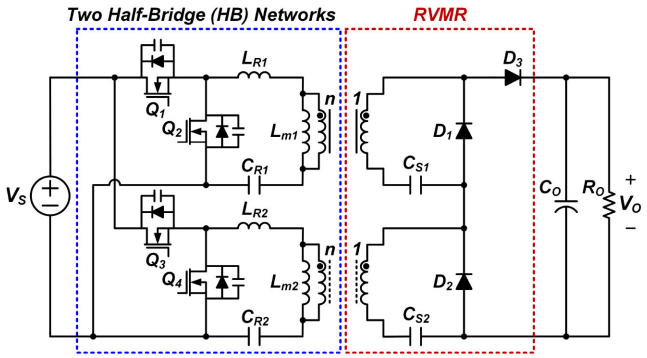


Fig. 3. Circuit diagram of the proposed RVMR *LLC* converter. The proposed RVMR consists of two blocking capacitors and three diodes.

B. Topology Description

Fig. 3 shows the circuit diagram of the proposed RVMR *LLC* resonant converter. In the primary side, two HB networks with the same resonant tank are connected in parallel. The primary MOSFETs (Q_1–Q_4) are driven with a fixed 50% duty ratio like conventional *LLC* resonant converters. The RVMR is on the secondary side. The RVMR is implemented with two blocking capacitors (C_{S1} and C_{S2}) and three diodes (D_1, D_2, and D_3). Note that the proposed RVMR does not require additional MOSFET, unlike previous studies [12]–[17]. Rather, it eliminates one diode compared to two single-ended VDRs, which may reduce conduction loss, cost, and volume of the proposed converter. By changing the modulation strategy of the primary MOSFETs, the RVMR can reconfigure its topology to a VDR or a VQR according to the output voltage condition. Detailed operation and analysis will be explained in the following sections.

III. Operational Principles

The proposed RVMR *LLC* converter uses general pulse frequency modulation (PFM) control to regulate the output voltage like conventional *LLC* converters in normal operation [19], [20]. During the mode transition, it additionally adopts a PS control to achieve smooth mode change. In normal mode, operational principles of the proposed converter are similar to those of the conventional one except for the RVMR operation. Thus, this section focuses on the operations of the RVMR: 1) VDR mode for low output voltage range and 2) VQR mode for high output voltage range. Several assumptions are made to simplify the analysis: 1) V_{CS1}, V_{CS2}, V_O, and I_O are constant; 2) dead times between primary gate signals are negligibly short; 3) all parasitic components are ignored except for those specified in Fig. 3; and 4) all components of two resonant tanks and secondary capacitors are matched ($L_{R1} = L_{R2}$, $C_{R1} = C_{R2}$, $L_{M1} = L_{M2}$, and $C_{S1} = C_{S2}$).

A. VDR Mode

In low output voltage range, two primary HB networks are controlled by 180° phase-shifted gate signals, as shown in Fig. 4(a), to make the RVMR operate as two VDRs connected in parallel. There are two simplified operation states in one switching period. Fig. 4(b) and (c) shows topological states of the proposed converter for two operation states.

Mode 1 [t_a–t_b, Fig. 4(b)]: At time t_a, Q_2 and Q_3 are turned ON. In this mode, the input power is transferred by the resonance between L_{R2} and C_{R2} to V_O through C_{S2}, D_1, and D_3. The other resonant operation of L_{R1} and C_{R1} charges C_{S1}. The voltage across the secondary winding of the transformers (v_{LM1s} and v_{LMs2}) can be expressed as follows:

$$v_{LM1s} = -V_{CS1} \tag{2}$$

$$v_{LM2s} = V_O - V_{CS2}. \tag{3}$$

Mode 2 [t_b–t_c, Fig. 4(c)]: At time t_b, the role of two resonant tanks is switched. C_{S2} is charged, and the energy stored in C_{S1} is delivered to V_O with the transferred energy through the resonance between L_{R1} and C_{R1}. v_{LM1s} and v_{LMs2} are

$$v_{LM1s} = V_O - V_{CS1} \tag{4}$$

$$v_{LM2s} = -V_{CS2}. \tag{5}$$

B. VQR Mode

By controlling two primary HB networks with the same gate signals (0° phase-shifted), as shown in Fig. 5(a), the RVMR operates as a VQR in high output voltage range. There are also

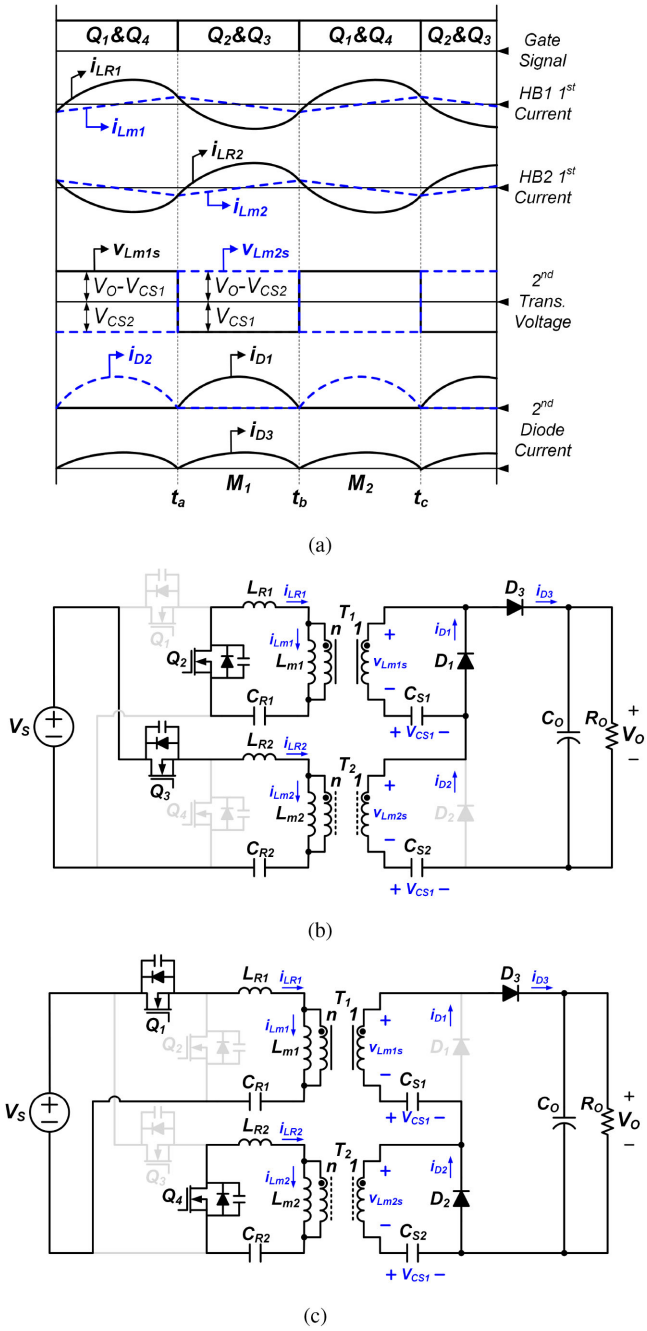


Fig. 4. Proposed RVMR *LLC* converter in low output voltage range. (a) Operational waveforms. (b) Topological state 1 (Mode 1). (c) Topological state 2 (Mode 2). Two secondary blocking capacitors (C_{S1} and C_{S2}) are connected in parallel.

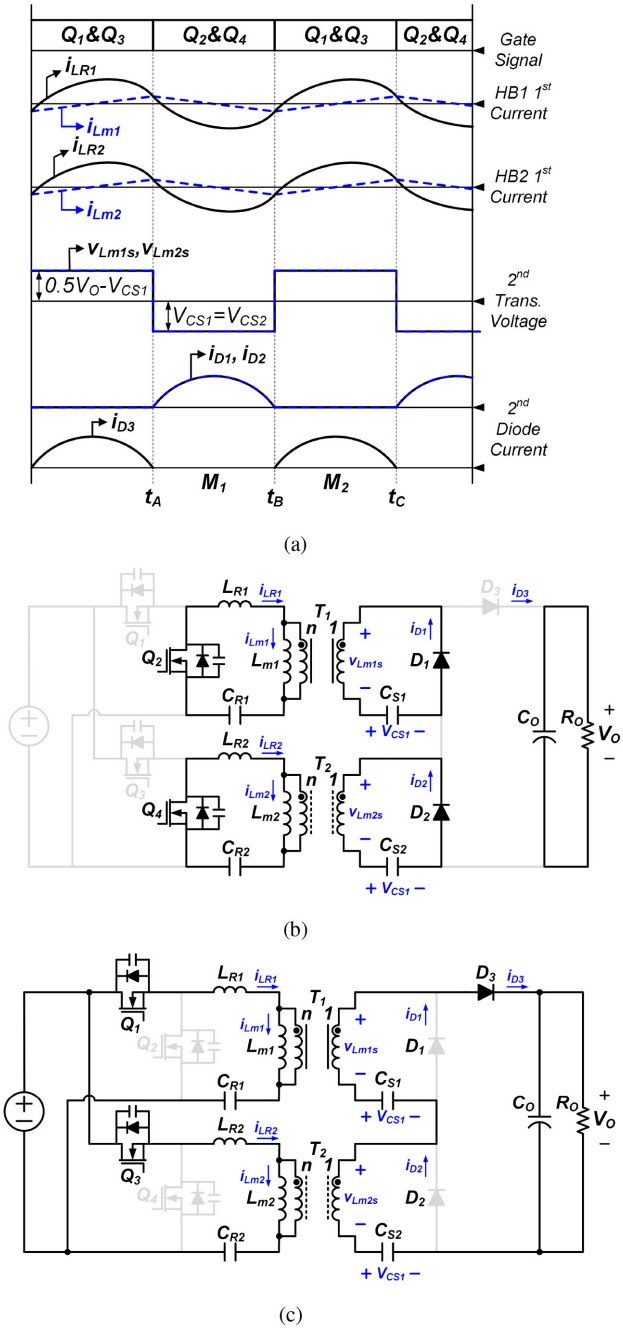


Fig. 5. Proposed RVMR *LLC* converter in high output voltage range. (a) Operational waveforms. (b) Topological state 1 (Mode 1). (c) Topological state 2 (Mode 2). C_{S1} and C_{S2} are connected in series.

two simplified operation states in one switching period. Fig. 5(b) and (c) shows the topological states of the proposed converter.

Mode 1 [t_A–t_B, Fig. 5(b)]: At time t_A, Q_2 and Q_4 are turned ON. Unlike VDR mode, each resonant tank charges C_{S1} and C_{S2}, respectively. Diode D_3 blocks the reverse current from the output capacitor. Thus, the voltage stress of D_3 is V_O. v_{LM1s} and v_{LMs2} can be expressed as follows:

$$v_{LM1s} = -V_{CS1} \tag{6}$$

$$v_{LM2s} = -V_{CS2}. \tag{7}$$

Mode 2 [t_B–t_C, Fig. 5(c)]: At time t_B, Q_1 and Q_3 are turned ON. During this mode, the energy stored in C_{S1} and C_{S2} is delivered to V_O with the energy transferred from the primary side. v_{LM1s} and v_{LMs2} are

$$v_{LM1s} = 0.5V_O - V_{CS1} \tag{8}$$

$$v_{LM2s} = 0.5V_O - V_{CS2}. \tag{9}$$

From Fig. 5(c), since D_1 and D_2 are connected in series, the voltage stress of D_1 and D_2 are $0.5V_O$, which is half of the voltage stress of the conventional *LLC* converter with the VDR.

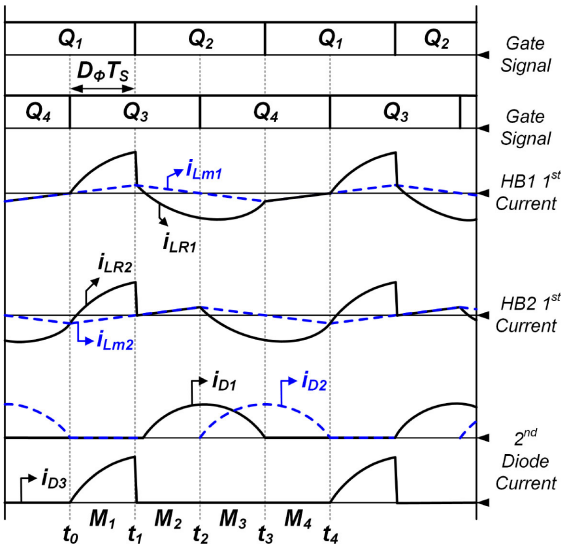


Fig. 6. Operational waveforms of the proposed RVMR *LLC* converter during mode transition ($D_\phi = 0.25$).

C. Mode Transient Operation

As mentioned above, the structure of the proposed RVMR is determined by the PS value (D_ϕ) between gate signals of two HB networks. In the VDR mode, two HB networks are controlled with 180° phase-shifted signals ($D_\phi = 0$), whereas they do in-phase signal ($D_\phi = 0.5$) in the VQR mode. When $0 < D_\phi < 0.5$, the proposed RVMR *LLC* converter operates in a hybrid mode, which is a combination of the VDR mode and the VQR mode. Fig. 6 shows operational key waveforms of the proposed converter with $D_\phi = 0.25$. One switching period is simply divided into four modes.

Mode 1 [t_0–t_1]: At time t_0, Q_1 and Q_3 are turned ON. Thus, the RVMR operates like the VQR mode, and two HB networks deliver the input power to V_O together. This operation is similar to Mode 2 of the VQR mode.

Mode 2 [t_1–t_2]: At time t_1, Q_1 is turned OFF, and Q_2 and Q_3 are turned ON. The resonant operation of L_{R1} and C_{R1} charges C_{S1} like the VDR mode. The other resonant tank current (i_{LR2}) circulates in the primary side.

Mode 3 [t_2–t_3]: At time t_2, Q_3 is turned OFF, and Q_2 and Q_4 are turned ON. Thus, two resonant tanks charge each secondary capacitor (C_{S1} and C_{S2}) like Mode 1 of the VQR mode.

Mode 4 [t_3–t_4]: At time t_3, Q_2 is turned OFF, and Q_1 and Q_4 are turned ON. This operation is opposite to Mode 2. The resonant operation of L_{R2} and C_{R2} charges C_{S2} and i_{LR1} circulates in the primary side.

As D_ϕ increases, i.e., duration of Mode 1, the average operation time of the VQR mode increases, and that of the VDR mode decreases, which increases the voltage gain of the proposed converter. Therefore, by adjusting D_ϕ (phase-shifted control), the proposed converter can also regulate the output voltage. However, since the primary and secondary current waveforms are not sinusoidal in this mode, the conduction loss and turn-OFF switching loss can be increased compared to the VDR and VQR modes. Therefore, it is recommended to use the PS control of the proposed converter for the mode transition where the operation time is very short and high efficiency is not required.

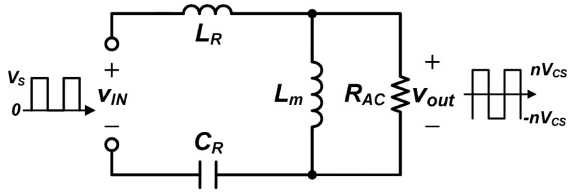


Fig. 7. AC equivalent circuit of an HB *LLC* converter with a VDR. It can be extended to analyze a voltage gain of the proposed RVMR *LLC* converter.

IV. Analysis of the Proposed Converter

A. Voltage Gain

In the proposed converter, each of the two HB networks operates as an independent square wave generator, which means no cross-regulation issue between two networks [16]. Since two rectifiers are connected in parallel (VDR mode) or in series (VQR mode), two operations modes of the proposed RVMR *LLC* converter have only impact on the equivalent output resistance. Consequently, the voltage gain of the proposed RVMR *LLC* converter can be obtained by the same manner of the conventional HB *LLC* resonant converter. Fig. 7 shows the ac equivalent circuit of an HB converter with a VDR, and the conversion ratio of V_S to nV_{CS} ($= M_{LLC}$) can be derived as follows:

$$M_{LLC} = \frac{V_{CS}}{V_S} = \frac{L_m \parallel R_{AC}}{2n[sL_R + \frac{1}{sC_R} + (L_m \parallel R_{AC})]} = \frac{k}{2n\sqrt{(1+k-f_N^{-2})^2 + k^2Q^2(f_N - f_N^{-1})^2}} \quad (10)$$

where $k = L_m/L_R$, $Q = (L_R/C_R)^{0.5}/R_{\text{AC}}$, and $f_N = f_S/f_R$.

From (10), the voltage gain of the proposed RVMR *LLC* converter ($=V_O/V_S$) can be obtained by substituting V_{CS} with terms of V_O, which can be derived by the volt–second balance of the transformer. In the VDR mode, from (2)–(5), V_{CS1} and V_{CS2} are equal to $0.5V_O$. From (6)–(9), V_{CS1} and V_{CS2} are $0.25V_O$ in the VQR mode. Therefore, the voltage gain of the proposed converter can be derived as follows:

$$M_{\text{Pro}} = \frac{V_O}{V_S} = \begin{bmatrix} 2M_{LLC}, \text{ VDR mode} \\ 4M_{LLC}, \text{ VQR mode} \end{bmatrix} \quad (11)$$

where R_{AC} is $4n^2R_O/\pi^2$ and n^2R_O/π^2 at the VDR mode and VQR mode, respectively, and R_O is the output resistance.

Fig. 8 shows the voltage gain of the proposed RVMR *LLC* converter and conventional FB *LLC* converter with a VDR. The conventional converter should have a wide switching frequency variation range to regulate a wide output voltage range (100–300 V in this article). The proposed converter has two voltage gain curves according to the configuration of the RVMR, which enables the proposed converter to operate in a much narrower switching frequency range. To obtain continuous output voltage regulation, the maximum voltage gain of the VDR mode should be higher than the minimum voltage gain of the VQR mode.

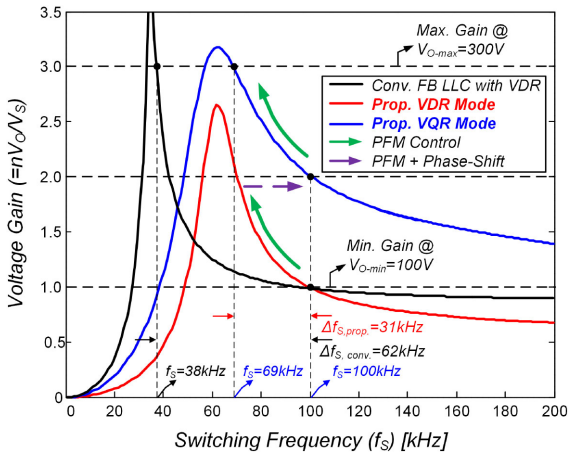


Fig. 8. Voltage gain of the proposed RVMR *LLC* converter and conventional FB *LLC* converter with a VDR. The proposed one can be designed with two times narrower switching frequency variation than the conventional one.

TABLE I
DESIGN SPECIFICATIONS OF THE PROTOTYPE

Items	Parameters
Input voltage, V_S	400 V
Output voltage, V_O	100-300 V
Output current, I_O	2.5 A (Maximum)
Resonant switching frequency, f_R	100 kHz

The proposed converter can be designed considering similar switching frequency variation (Δf_S) for two operation modes.

B. Design Considerations

To illustrate the design procedure of the proposed RVMR *LLC* converter, a 750-W LED driver specification for industrial lighting shown in Table I is used in this part. The proposed converter operates like the conventional *LLC* resonant converters in each configuration (VDR and VQR modes). For this reason, the design of the proposed converter can follow the design procedure of the conventional *LLC* converters.

The conventional FB *LLC* resonant converter with a VDR (see Fig. 1) should be designed with a considerably wide switching frequency range to regulate the wide output voltage range, as shown in Fig. 8, which results in low efficiency and large size of energy storage components. On the other hand, the proposed RVMR enables the *LLC* resonant converter to be designed in a narrower output voltage range; VDR and VQR modes of the proposed RVMR *LLC* converter can be designed to cover 100–200 and 200–300 V, respectively. Therefore, the proposed converter can have a much narrower switching frequency range leading to high efficiency and smaller energy storage components. In the proposed converter, two HB networks are designed to have the same parameters. Thus, only one HB network is designed in this part.

1) Parameters of Resonant Tank: From (10) and (11), the transformer turns ratio (n_{Pro}) is designed as 4 to make the proposed RVMR *LLC* converter operate at the resonant frequency (f_R) when V_O is 100 V. The magnetizing inductance (L_m) of the transformer should be designed as large as possible because a larger L_m can more reduce the primary conduction loss and switch turn-OFF loss [6]. However, a larger L_m generally causes lower voltage gain and worse ZVS condition of the *LLC* resonant converter. In the proposed converter, since the RVMR reduces the output voltage range of each mode, L_m can be determined only by considering the ZVS condition as follows:

$$L_m \le \frac{n_{\text{Pro}} V_{CS} t_{\text{dead}}}{8 C_O(tr) V_S f_R} \tag{12}$$

where t_{dead} is the dead time between the primary switches, $C_O(tr)$ is the time-related effective output capacitance of the MOSFET, and V_S is the input voltage.

Provided that t_{dead} is 100 ns, $C_O(tr)$ is 136 pF, V_S is 400 V, and f_R is 100 kHz, maximum L_m is obtained as 460 μH at V_{CS} = 50 V. With some design margin, L_m of the proposed RVMR *LLC* converter can be chosen as 400 μH. Once L_m is designed, resonant inductance and resonant capacitance can be determined by considering the switching frequency range of the proposed converter. Since C_R is $1/[(2\pi f_R)^2 L_R]$ and $k = L_m/L_R$, the switching frequency range of the proposed converter can be designed according to k from (10). k can be designed as 3.5 to make the proposed converter have a similar switching frequency range in VDR and VQR modes, as shown in Fig. 8. Thus, L_R and C_R are 114 μH and 22 nF, respectively, in this design example.

The resonant tank parameters of the proposed RVMR and conventional FB *LLC* converters can also be designed to regulate the output voltage over 100 V at the resonant frequency, considering the above resonant operation. This design can increase the minimum switching frequency and improve the efficiency at higher output voltage conditions. However, due to low Q, two converters have flattened voltage gain slope at the above resonance region, which results in much higher maximum switching frequency and light-load regulation problems. Therefore, it is better to design two converters to operate at resonance and below regions in this example.

2) Transformer Core: In general, a transformer core can be designed by using the area product value (A_P), which is the product of the effective cross-sectional area (A_C) and window area (A_W) of a core. A_P of the proposed RVMR *LLC* converter can be expressed as follows:

$$A_P = A_C \times A_W = \frac{nV_{CS}}{4B_{\max} f_{S-\min}} \times \frac{i_{LR-\text{rms}} + \frac{i_{\text{sec}-\text{rms}}}{n}}{K_U J} \tag{13}$$

where n is the transformer turns ratio, $B_{\max}$ is the maximum flux density of the transformer, $i_{LR-\text{rms}}$ is the rms current of L_R, $i_{\text{sec}-\text{rms}}$ is the secondary rms current of the transformer, K_U is the window utility factor, and J is the current density.

Among output voltage conditions, since n, $B_{\max}$, K_U, and J are constant, A_P is proportional to V_{CS}, $i_{LR-\text{rms}}$, $i_{CS-\text{rms}}$, and switching period ($=1/f_S$). Thus, the worst condition in designing the transformer is V_O = 300 V, where the transformer delivers maximum power. Table II shows the parameters related to A_P for the conventional and proposed converters at V_O = 300 V. In the conventional FB *LLC* converter with a VDR, V_{CS} = 150 V, n = 8, and $f_{S-\min}$ = 38 kHz at V_O = 300. On the

TABLE II
REQUIRED TRANSFORMER A_P OF TWO CONVERTERS AT $V_O = 300$ V

Items	Conv. FB *LLC* Converter	Proposed Converter
n	8	4
V_{CS}	150 V	75 V
f_{S-min}	38 kHz	69 kHz
i_{LR-rms}	4.6 A	2.3 A
$i_{sec-rms}$	9.2 A	6.8 A
B_{max}	0.13 T	
K_U	0.3	
J	8.5 A/mm^2	
$RequiredA_P$	136,937 mm^2 × 1EA	13,116 mm^2 × 2EA

TABLE III
MAXIMUM VOLTAGE STRESS OF SECONDARY COMPONENTS

Items	Conv. FB *LLC* Converter	Proposed Converter
D_{S1} & D_{S2}	V_O	$0.5V_O$
D_{S3}	-	V_O
C_{S1} & C_{S2}	$0.5V_O$	$0.25V_O$

other hand, with the proposed RVMR, $V_{CS} = 75$ V, $n = 4$, and $f_{S-\min} = 69$ kHz in the proposed converter. Moreover, since two HB networks of the proposed converter share the output current and operate at a higher switching frequency, the proposed converter can have much lower primary and secondary rms currents than the conventional converter. Thus, when two converters are designed to achieve the same $B_{\max}$ and J, the required A_P of the two transformers in the proposed converter is 5.22 times smaller than that of one transformer in the conventional FB *LLC* converter. Therefore, under the same $B_{\max}$ and J design conditions, the proposed converter can be designed with around five times smaller transformer size, which also reduces wire resistance and core loss. In the experiment, the conventional FB *LLC* converter is designed with $B_{\max} = 0.385$ T to reduce the transformer size despite increased core loss. Thus, two PQ3230 cores with $A_P = 24086$ mm^4 (required $A_P = 46239$ mm^4) are used for the conventional converter. In the proposed converter, each of the two transformers is designed with a PQ3220 core with $A_P = 13\,736$ mm^4.

3) Secondary Diode: Three secondary diodes of the proposed RVMR *LLC* converter can be chosen considering the VQR mode operation because the voltage stress of them is maximum at the highest output voltage condition. The maximum voltage stress of the secondary diodes is shown in Table III. Due to an additional diode (D_{S3}), the proposed converter has additional conduction loss. However, since the other two diodes (D_{S1} and D_{S2}) have half of the voltage stress of diodes of the conventional FB *LLC* converter, the proposed converter can relieve the increased conduction loss of an additional diode.

4) Secondary Capacitor: The secondary blocking capacitors (C_{S1} and C_{S2}) can be designed considering rms current stress and voltage stress. In the VDR mode of the proposed RVMR *LLC* converter, C_{S1} and C_{S2} are connected in parallel to share the output current, and the output voltage is low, which results in low voltage stress and low rms current stress on C_{S1} and C_{S2}. In the VQR mode, due to the series connection of C_{S1} and C_{S2}, the proposed converter may result in higher current stress on C_{S1}

TABLE IV
MAXIMUM RMS CURRENT OF SECONDARY CAPACITORS

Items	Conv. FB *LLC* Converter	Proposed Converter
C_{S1} & C_{S2}	$\pi I_O\sqrt{\frac{f_R}{4f_{S-min}} - \frac{1}{\pi^2}}$	$\pi I_O\sqrt{\frac{f_R}{2f_{S-min}}}$

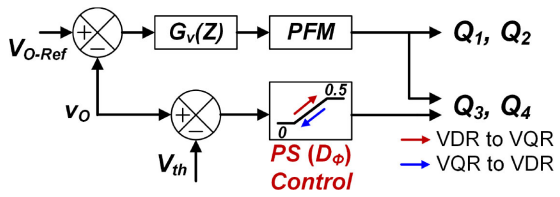


Fig. 9. Control block diagram of the proposed RVMR *LLC* converter.

and C_{S2}. As shown in Table IV, due to the series connection of C_{S1} and C_{S2}, the proposed converter has about 1.5 times higher rms current than the conventional converter. However, since the proposed converter has a much higher minimum operating switching frequency ($f_{S-\min}$), it can have similar rms current stress to the conventional converter.

The volume of a family of capacitor components (Vol_C) can be represented by [21]

$$\mathrm{Vol}_C = k_C \times C \times V_C^2 \tag{14}$$

where k_C describes the proportionality of the capacitor volume and the stored energy, C is the capacitance, and V_C is the voltage of the capacitor.

Since k_C and C are the same in both the conventional and proposed converters, the maximum V_C determines the volume of the secondary capacitor. As shown in Table III, C_{S1} and C_{S2} of the proposed converter have half of the voltage stress of the conventional converter, which results in four times smaller size of the secondary capacitors. Therefore, the proposed converter can reduce the size of the secondary capacitor compared to the conventional FB *LLC* converter with a VDR. Besides, with the same principle, the total size of two primary resonant capacitors of the proposed converter (C_{R1} and C_{R2}) is also smaller than a resonant capacitor of the conventional converter.

C. Control Strategy

The proposed RVMR *LLC* converter basically uses a PFM control to regulate the output voltage under the VDR and VQR modes, which enables the proposed converter to use the state-of-the art control scheme for the *LLC* resonant converter [22]–[24]. During mode transitions between VDR and VQR modes, the proposed converter additionally adopts a PS control with the PFM control to achieve a smooth mode transient operation. Fig. 9 shows the control block diagram of the proposed converter, composed of a PFM closed loop and a PS open loop. When the output voltage is under V_{th}, the proposed converter regulates the output voltage with the PFM closed-loop control and 180° phase-shifted gate signals ($D_\phi = 0$). When the output voltage reaches V_{th}, D_ϕ gradually increases to 0.5 achieving higher voltage gain, and the PFM control regulates the output voltage increasing the switching frequency. This mode ends at $D_\phi = 0.5$. When V_O

TABLE V
DESIGNED PARAMETERS OF TWO PROTOTYPES

Parameters	Conventional FB *LLC*	Proposed RVMR *LLC*
Primary switch, Q_1-Q_4	IPAW60R380CE	
Transformer core, T (Material: PL-13)	PQ3230*2EA	T_1: PQ3220 T_2: PQ3220
Magnetizing inductance	L_m: 800 μH	L_{m1}: 400 μH L_{m2}: 400 μH
Transformer turns-ratio, n	8	4
Resonant inductor core	RM10	L_{R1}: RM8 L_{R2}: RM8
Resonant inductance	105.3 μH	L_{R1}:104.8 μH L_{R2}:104.9 μH
Resonant capacitor, C_R	22 nF (V_R: 1000 V_{AC})	22 nF (V_R: 500 V_{AC})
Secondary capacitor, C_{S1}, C_{S2}	6.6 μF (V_R: 250 V_{DC})	6.6 μF (V_R: 100 V_{DC})
Secondary diode, D_{S1}, D_{S2}	STTH30R04	STPS20200C
Secondary diode, D_{S3}	-	STTH30R04

is over V_{th}, the proposed converter is controlled by the PFM control and in-phase gate signals ($D_\phi = 0.5$). Therefore, the mode transition can be implemented easily.

D. Impact of Mismatch of Two Resonant Tanks

In a practical case, two resonant tanks of the proposed RVMR converter are difficult to be identical. The proposed RVMR converter has an automatic balancing mechanism in VQR mode under the mismatch of two resonant tanks, but it can undergo an unbalanced power sharing problem in VDR mode like two parallel-connected *LLC* converters. However, unlike general parallel-connected *LLC* converters, since the VDR mode covers less than half power of the rated maximum power, even though one HB network covers only output power in the VDR mode, the HB network has less power stress than the stress at the VQR mode. Thus, unbalanced power sharing of the VDR mode cannot have impact on the design and reliability of the proposed converter. Moreover, the proposed converter can adjust the dead time of the primary switches to match the voltage gain of two HB networks as well as adopt a magnetic-coupling current-balancing cell to solve the unbalance problem.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed RVMR *LLC* resonant converter, a 750-W prototype for industrial lighting driver with specifications shown in Table I was built and tested. For the comparison, we also implemented a conventional FB *LLC* resonant converter with a VDR. The designed parameters are presented in Table V. The proposed converter is able to use low voltage rating (200 V) diodes for D_{S1} and D_{S2}, whereas it requires an additional diode for D_{S3} with a 400-V rating.

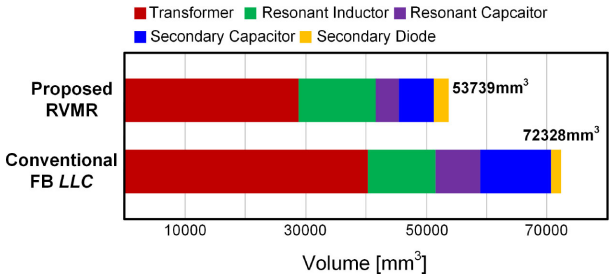
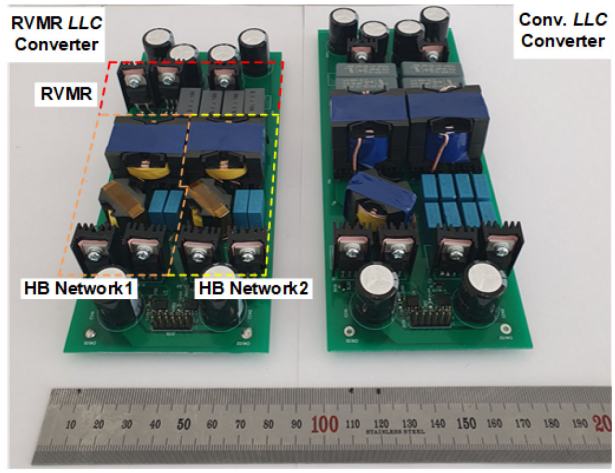
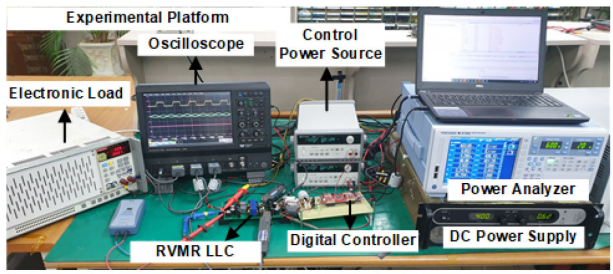


Fig. 10. Volume comparison between two prototypes.



(a)



(b)

Fig. 11. Photographs of (a) two prototypes: above—RVMR *LLC* converter and below—conventional FB *LLC* converter and (b) experimental platform.

Two low-voltage-rating diodes can relieve additional power loss of D_{S3}. Fig. 10 shows the volume comparison between the two prototypes. As discussed in Section IV-B, the proposed RVMR *LLC* converter has a lower volume than the conventional converter due to smaller transformers, resonant capacitor, and secondary capacitor. Fig. 11 shows photographs of the prototype and experimental platform. The proposed converter has a total box volume of 9.69 in^3 and 750-W maximum power leading to 77.4-W/in^3 power density including heat sink, whereas the conventional converter has 17.26-in^3 box volume and 43.4-W/in^3 power density due to the high height of the transformer.

Fig. 12 shows the captured waveforms of the two prototypes under different output voltage and full-load conditions. The RVMR enabled the proposed converter to have a narrower switching frequency range in 100–300-V output voltage range because of its reconfigurable structure: 1) VDR mode and 2)

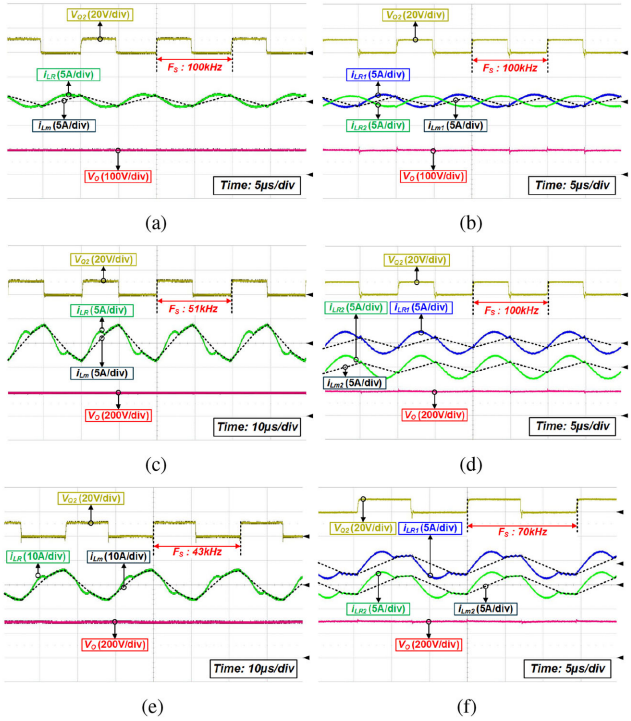


Fig. 12. Measured waveforms of conventional and proposed converters. (a) Conventional at $V_O = 100$ V. (b) Proposed at $V_O = 100$ V. (c) Conventional at $V_O = 200$ V. (d) Proposed at $V_O = 200$ V. (e) Conventional at $V_O = 300$ V. (f) Proposed at $V_O = 300$ V. i_{Lm} is an expected magnetizing current.

VQR mode. Therefore, the proposed RVMR *LLC* converter has a smaller primary current (i_{LR}) and magnetizing current (i_{Lm}) than the conventional FB *LLC* resonant converter, resulting in lower conduction loss, switching loss, and core loss. Fig. 13 shows the captured waveforms during the mode transition of the proposed RVMR *LLC* converter. The output voltage is well regulated during the mode transition with the mixed control of the PFM and PS. The proposed converter operates well with the phase-shifted signal, as illustrated in Fig. 13(b).

Fig. 14 shows the measured efficiency of the two prototypes. The efficiency was measured with a Yokogawa WT 1800. At full-load condition, the conventional FB *LLC* converter achieves its highest efficiency at 100 V (= 250 W), where it operates near its resonant frequency. However, it has considerably lower efficiency as the output voltage increases because its switching frequency is further away from the resonant frequency. The proposed RVMR *LLC* converter has a slightly lower efficiency than the conventional converter at 100 V due to its additional diode conduction loss. However, benefiting from the RVMR and narrow switching frequency range design, the proposed converter achieves higher efficiency than the conventional converter as the output voltage increases. As illustrated in Fig. 15, it achieves 97.82% peak efficiency by reducing the switch loss and transformer loss. Note that the VDR mode of the proposed converter has a lower efficiency than the VQR mode at 160 V, which means 160 V is preferred for the threshold voltage (V_{th}) of the mode change. From Fig. 14(b), the proposed converter achieves much higher efficiency as the output current decreases.

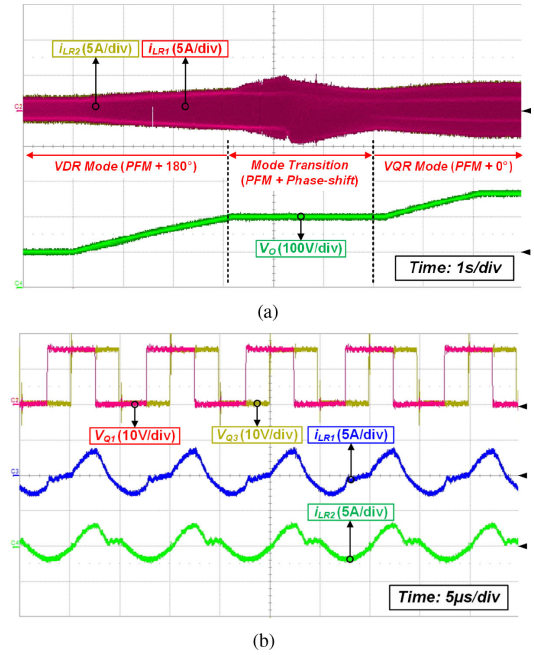


Fig. 13. Measured waveforms of the proposed RVMR *LLC* converter during the mode transition. (a) VDR-to-VQR mode transition. (b) 90° phase-shifted operation.

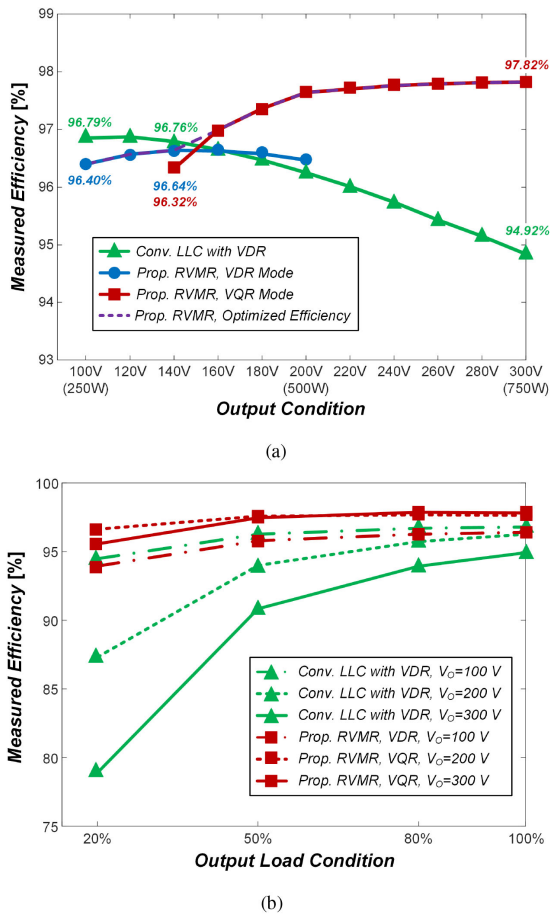


Fig. 14. Measured efficiency. (a) Different output voltage at full-load condition. (b) Different output current conditions.

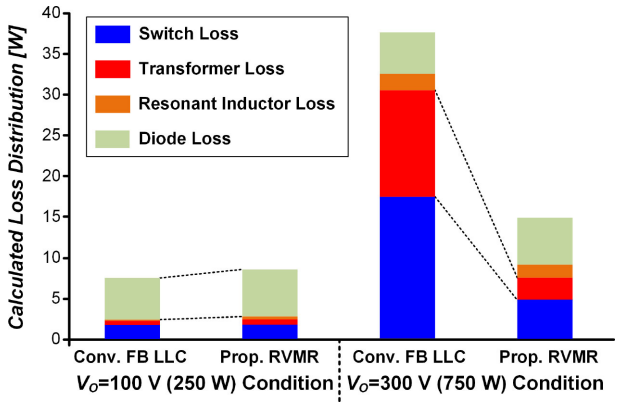


Fig. 15. Loss analysis of conventional and proposed prototypes at 250- and 750-W conditions.

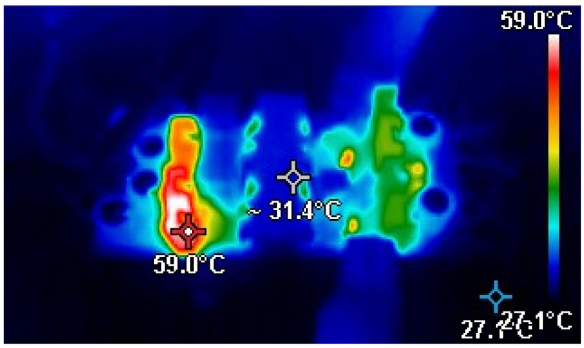


Fig. 16. Thermal image of the proposed converter at 750-W condition with 0 LFM and 23 °C air flow.

TABLE VI
COMPARISON WITH STATE-OF-THE-ART *LLC* TOPOLOGIES

Topologies	[14]	[16]	[17]	This work
Primary MOSFETs	4	4	4	4
Secondary diodes	2	6	4	3
Secondary switch	2	2	2	-
Resonant inductor	1	2	1	2
Transformer	1	2	2	2
Input [V]	400	390	400	400
Output [V]	100-500	250-450	150-450	100-300
Rated Power [W]	1500	1350	3300	750
Frequency [kHz]	70-150	100	150-250	69-129
Efficiency [%] (Max. I_{OUT})	93-95.3	96.7-97.3	96.3-96.9	96.4-97.8

This is because the proposed converter has a much lower magnetizing current resulting in lower primary conduction loss and turn-OFF switching loss. Fig. 16 shows a thermal image of the proposed RVMR converter at full power conditions without a fan. It shows that transformers have low temperature due to low loss with the narrow switching frequency range.

Table VI shows the qualitative comparison between the proposed converter and some recently reported *LLC* topologies. Compared to other topologies, the proposed converter does not require additional secondary switches, which simplifies the control scheme and achieve high efficiency.

VI. CONCLUSION

This article presents an RVMR to achieve high-efficiency *LLC* resonant converter for wide output voltage applications. By changing the primary switching strategy, the RVMR can be a VDR mode or VQR mode. This enables the resonant tank of the *LLC* converter to be optimized for narrow switching frequency range and achieve higher efficiency over the entire output voltage range. During the mode transition, the proposed converter uses PFM control and PS control to smoothly regulate the output voltage without any additional switch. The effectiveness of the proposed RVMR *LLC* converter has been verified with a 750-W prototype. The proposed converter can keep its high efficiency over the entire output voltage range and achieve 2.9% higher efficiency than the conventional converter at the full-load condition with reduced core loss and magnetizing current while having 26% reduced component volume. As a result, the proposed RVMR *LLC* converter can be used for wide output voltage applications such as LED drivers, battery chargers, and so on to achieve high efficiency and high power density. Especially, the proposed RVMR *LLC* converter is more suitable for the applications, where core loss and magnetizing current are important power loss factors: 1) all load conditions of high-output-voltage and low-output-current applications, and 2) light-load condition of low-output-voltage and high-output-current applications.

REFERENCES

[1] J. I. Baek, C. E. Kim, K. W. Kim, M. S. Lee, and G. W. Moon, "Dual half-bridge LLC resonant converter with hybrid-secondary-rectifier (HSR) for wide-output-voltage applications," in *Proc. IEEE Int. Power Electron. Conf.*, 2018, pp. 108–113.
[2] Efficiency Standards of European Union (EU). Apr. 2020. [Online]. Available: http://e3p.jrc.ec.europa.eu/
[3] Efficiency Standards of USA. Feb. 2016. [Online]. Available: http://energy.gov/
[4] 80 Plus Incentive Program. Feb. 2012. [Online]. Available: http://www.80plus.org/
[5] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power-applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
[6] J. I. Baek, J. K. Kim, J. B. Lee, H. S. Youn, and G. W. Moon, "A boost PFC stage utilized as half-bridge converter for high-efficiency DC-DC stage in power supply unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7449–7457, Oct. 2017.
[7] Z. Fang, T. Cai, S. Duan, and C. Chen, "Optimal design methodology for LLC resonant converter in battery charging applications based on time-weighted average efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5469–5483, Oct. 2015.
[8] C. Buccella, C. Cecati, H. Latafat, P. Pepe, and K. Razi, "Observer-based control of LLC DC/DC resonant converter using extended describing functions," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5881–5891, Oct. 2015.
[9] J. B. Lee, J. K. Kim, J. I. Baek, J. H. Kim, and G. W. Moon, "Resonant capacitor on/off control of half-bridge LLC converter for high-efficiency server power supply" *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5410–5415, Sep. 2016.
[10] H. Hu, X. Fang, F. Chen, J. Shen, and I. Batarseh, "A modified high-efficiency LLC converter with two transformers for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1946–1960, Apr. 2013.
[11] M. M. Jovanovic and B. T. Irving, "On-the-fly topology-morphing control-efficiency optimization method for LLC resonant converters operating in wide input- and/or output-voltage range," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2596–2608, Mar. 2016.
[12] W. Sun, Y. Xing, H. Wu, and J. Ding, "Modified high-efficiency LLC converters with two split resonant branches for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7867–7879, Sep. 2018.

[13] M. K. Ranjram, I. Moon, and D. J. Perreault, "Variable-inverter-rectifier-transformer: A hybrid electronic and magnetic structure enabling adjustable high step-down conversion ratios," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6509–6525, Aug. 2018.
[14] H. Wu, Y. Li, and Y. Xing, "LLC resonant converter with semiactive variable-structure rectifier (SA-VSR) for wide output voltage range application," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3389–3394, May 2016.
[15] H. Wang and Z. Li, "A PWM LLC type resonant converter adapted to wide output range in PEV charging applications," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3791–3801, May 2018.
[16] Z. Li and H. Wang, "An interleaved secondary-side modulated LLC resonant converter for wide output range application," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1124–1135, Feb. 2020.
[17] X. Tang, Y. Xing, H. Wu, and J. Zhao, "An improved LLC resonant converter with reconfigurable hybrid voltage multiplier and PWM-Plus-PFM hybrid control for wide output range applications," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 185–197, Jan. 2020.
[18] M. I. Shahzad, S. Iqbal, and S. Taib, "A wide output range HB-2LLC resonant converter with hybrid rectifier for PEV battery charging," *IEEE Trans. Transp. Electrific.*, vol. 3, no. 2, pp. 520–531, Jun. 2017.
[19] Y. Gu, L. Hang, Z. Lu, Z. Qian, and D. Xu, "Voltage doubler application in isolated resonant converter," *IEEE Ind. Electron. Soc.*, Raleigh, NC, USA, 2005, pp. 1184–1188.
[20] B. R. Lin, W. R. Yang, J. J. Chen, C. L. Huang, and M. H. Yu, "Interleaved LLC series converter with output voltage doubler," in *Proc. IEEE Int. Power Electron. Conf.*, Sapporo, Japan, 2010, pp. 92–98.
[21] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.
[22] Y. Wang, S. Gao, Y. Guan, J. Huang, D. Xu, and W. Wang, "A single-stage LED driver based on double LLC resonant tanks for automobile headlight with digital control," *IEEE Trans. Transp. Electrific.*, vol. 2, no. 3, pp. 357–368, Sep. 2016.
[23] S. W. Kang and B. H. Cho, "Digitally implemented charge control for LLC resonant converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6159–6168, Aug. 2017.
[24] K. W. Kim, H. S. Youn, J. I. Baek, Y. Jeong, and G. W. Moon, "Analysis on synchronous rectifier control to improve regulation capability of high-frequency LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7252–7259, Aug. 2018.

Jaeil Baek (Member, IEEE) received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015 and 2018, respectively.

Since 2019, he has been a Postdoctoral Research Associate with the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA. His current research interests include point-of-load power converters, grid interface power electronics, digital control approach of converters, and advanced power electronics architecture.

Dr. Baek was the recipient of the Research Outstanding Award from the Korea Advanced Institute of Science and Technology and Global Ph.D. Fellowship and Postdoctoral Fellowship from the National Research Foundation of Korea.

Keon-Woo Kim (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering in 2015 and 2017, respectively, from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, where he is currently working toward the Ph.D. degree.

His main research interests include digital control and low-electromagnetic-interference noise dc–dc converter with high efficiency.

Han-Shin Youn (Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2009, and the M.S. and Ph.D. degrees from the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejoen, South Korea, in 2011 and 2017, respectively.

He was a Senior Researcher with Hyundai Motor Company, Hwaseong, South Korea, from 2017 to 2019. He is currently an Assistant Professor with Incheon National University, Incheon, South Korea. His research interests include high-efficiency ac–dc and dc–dc converters, drive systems, and digital control methods for electric vehicles and renewable energy systems.

Chong-Eun Kim (Member, IEEE) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2001, and the M.S. and Ph.D. degrees in power electronics from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003 and 2008, respectively.

From 2008 to 2015, he was a Senior Engineer with the Power R&D Team, Samsung Electro-Mechanics, Suwon, South Korea, where he developed high-efficiency server power supply. He kept developing server power supply in Power R&D team of SoluM, as a Principal Engineer. Since 2019, he has been an Assistant Professor with the Department of Control and Instrumentation Engineering, Gyeongsang National University, Jinju, South Korea. His research interests include ac–dc and dc–dc converters, including bridgeless power factor correction boost converter, high-frequency LLC resonant converter, and high-efficiency phase-shifted full-bridge converters.