Extended Analysis of the Asymmetrical Half-Bridge Flyback Converter

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***Abstract*—Isolated, zero-voltage-switching dc–dc converter topologies represent attractive solutions in the continuous run toward higher switching frequencies, allowing more compact power supplies. Among them, the asymmetrical half-bridge flyback converter represents an interesting option, featuring simple duty-cycle control at constant switching frequency, as opposed to the popular LLC converter. The majority of papers dealing with this topology consider an approximated voltage gain similar to that of an isolated buck converter operating in continuous conduction mode, i.e., proportional to the duty cycle and, practically, load independent. On the contrary, the true voltage gain is nonmonotonic at high duty-cycle values. Anytime the converter is designed for a resonant operation, as is advisable to eliminate any reverse recovery problem of the rectifier diode, the voltage gain not only increases, but also becomes a function of the switching frequency. This article investigates the converter's voltage gain in detail, deriving a theoretical framework capable of capturing its real behavior and dependencies. The proposed analytical model has been verified through simulations as well as experimental measurements taken on a 160-W prototype working at 400 kHz.**

***Index Terms*—High-frequency dc–dc converter, resonant converter, soft switching.**

I. Introduction

When dealing with high-frequency dc–dc power conversion, guaranteeing zero-voltage switching (ZVS) for all switches in any operating condition is essential to keep the switching losses below an acceptable level. If isolation is also a desired feature, resonant topologies capable of exploiting the unavoidable transformer leakage inductance are certainly the preferred solutions. Among them, the asymmetrical half-bridge flyback converter (AHBFC) is receiving increasing attention, thanks to its ability to control the output voltage through a simple duty-cycle modulation at a constant switching frequency, as opposed to the popular LLC converter. This topology appeared the first time (at least in our knowledge) in [1], where different soft-switching isolated dc–dc converters with the same half-bridge configuration at the primary side and different secondary arrangements have been studied. In 1998, a U.S. patent request was filed and issued the year after [2]. Successively, it appeared in several papers, like in [3]–[7], concentrating on the ZVS condition, as in [8], or exploiting both duty cycle and switching frequency to increase the input voltage range, as in [9] and [10]. The use of synchronous rectification employing a GaN high-electron-mobility transistor device was explored in [11], while a wireless power transfer application was investigated in [12]. High-power-factor rectifier applications are also described in the literature, as in [13]–[15], where a buck-type input rectifier has been integrated with an AHBFC stage, sharing one switch.

An attempt to study the dependence of the voltage gain on the switching frequency using the fundamental harmonic approximation, as usually done with the LLC converter, was proposed in [16]. However, such an approach is questionable, given the half-wave rectification at the output and the asymmetric operation. The impact on the switching intervals of the rectifier parasitic capacitance, which affects the ZVS condition, was studied in [17] for a very high frequency converter implementation.

In all these papers, the voltage gain was derived assuming piecewise linear current waveforms, a condition that is achieved when the series capacitor works as a dc blocking one, i.e., with a negligible voltage ripple. In this case, the voltage gain resembles that of an isolated buck topology operating in continuous conduction mode (CCM) and, as such, appears to be proportional to the duty cycle and almost load and frequency independent. However, even in this condition, at high duty-cycle values, the converter's gain starts to deviate from the linear behavior and becomes nonmonotonic. This phenomenon is enhanced if the converter is designed for a resonant operation, so as to eliminate any reverse recovery problem of the rectifier diode. In [18], the gain nonmonotonicity was indeed discovered, but, unfortunately, the derived expression does not correctly predict the gain behavior at high duty-cycle values.

In this article, based on the work in [19], the voltage gain of the AHBFC is derived assuming a nonnegligible voltage ripple across the resonant capacitor. Accordingly, the main contributions of this article are the following: 1) the derivation of a closed-form formula for the converter voltage gain operating in the CCM, highlighting its nonmonotonicity, as well as its dependence on the switching frequency; and 2) the definition of a numerical calculation procedure for the voltage gain when the converter works in the discontinuous conduction mode (DCM), demonstrating its linearity with the duty cycle and its independence of the load current.

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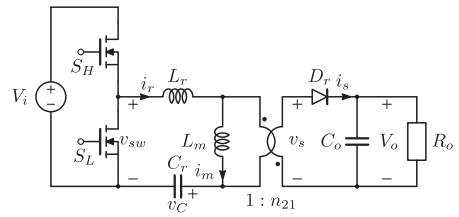

Fig. 1. Schematic of the AHBFC.

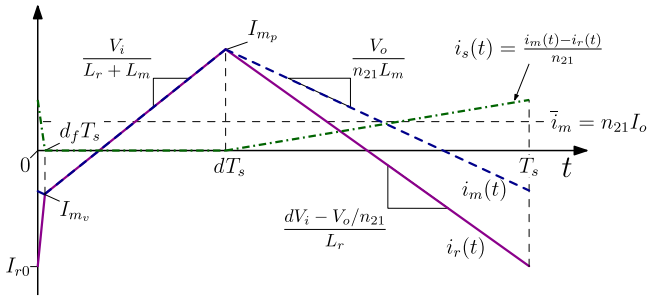

Fig. 2. Inductor currents in the case $v_C(t) \approx V_C = dV_i$.

The rest of this article is organized as follows. In Section II, the converter operation is reviewed, highlighting the differences between the resonant and nonresonant operating modes; the gain analysis is detailed in Section III, starting from the nonresonant case, where the exact expression is found, and moving to the resonant case both in the CCM and the DCM. A proposed design procedure is outlined in Section IV, while the theoretical analysis validation is reported in Section V, using both simulations and experimental data. Section VI illustrates the experimental setup, involving a 160-W prototype working at 400 kHz, and reports the main waveforms in different operating conditions. Finally, Section VII concludes this article.

II. Review of Converter Operation

The AHBFC, shown in Fig. 1, can be seen as a modified LLC converter, where the original full-wave rectifier is substituted by a simple half-wave rectifier. As such, many of the considerations done for the LLC apply to the resonant AHBFC as well. Assuming a steady-state condition, the inductors' *charge* balance and the capacitors' *volt-second* balance yield the following relations (overbar means averaging in a switching period):

$$\begin{cases} \bar{v}_C = \bar{v}_{\text{sw}} = dV_i & \text{inductor flux balance} \\ \bar{i}_r = 0 & \text{resonant capacitor charge balance} \\ \bar{i}_m = n_{21}\bar{i}_s = n_{21}I_o & \text{capacitors' charge balance} \end{cases} \tag{1}$$

where d is the duty cycle of the high-side switch S_H. The first two equations are also encountered in the analysis of the LLC converter, being the resonant tank the same, while the third one is a unique property of this topology and a consequence of the half-wave rectification. The latter highlights one of the drawbacks of the AHBFC, compared to the LLC converter, that is the switched current values become load-dependent, and so is the primary-side switches' ZVS condition.

A. Constant Capacitor Voltage

If the value of capacitor C_r is chosen high enough to have an almost ripple-free voltage $v_C(t) \approx V_C = dV_i$, all currents are piecewise linear, as shown in Fig. 2. Only three topological states are encountered: two of them ($0 \le t < d_fT_s$ and $d_fT_s \le t < dT_s$) take place during the upper switch on time; the related subtopologies are shown in Fig. 3(a) and (b), respectively. The third one ($dT_s \le t < T_s$) takes place during the lower switch conduction interval; its topology can be seen in Fig. 3(c). The peculiarity of such a nonresonant operating mode is that this behavior is maintained independently of the output current.

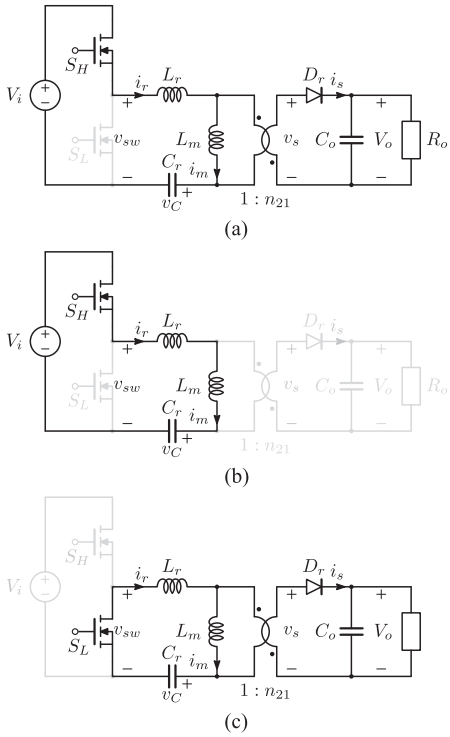

Fig. 3. Subtopologies in a switching period in the case of a constant capacitor voltage: (a) during subinterval d_fT_s; (b) during subinterval $(d-d_f)T_s$; and (c) during subinterval $(1-d)T_s$.

Indeed, the only difference in case of load current reduction is that $i_r(t)$ gets closer to $i_m(t)$ during interval $(1-d)T_s$, so as to account for the reduced output power.

B. Nonnegligible Capacitor Voltage Ripple

When the C_r value is reduced so as to exploit its resonance with L_r, the voltage ripple on $v_C(t)$ becomes not negligible, and both DCM and CCM operations are possible, as illustrated by the main converter waveforms shown in Fig. 4. In particular, Fig. 4(a) shows an example of what we call, for simplicity, DCM operation (other discontinuous modes, with different topological sequences, are possible), while Fig. 4(b) illustrates the CCM operation. As we can see, we identify the CCM with the situation where the rectifier diode conducts, at least, for the entire $(1-d)T_s$ interval, i.e., when both subintervals d_1T_s and d_3T_s

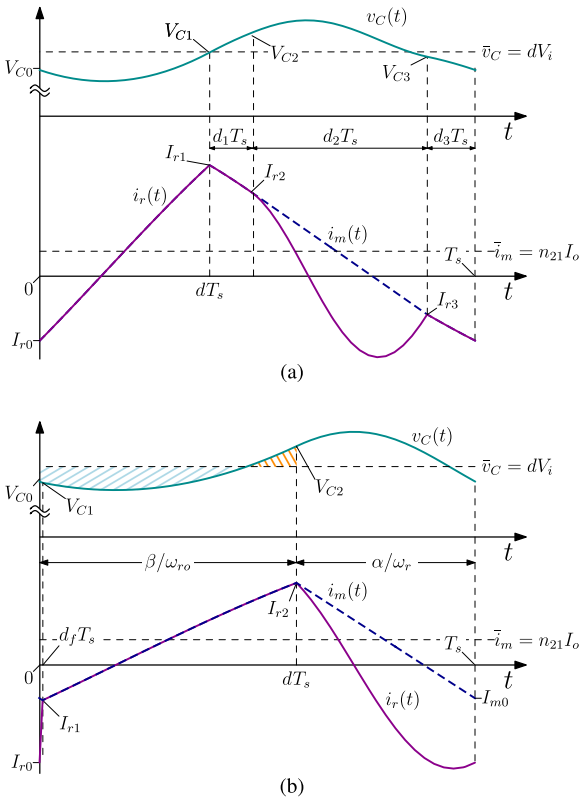

Fig. 4. Main waveforms in a switching period. (a) Example of DCM operating mode. (b) Example of CCM operating mode.

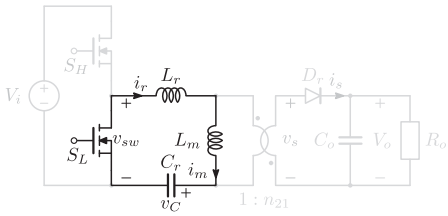

Fig. 5. Subtopology that appears in case of a nonnegligible capacitor voltage ripple during subintervals d_1T_s and d_3T_s.

are missing, while DCM operation is entered as soon as either subinterval d_1T_s or d_3T_s comes into play.

During these subintervals, a fourth subtopology appears, as shown in Fig. 5. Since two different resonant tanks are involved, the following parameters, that are used throughout the article, are defined:

$$\begin{cases} Z_r = \sqrt{\dfrac{L_r}{C_r}},\ \omega_r = \dfrac{1}{\sqrt{L_rC_r}} & D_r \text{ is ON} \\ Z_{ro} = \sqrt{\dfrac{L_r+L_m}{C_r}},\ \omega_{ro} = \dfrac{1}{\sqrt{(L_r+L_m)C_r}} & D_r \text{ is OFF.} \end{cases} \tag{2}$$

Also, parameter $\lambda = L_r/L_m$ will be used.

1) *Interval* $0 \le t \le d_fT_s$ [see Fig. 3(a)]. When the upper switch S_H is turned ON, if the rectifier diode was already conducting, as in CCM condition, it remains ON, until its current goes to zero. In fact, the magnetizing current continues to decrease, with a slope equal to $-V_o/(n_{21}L_m)$, while the resonant current increases, under the effect of the positive voltage $V_i - v_C(t) + V_o/n_{21}$. When the resonant current reaches the value of the magnetizing current at instant d_fT_s, the rectifier diode D_r turns OFF, being its current given by $i_s(t) = (i_m(t) - i_r(t))/n_{21}$. If, before instant $t = 0$, the rectifier diode was already OFF, this subtopology disappears, and $d_f = 0$.
2) *Interval* $d_fT_s \le t \le dT_s$ [see Fig. 3(b)]. Here, currents i_r and i_m increase, in a resonant manner, under the effect of the total voltage $V_i - v_C(t)$ applied to their series combination. If $\omega_{ro}T_s \ll 2\pi$, the currents increase almost linearly.
3) *Interval* $dT_s \le t \le (d+d_1)T_s$ (see Fig. 5). After the switches commutation (turn OFF of S_H followed by the turn-ON of S_L after a suitable dead time), if the condition

$$\frac{v_C(t)}{1+\lambda} < \frac{V_o}{n_{21}} \tag{3}$$

is verified at $t = dT_s$, the topology appears as shown in Fig. 5. Here, diode D_r remains OFF, and the resonance between C_r and $L_r + L_m$ continues, thus making $v_C(t)$ rise until D_r becomes forward polarized. In case inequality (3) is violated at $t = dT_s$, the subinterval d_1T_s disappears, as in Fig. 4(b).
4) *Interval* $(d+d_1)T_s \le t \le (d+d_1+d_2)T_s$ [see Fig. 3(c)]. In this subtopology, the magnetizing inductance voltage is clamped by the output voltage reflected to the primary side, thus causing its current to linearly decrease, while C_r and L_r continue to resonate at a much higher resonance frequency (the resonant inductance value is, usually, much lower than the magnetizing inductance one).
5) *Interval* $(d+d_1+d_2)T_s \le t \le T_s$ (see Fig. 5). If the resonant current i_r, during its oscillation, becomes equal to the magnetizing current i_m before the end of the switching period, the rectifier diode D_r turns OFF, thus making subinterval d_3T_s appear, as in Fig. 4(a). The equivalent circuit is the same as the previous subinterval d_1T_s, illustrated in Fig. 5, and it remains such until a new switching cycle begins.

The resonant current $i_r(t)$ and voltage $v_C(t)$, in the different subintervals, are described by the following relations:

$$\begin{cases} i_r(t) = \dfrac{V_a - V_{C_i}}{Z_o}\sin\left(\omega_o(t-t_i)\right) \\ \qquad + I_{r_i}\cos(\omega_o(t-t_i)) \\ v_C(t) = Z_oI_{r_i}\sin(\omega_o(t-t_i)) \\ \qquad + (V_{C_i} - V_a)\cos(\omega_o(t-t_i)) + V_a \end{cases} \tag{4}$$

with $i = 0,1,2,3$, and t_i representing the beginning of each subinterval ($t_0 = 0$). The coefficients that appear in (4) are defined according to the particular subinterval under consideration, as reported in Table I. The state variable initial conditions are also highlighted in Fig. 4. The magnetizing current $i_m(t)$ assumes the same expressions of $i_r(t)$ in all subintervals, except in d_fT_s

TABLE I
COEFFICIENTS USED IN THE RESONANT VOLTAGE AND CURRENT EQUATIONS

Interval	$\mathbf{V_a}$	$\mathbf{Z_o}$	ω_o
$d_f T_s$	$V_i + \frac{V_o}{n_{21}}$	Z_r	ω_r
$(d-d_f)T_s$	V_i	Z_{ro}	ω_{ro}
$d_1 T_s$ & $d_3 T_s$	0	Z_{ro}	ω_{ro}
$d_2 T_s$	$\frac{V_o}{n_{21}}$	Z_r	ω_r

and $d_2 T_s$, in which it decreases linearly according to

$$i_m(t) = I_{m_i} - \frac{V_o}{n_{21} L_m}(t - t_i) \tag{5}$$

with $t_i = 0$ or $t_i = (d + d_1)T_s$ in subintervals $d_f T_s$ and $d_2 T_s$, respectively. The current values I_{m_i} at the beginning of each subinterval are equal to I_{r_i}, except for $i = 0$ in CCM condition [see Fig. 4(b)].

III. VOLTAGE GAIN ANALYSIS

A. Constant Capacitor Voltage $v_C(t) \approx V_C = dV_i$

With piecewise linear current waveforms, as in Fig. 2, an approximated voltage gain can be easily found once the small subinterval $d_f T_s$ is neglected. In this case, the *volt–second* balance of the magnetizing inductance yields

$$\frac{(1-d)V_i}{1+\lambda} d \approx \frac{V_o}{n_{21}}(1-d) \quad \rightarrow \quad \frac{V_o}{V_i} = \frac{n_{21}}{1+\lambda} d. \tag{6}$$

Such an approximated voltage gain is load and frequency independent. However, the exact expression can be easily derived modifying the magnetizing inductance *flux* balance equation and exploiting also the capacitors' *charge* balance, i.e.,

$$\begin{cases} \bar{v}_m = \dfrac{(1-d)V_i}{1+\lambda}(d - d_f) - \dfrac{V_o}{n_{21}}(1 - d + d_f) = 0 \\ \bar{i}_{C_o} = \dfrac{1-d+d_f}{2f_s}\left(\dfrac{dV_i - \dfrac{V_o}{n_{21}}}{L_r} - \dfrac{V_o}{n_{21} L_m}\right)(1-d) = 0. \end{cases} \tag{7}$$

Combining these two equations yields the final expression of the voltage gain (the superscript *PWL* stands for piecewise linear)

$$M^{\text{PWL}} = \frac{n_{21} d}{1+\lambda}\left(1 - \frac{1}{\dfrac{d(1-d)^2 V_i}{2 L_r f_s n_{21} I_o} + d}\right) \tag{8}$$

which shows the dependence on the load current I_o and on the switching frequency (this expression coincides with the one calculated in [8], once the parameter λ is set to zero). An equivalent expression can be found considering a resistive load, i.e., substituting $I_o = V_o / R_o$ in (8), and rearranging for M, yielding

$$M^{\text{PWL}} = \frac{n_{21} d}{(1+\lambda)}\left[-\frac{1-d}{2d}\left(\frac{(1-d)(1+\lambda)}{k} + 1\right)\right.$$
$$\left. + \frac{1}{d}\sqrt{\frac{(1-d)^2(1+\lambda)^2}{k^2} + \frac{4(1+\lambda)}{k} + 1}\right]$$
$$\text{with } k = \frac{2 L_r f_s n_{21}^2}{R_o}. \tag{9}$$

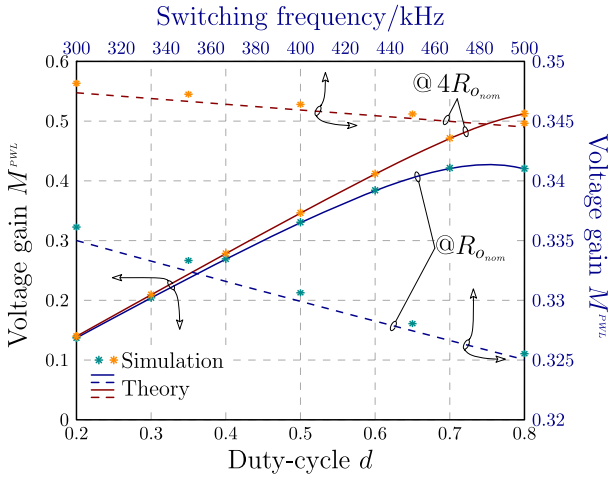

Fig. 6. Plots of the voltage gain in case of a constant capacitor voltage [see (9)], for two load resistor values: as a function of the duty cycle (continuous lines, lower-left axes in black) and as a function of the switching frequency (dashed lines, upper-right axes in blue).

TABLE II
CONVERTER SPECIFICATIONS

Parameter	Symbol	Value	
Nominal input voltage	V_i	370	V
Input voltage range	ΔV_i	$300 - 420$	V
Nominal output voltage	V_o	160	V
Nominal output power	P_o	160	W
Switching frequency	f_s	400	kHz

The plot of (9) versus the duty cycle for two load resistance values is reported in Fig. 6, together with simulation results: a nonmonotonic behavior is observed at high duty-cycle values at the nominal output power. The parameters used are the same considered for the experimental setup and are reported in Tables II and III (the sole difference is the value of C_r that, in simulation, was increased to 2 μF so as to obtain a negligible voltage ripple). The dependence on the switching frequency was investigated as well, and the result is shown in Fig. 6, once again for two load resistance values. With this operating mode, characterized by piecewise linear current waveforms, the voltage gain is practically independent of the switching frequency (note the expanded scale for the voltage gain on the right axis).

B. Resonant Case: CCM

In the following analysis, with reference to Fig. 4(b), we neglect subinterval $d_f T_s$, meaning that we assume $V_{C1} \approx V_{C0}$. Thus, we can consider only two subintervals in a switching period, whose corresponding angles are $\alpha = \omega_r (1-d) T_s$ and $\beta = \omega_{ro} d T_s$. Let us start again from the magnetizing inductance

volt–second balance, which yields

$$\bar{v}_{L_m} = \frac{1}{T_s}\int_0^{dT_s} \frac{V_i - v_C(t)}{1+\lambda}dt - \frac{V_o}{n_{21}}(1-d) = 0. \quad (10)$$

The term $f_s \int_0^{dT_s} v_C(t)dt$, using the second of (4) with parameters taken from the second row of Table I, can be expressed as $V_i d - V_{\text{ofs}}$, which, substituted into (10), yields

$$V_o = \frac{n_{21}}{1+\lambda}\frac{V_{\text{ofs}}}{1-d}. \quad (11)$$

The *offset* voltage V_{ofs} is given by

$$V_{\text{ofs}} = \frac{f_s}{\omega_{ro}}\left\{(V_i - V_{C1})\sin(\beta) - Z_{ro}I_{r1}\left(1-\cos(\beta)\right)\right\}. \quad (12)$$

In order to evaluate V_{ofs}, we need to find suitable expressions for the initial conditions V_{C1}, V_{C2}, I_{r1}, and I_{r2}. To this purpose, we exploit the continuity property of variable $v_C(t)$, using the second of (4) with parameters taken from the second and fourth row of Table I, i.e.,

$$\begin{aligned} V_{C2} &= V_i\left(1-\cos(\beta)\right) + V_{C1}\cos(\beta) + Z_{ro}I_{r1}\sin(\beta) \\ V_{C1} &= \frac{V_o}{n_{21}}\left(1-\cos(\alpha)\right) + V_{C2}\cos(\alpha) + Z_r I_{r2}\sin(\alpha). \end{aligned} \quad (13)$$

Then, by assuming an approximated triangular waveform for the magnetizing current, we can use (5) to estimate I_{r1} and I_{r2}, i.e.,

$$\begin{aligned} I_{r1} &\approx \bar{i}_m - \frac{\Delta i_{m_{pp}}}{2} = n_{21}\frac{V_o}{R_o} - \frac{V_o}{2n_{21}L_m f_s}(1-d) \\ I_{r2} &\approx \bar{i}_m + \frac{\Delta i_{m_{pp}}}{2} = n_{21}\frac{V_o}{R_o} + \frac{V_o}{2n_{21}L_m f_s}(1-d). \end{aligned} \quad (14)$$

Substituting (14) and (13) into (12), we obtain

$$V_{\text{ofs}} = k_1\left(V_i - k_2\frac{V_o}{n_{21}}\right). \quad (15)$$

The coefficients k_1 and k_2 are

$$k_1 = \frac{f_s}{\omega_{ro}}\frac{\sin(\beta)(1-\cos(\alpha))}{1-\cos(\alpha)\cos(\beta)} \quad (16)$$

$$\begin{aligned} k_2 = 1 &+ \frac{n_{21}^2 Z_r}{R_o}\left[1+\frac{\lambda}{k}(1-d)\right]\frac{\sin(\alpha)}{1-\cos(\alpha)} \\ &+ \frac{n_{21}^2 Z_{ro}}{R_o}\left[1-\frac{\lambda}{k}(1-d)\right]\frac{(1+\cos(\alpha))(1-\cos(\beta))}{\sin(\beta)(1-\cos(\alpha))}. \end{aligned} \quad (17)$$

Combining (11) and (15), the voltage gain is expressed as

$$M^{\text{CCM}} = \frac{V_o}{V_i} = \frac{n_{21}d}{1+\lambda}\left(\frac{1}{\frac{d(1-d)}{k_1} + \frac{k_2 d}{1+\lambda}}\right) \quad (18)$$

where the expression inside the round parenthesis is a correction term that accounts for the nonnegligible resonant capacitor voltage ripple.

TABLE III
CONVERTER PARAMETERS

Parameter	Symbol	Value	
Resonant inductance	L_r	6.2	μH
Magnetizing inductance	L_m	55.4	μH
Resonant capacitor	C_r	2×8.2	nF
Transformer turns ratio	n_{21}	$18/23$	
Output capacitor	C_o	10	μF

C. Resonant Case: DCM

Decreasing the converter duty cycle and/or the load, subintervals d_1T_s and/or d_3T_s start to appear, thus entering a DCM operating mode. The analytical voltage gain calculation in this condition is much more complicated, being the duration of such subintervals a function of the converter operating point. To go around that, we decided to apply a brute-force approach, consisting in numerically solving, using a MATLAB script, a nonlinear system of 11 equations with the following unknowns $[V_{C0}, V_{C1}, V_{C3}, I_{r0}, I_{r1}, I_{r2}, I_{r3}, d_1, d_2, f_s, V_o]$ [see Fig. 4(a)], for a given input voltage and load resistance. The value of V_{C2} represents the voltage, at which D_r becomes forward polarized and, as such, is a function of the output voltage only. Thus, expression (3), that for $t = t_2$ becomes an equality, is substituted for V_{C2} in all equations, where this parameter appears. The equations come from the continuity property of state variables $v_C(t)$ and $i_r(t)$ using (4) [for each state variable, four equations are considered, one for each of the four subintervals in Fig. 4(a)] plus the three steady-state equations in (1). As described in the next section, the converter was designed to operate at the DCM/CCM boundary condition at the nominal operating point with $d = 0.5$. From this point, where, with reference to Fig. 4(a), we have $V_{C0} = V_{C1}$, $I_{r0} = I_{r3}$, and $d_2 = d_3 = 0$, the DCM region is entered either reducing the duty cycle, or increasing the load resistance, or reducing the switching frequency. Thus, the MATLAB script was run, starting from this boundary operating point, with guessed values for the 11 unknown parameters obtained from the design procedure described in the next section, and verified by a single-converter simulation. For example, to determine the behavior of the voltage gain as a function of the duty cycle in the DCM, the system of 11 equations was solved iteratively starting from $d = 0.5$ and reducing the duty cycle in small steps. The outcomes of each iteration were used as guessed values for the subsequent iteration, thus avoiding any convergence problem. In this way, we have been able to obtain results that match almost perfectly the simulation results, as shown in Section V.

IV. PROPOSED DESIGN PROCEDURE

In this section, we propose a design procedure based on the specifications listed in Table II, coming from a LED lamp application with a front-end high-power-factor rectifier. This is an interesting application for the AHBFC, that is combined with a boost rectifier operating in the DCM and sharing the same switches (i.e., with the boost inductor connected to the switching node and the input voltage generator V_i in Fig. 1

substituted by the output capacitor of the boost stage). In fact, in this configuration, the boost duty cycle, which refers to the ON-time of the bottom switch, becomes equal to $1-d$. At light load, the boost duty cycle must decrease, to account for the reduced input power, which makes d increase. Being the AHBFC voltage gain roughly proportional to d, this behavior implies a reduction of the converter input voltage (being V_o constant), thus solving the problem of an increasing voltage stress at light load, showed by many similar integrated high-power-factor rectifiers that combine a DCM boost rectifier with a different isolated dc–dc stage, like in [20].

The resonant tank parameters L_r, L_m, and C_r and the transformer turns ratio n_{21} are derived by imposing the DCM/CCM boundary condition at the nominal operating point. This is the most favorable operating point for the AHBFC, with minimum devices' rms current and soft rectifier diode turn-OFF. At this boundary condition, each switching period contains only two topological states, whose duration is dT_s, and $(1-d)T_s$, respectively. Consequently, we have $I_{r0}=I_{r1}$ and $V_{C0}=V_{C1}$ in Fig. 4(b). The solution is found numerically, building a system of seven equations made up by four relations exploiting the continuity property of state variables $i_r(t)$ and $v_C(t)$, plus the three constraints (1). However, there are eight unknowns, i.e., the four state variables V_{C1}, V_{C2}, I_{r1}, and I_{r2} and the four converter parameters L_r, L_m, C_r, and n_{21}. Thus, we can use one of the two current values, that affect the ZVS turn-ON of the switches, to set an additional constraint. The less favorable condition regards the ZVS turn-ON of the upper switch S_H that involves the current I_{r1}, due to the offset equal to $n_{21}I_o$ of the magnetizing current waveform. For this reason, the current value I_{r1} is imposed as a constraint.

The key for a successful convergence of the solver algorithm is the choice of the initial guessed values for the seven unknowns. Thus, we start selecting the inductance ratio $\lambda_G=0.2$ (subscript G denotes *guessed* values), sufficiently low so as to avoid the use of an external resonant inductor. Then, the transformer turns ratio is estimated from (6) as $n_{21_G}=1.04$, imposing a nominal duty-cycle value $d=0.5$. The magnetizing inductance is estimated from the first of (14), by imposing $I_{r1_G}=0.92\,A$ (value estimated from the charge-equivalent output capacitance of the selected MOSFETs), giving $L_{m_G}=49\,\mu$H. From the latter, the resonant inductance turns out to be $L_{r_G}=\lambda_G L_{m_G}=9.8\,\mu$H. The resonant capacitor is estimated imposing the condition $\frac{\pi}{\omega_r}\approx(1-d)T_s$, yielding $C_{r_G}=16\,nF$. The initial condition I_{r2_G} is found using the second of (14), obtaining $I_{r2_G}=3$ A. Finally, the initial conditions V_{C1_G} and V_{C2_G} are estimated as $V_{C2,1_G}\approx\bar{v}_C\pm\Delta Q/(2C_r)$ (this is a quite rough estimation, being the voltage waveform far from piecewise linear). Charge ΔQ is calculated integrating the resonant current, which is assumed to increase linearly, giving

$$\Delta Q=\int_0^{dT_s} i_r(t)dt\approx I_{r1_G}dT_s+\frac{V_i(1-d)}{L_{r_G}+L_{m_G}}\frac{(dT_s)^2}{2}. \tag{19}$$

The calculated values are $V_{C1_G}=145$ V and $V_{C2_G}=225$ V. Using these initial conditions and guessed parameter values, the solver returned the following values: $L_r=6.17\,\mu$H, $L_m=55\,\mu$H, $C_r=16.1\,\mu$F, and $n_{21}=0.806$, pretty close to the values used in the experimental prototype, listed in Table III.

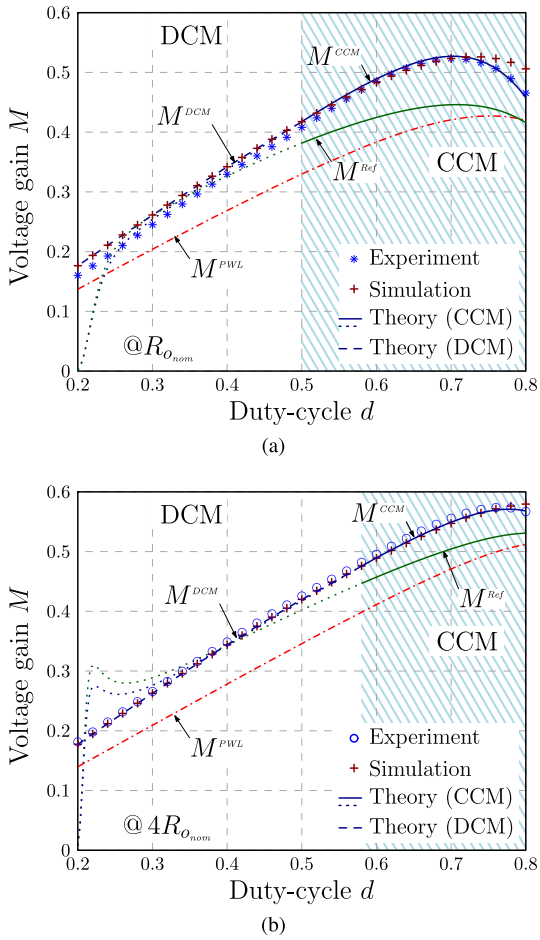

Fig. 7. Voltage gain comparison between theory, simulation, and experimental measurements: (a) with $R_o=160\,\Omega$ and (b) with $R_o=640\,\Omega$.

V. Validation of the Theoretical Analysis

Based on the design outcomes and the described theoretical analysis, the voltage gain plots, according to theory, simulations, and experimental measurements, can be seen in Fig. 7, for the nominal load resistance $R_o=R_{o_{\rm nom}}=160\,\Omega$ and for $R_o=4R_{o_{\rm nom}}=640\,\Omega$. The figures also report the voltage gain $M^{\rm PWL}$ as well as the voltage gain $M^{\rm Ref}$ derived in [18], both calculated for the same converter parameters. First of all, it is important to recognize that the expression derived in (18) is well approximated for CCM operation only, i.e., in the highlighted areas in Fig. 7 (roughly above $d=0.5$ and $d=0.58$, for $R_{o_{\rm nom}}$ and $4R_{o_{\rm nom}}$, respectively). For this reason, the plot of (18) uses a continuous line in the CCM region and a dotted line in the DCM region. From Fig. 7, we can make the following general considerations.

1) The voltage gain appears to be nonmonotonic, with a maximum value that is load dependent. This behavior is also captured by the exact voltage gain expression $M^{\rm PWL}$, corresponding to a converter designed for a negligible voltage ripple across C_r, but the resonant behavior shows

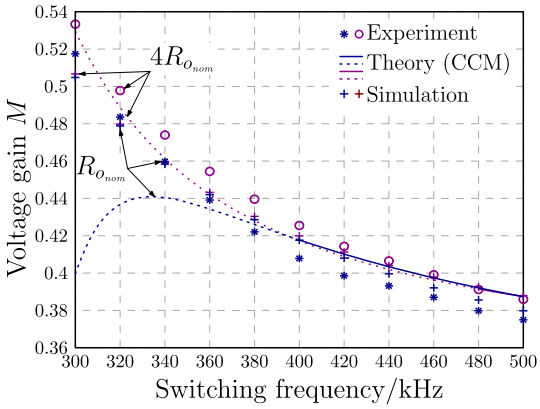

Fig. 8. Voltage gain comparison as a function of the switching frequency for two load current values.

a substantial increase of the voltage gain in the whole duty-cycle range.

2) The expression derived in [18] is far less precise, even if it correctly reveals the nonmonotonic behavior at high duty-cycle values.
3) The gain expression derived for the CCM with the nominal load resistance is reasonably precise, at least up to $d = 0.7$, when it starts to deviate from the simulation results. At higher load resistances, the matching is even better, as Fig. 7(b) reveals. The fact that the measured gain fits very well with the theoretical prediction even for $d > 0.7$ is a mere coincidence. Its deviation from the simulation results is caused by phenomena not accounted for in the simulated model, such as the losses and the dead time in the driving signals that, put together, make it apparently track the theoretical gain.
4) The theoretical analysis done in the DCM, reported as dashed lines in Fig. 7, matches exactly the values obtained in simulation and gets also pretty close to the experimental results, even at the nominal load resistance.
5) Far from the gain curve peak, the voltage gain turns out to be almost load independent, except for very small variations caused by the converter losses. This property is maintained also in the DCM.
6) Expression (18), as well as the one proposed in [18], fits reasonably well even when the converter enters the DCM operating mode, except for very low duty-cycle values. This is because during both subintervals d_1T_s and d_3T_s [see Fig. 4(a)], the voltage across the magnetizing inductance is not much lower than the value V_o/n_{21} corresponding to the CCM operation. Thus, the error made in the volt–second balance calculation in (10), which is the pillar of the voltage gain derivation, is not so high, at least until a deep discontinuous operation is entered.

It is interesting to analyze the sensitivity of the voltage gain with respect to the switching frequency, which affects the dimensionless parameter k and angles α and β. Fig. 8 compares the voltage gain given by (18) with simulations as well as experimental measurements. Once again, it is important to recognize that, varying the frequency in the range from 300 to 500 kHz, the converter moves from the DCM to the CCM. In particular, for the nominal load resistance, the transition takes place at $f_s = 400$ kHz, while for the higher load resistance, the CCM appears only above $f_s = 480$ kHz. For this reason, the plot of (18) uses a continuous line in the CCM region and a dotted line in the DCM region. Nonetheless, similarly to what we observed in Fig. 7, (18) works reasonably well also in DCM, except for the nominal load, where a substantial deviation from the simulated/experimental data is observed. Taking the nominal switching frequency of $f_s = 400$ kHz as a reference, looking at the experimental measurements, a frequency variation of -25% causes a voltage gain increase in the order of $+25\%$ ($\approx +20\%$ in simulation), while for the same amount of frequency variation of $+25\%$, the gain reduces by 8–9% (roughly the same in simulation). This means that the voltage gain sensitivity with respect to the switching frequency is much higher in the DCM than in the CCM.

Finally, by comparing Fig. 8 with Fig. 6, we can conclude that, once the resonant operation is considered, the sensitivity of the voltage gain with the switching frequency becomes nonnegligible. This behavior could be exploited, using the switching frequency as an addition control parameter.

VI. Experimental Results

The implemented prototype employs two MOSFETs STB26N60M2 from STMicroelectronics, while the rectifier SiC diode is IDD03SG60C from Infineon. The transformer has been realized with a PQ 26/25 magnetic core (material N49), with primary and secondary windings made by 23 and 18 turns, respectively, both using a Litz wire (bundle of 200 strands, having each a diameter of 50 μm). The values obtained for the magnetizing inductance and the total primary-side leakage inductance are reported in Table III, measured at 400 kHz with the Agilent 4294A precision impedance analyzer. The voltage gain, reported in Fig. 7, was measured at $V_i = 250$ V at nominal output resistance ($R_o = 160\,\Omega$), and at $V_i = 300$ V with an output resistor four times the nominal one ($R_o = 640\,\Omega$). The converter main waveforms, taken at $V_i = 300$ V and $R_o = 160\,\Omega$, with two different duty-cycle values are shown in Fig. 9: with $d = 0.3$, the converter operates in the DCM, while at $d = 0.7$, the converter works in the CCM. Time intervals are also highlighted for an easy comparison with the theoretical waveforms of Fig. 4: subintervals d_1T_s and d_3T_s are revealed by the small oscillations visible in the secondary winding voltage. ZVS is achieved, thanks to the 200-ns dead time inserted in the driving signals. As far as the rectifier diode is concerned, both DCM and CCM operating modes in Fig. 9 are characterized by a soft-switching condition. However, the higher current slope that occurs in the CCM during subinterval d_fT_s is likely to excite more oscillations between the unavoidable transformer secondary leakage inductance and the diode parasitic capacitance, a condition clearly visible in Fig. 9(b). This problem is partially mitigated by the higher average voltage across the resonant capacitor ($\bar{v}_C = dV_i$) at high duty-cycle values, which reduces the peak of the negative voltage at the transformer secondary side [compare $v_s(t)$

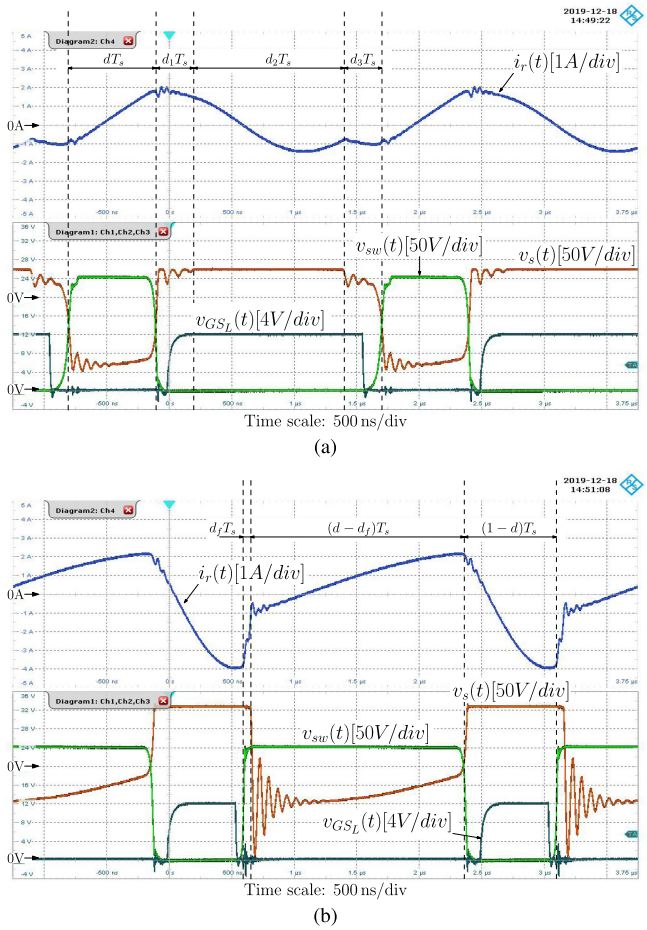

Fig. 9. Main converter waveforms at different operating points ($V_i = 300$ V, $f_s = 400$ kHz). (a) Example of DCM operating mode with $D = 0.3$. (b) Example of CCM operating mode with $D = 0.7$.

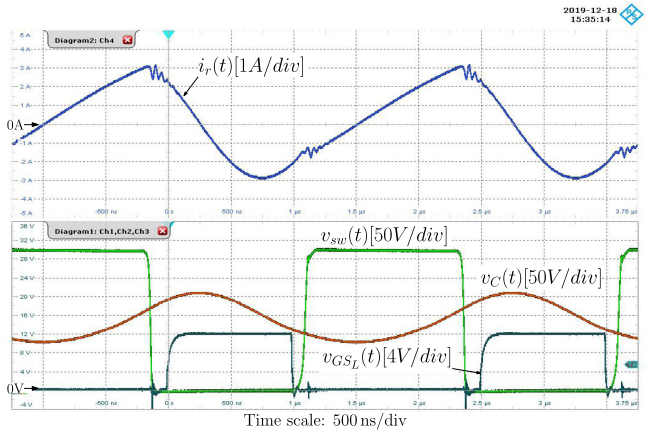

Fig. 10. Main converter waveforms taken at nominal input/output voltages and power ($f_s = 400$ kHz and $d = 0.52$).

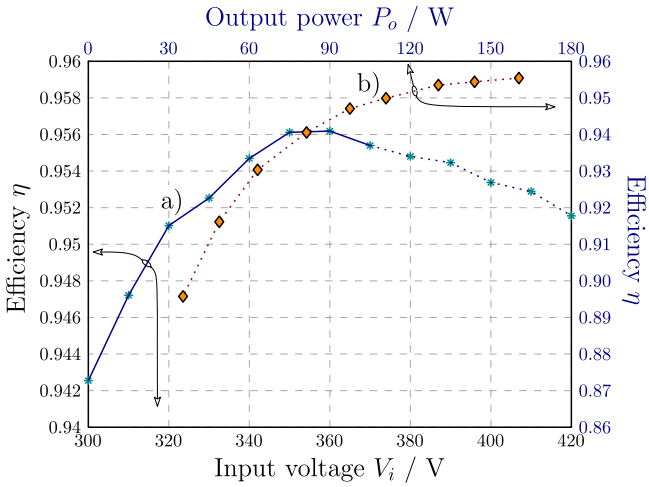

Fig. 11. Power stage efficiency: (a) as a function of the input voltage at nominal output voltage and power (lower/left axes) and (b) as a function of the output power at nominal input/output voltages (upper/right axes). Continuous line: CCM operation; dotted line: DCM operation.

in Fig. 9(a) and (b)]. In any case, this is the reason why a 600-V rectifier diode was used, even if its theoretical voltage stress is below 350 V. From this standpoint, DCM operation is preferable. This can be an additional motivation for choosing to design the converter to operate in the resonant mode.

The converter waveforms, including the resonant capacitor voltage, taken at nominal input/output voltages and power, are shown in Fig. 10 ($f_s = 400$ kHz and $d = 0.52$): according to the proposed design procedure, the operating point is at the boundary between the DCM and the CCM, and the measured efficiency is $\eta = 95.5\%$. Fig. 11 shows the measured efficiency taken at nominal output voltage and power in the whole input voltage range (curve a, lower/left axes), as well as a function of output power at nominal input/output voltages (curve b, upper/right axes). The continuous line indicates CCM operation, while the dotted line stands for DCM operation. As can be seen, the maximum efficiency is measured around the operating point corresponding to the boundary condition between the DCM and the CCM, which, by design, corresponds to the nominal conditions. From this point, looking at curve a, the efficiency drop is more pronounced when the converter enters into a deep CCM operation, when the input voltage is reduced, thus forcing an increase of the duty cycle. On the other hand, reducing the output power, the operating point remains in the DCM, since, as previously demonstrated, this converter shows a weak dependence on the load. At the nominal operating point, the different calculated loss contributions, in percentage of the total measured losses, are: switches conduction losses 14.4%, rectifier diode conduction losses 25.3%, transformer winding losses 26.4%, transformer core losses 21.7%, and other losses including residual switches turn-OFF losses 12.2%. In these calculations, the considered device's temperature, as well as the transformer winding and copper temperature, was $T_{op} = 100\,^{\circ}$C.

VII. Conclusion

This article investigates the voltage gain of the AHBFC taking into account the resonant behavior of this topology. Both CCM and DCM operating modes have been considered, even if an analytical expression is found for CCM operation only. In addition, a methodology to numerically derive the DCM gain has

been illustrated that circumvents the analytical complexities and provides highly accurate results. Overall, it has been proved that, when the converter is designed for resonant operation, so as to eliminate any reverse recovery problem of the rectifier diode, its voltage gain shows a nonmonotonic behavior and varies with the switching frequency. To corroborate these results, the proposed theoretical analysis has been verified through simulations as well as experimental measurements taken on a 160-W prototype switching at 400 kHz.

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