Characterization of Low-Inductance SiC Module With Integrated Capacitors for Aircraft Applications Requiring Low Losses and Low EMI Issues

Bernardo Cougo, Hans Hoffmann Sathler, Raphael Riva, Victor Dos Santos, Nicolas Roux, and Bruno Sareni

***Abstract*—Future aircrafts will be composed of high number of power converters having always higher power density and efficiency. In order to increase performance of such converters, a good option is the use of silicon carbide (SiC) transistors. Although these components reduce losses when compared to their silicon-based counterpart, they increase switching speed and overshoot during commutation, which can cause serious electromagnetic interference issues and overvoltages on loads connected to these converters. For that reason, power modules containing SiC transistors must have the lowest possible parasitic inductance. This article presents a multilevel low-inductance SiC power module designed to optimize a three-phase 540 V/15 kVA inverter for modern aircrafts. Precise dynamic characterization is performed in order to accurately determine switching energies and to show improvement of loss performance of this power module when compared to discrete components and also to power modules from the market. Inverter input and output common mode current reduction due to integrated common mode capacitors in the power module is experimentally shown.**

***Index Terms*—Electromagnetic interference (EMI), low-inductance module, loss measurement, more electrical aircraft (MEA), modified opposition method (MOM), silicon carbide (SiC) module, switching energy.**

I. Introduction

In order to reduce emission of greenhouse gases and at the same time fuel consumption, modern aircraft are designed so pneumatic, hydraulic, and mechanical systems are replaced by electrical ones [1]–[5]. Examples of such systems are fuel pumps, flight control actuators, fans, cabin pressurization system, engine start, and others. Many of these applications are power drive systems, which are usually composed of three-phase inverter, cable, and motor, as shown in Fig. 1.

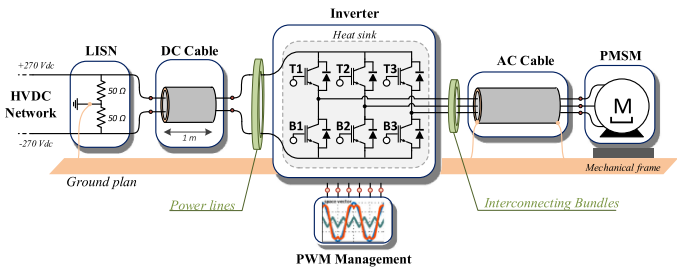


Fig. 1. Representation of a typical power drive system of modern aircraft.

In such applications, the power drive systems must have low weight and volume and very high efficiency. One of the enabling technologies for high power density power converters is wide bandgap (WBG) semiconductors [6]–[9]. This WBG technology opened the door for more efficient systems in any aircraft power conversion application in the near future.

Some of future aircraft will have distributed dc voltage of 540 V [1]. For that reason, silicon carbide (SiC) MOSFETs are promising candidates to replace Si insulated gate bipolar transistor (IGBT) [4], [6], instead of low-voltage (up to 650 V) GaN transistors. The efficiency of SiC converters are significantly better than their Si counterparts due to the inherently lower conduction and switching losses of SiC MOSFETs compared to Si IGBTs [10]–[13]. Moreover, SiC semiconductors may operate at higher junction temperatures when compared to Si semiconductors, with the consequent reduction of the cooling system [11].

SiC devices usually present faster switching that reduces switching losses and allow higher switching frequencies. This, in some cases, reduces filtering needs, consequently increasing the converter's power density. However, converters to aircraft applications must comply with electromagnetic interference (EMI) standards which, in most of the cases, have to increase differential-mode filtering needs when increasing the switching frequency [14], [15]. Increasing the switching frequency and also the switching speed (higher dV/dt) may also produce bulkier common mode filters [16], [17].

Manuscript received April 17, 2020; revised June 24, 2020; accepted July 29, 2020. Date of publication September 17, 2020; date of current version March 5, 2021. This work was supported by Integration Project, which is funded Airbus Operations, Airbus Group Innovations, Altran Technologies, Liebherr—Aerospace Toulouse, Safran Electrical and Power, Safran Electronics and Defense, Zodiac Aero Electric, Zodiac Actuations Systems, and the French National Agency of Research (ANR) Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Bernardo Cougo.)*

Bernardo Cougo, Hans Hoffmann Sathler, and Raphael Riva are with the IRT Saint-Exupery, 31405 Toulouse, France (e-mail: bernardo.cogo@irt-saintexupery.com; hans.hoffmann@irt-saintexupery.com; raphael.riva@irt-saintexupery.com).

Victor Dos Santos was with the IRT Saint-Exupery, 31405 Toulouse, France. He is now with SAFRAN S.A., 31700 Blagnac, France (e-mail: victor.dos-santos2@safrangroup.com).

Nicolas Roux and Bruno Sareni are with the Laplace Laboratory, Laplace, 31071 Toulouse, France (e-mail: nicolas.roux@laplace.univ-tlse.fr; bruno.sareni@laplace.univ-tlse.fr).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3014529

High switching speeds together with high parasitic inductances and capacitances of SiC devices and converters may induce high overvoltage on motors connected to these converters through long cables [18]–[22]. In aircraft, some applications, such as flight control actuators, may have the converter up to 20 m away from motors. In these cases, the voltage at the motor terminals can be higher than twice the dc bus voltage of the converter [22], which may significantly increase partial discharge (PD) issues and reduce the power drive system lifetime.

For all these reasons, converters for aircraft must be carefully designed with SiC components not only to reduce losses and consequently increase efficiency and power density, but also to ensure proper commutation to reduce EMI and PD issues. Thus, reducing parasitic inductance and capacitance of SiC power modules and the associated converter is a key element to an efficient and low-weight power drive system.

This article presents a low-inductance six-phase SiC power module [23] designed to be used in a parallel multilevel inverter for aircraft applications, as shown in [24]. Design of main components is shown in Session II and switching characterization of one version of this module is shown in Session III. Results show lower switching losses and overvoltage when compared to commercial power modules. Furthermore, they show lower electromagnetic emissions, which reduces the weight of the common mode filter of about 24% for a specific aircraft application.

II. Power Module Design

The power module shown in this article is designed for a three-phase inverter to drive a 15-kVA high-speed motor. The objective is to design a power drive system having the highest possible efficiency and power density. Thus, the converter has to produce not only the lowest possible losses but, at the same time, it is desired to have reduced switching speed and overshoot during commutation in order to keep low filtering needs. Also, low levels of voltage step in the output are desired in order to limit overvoltage in the motor terminals amplified by cable length and impedance [22], [25].

A low switching speed may also reduce the Miller effect (i.e., crosstalk) in a switching cell [26] as well as the common mode transient immunity of isolation barriers around the converter [27]. However, switching speed reduction is usually achieved by changing gate resistance, which increases switching losses and decreases efficiency. On the other hand, active gate drivers produce a lower switching speed for the same switching losses [28]. In any case, the "optimal" switching speed is a tradeoff between losses and filter size, and not necessarily the highest switching speed is the best for a system as it is shown in [29].

Given the application, converter output current is nearly sinusoidal and has a maximum root mean square (rms) value of 26 A. A nominal input voltage of the converter is 540 V although aircraft standards specify maximum voltage at transient of 900 V. For that reason, 1200-V components must be used if two-level bridge legs are used in each phase of the converter. Since the goal is to reduce losses and at the same time operate at high frequency in order to correctly drive a high-frequency motor, SiC transistors is the best option.

The choice of which SiC MOSFET die and the number of these components to parallel is done by comparing total losses (conduction + switching) in a bridge leg.

Loss calculation methods can be found in detail in [30]–[33]. Conduction losses can be easily calculated by

$$P_{\mathrm{cond}} = R_{\mathrm{DSon}} \cdot \left({I_{\mathrm{fRMS}}}^2 + {I_{\mathrm{rRMS}}}^2 \right) \tag{1}$$

where $I_{f\mathrm{rms}}$ is the rms value of the fundamental current and $I_{r\mathrm{rms}}$ is the rms value of the high-frequency ripple, which is, in this case, negligible since motors have usually high inductance and then very low high frequency current ripple. $R_{DS\mathrm{on}}$ is the ON-state resistance of a MOSFET at a certain junction temperature, which can be found on the components datasheet. Here, conduction loss calculation was performed at 135 °C junction temperature, which is 15 °C below the maximum junction temperature fixed by the SiC MOSFET manufactures.

Switching losses are calculated using the datasheet curves related to the variation of turn-ON and turn-OFF energies with the switching current, for given switching voltages V_{DS}, gate resistance R_G, gate-source voltage V_{GS}, and junction temperature T_j.

Motor current is considered to be sinusoidal with negligible ripple. Since the switching frequency is much higher than the fundamental frequency of the current (although it could be higher than 1 kHz), one can consider that, at each switching period, the same current value is switched ON and OFF, and thus switching losses P_{sw} can be calculated as follows:

$$P_{sw} = \frac{F_{sw}}{N_p} \cdot \sum_{n=0}^{N_p} \left[E_{\mathrm{off}}\left(i\left(n\right)\right) + E_{\mathrm{on}}\left(i\left(n\right)\right) \right] \tag{2}$$

where N_p is the number of switching periods inside a fundamental period of the motor current, E_{on} and E_{off} are, respectively, the turn-ON and turn-OFF energies at a certain current, $i(n)$ is the current value at each switching period n, and F_{sw} is the switching frequency.

Note that manufacturers usually do not give E_{on} and E_{off} curves for different switching voltages or gate resistances. For that reason, in a first and simple approach, we have decided to calculate switching energies by first taking the energy curves E_{xd} and scaling them down to the desired switching voltage V_{DSc} as follows:

$$E_{\mathrm{x}}(V_{\mathrm{DSc}}) = E_{xd}\left(V_{\mathrm{DSd}}\right) \cdot \left(\frac{V_{\mathrm{DSc}}}{V_{\mathrm{DSd}}} \right) \tag{3}$$

where V_{DSd} is the voltage level for which the switching energy E_{xd} (either E_{on} or E_{off}) is given in the datasheet.

Equation (3) may not find switching energies as accurate as in some other methods [33]–[37], but it has limited inaccuracy at high current values since turn-ON plus turn-OFF energies mainly depend on the reverse recovery energy of body diodes and the energy related to fact that the transistor crosses the linear region (VxI crossing losses). These two mechanisms are directly proportional to the switching voltage. Also, this inaccuracy is low if the voltage difference between V_{DSd} and V_{DSc} is small, which is the case here since dc bus voltage is 540 V and components datasheet energies are given for 600 V.

Another mechanism of losses during commutation is losses at the body diode during dead time. They are quite low for high-voltage components.

The last important loss mechanism is the energy lost due to charge and discharge of the output parasitic capacitance C_{oss} when a switch turns ON at hard switching operation. Capacitive energy is proportional to the square of the voltage over the capacitance. However, in a power MOSFET, C_{oss} decreases with the drain-source voltage V_{DS} and thus total switching energy ($E_{\text{on}} + E_{\text{off}}$) at zero current is not zero and also it is not proportional to the square of the switching voltage. However, it is sometimes given in the datasheet of components as E_{oss}.

One can rarely find in datasheets E_{on} and E_{off} values for currents lower than 30% of the rated current. For that reason, in order to find a total energy curve ($E_{\text{on}} + E_{\text{off}}$) for currents from 0 to a certain maximum current, the idea is to scale down the datasheet ($E_{\text{on}} + E_{\text{off}}$) curve as in (3) and complete this curve with a point at zero current which is equal to $4 \cdot E_{oss}$, for E_{oss} given at V_{DSc}. At zero current, when a transistor in a bridge leg turns OFF, it has no energy lost. However, when it turns ON, it loses the energy stored in its parasitic capacitance (E_{oss}) plus the same amount of energy to charge the parasitic capacitance of the opposite transistor. For that reason, since there are two turn-ON commutations in a switching period at zero current, there is 4 E_{oss} lost in this switching period in this bridge leg.

A. Comparison of Different Switches to Compose the Power Module

Total losses in a bridge leg were calculated and compared for different SiC MOSFET dies. This calculation was performed using datasheet information of different 1200 V SiC MOSFETs on TO-247 packaging. Comparison is made for four 1200 V components from Wolfspeed, having rated ON-state resistance (R_{DSon}) of 160, 80, 40, and 25 mΩ. Switching energy curves were extracted for V_{DSd} voltage of 600 V, and for the standard external gate resistance R_G value given at each datasheet, which is 2.5 Ω for all components except for the 25 mΩ device which was tested at $R_G = 6.8\ \Omega$.

Given the output current (maximum of 26 A rms), comparison was also performed for two paralleled 80 mΩ dies and two or three paralleled 160 mΩ dies. Results of calculated total losses in all the transistors of a bridge leg for output current from 0 to 26 A and for all options abovementioned are performed for switching frequencies of 20 and 140 kHz. Results can be seen in Fig. 2.

Note in Fig. 2(a) that at low frequency, configuration having one 25-mΩ component presents lower losses since it has the lowest R_{DSon} and thus the lowest conduction losses. At high frequency, since switching losses are predominant, configuration with two 80 mΩ in parallel is the one presenting lowest loss.

Although all components compared here are from the same manufacturer and have the same technology, based on the manufacturers datasheets, switching energy of two 80 mΩ dies in parallel is lower (if they are ideally paralleled), than that of one 40 mΩ die. It is also the case if two 160 mΩ dies are compared to one 80 mΩ die.

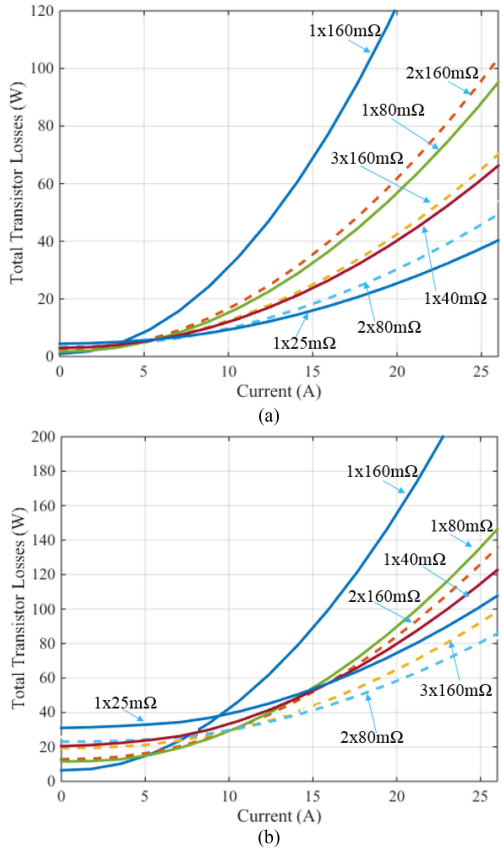


Fig. 2. Total switching losses of a bridge leg for sinusoidal output current, for different SiC MOSFET dies and number of dies in parallel, for switching frequencies. (a) 20 kHz. (b) 140 kHz.

Consequently, the best option to reduce losses at high frequency would be four paralleled 160 mΩ dies instead of two paralleled 80 mΩ dies. However, that many numbers of dies would be impossible to enter in a power module packaging as the one which will be shown in the following section. Furthermore, the higher the number of parallel dies is, the more difficult the routing of copper on the ceramics is and also the more difficult it gets to achieve perfect current sharing between all paralleled dies during conductions and switching.

For all these reasons and since this power module will be used in high-speed motor applications, a solution with two 80 mΩ dies in parallel was chosen. However, instead of directly paralleling the SiC dies, the best idea is to parallel switching cells through coupled or uncouple inductors (as shown schematically in Fig. 3) resulting in a multilevel converter, with the result of having a multilevel voltage applied to each phase of the motor in order to decrease EMI and overvoltage issues [25], [38], [39]. For these reasons, it was decided to design a power module having six switching cells using 1200 V/80 mΩ dies from Wolfspeed reference CPM2-1200-0080B.

B. Low-Inductance Architecture of Multilevel Power Module

It is now a common knowledge that, in a switching cell, reducing parasitic inductance of the power loop and of the gate loop reduces switching losses and overshoots [40].

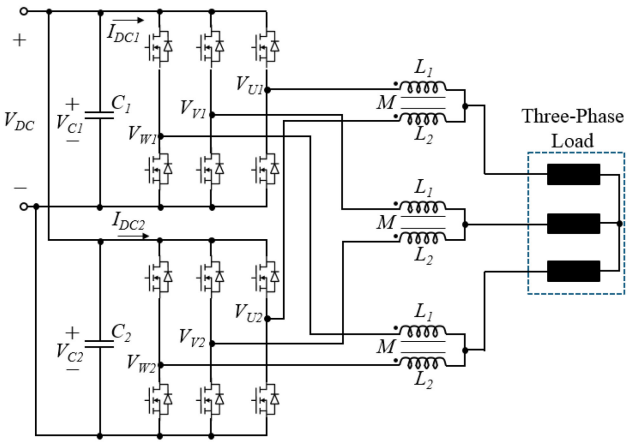


Fig. 3. Representation of a typical power drive system using six switching cells connected to drive a three-phase load. Each load phase is connected to two switching cell though coupled inductors. The voltage in the output of coupled inductors is the instantaneous average of voltages in two cells, which results in a three-level voltage when switching cells have interleaved signals.

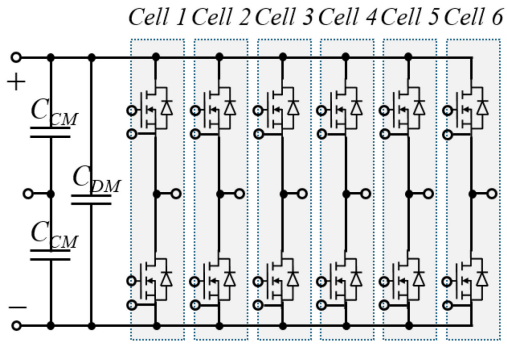


Fig. 4. Internal circuit of the developed low parasitic inductance multilevel SiC power module.

If the parasitic inductance is high on the source terminal of the component and it is part of the power loop and also of the gate loop, then it will significantly slow down the component and increase turn-ON losses [41]–[43].

However, if the parasitic inductance is part of the power loop but not of the gate loop, then switching losses may increase mainly during turn-OFF since the energy stored in this inductance at the ON-state of the component is lost when the component turns OFF. Turn-ON energy is usually slightly reduced by this parasitic inductance. However, the higher this inductance is, the higher the overshoot during turn-ON and turn-OFF will be, and thus, it limits the minimal gate resistance one can use, and as a consequence, it indirectly increases switching losses.

One can reduce power-loop parasitic inductance by reducing the length of supply terminals of a switching cell [40], by reducing the inductance of bus bars and also by choosing bus capacitors with reduced series equivalent inductance (ESL). Another way is to place ceramic capacitors, which present low ESL when compared to film or aluminum capacitors, as close as possible of the switching cells [40]. These capacitors must have enough capacitance to provide the necessary energy lost and stored during a commutation instant.

Most of the switching energy in SiC MOSFET is lost during hard switching turn-ON. In a turn-ON commutation of a transistor of a bridge leg connected to an inductive load, the energy provided by the decoupling capacitor accounts for the energy to charge the parasitic capacitance of the turned-OFF transistor as well as the losses due to fact that the transistor crosses the linear region. This energy is almost the same as the turn-ON energy.

In the case of the designed power module, in the worst case, there would be six components 1200 V/80 mΩ turning ON 540 V and 20 A at the same time. Total energy lost at these conditions, according to the components datasheet, would be $E_t = 6 \cdot 181\ \mu\text{J} = 1086\ \mu\text{J}$.

The final voltage level V_f at a capacitance C_{DM} providing a certain energy E_t at initial voltage V_{dc} is

$$V_f = \sqrt{{V_{\text{dc}}}^2 - \frac{2 \cdot E_t}{C_{DM}}}. \tag{4}$$

If a maximum voltage drops ($V_{\text{dc}} - V_f$) of 1% (5.4 V) is accepted in this capacitor when the six transistors switch at the same time, the minimum value of this capacitance would be 375 nF. For that reason, the power module was designed with two paralleled TDK CeraLink ceramic capacitors of 900 V and 250 nF.

Lower parasitic inductance results in a higher switching speed and then higher EMI issues. For that reason, common mode capacitors were integrated into the power module. One connected from the positive dc-bus terminal to the ground pin, and the other from the negative dc-bus terminal to the ground pin. These capacitors reduce common mode current in the converter input [44], which must comply with aircraft standards.

The design and integration of common mode capacitors are complex. Ceramic technology is preferred due to its high bandwidth, capacitance density, and high temperature robustness. The voltage these capacitors should stand depends on the maximum voltage they could exist between input terminals and ground (usually defined by standards). The capacitance value is the trickiest parameter. As pointed out in [44], it is a tradeoff between how much filtering is needed of certain high-frequency currents and the space it can take inside the module. Higher values of capacitance have also lower bandwidth and do not efficiently filter high-frequency current. The best capacitance value obviously depends on the impedance of the whole system (inverter, cables, and motor) and the most precise approach to choose the best capacitance value is by experimental means. For the module designed here, no empirical evaluation was possible to be applied due to limited time in the design phase. Thus, two 22 nF/450 V ceramic capacitors were integrated for a first test.

The internal circuit of the developed module as well as a photograph of its packaging is shown in Figs. 4 and 5, respectively. Note that no Schottky diode was connected in parallel with MOSFETs in order to decrease losses at low current and to save space inside the module.

Fig. 5. Photograph of the developed multilevel SiC power module with integrated common mode and differential-mode capacitors.

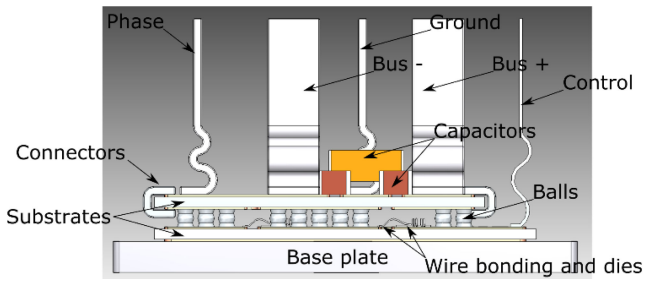


Fig. 6. Principle of the architecture in layers of the six-phase SiC power module.

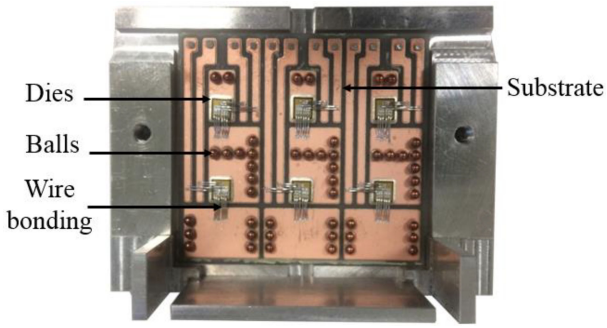


Fig. 7. Bottom substrate with dies, wire bonding, and balls.

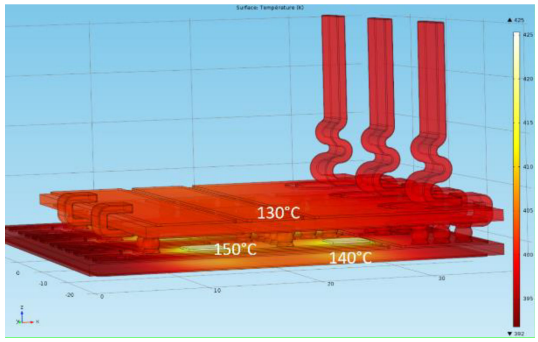


Fig. 8. Distribution of temperature between the two ceramic substrates.

This power module was designed to be put in a packaging having the same size of the SiC power module CCS020M12CM2 or CCS050M12CM2 from Wolfspeed.

One of the major problems about the assembly of this SiC power module is the difference in the maximum operation temperature of the dies and the capacitors to integrate as closely as possible (SiC MOSFET at 150 to 200 °C, capacitors at 150 °C).

In order to ensure the integration of each of these components, it is therefore necessary to create two layers of different temperatures inside this module. The latter are created using two ceramic substrates, copper balls, and wire bonding. The principle of this architecture in layers is illustrated in Fig. 6.

Capacitors are soldered to the top substrate and MOSFET are attached on the bottom substrate.

The copper balls ensure the mechanical holding and electrical connection of both substrates. They are away from hot spots (no direct contact with the dies) in order to serve as a heat diffuser for the top layer (cf., Fig. 7). This absence of direct contact also makes it possible to create a thermal insulation barrier between the dies and the capacitors and, thus, to limit the heating of the top substrate during the operation of the dies.

Thermal simulations made with COMSOL software (cf., Fig. 8) have shown that for normal operation of the module, the gap from the maximal temperatures between the two layers could reach 20 °C, with a top substrate temperature not exceeding 130 °C (less than 150 °C supported by capacitors) and, therefore, allowed to validate this architecture.

Aluminum bonding wires are used to interconnect the top side of the dies. Due to the "sandwich" architecture of this module, the height of these wires between the two substrates becomes critical and must be controlled in order to respect the isolation distance between the different potentials.

Ideally, at the electrical level, capacitors should be located as close as possible to each module switching cell (composed of two MOSFET). The "sandwich" architecture presented above should therefore be duplicated six times to achieve this module, which seems delicate given the lack of space inside the module. Electrical simulations, made with the PSIM software, during the design have shown that the dynamic behavior of a group of capacitors per cell was substantially identical to that of a group for the six cells of the module. Consequently, and for thermomechanical reasons, the choice was to make two independent submodules of three cells with a group of capacitors each to achieve a design as symmetric as possible. This choice is illustrated in Fig. 9.

The substrates used in this module are of two types. The bottom substrate is in all cases a metallic substrate with an aluminum nitride ceramic (AlN). However, the top substrate is either the same type as the bottom one, or metallic with a silicon nitride ceramic (Si3N4). In the first case, it is necessary to use routing connection rings to electrically connect the bottom and top surfaces of the substrate while in the second case this connection is carried out through "vias" directly in the ceramic (which is not easily done using aluminum nitride).

Simulated values of the whole power-loop inductance of only one switching cell is 20 nH for the version of the power

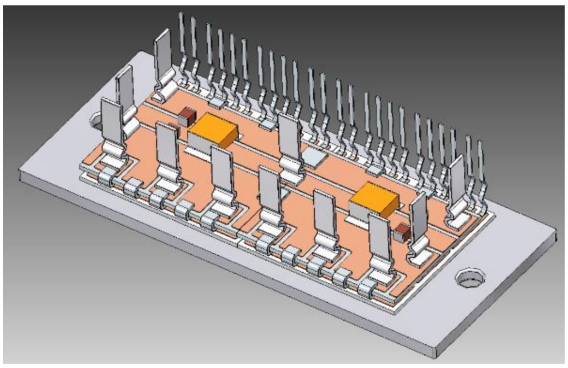


Fig. 9. Distribution of the two submodules in the SiC power module developed.

module with AlN substrate and 16 nH for the version with Si3N4 substrate. These values are considerably lower than the 30 nH inductance of the three switching cells in parallel and in short-circuit of a commercial module (CCS020M12CM2 from Wolfspeed) made with the same dies. It is also lower than the inductance of two series connected TO-247 components, which is at least 28 nH since each terminal (drain or source) is estimated to have a stray inductance of 7 nH [45].

Since the goal of this article is to show how the proposed power module architecture can lead to lower losses and filtering needs than commercial modules, packaging issues will not be developed here. Power module's minimum temperature, maximum temperature, reliability, and lifetime are the subject of the next stage, which is a step to industrialization. However, these issues can be entirely overcome by power module's manufacturer, even with integrated capacitors. This is already the case of commercial modules (e.g., SiC power module 10-PC094PB017ME02-L620F36Y, from VINCOTECH) having integrated capacitors and operating temperature of −55 °C to 125 °C.

III. Characterization of Fast Switches

Measuring switching losses in fast power transistors such as SiC MOSFET and GaN Hugh electron mobility transistor (HEMT) can be very tricky and classical measurement methods may not be accurate enough [46]. For that reason, we have used the modified opposition method (MOM) [33], [45] to characterize switching energies of the designed power module as well as of a commercial power modules and discrete components.

In this method, four identical devices are used in a full-bridge configuration and an inductor is connected between the middle points of both half bridges, as shown in Fig. 10.

In Mode 1, converter is operated imposing 0.5 duty cycle (α) in both legs and phase shifting (ϕ) switching signals. Like this, trapezoidal current flows through the inductor and turn-OFF energies can be calculated from the measured power at the input of the converter, as explained in [33] and [46].

In Mode 2, phase shift between switching signals of both legs is zero, but their duty cycles are slightly different. Thus, dc current will flow through the inductor and the sum of turn-ON

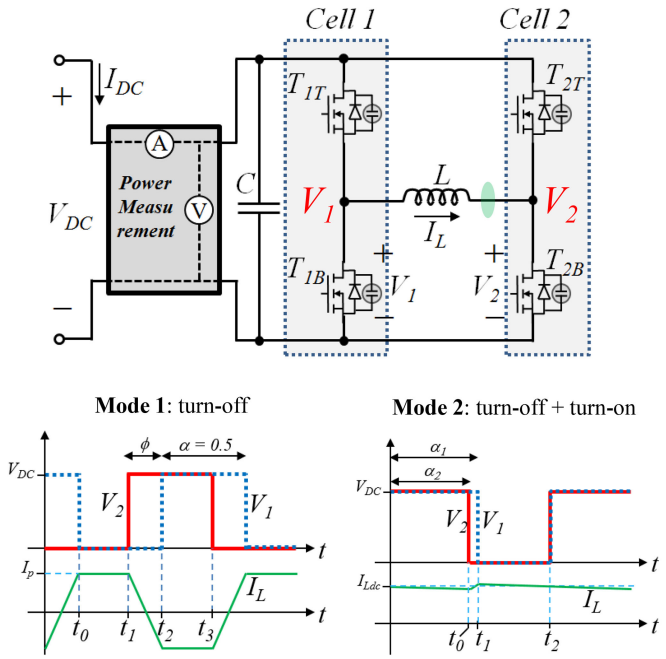


Fig. 10. Electrical circuit of the MOM to accurately measure switching energy of fast transistors. Bottom figures show voltage and current waveforms of the two modes the converter is operated in order to separately measure turn-ON and turn-OFF energies.

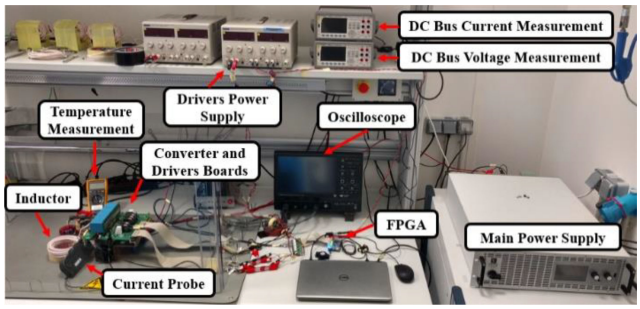


Fig. 11. Test bench to measure switching losses of fast transistors using the MOM.

and turn-OFF energies can be calculated. Since turn-OFF energy is calculated in Mode 1, turn-ON energy is calculated in Mode 2.

Using the MOM and the developed test bench shown in Fig. 11, switching energies can be measured for different parameters, such as gate resistance (R_G), gate-source voltage level (V_{GS}), switched voltage (V_{DS}) and current (I_{DS}), deadtime (D_T), and junction temperature (T_j). Variation of energy with all these parameters cannot be found in components datasheet.

A. Switching Energies of Developed Low-Inductance SiC Module

MOM characterization was applied to the first version of the designed low-inductance SiC power module ($L_p = 20$ nH) as well as to some other SiC components for comparison. Characterization of all components was performed for the same conditions, which is $R_G = 10\ \Omega$, $V_{GS} = 20$ V/−5V, $V_{DS} =$

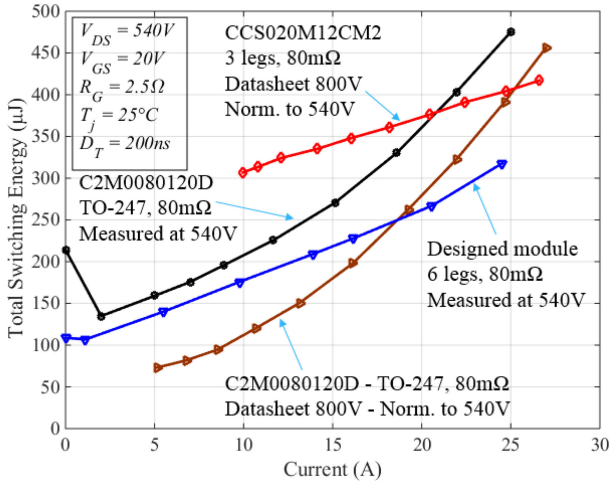


Fig. 12. Total switching energy ($E_{\rm on} + E_{\rm off}$) obtained from measurement and datasheet for different SiC devices using the same 1200 V/80 mΩ SiC MOSFET die.

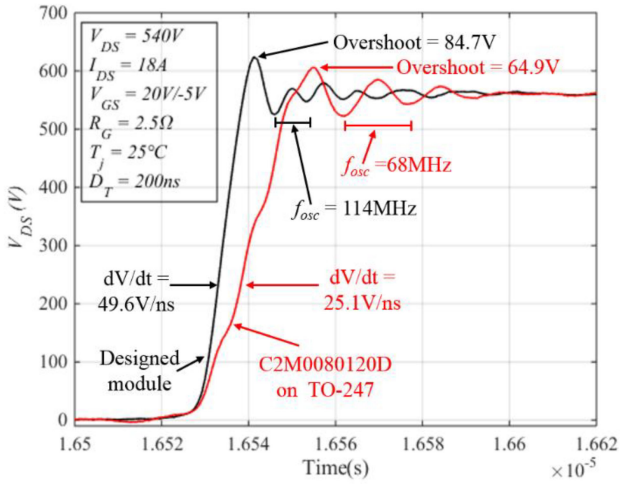


Fig. 13. Turn-OFF voltage waveform from the designed module and from the discrete component using the same 1200 V/80 mΩ SiC MOSFET die.

540 V, $D_T = 200$ ns, and T_j around 25 °C. Switched current I_{DS} is variable.

The first graph, shown in Fig. 12, compares total switching energy in a switching period ($E_{\rm on} + E_{\rm off}$) measured for the designed power module and for device C2M0080120D, which has exactly the same die of the designed power module but which is in a TO-247 packaging. We have added to this figure the curve of total energy which can be calculated using the datasheet information for the discrete device and also for one Wolfspeed six-pack power module made with the same 80 mΩ die and Schottky diode (reference CCS020M12CM2). They both were characterized by the manufacturer for the same conditions of our characterization, but for $V_{DS} = 800$ V, and using the double pulse method with a Schottky diode. We normalize the energies to 540 V, by the method shown in Session II.

Note in Fig. 12 that the experimental curve and the calculated one from datasheet for the discrete device C2M0080120D are very different. This is due to two reasons: Double pulse method used by manufacturers is less precise than the MOM used here; manufactures use a Schottky diode in the double-pulse method, which means that no reverse recovery of the MOSFET'S body diode is measured during turn-ON. This reverse recovery energy cannot be calculated from manufacturers datasheet.

Note also from the measured curves that the designed module has significant lower switching energy than the discrete component, for any current. At relative high current, the energy difference is high (about 1/3 lower at 25 A) due to the fact that the designed power module has lower parasitic inductances.

At zero current, which corresponds to the losses and energy measured when no current flows through the inductor (both legs have the same duty cycle and phase shift), the designed module has almost half the energy of the discrete component. It indicates that discrete component has twice higher parasitic capacitance (especially common mode capacitance at the converter) than the designed module although they are composed by the same 1200 V/80 mΩ die.

Higher parasitic capacitance and inductance of the discrete component in the full-bridge converter are confirmed by the switching time and ringing of the components when they are turned OFF, as shown in Fig. 13. During turn-OFF, the voltage rise on the component mainly depends on the switched current, which charges the parasitic capacitance C_{oss} (and also the common mode parasitic capacitances) of the transistor that is turning OFF.

As can be seen in Fig. 13, the switching speed of the designed module is about twice higher than that of the discrete component, for the same switched current (18 A), which indicates that the designed module has about half the parasitic capacitance of the discrete device (the parasitic inductance does not significantly change the switching speed at these conditions).

Although the switching speed is twice higher in the designed module, its corresponding overshoot (84.7 V) is slightly higher when compared to that corresponding to the discrete component (64.9 V). It indicates lower parasitic inductance and capacitance of the designed module.

Fig. 13 also shows that ringing after commutation has frequencies of 68 MHz and 114MHz for the designed module and discrete component, respectively. Since this frequency corresponds, in a first simple approach, to the resonance of the parasitic capacitances (C_p) and the total parasitic inductance (L_p), it means that the product $L_p \cdot C_p$ corresponding to the designed module is (114 MHz/68 MHz)^2 = 2.8 times higher than that corresponding to the discrete component. Thus, if we consider that the designed module has half the parasitic capacitance (as shown before), this means that it has also 1.4 times lower parasitic inductance. This value is exactly the ratio between the minimal value of parasitic inductance of a power loop with discrete components (28 nH) and the value related to the designed power module (20 nH).

B. Comparison With Commercial Module for Inverter Application

In order to verify if the designed multilevel power module would be a better option than a high-performance commercial

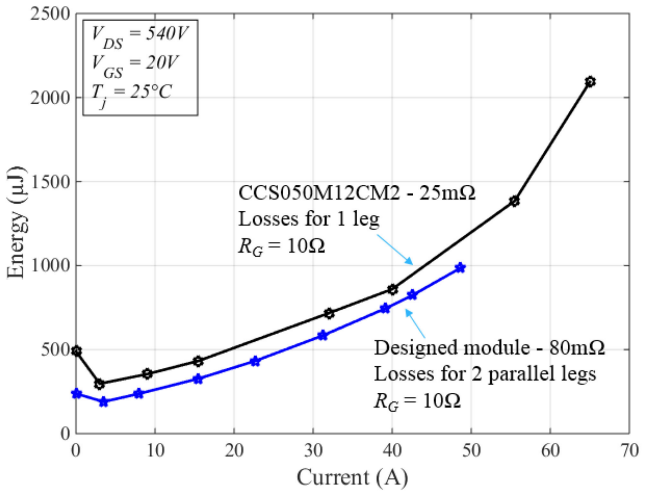


Fig. 14. Measured total switching energy of developed SiC multilevel module and a commercial high performance SiC module suitable to the same application (540 V/15 kVA inverter).

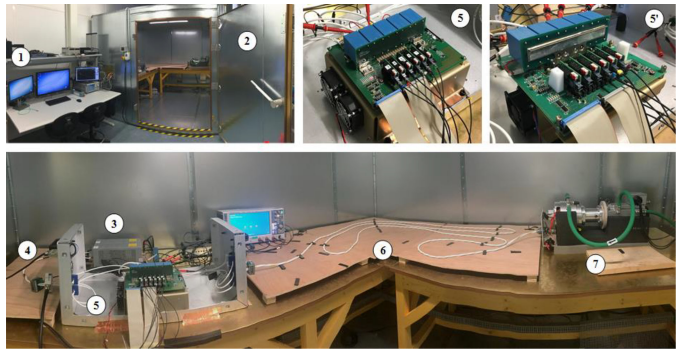


Fig. 15. Experimental setup in DO-160 normative test conditions. (1) Bench control center. (2) Faraday cage. (3) LISN. (4) Dc cable. (5) Commercial module SiC inverter (5') designed module SiC inverter. (6) Ac cable. (7) Motor generator bench.

power module suitable for 15 kVA applications, we have also characterized the six-pack SiC module CCS050M12CM2 (from Wolfspeed) having one 1200 V/25 mΩ die in parallel with Schottky diode for each switch inside the module. It was characterized with the same conditions as the characterization for the designed module (and shown above), except for the gate resistance R_G which is now equal to 10 Ω for both modules.

In order to compare the performance of both solutions, one should note that commercial module CCS050M12CM2 has three half bridges and would be used connected to a motor as in a typical power drive system as shown in Fig. 1. Thus, the load current flows through one bridge leg of the commercial power module.

However, the designed power module is to be used in a multilevel power drive system as shown in Fig. 3. Thus, the load current flows through two bridge legs of this designed module.

Consequently, for a fair comparison of performance of both modules, the measured switching energy curves for the designed module corresponds to the total energy lost in a switching period in both paralleled switching cells, when half of the output current flows through each switching cell.

Characterization curves of total energy ($E_{\text{on}} + E_{\text{off}}$) are shown in Fig. 14. Note that switching energies using the designed module is about 200 µJ lower than that of the commercial module for many different switched currents. At zero current and at 50 A, it corresponds respectively to 60% and 17% lower switching losses.

Measurements also show that, at these currents, the commercial module presents overshoot after a turn-ON of respectively 40 V (and $dV/dt = 28$ V/ns) and 90 V (and $dV/dt = 33$ V/ns), while the designed module presents an overshoot of 30 V (and $dV/dt = 36$ V/ns) and 18 V (and $dV/dt = 33$ V/ns).

These results confirm that the designed low inductance power module presents lower switching losses than commercial modules or discrete components although no Schottky diode is used. Also, since it will be used in a multilevel converter, the dV/dt and overshoot levels seen by cable and load are much lower than that of a commercial module inserted in a three-phase converter.

IV. Reduction of Common Mode Conducted Electromagnetic Emission

In order to show the reduction on the common mode conducted electromagnetic emissions, the considered system is a variable speed electrical power drive system, as shown in Fig. 1. It is composed of two line impedance stabilization networks (LISN), a three-phase SiC MOSFET inverter, an aeronautical permanent magnet synchronous motor, and two aeronautical cables (AWG eight copper strands, insulation poly tetra fluoro ethylene (PTFE) and polyimide tapes): one links up the LISN and the inverter (two conductors nonshielded, one meter length) and another connects the inverter to the motor (three conductors, two meter length). The electromechanical drive is situated on a 6 m^2 copper plane, excluding a loaded induction generator used as the load of the system placed over insulation foams to insulate them from the ground. The complete system is placed in a Faraday cage, as shown in Fig. 15.

Although the SiC power module was designed for a six-phase converter or a double three-phase converter, only three switching legs are used in order to compare with a regular three-phase converter with a SiC power module from the market. The converter power is therefore limited to 7.5 kW.

Previous works have already considered the integration of passive components in power electronics and on the integration of capacitors in the power module [44]. Discrete passive filters possess limited attenuation at high frequency (>10 MHz) due to intrinsic noise components. The purpose of integrating capacitors into the module is not to replace passive filtering, but to allow the constraint to be distributed. This solution is particularly interesting for counteracting the negative effects of SiC occurring at identified high frequencies [47].

The details of the electromechanical chains tested are described in Table I. Input and output filters are not considered.

Results of the measured input and output common mode current spectra are illustrated for two configurations of the power drive in Figs. 16 and 17. First, as shown in Fig. 16(a), when the

TABLE I
CONFIGURATION OF THE TESTED ELECTROMECHANICAL CHAINS

Parameters	Case 1	Case 2	Case 3	Case 4
Module	Commercial		Designed	
PWM Method	Sinusoidal PWM			
Gate resistor	10 Ω			
Drain-Source Voltage	20 V			
AC Cable length	2 m			
AC Cable shield	NO	YES	NO	YES
Motor speed	4160 rpm			
Motor torque	9 N.m			

Sinusoidal PWM (SPWM).

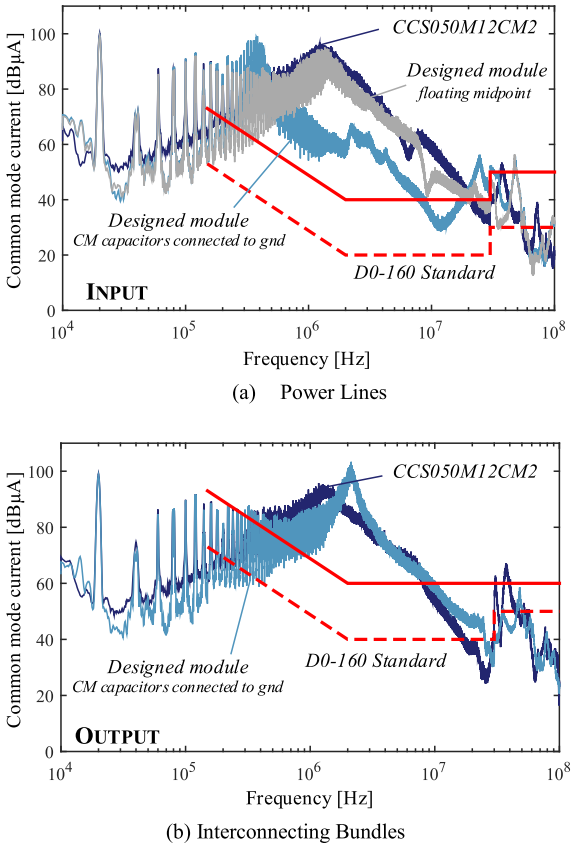


Fig. 16. Common mode currents for cases #1 and #3. (a) Power lines. (b) Interconnecting bundles.

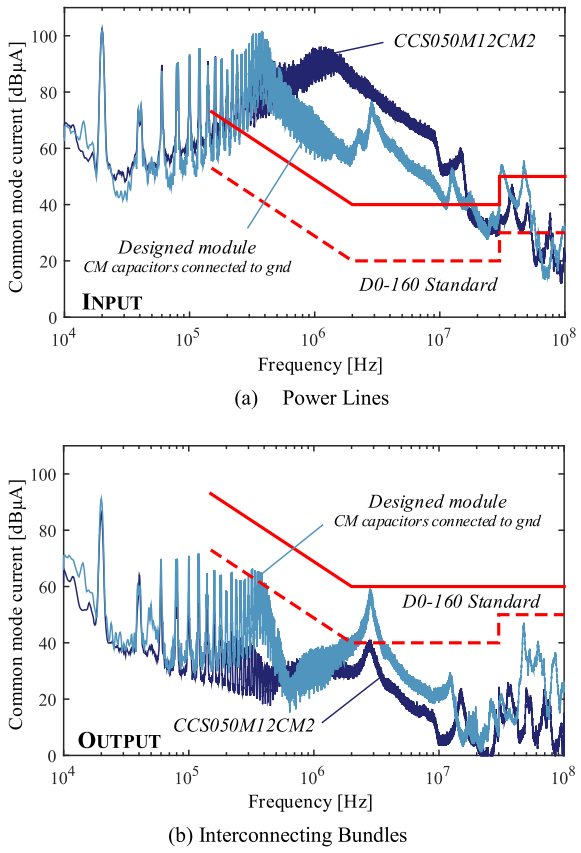


Fig. 17. Common mode currents for the cases #2 and #4. (a) Power lines. (b) Interconnecting bundles.

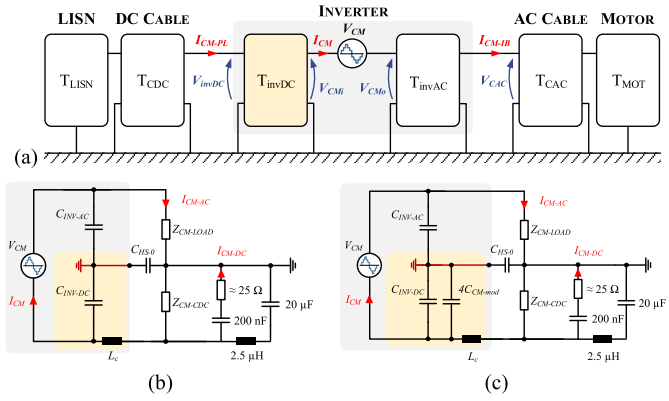


Fig. 18. (a) CM equivalent circuit as a chain of two-port networks. (b) CM equivalent circuits of the commercial. (c) Proposed drives.

midpoint of common mode capacitors of the designed module is not connected to the ground, the total measured conducted emissions are like that of the commercial module.

The integration of common mode capacitors in the module allows the creation of a preferred common mode loop, as shown in Fig. 18.

The integrated common mode capacitors provide a significant gain of attenuation on the common mode currents, which can be expressed by

$$A_{CM} = \frac{1}{1 - (4 \cdot C_{CM-\mathrm{mod}} + C_{INV-\mathrm{dc}}) \cdot L_c \cdot w^2}. \quad (5)$$

Between 500 kHz and 20 MHz, a reduction in the amplitude of the harmonics is observed thanks to the inductor-capacitor (LC) filter composed of the stray inductances and integrated capacitors. Indeed, the cut off frequency of the *LC* filter is equal to

$$f_{cut} \approx \frac{1}{2\pi\sqrt{L_c \cdot 4 \cdot C_{CM-\mathrm{mod}}}} \quad (6)$$

where the stray inductances resulting from the presence of the power leads and connections are modeled by the inductance L_c and $C_{CM\text{-mod}}$ are the integrated capacitors equal to 22 nF each.

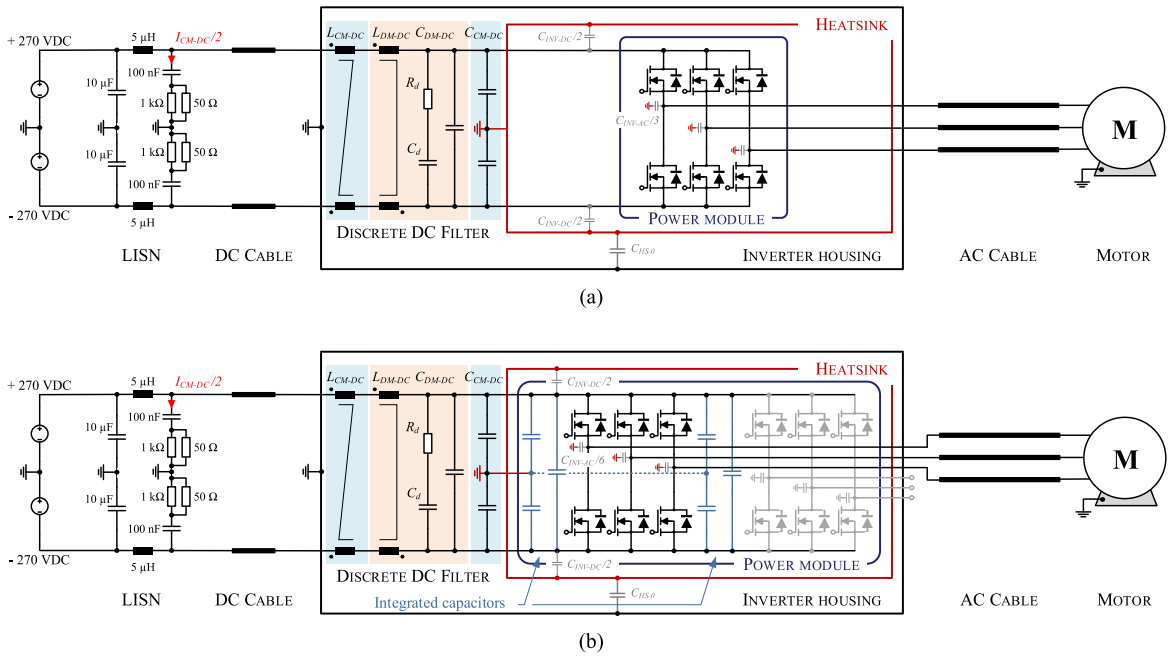


Fig. 19. Electrical circuits of the drives. (a) Commercial module. (b) Designed module.

A gain of around 30 dBμA is found at the maximum amplitude harmonic of the inverter case #2, the line from which the filtering was sized. Finally, the addition of input common mode filter capacitors changes the amplitude of the common mode currents measured at the output because the equivalent input common mode impedance is changed.

The discrete filter needed at the input is naturally different because the cutoff frequency is no longer the same. The sizing of the input filter with the inverter case #3 is carried out with the same methodology as that explained in [29]. The differential-mode filter is sized to fulfill Airbus power quality standard and the common mode filter to fulfill RTCA DO-160G category L, M, and H standard.

To comply with power quality and stability dc network requirements, a single stage with a parallel branch formed by R_d C_d to achieve damping is used for a differential-mode dc filter. A multistage EMI filter usually provides a bigger attenuation, thus, a higher cutoff frequency and could lead to a lighter filter than a single-stage filter [48], [49]. For this study, a single stage for both differential and common filters is chosen for design simplicity, since the goal here is to show that the designed module has a better EMI performance. The input common and differential-mode filters are shown in Fig. 19 and the components values are listed in Tables II and III. The technical specifications for the manufacturing are also listed. Those specifications allow to calculate total filtering mass between the solutions with and without integrated capacitors in the power module.

The mass of the filter is reduced by 42.5%. This gain is mainly explained by the fact that the filter has a greater equivalent common mode capacitance.

When we compare this solution to filtering inverter case #2 to common mode having the same capacitance (filters parameters listed in Table IV), it still gets a reduction of the total dc filter mass by 24%. As shown in Fig. 20, a gain in mass compared to the previous sizing is observed. This mass balance therefore allows us to illustrate the great interest of the integrated passive components in the developed power module in order to reduce

TABLE II
INPUT COMMON AND DIFFERENTIAL-MODE FILTER SPECIFICATIONS FOR THE COMMERCIAL MODULE INVERTER. TOTAL MASS = 808 G

Components	Value	Specifications
DM Inductance ($L_{DM\text{-}DC}$)	75.7 µH	Tore Magnetics High Flux 58585 AWG 20 (7 wires) - 2×15 turns
DM Capacitor ($C_{DM\text{-}DC}$)	40 µF	EPCOS B32776G0206 20 µF – 2 mounted in parallel
Damping resistor (R_d)	4.61 Ω	CMS resistor – 4.7Ω / 2W
Damping capacitor (C_d)	24 µF	EPCOS B3277D8126K000 12 µF – 2 mounted in parallel
CM Inductance ($L_{CM\text{-}DC}$)	13 mH	Tore VAC T60006-L2090-W518 AWG 12 – 2×14 turns
CM Capacitor ($C_{CM\text{-}DC}$)	47 nF	EPCOS B32682A6473K000

TABLE III
INPUT COMMON AND DIFFERENTIAL-MODE FILTER SPECIFICATIONS FOR THE DESIGNED INVERTER. TOTAL MASS = 465 G

Components	Value	Specifications
DM Inductance ($L_{DM\text{-}DC}$)	64.7 µH	Tore Magnetics High Flux 77586 AWG 20 (6 wires) - 2×21 turns
DM Capacitor ($C_{DM\text{-}DC}$)	40 µF	EPCOS B32776G0206 20 µF – 2 mounted in parallel
Damping resistor (R_d)	4.61 Ω	CMS resistor – 4.7 Ω / 2 W
Damping capacitor (C_d)	24 µF	EPCOS B3277D8126K000 12 µF – 2 mounted in parallel
CM Inductance ($L_{CM\text{-}DC}$)	4.8 mH	VAC – T60006 – L2045 – V102 AWG 12 - 2×8 turns
CM Capacitor ($C_{CM\text{-}DC}$)	47 nF	EPCOS B32682A6473K000

TABLE IV
INPUT COMMON AND DIFFERENTIAL-MODE FILTER SPECIFICATIONS FOR THE COMMERCIAL MODULE INVERTER WITH EQUAL COMMON MODE CAPACITANCE. TOTAL MASS = 609 G

Components	Value	Specifications
DM Inductance ($L_{DM\text{-}DC}$)	50.7 µH	Tore Magnetics High Flux 58585 AWG 20 (7 wires) - 2×13 turns
DM Capacitor ($C_{DM\text{-}DC}$)	40 µF	EPCOS B32776G0206 20 µF – 2 mounted in parallel
Damping resistor (R_d)	4.61 Ω	CMS resistor – 4.7 Ω / 2 W
Damping capacitor (C_d)	24 µF	EPCOS B3277D8126K000 12 µF – 2 mounted in parallel
CM Inductance ($L_{CM\text{-}DC}$)	6.7 mH	VAC – T60006 – L2063 – W517 AWG 12 - 2×12 turns
CM Capacitor ($C_{CM\text{-}DC}$)	91 nF	EPCOS B32682A6473K000 47 µF - 2 mounted in parallel

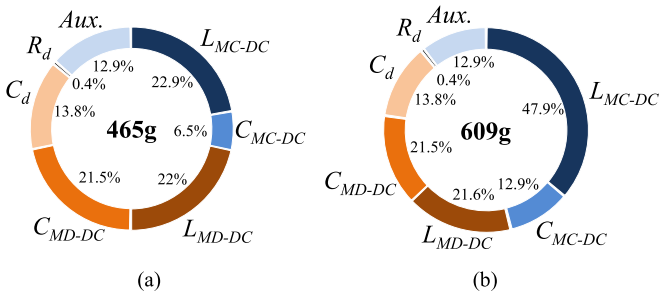


Fig. 20. (a) Mass distribution of the dc filter components. (b) Without integrated common mode capacitors in the power module.

common mode electromagnetic emissions. Note that reduction on common and differential-mode filters due to integration of passive components inside the power module may be higher or lower depending on the system impedance, standards to cope with, and filtering solution such as two-stage topologies instead of a single-stage one.

According to [50], fuel cost per weight unit in 2007, in the lifetime of an aircraft, was in the range of 1500 €/kg to 2000 €/kg. It means that the filter weight reduction by the integration of passive components which was estimated to 0.144 kg in the reference application (refer to Fig. 20), would save not only some euros on the filter fabrication but also around 288 euros on fuel in the lifetime of an aircraft. This cost saving is certainly much higher than the increase on price of producing such a specific power module for a 15 kVA application.

V. CONCLUSION

Power converter for aircrafts requires not only high switching frequency in some applications, but also low losses and high power density. For that reason, SiC MOSFET are very good candidates to be used in the next generation of more electrical aircrafts.

We have developed a SiC power module suitable to be used in a parallel multilevel inverter for a 540 V/15 kVA three-phase power drive system. These types of converters have the advantage of having low *dV/dt*, overshoot and voltage steps in the output voltage, which reduces EMI and partial discharge issues in a power drive system.

The developed power module has six switching cells composed of 1200 V/80 mΩ SiC MOSFETs. It was designed with integrated common mode capacitors to reduce EMI issues. Also, differential-mode capacitors were integrated in order to reduce power-loop parasitic inductance. Two different versions of the power module were designed and had 20 and 16 nH of power-loop parasitic inductance.

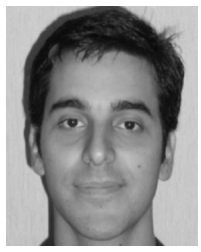
Switching energy measurements were applied to this module as well to discrete components having the same dies and also to a commercial SiC power module. Results show that the developed power module has lower switching energy ($E_{\text{on}} + E_{\text{off}}$) and lower overshoot for the same *dV/dt*. This overshoot and *dV/dt* is even lower when inserting this power module into a multilevel system, and consequently, filtering needs are significantly reduced.

Normative electromagnetic tests were performed in order to evaluate the gain on common mode conducted emissions. Results show that the designed power module leads to a lower common mode currents level, which may reduce around 24% the mass of common mode filtering when compared with filters designed for a converter with a SiC module from the market. Indeed, since integrated capacitors and parasitic loop inductance provide a high cutoff frequency filter, the needed input filter has reduced weight.

REFERENCES

[1] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 1, pp. 54–64, Jun. 2015.
[2] R. T. Naayagi, "A review of more electric aircraft technology," in *Proc. Int. Conf. Energy Efficient Technol. Sustain.*, Apr. 2013, pp. 750–753.
[3] K. Ni *et al.*, "Electrical and electronic technologies in more-electric aircraft: A review," *IEEE Access*, vol. 7, pp. 76145–76166, 2019.
[4] B. Revol *et al.*, "Overview and new trends in technology bricks for reliability enhancement in future wide band gap power converters for more electrical aircraft (MEA) and More Electrical Propulsion (MEP) systems," in *Proc. IEEE45th Annu. Conf Ind. Electron. Soc.*, Lisbon, Portugal, 2019, pp. 7128–7134.
[5] Q. Xu, Y. Xu, P. Tu, T. Zhao, and P. Wang, "Systematic reliability modeling and evaluation for on-board power systems of more electric aircrafts," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 3264–3273, Jul. 2019.
[6] K. C. Reinhardt and M. A. Marciniak, "Wide-bandgap power electronics for the more electric aircraft," in *Proc. Energy Convers. Eng. Conf.*, Aug. 1996, pp. 127–132.
[7] S. Qin, Y. Lei, Z. Ye, D. Chou, and R. C. N. Pilawa-Podgurski, "A high-power-density power factor correction front end based on seven-level flying capacitor multilevel converter," *IEEE J. Emerg. Sel.Topics Power Electron.*, vol. 7, no. 3, pp. 1883–1898, Sep. 2019.
[8] J. Azurza Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 50–61, 2019.
[9] K. Shenai, "High-density power conversion and wide-bandgap semiconductor power electronics switching devices," *Proc. IEEE*, vol. 107, no. 12, pp. 2308–2326, Dec. 2019.
[10] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si - Evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.
[11] R. Wang *et al.*, "A high-temperature SiC three-phase ac-dc converter design for >100 °C ambient temperature," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 555–572, Jan. 2013.
[12] N. Tega, S. Sato, and A. Shima, "Comparison of extremely high-temperature characteristics of planar and three- dimensional SiC MOSFETs," *IEEE Electron. Device Lett.*, vol. 40, no. 9, pp. 1382–1384, Sep. 2019.

[13] K. Saito *et al.*, "High-temperature cycle durability of superplastic Al–Zn eutectoid solder joints with stress relaxation characteristics for SiC power semiconductor devices," *IEEE Electron. Device Lett.*, vol. 40, no. 2, pp. 303–306, Feb. 2019.
[14] T. Meynard, B. Cougo, and J. Brandelero, "Design of differential mode filters for two-level and multicell converters," in *Proc. IEEE 11th Int. Workshop Electron., Control, Meas., Signals Appl. Mechatronics*, 2013, pp. 1–6.
[15] A. Charalambous, X. Yuan, and N. McNeill, "High-frequency EMI attenuation at source with the auxiliary commutated pole inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5660–5676, Jul. 2018.
[16] B. Cougo, V. Dos Santos, A. Hilal, and D.-H. Tran, "Trade-off between losses and EMI issues in three-phase SiC inverters for more electrical aircrafts," in *Proc. MEA More Elect. Aircraft*, Bordeaux, France. Feb. 2017, pp. 1–4.
[17] J. Wang, X. Liu, Y. Xun, and S. Yu, "Common mode noise reduction of three-level active neutral point clamped inverters with uncertain parasitic capacitance of photovoltaic panels," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6974–6988, Jul. 2020.
[18] B. Taghia, B. Cougo, H. Piquet, D. Malec, A. Belinger, and J.-P. Carayon, "Overvoltage at motor terminals in Sic-based PWM drives," *Math. Comput. Simul.*, vol. 158, pp. 264–280, 2019.
[19] S. De Caro *et al.*, "Motor overvoltage mitigation on SiC MOSFET drives exploiting an open-end winding configuration," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11128–11138, Nov. 2019.
[20] H. Lu, F. Zhu, Q. Liu, X. Li, Y. Tang, and R. Qiu, "Suppression of cable overvoltage in a high-speed electric multiple units system," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 2, pp. 361–371, Apr. 2019.
[21] R. Leuzzi, V. G. Monopoli, F. Cupertino, and P. Zanchetta, "Comparison of two possible solution for reducing over-voltages at the motor terminals in high-speed AC Drives," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, Genova, Italy, 2019, pp. P.1–P.10.
[22] B. Cogo and M. Wu, "Module electronique de puissance compact," French Patent, FR3047141 INPI, 2016.
[23] B. Cougo, H. Sathler, and R. Riva, "Switching characteristics of low inductance SiC module with integrated capacitors for aircraft applications," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, Stuttgart, Germany, 2018, pp. 1–8.
[24] S. L. Capitaneanu, "Optimisation de la fonction MLI d'un onduleur de tension deux-niveaux," Doctoral thesis, Institut Nat. Polytechnique De Toulouse, Toulouse, France, 2002.
[25] B. Cougo, D.-H. Tran, G. Segond, and A. Hilal, "Influence of PWM methods in semiconductor losses of 15kVA three-phase SiC inverter for aircraft applications," in *Proc. EPE Conf.*, Varsow, Poland, Sep. 2017, pp. 1–10.
[26] Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.
[27] D. Colin and N. Rouger, "High speed optical gate driver for wide band gap power transistors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.
[28] P. Bau, M. Cousineau, B. Cougo, F. Richardeau, and N. Rouger, "CMOS active gate driver for closed-loop dv/dt control of GaN transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13322–13332, Dec. 2020.
[29] V. Dos Santos, "Modélisation des émissions conduites de mode commun d'une chaîne électromécanique. Optimisation paramétrique de l'ensemble convertisseur filtres sous contraintes CEM," Ph.D. dissertation, Inst. Nat. Polytechnique de Toulouse, Toulouse, France, 2019.
[30] J. A. Anderson, L. Schrittwieser, M. Leibl, and J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2017, pp. 456–463.
[31] B. Cougo, D.-H. Tran, G. Segond, and A. Hilal, "Influence of PWM methods in semiconductor losses of 15kVA three-phase SiC inverter for aircraft applications," in *Proc. 18th Int. Conf. Electron. Power Eng.*, Warsaw, Poland, 2017, pp. 1–10.
[32] B. Cougo, L. M. F. Morais, G. Segond, R. Riva, and H. Tran-Duc, Influence of PWM methods in semiconductor losses and thermal cycling of 15kVA three-phase SiC inverter for aircraft applications, *Electronics*, vol. 9, 2020, Art. no. 620.
[33] H. Sathler and B. Cougo, "Improvement of the modified opposition method used for accurate switching energy estimation of WBG transistors," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Oct. 2017, pp. 308–315.
[34] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10-kV SiC mosfets and diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, Jun. 2018.
[35] M. Guacci *et al.*, "On the origin of the ¨Coss-losses in soft-switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019.
[36] M. Guacci *et al.*, "Experimental characterization of silicon and gallium nitride 200V power semiconductors for modular/multi-level converters using advanced measurement techniques," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2238–2254, Sep. 2020.
[37] B. Cougo, H. Schneider, and T. Meynard, "High current ripple for power density and efficiency improvement in wide Bandgap transistor-based buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4489–4504, Aug. 2015.
[38] R. Hou, J. Xu, and D. Chen, "A multivariable turn-On/Turn-Off switching loss scaling approach for high-voltage GaN HEMTs in a hard-switching half-bridge configuration," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Oct. 2017, pp. 171–176.
[39] A. Videt, P. Le Moigne, N. Idir, P. Baudesson, J. J. Franchaud, and J. Ecrabey, "Motor overvoltage limitation by means of a new EMI-reducing PWM strategy for three-level inverters," *IEEE Trans. Industry Appl.*, vol. 45, no. 5, pp. 1678–1687, Sept./Oct. 2009.
[40] E. Hoene, A. Ostmann, and C. Marczok, "Packaging very fast switching semiconductors," in *Proc. 8th Int. Conf. Integrated Power Electron. Syst.*, Nuremberg, Germany, 2014, pp. 1–7.
[41] F. Yang, Z. Wang, Z. Liang, and F. Wang, "Electrical performance advancement in SiC power module package design with kelvin drain connection and low parasitic inductance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 84–98, Mar. 2019.
[42] Z. Wang, F. Yang, S. L. Campbell, and M. Chinthavali, "Characterization of SiC Trench MOSFETs in a low-inductance power module package," *IEEE Trans. Industry Appl.*, vol. 55, no. 4, pp. 4157–4166, Jul./Aug. 2019.
[43] Y. Chang *et al.*, "Compact sandwiched press-pack SiC power module with low stray inductance and balanced thermal stress," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2237–2241, Mar. 2020.
[44] R. Robutel *et al.*, "Design and implementation of integrated common mode capacitors for SiC-JFET inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3625–3636, Jul. 2014.
[45] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Master thesis, Virginia Polytechnic Inst. State Univ., Blacksburg, VA, USA, 2009.
[46] B. Cougo, H. Schneider, and T. Meynard, "Accurate switching energy estimation of wide bandgap devices used in converters for aircraft applications," in *Proc. Eur. Conf. Power Electron. Appl.*, Lille, France, 2013, pp. 1–10.
[47] V. Dos Santos, B. Cougo, N. Roux, B. Sareni, B. Revol, and J. P. Carayon, "Trade-off between losses and EMI issues in three-phase SiC inverters for aircraft applications," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integrity*, Aug. 2017, pp. 55–60.
[48] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.
[49] G. Giglia *et al.*, "Automatic EMI filter design for power electronic converters oriented to high power density," *Electronics*, vol. 7, no. 1, pp. 1–16, 2018.
[50] M. Kaufmann, D. Zenkert, and P. Wennhage, "Integrated cost/weight optimization of aircraft structures," *Struct. Multidiscipl. Optimiz.*, vol. 41, pp. 325–334, Jul. 2010.



Bernardo Cougo received the B.S. and M.Sc. degrees in electrical engineering from the UFMG/ Brazil, Belo Horizonte, Brazil, in 2003 and 2005, respectively, and the Ph.D. degree from the Institut National Polytechnique, Toulouse, France, in 2010. He also studied at the University of Texas at Austin, Austin, TX, USA, in 2001.

He worked as a Postdoctoral Fellow with the PES Laboratory ETH-Zurich, in Switzerland, and also with LAAS and LAPLACE laboratories, Toulouse, France. He is currently working as a Power Electronics Expert with the French Institute of Research IRT Saint-Exupery, Toulouse, France. He has taught in different universities in Brazil and France, and is currently a Lecturer with ENSEEIHT/INP on subjects related to power electronics integration and wide bandgap semiconductors. He advises several Ph.D. students and postdoctoral fellows on research projects related to SiC and GaN power module and converters, mainly for aircraft applications. He has more than 60 publications since 2008 about power electronics integration and WBG semiconductor characterization and applications.

Hans Hoffmann Sathler was born in Governador Valadares, Brazil. in 1991. He received the bachelor's degree in electrical engineering from the Federal Center for Technological Education of Minas Gerais, Belo Horizonte, Brazil, in 2015, and the master's degree in power electronics from Federal University of Minas Gerais, Belo Horizonte, Brazil, in 2017. He is currently working toward the Ph.D. degree in power electronics with Paris-Saclay University, Saint-Aubin, France.

He is currently a Research Engineer with IRT Saint Exupery, Toulouse, France. His research interests include multilevel power converters, EMI filters design, and wide-bandgap semiconductors.

Raphael Riva received the Ph.D. degree from the Institut National des Sciences Appliquées de Lyon, Lyon, France, in 2014.

He was a Postdoctoral Research Fellow with the More Electrical Aircraft Research Team, Institute of Technology Antoine de Saint Exupéry, Toulouse, France, from 2014 to 2015. Since 2015, he has been a Research Engineer with the Institute of Technology Antoine de Saint Exupéry, Toulouse, working on power module packaging technologies.

Victor Dos Santos was born in Neuilly-Sur-Seine, France, in 1992. He received the Diploma in electrical engineering from the Institut National Polytechnique de Toulouse, ENSEEIHT, Toulouse, France, in 2015, and the Ph.D. degree from the Laboratoire Laplace, Toulouse, France, in 2018.

He was working with IRT Saint-Exupéry. His research was focused on the optimization of an electrical power drive system used for aircraft application under EMC constraints. Since 2019, he has been a Ph.D. Engineer and is currently working on propulsion control related topics with Safran Tech, Toulouse, France.

Nicolas Roux was born in France, in 1977. He received the bachelor's degree the École Normale Supérieure de Cachan, Cachan, France, in 2001, and the Ph.D. degree from the Institut National Polytechnique de Toulouse, Toulouse, France, in 2004.

He works in the Genesys Research Group with Laboratory of Plasma and Conversion of electrical Energy He also works on railway electrification systems. His research interests include new structures of power converters and stability, quality and management of small power network like airbone one.

Bruno Sareni was born in Bron, France, in 1972. He received the Ph.D. degree from the École Centrale de Lyon, Écully, France, in 1999.

He is currently a Professor in electrical engineering and control systems with the National Polytechnic Institute of Toulouse, Toulouse, France. He is also a Researcher with the Laboratory on Plasma and Conversion of Energy, Université de Toulouse, Toulouse, France. His research interests include integrated design approaches for electrical embedded systems or renewable energy systems.