# Analysis of a Hybrid Variable-Frequency-Duty-Cycle-Modulated Low-$Q$ $LLC$ Resonant Converter for Improving the Light-Load Efficiency for a Wide Input Voltage Range

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***Abstract*—Light load efficiency and output voltage regulation of a low-*Q* *LLC* resonant converter is a critical problem for wide input voltage and load range applications. Parasitic capacitances such as rectifier diode junction capacitance ($C_j$) degrade the soft switching performance. Compact size, high density, and high transformer turns-ratio requirements for microinverter applications add significant distributed capacitance ($C_d$) of the low-profile transformer, worsening the output regulation and zero-voltage-switching (ZVS) capability at light loads. Wide switching frequency requirement for regulation at light loads, which increases core losses and turn-OFF switching losses in power MOSFETs, further degrades the power conversion efficiency. The conventional phase-shift modulation causes a high circulating current and loss of ZVS at light loads. Therefore, a hybrid adjustable switching-frequency-duty-cycle modulation technique for improving the light load efficiency is proposed and analyzed for a full-bridge $LLC$ resonant converter. Accurate loss analysis for the proposed modulation scheme, including the effect of parasitic capacitances, is performed using time-domain equations. The proposed methodology precalculates the optimal duty cycle at light load conditions for the required input voltage range such that minimum power losses are incurred. Variation in switching frequency at the preselected duty-cycle value regulates the output voltage. ZVS over a wide range of operating conditions is observed. An experimental prototype for a 20–40 V input, 380-V/300-W output $LLC$ converter is tested for the validation of theoretical analysis.**

***Index Terms*—Circulating current, core loss, hybrid modulation, *LLC* resonant converter, switching loss, wide-input range, zero-voltage-switching (ZVS).**

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## I. Introduction

MICROINVERTER applications require efficient operation over a wide range of input voltage and output loading conditions. An $LLC$ resonant converter demonstrates excellent soft-switching characteristics for such applications [1]–[9]. Fixed-frequency pulsewidth-modulated (PWM) $LLC$ resonant converters, such as phase-shift modulation (PSM) [10]–[13], can achieve soft switching at nominal operating conditions without any additional circuitry [14]. However, for wide input voltage range applications, the conventional phase-shift technique loses ZVS of the leading leg at light load conditions due to capacitive loading. Operation at a higher switching frequency is required to maintain soft switching, which leads to increased magnetic core losses. Another disadvantage of the conventional phase-shift strategy at light loads is the flow of the circulating current in the primary resonant tank side when either both top or bottom power MOSFETs are ON (effective input voltage applied across the resonant tank is zero). High-frequency ringing in the primary-side resonant current is observed due to the resonance between $LLC$ resonant tank elements and the parasitic capacitance of output rectifier diodes and high-frequency transformer. This phenomenon further increases the circulating current at light loads, thereby, degrading the efficiency [15].

A variable frequency-modulated (FM) $LLC$ resonant converter requires a relatively high-quality factor ($Q > 0.5$) circuit design for the operation over a wide range of load and input voltage variations [16]–[18]. High-$Q$ tuned resonant components result in a bulky component size and increased magnetic losses [12]. It can achieve ZVS and voltage regulation for any wide-input voltage and load range but requires wide switching frequency operation, making it difficult to optimize the magnetics design and gate drive circuitry layout for entire line/load range specifications. Due to the wide switching frequency requirement, the FM *LLC* converter can generate a very wide range of harmonics, which generates high electromagnetic interference (EMI) issues. Compared to the constant-frequency PSM, FM *LLC* converters exhibit lower power efficiency levels.

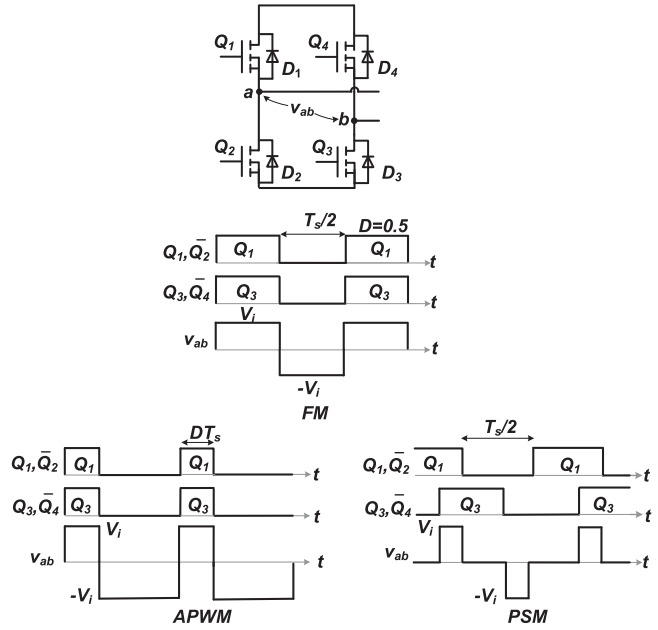



Fig. 1. Various modulation schemes for a full bridge switching network.

Due to the restriction on allowable frequency deviation, the FM-operated *LLC* converter has a narrow control range compared to PSM, which can be extended to include zero output [19], [20].

Burst-mode control schemes are popular for improving the extremely light load efficiency but suffer from filter design, noise problems, and startup response after the burst-mode cycle [21], [22]. Hybrid modulation techniques that consist of employing a variable frequency control up to a precalculated switching frequency and transitioning to the PWM-based duty-cycle control at the maximum switching frequency [23] or variable frequency-based phase-shift control [24], [25] have either been implemented with a high $Q$ circuit design or requires a wide switching frequency range. Fig. 1 shows the conventional modulation waveforms applicable to a full-bridge switching network. Apart from MOSFET turn-ON and turn-OFF switching losses, load-independent losses, such as core losses, dominate, thereby, degrading the efficiency.

Another critical issue that impacts the implemented modulation strategy's performance at light loads is the high-frequency transformer design. Low input voltage to high output voltage applications (such as photovoltaic (PV) microinverters) generally require a high turns-ratio low-profile transformer core for a high power density and dc bus voltage regulation. Due to an excellent magnetic coupling between the primary and secondary sides, low-profile cores exhibit low leakage inductance in exchange for higher capacitive coupling between the primary and secondary windings [26]. The high output voltage on the transformer secondary side is divided between windings. It leads to the existence of a distributed capacitance element from the secondary winding to ground, $C_d$, which becomes prominent at the high-frequency converter operation [27], [28]. Switching of secondary-side rectifier diodes causes current to charge/discharge these intrinsic capacitances, leading to interaction of $C_d$ with the diode junction capacitance, $C_j$ [29]–[31]. Such interaction further increases the peak magnitude of the oscillating current, which gets reflected to the primary side. These oscillations can lead to multiple zero crossings of the resonant current during light load conditions, which can either charge or discharge the output capacitance of MOSFET during the ZVS dead-time transition. Hence, true ZVS operation cannot be guaranteed under such circumstances.

This article proposes an adjustable duty-cycle-switching-frequency modulation technique that ensures ZVS and output voltage regulation for a wide input voltage range low-$Q$ *LLC* converter at light loading conditions [32]. The biggest disadvantage for a low-$Q$ tuned $LLC$ resonant circuit is difficulty in voltage regulation and loss of ZVS at light loads. The previous work solved these two critical issues and dealt with the analysis of an ideal low-$Q$ $LLC$ converter operating under the proposed modulation scheme. However, the effect of the presence of significant capacitance values of $C_d$ and $C_j$ for wide input voltage and load range applications was not considered in the analysis. Also, there was no quantitative basis for the selection of duty cycle, $D$, and normalized frequency of operation, $\omega$, which were chosen heuristically, based on the turn-OFF current trend of the leading leg. In this article, accurate loss analysis using a steady-state time-domain model of the proposed technique is performed to calculate and store optimal duty-ratio ($D$) values in a lookup table for minimum power loss at different light load conditions for the required input voltage range. Due to smooth, nonmonotonous gain characteristics of the proposed modulation strategy, voltage regulation can be performed by simply varying the switching frequency $\omega$, leading to optimal combinations of $\omega$ and $D$. Such an approach ensures a high efficiency at light load conditions for a wide range of operating conditions. An experimental prototype for a 20–40 V input, 380-V/300-W output $LLC$ converter is tested for the validation of theoretical analysis.

## II. Concept of the Proposed Modulation Scheme

The basic idea for using hybrid control can be understood easily by using the voltage gain equation for the $LLC$ converter obtained using fundamental harmonic approximation (FHA) under the following assumptions:

1) all MOSFET switches are ideal, ignoring the effect of the intrinsic resistors;
2) all the resonant variables can be regarded as sinewaves, ignoring the harmonics;
3) dead time between switches is neglected.

Fig. 2(a) shows a circuit diagram for a full-bridge $LLC$ resonant converter for PV microinverter applications. It is composed of primary MOSFET switches $Q_1$–$Q_4$, resonant inductor $L_s$, resonant capacitor $C_s$, magnetizing inductance $L_m$, transformer $T_1$ with turns ratio $n$ ($N_p : N_s$), diode rectifier $D_{o1}$–$D_{o4}$ with a junction capacitance $C_d$, filter output capacitor $C_o$, and output load $R_l$.

As shown in Fig. 2(b), the output gain equation given by (1) can be characterized by dividing the equivalent resistance $R_{\text{eq}}$ by total impedance of the resonant network, $Z_{\text{in}}$. Expression for $Z_{\text{in}}$ is given in (7). It can be observed that $Z_{\text{in}}$ increases with the increase in switching frequency, $\omega_s$, above the resonant

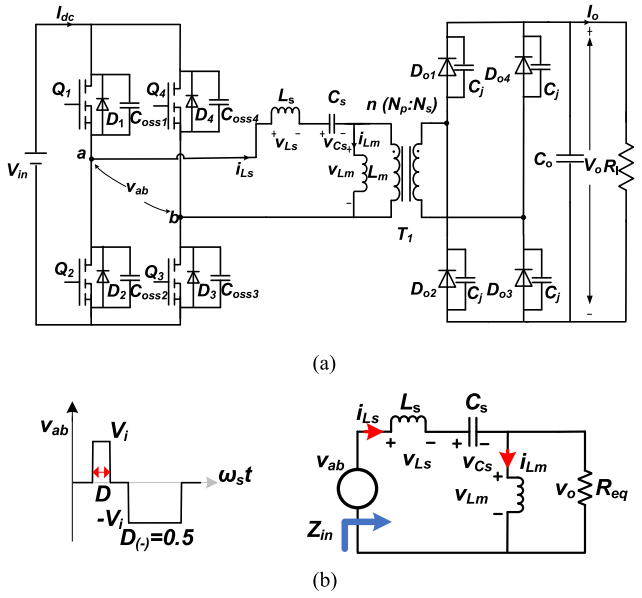



Fig. 2. (a) Full-bridge $LLC$ resonant converter with control structure. (b) Ideal FHA equivalent circuit.

frequency, $\omega_r$. Therefore, for the relative switching frequency, $\omega > 1$, the input impedance angle is directly proportional to $\omega$. Variable frequency control with duty cycle, $D = 0.5$, implies that the root-mean-square (rms) value of the input square wave voltage, $v_{ab}$ applied to the $LLC$ resonant tank is constant. Hence, $Z_{\text{in}}$ is increased with a corresponding reduction in load (i.e., $R_{\text{eq}}$ increases in value) to maintain the gain ratio relationship constant. It can be inferred that the input impedance of the $LLC$ resonant tank should be adjusted for fixed $D = 0.5$, depending on load variations such that the output voltage is held constant. However, since the duty-cycle controls the rms value of the square wave input voltage, $v_{ab}$, simultaneous variation of duty cycle and $\omega$ can be employed

$$G_{\text{FHA}} = \frac{1}{\sqrt{\left(1 + K - \frac{K}{\omega^2}\right)^2 + Q^2\left(\omega - \frac{1}{\omega}\right)^2}} \tag{1}$$

$$Q = \sqrt{\frac{L_s}{C_s}}/R_{\text{eq}} \quad \text{and} \quad K = \frac{L_m}{L_s} \tag{2}$$

$$R_{\text{eq}} = \frac{8n^2 R_l}{\pi^2} \tag{3}$$

$$n = N_p/N_s \tag{4}$$

$$\omega_r = 1/\sqrt{L_s C_s} \tag{5}$$

$$\omega = \frac{\omega_s}{\omega_r} \tag{6}$$

$$Z_{in} = j\omega_s L_s - \frac{j}{\omega_s C_s} + \frac{j\omega_s L_m \text{Req}}{j\omega_s L_m + \text{Req}}. \tag{7}$$

The proposed modulation technique uses the same concept. Using Fourier series, the fundamental harmonic component of the proposed modulation scheme can be expressed as

$$v_{ab_1} = \frac{V_i\,(1-2D)}{2} + \frac{2V_i}{\pi}\left[1 + \sin(\pi D)\right]\sin(\omega_s t)\,. \tag{8}$$

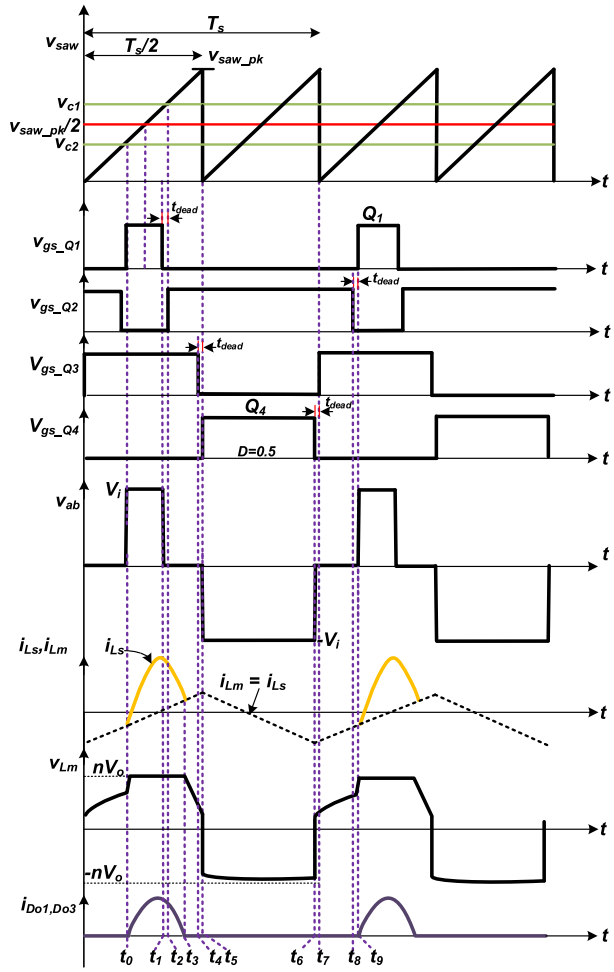


Fig. 3. Key waveforms at light load conditions for the proposed modulation technique.

Existence of even harmonics due to the asymmetrical nature of the $v_{ab}$ waveform leads to the presence of a dc component equal to $\frac{V_i(1-2D)}{2}$ for the duty-cycle range of 0–0.5. It can be inferred that the peak fundamental harmonic magnitude (and correspondingly the rms value) can be decreased by reducing the duty cycle as inferred from the relationship given in (8). Such variation reduces the maximum value of $\omega$ required for gain regulation during wide input voltage operating conditions. The extra degree of freedom allows the converter to be operated at lower switching frequencies while simultaneously varying the duty cycle. This feature is advantageous as narrow switching frequency variation simplifies the EMI filter design, magnetics selection, and gate drive circuitry requirements. Such hybrid control methodologies can ensure optimum efficiencies throughout the operating range rather than at a fixed switching frequency. The operational principles are described in the next section.

## III. Operational Principles

Key converter and control logic waveforms during light load conditions for the proposed modulation technique are shown in Fig. 3. The rising and falling edge of $Q_2$ gate pulse are symmetrically placed from the rising and falling edge of $Q_1$ gate

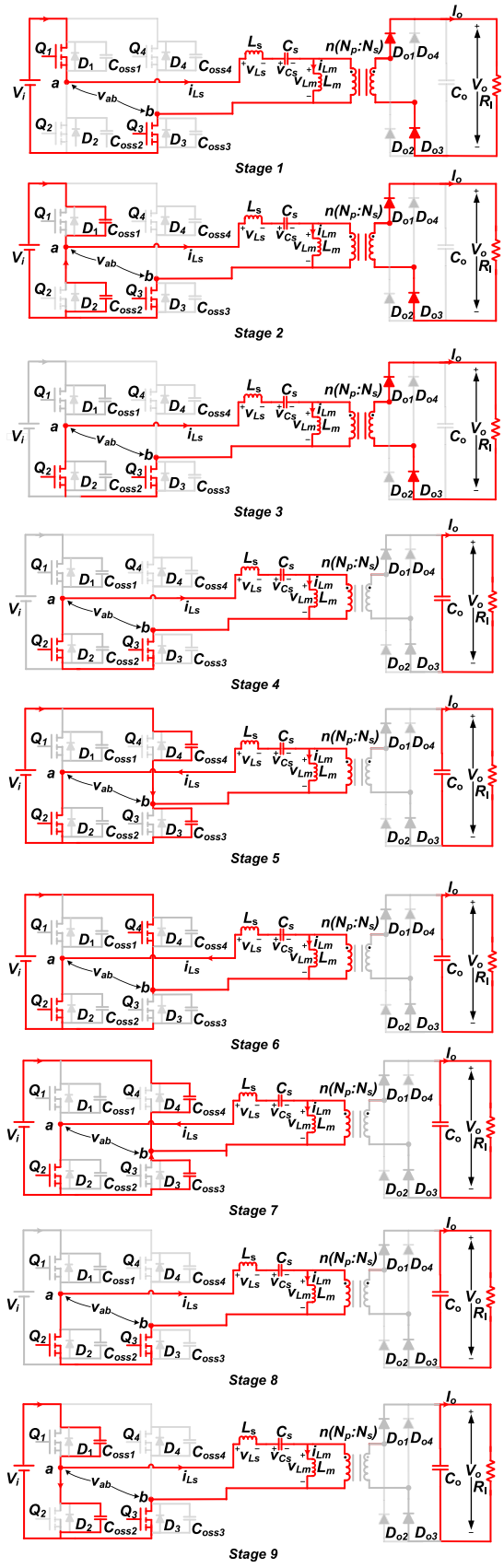



Fig. 4. Equivalent circuits during the proposed modulation operation.

pulse such that ZVS of $Q_1$ is achieved. $v_{c_1}$ and $v_{c_2}$ are the control signals generated by adding and subtracting one half of the calculated duty-cycle counter value to $v_{\text{saw\_}pk}/2$, which produces the symmetrical gate pulse for $Q_1$. The resulting bipolar wave, $v_{ab}$ is more symmetrical than the conventional asymmetrical PWM (APWM), which would reduce peak stresses on circuit components compared to an asymmetrical modulation waveform. Resonant capacitor, $C_s$, acts as a dc-blocking capacitor and prevents the occurrence of dc bias in a high-frequency transformer. Following quantities are defined for analysis purposes:

$$Z_0 = \sqrt{\frac{L_s}{C_s}}; Z_1 = \sqrt{\frac{L_s + L_m}{C_s}};$$
$$\omega_r = \frac{1}{\sqrt{L_s C_s}}; \omega_{r_1} = \frac{1}{\sqrt{(L_s + L_m)\, C_s}}. \tag{9}$$

The following assumptions are made during analysis of steady-state behavior of the converter.

1) The semiconductor MOSFET switches along with the rectifier diodes and high-frequency transformer are ideal.
2) Rectifier junction and MOSFET capacitances are negligible.
3) The output filter capacitor is large enough to keep the output voltage constant.
4) Dead time between switches is assumed only for explaining the ZVS operation of the proposed modulation technique. State variable dynamics are assumed to be unaffected due to small dead-time duration compared to the switching cycle.

*1) Stage 1 [$t_0$–$t_1$]:* At $t_0$, $Q_1$ switch in the leading leg is turned ON under ZVS, while $Q_3$ was already conducting. The tank voltage, $v_{ab}$, becomes equal to the input voltage. The resonant tank current, $i_{Ls}$, starts flowing through the $LLC$ resonant tank during this power delivery period. Magnetizing inductor, $L_m$ is clamped to the reflected output voltage $+nV_o$. The output diode rectifiers $D_{o1}$ and $D_{o3}$ are turned ON and transfer power to the load. Fig. 4 shows the $LLC$ circuit during this stage of operation. This stage ends when $Q_1$ is turned OFF at $t = t_1$, which is dependent on the duty cycle

$$i_{Ls}(t) = i_{Ls}(t_0)\cos(\omega_r t) + \left[\frac{V_i - nV_o - v_{Cs}(t_0)}{Z_0}\right]\sin(\omega_r t)$$
$$i_{Lm}(t) = \frac{nV_o}{L_m}t + i_{Lm}(t_0)$$
$$v_{Cs}(t) = Z_0 i_{Ls}(t_0)\sin(\omega_r t) + v_{Cs}(t_0)\cos(\omega_r t) + [V_i - nV_o]\,[1 - \cos(\omega_r t)]\,. \tag{10}$$

*2) Stage 2 [$t_1$–$t_2$]:* $Q_1$is turned OFF at the beginning of this interval and the dead time $t_d$ starts. Large $Q_1$ turn-OFF current, $i_{Ls}(t_1)$ starts discharging $C_{oss2}$ and charges $C_{oss1}$ to $V_i$. Once $C_{oss2}$ is completely discharged to $V_i$, the body diode starts conducting and zero voltage turn-ON of $Q_1$ is achieved.

*3) Stage 3 [$t_2$–$t_3$]:* At time instant $t_2$, $Q_2$ is turned ON. Since the turn-OFF current of $Q_1$ was positive, the low-side switch $Q_2$ will turn ON with ZVS. The equivalent input tank voltage, $v_{ab}$ becomes zero and the magnetizing inductance $L_m$ is clamped with the reflected output voltage, $nV_o$, until the resonant tank

current, $i_{Ls}$, becomes equal to $i_{Lm}$ at $t = t_3$. Fig. 4 shows the equivalent $LLC$ circuit during stage 2

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_2)\cos\left[\omega_r(t-t_2)\right] \\ &\quad - \left[\frac{nV_o + v_{Cs}(t_2)}{Z_0}\right]\sin\left[\omega_r(t-t_2)\right] \\ i_{Lm}(t) &= \frac{nV_o}{L_m}t + i_{Lm}(t_2) \\ v_{Cs}(t) &= Z_0 i_{Ls}(t_2)\sin\left[\omega_r(t-t_2)\right] + v_{Cs}(t_2)\cos\left[\omega_r(t-t_2)\right] \\ &\quad - nV_o\left\{1-\cos\left[\omega_r(t-t_2)\right]\right\}. \end{aligned} \tag{11}$$

*4) Stage 4 [$t_3$–$t_4$]:* At $t = t_3$, $L_m$ starts resonating with $L_s$ and $C_s$ as there is no clamping on $L_m$ by the reflected voltage. The resulting dynamics can be expressed by the following tank current, $i_{Ls}$, and capacitor voltage, $v_{Cs}$, equations solved using the $LLC$ circuit shown in Fig. 4. This stage ends when the switch $Q_3$ of the lagging leg is turned OFF at $t = t_3$

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_3)\cos\left[\omega_{r_1}(t-t_3)\right] - \frac{v_{Cs}(t_3)}{Z_1}\sin\left[\omega_{r_1}(t-t_3)\right] \\ v_{Cs}(t) &= Z_1 i_{Ls}(t_3)\sin\left[\omega_{r_1}(t-t_3)\right] \\ &\quad + v_{Cs}(t_3)\cos\left[\omega_{r_1}(t-t_3)\right]. \end{aligned} \tag{12}$$

*5) Stage 5 [$t_4$–$t_5$]:* $Q_3$ is turned OFF at the beginning of this interval. During the dead-time interval, the turn-OFF current of $Q_3$ should be positive enough to completely discharge $C_{oss4}$ and charge $C_{oss3}$ to $V_i$. The antiparallel diode of $Q_4$ starts conducting, thereby, ensuring ZVS of $Q_4$, while $Q_4$ is turned ON with ZVS.

*6) Stage 6 [$t_5$–$t_6$]:* $Q_4$ is turned ON at $t = t_5$, while $Q_2$ is already conducting. $L_m$ is still resonating with series $L_s$ and $C_s$ and no energy transfer to the output takes place. This stage ends when $Q_4$ is turned OFF. The resultant $LLC$ circuit during this stage of operation is shown in Fig. 4

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_5)\cos(\omega_{r_1}(t-t_5)) \\ &\quad - \left[\frac{V_i + v_{Cs}(t_3)}{Z_1}\right]\sin(\omega_{r_1}(t-t_5)) \\ v_{Cs}(t) &= Z_1 i_{Ls}(t_5)\sin(\omega_{r_1}(t-t_5)) + v_{Cs}(t_5)\cos(\omega_{r_1}(t-t_5)) \\ &\quad - V_i\left[1-\cos(\omega_{r_1}(t-t_5))\right]. \end{aligned} \tag{13}$$

*7) Stage 7 [$t_6$–$t_7$]:* Similar to the stage 5 dead-time interval, $C_{oss3}$ starts discharging, whereas $C_{oss4}$ starts charging to $V_i$. $Q_3$ is turned ON with ZVS.

*8) Stage 8 [$t_7$–$t_8$]:* This period is similar to the stage 4 with MOSFETs $Q_2$ and $Q_3$ conducting. There is no transfer of energy to the output as $L_m$ is not clamped to $nV_o$. $L_m$ charges upto $+nV_o$ by the end of this interval

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_7)\cos\left[\omega_{r_1}(t-t_7)\right] - \frac{v_{Cs}(t_7)}{Z_1}\sin\left[\omega_{r_1}(t-t_7)\right] \\ v_{Cs}(t) &= Z_1 i_{Ls}(t_7)\sin\left[\omega_{r_1}(t-t_7)\right] \\ &\quad + v_{Cs}(t_7)\cos\left[\omega_{r_1}(t-t_7)\right]. \end{aligned} \tag{14}$$

*9) Stage 9 [$t_8$–$t_9$]:* $Q_2$ is turned OFF at $t = t_8$ with a low resonant current. The negative resonant current should be large enough to discharge the intrinsic capacitance of $Q_1$ to ensure antiparallel diode conduction prior to $Q_1$ turn-ON. Maximum dead-time duration is required for the transition between $Q_2$ turn-OFF and $Q_1$ turn-ON.

## IV. Analysis

The resulting transcendental equations in Section III can be solved by using any iterative numerical technique. Due to its simplicity and reliability, The Newton–Raphson technique was selected. Dead-time duration is neglected to simplify analysis, i.e., $t_2 \approx t_1$, $t_5 \approx t_4$, $t_6 \approx t_7$, and $t_8 \approx t_9$. The switching instants $t_1$, $t_4$, $t_6$, and $t_8$ are known time quantities that can be expressed relatively with respect to the previous time instant as

$$\begin{aligned} t_{1\_t_0} &= DT_s/2; t_{4\_t_3} = (1-D)T_s/4 - t_{3\_t_1} \\ t_{6\_t_5} &= T_s 2; t_{8\_t_7} = (1-D)T_s/4 \end{aligned} \tag{15}$$

where

$$t_{x\_t_y} = t_x - t_y. \tag{16}$$

For ease of understanding, it should be noted that any time instant expressed, hereafter, should be considered to be with respect to the previous time instant.

Time instant $t_1$ is the ON time of the switch $Q_1$. Time instant $t_3$ is the only unknown quantity that depends on the operating state of the $LLC$ resonant converter. It is necessary to eliminate all occurrences of $i_{Ls}$ and $v_{Cs}$ from the aforementioned equations to obtain a nonlinear equation in terms of $t_3$ and converter design parameters, $V_i$, $V_o$, $P_o$, $Z_0$, etc.

In steady-state operating conditions, the following conditions are valid for the proposed light load modulation technique:

$$\begin{aligned} i_{Ls}(t_0) &= i_{Lm}(t_0) = i_{Ls}(T_s) \\ v_{Cs}(t_0) &= v_{Cs}(T_s). \end{aligned} \tag{17}$$

Solving (17), the initial values of resonant capacitor voltage, $v_{Cs}(t_0)$, and resonant tank current $i_{Ls}(t_0)$ (at the bottom of this page) can be expressed in terms of design parameters $V_i$ and $V_o$ and variables $\alpha_1$ and $\beta_1$, which ultimately depends on the unknown time instant, $t_3$

$$v_{Cs}(t_0) = V_i - nV_o - \left(\alpha_1\left\{1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right\}/\beta_1\right). \tag{18}$$

It can be seen that both $v_{Cs}(t_0)$ and $i_{Ls}(t_0)$ depend on unknown time parameter $t_3$. Simplifying (18) and (19), shown at the bottom of the next page, such that $v_{Cs}(t_0)$ and $i_{Ls}(t_0)$ are eliminated leads to the formulation of function, $f_{\text{fixedgain}} = f(t_1+t_3) = 0$, which can be expressed as

$$f(t_1+t_3) = \alpha_1\beta_2 - \alpha_2\beta_1. \tag{20}$$

This function is valid for the constant output voltage, variable output power calculations. The output power expression has been derived as (21) shown at the bottom of the next page. $\alpha_1$, $\beta_1, \alpha_2$, and $\beta_2$ are defined in Appendix A. Using Newton–Raphson iterative method, $t_3$ is calculated by solving the following nonlinear equation for the $j$th iteration

$$t_{3_{[j+1]}} = t_{3_{[j]}} - \frac{f_{[j]}}{df_{[j]}}. \tag{22}$$

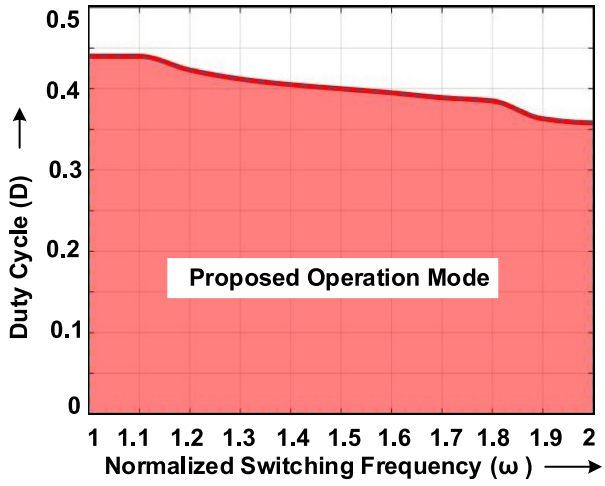



Fig. 5. Mode operation boundary for the proposed modulation technique operating at $K = 6$, $Q = 0.1$ $LLC$ converter.

Once the unknown time instant $t_3$ is calculated for a given operating condition, each time interval mode can be solved. Depending on the circuit design and converter operating condition, there is no power transfer to the secondary side during Stage 6, since $i_{Ls} = i_{Lm}$. Therefore, solving for the $i_{Ls} = i_{Lm}$ condition gives the boundary surface for the proposed mode, which has been shown in Fig. 5 for $K = 6$, $Q = 0.1$. Area lying above the boundary represents the mode of operation in which the power is transferred during the Stage 6, i.e., $i_{Ls} \neq i_{Lm}$. It is observed that as $Q$ increases, area under the $D$–$\omega$ curve decreases for the same $K$ value.

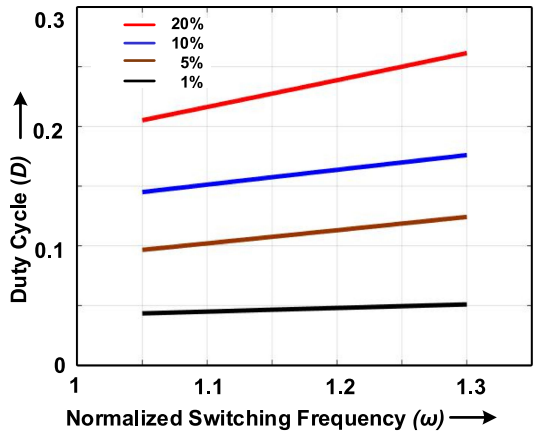
It should be noted that the present analysis and mode boundary conditions have been established for a fixed output voltage application with a varying output power. Similar analysis can be formulated for applications when the output power is fixed with a varying output voltage [12]. Appendix B contains these equations. The specifications of a full-bridge $LLC$ resonant converter developed for the dc–dc stage of microinverter application have been tabulated in Table I .

### A. Voltage Gain Characteristics

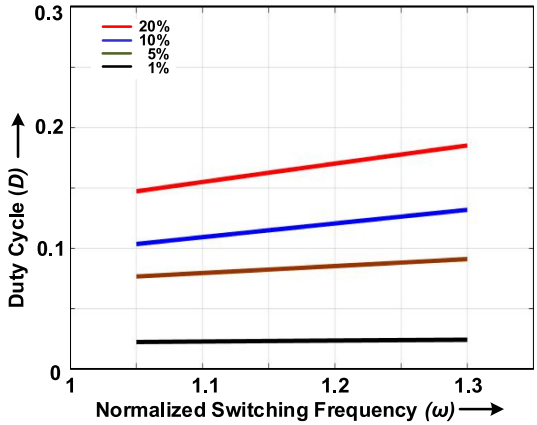
Voltage regulation characteristics of any modulation technique at light loads for a low-$Q$ resonant circuit design is an important characteristic. The voltage gain curve becomes flatter at light load operation, thereby, requiring a wide switching frequency range. This modulation technique allows for achieving a tight output voltage regulation at extremely light load conditions as shown in Fig. 6. Fig. 6(a) and 6(b) shows possible combinations of duty cycle and switching frequency at loading

TABLE I
MICROINVERTER SPECIFICATIONS

| Parameters | Value |
|---|---|
| Input voltage range, $V_i$: | $20 - 40V$ (30V nominal-60 cell panel) |
| Resonant inductor, $L_s$ | $1\mu H$ |
| Magnetizing inductor, ($L_m$) | $6\mu H$ |
| Resonant capacitor, $C_s$ | $1.1\mu F$ |
| Rated quality factor, $Q$ | 0.34 |
| Transformer turns ratio, $n$ | 1:14 |
| Output power, $P_o$ | 300W |
| Resonant frequency, $f_r$ | 152kHz |




(a)




(b)

Fig. 6. Duty cycle versus normalized switching frequency curve for $V_o$ = 380 V at light loading conditions at (a) $V_{\text{in}} = 35$ V and (b) $V_{\text{in\_max}} = 40$ V.

$$i_{Ls}(t_0) = \frac{V_i - nV_o - \left[\frac{v_{Cs}(t_0)}{\omega_r L_s}\right]\sin\left[\omega_r\left(t_1+t_3\right)\right] - \left[\frac{V_i}{\omega_r L_s}\right]\sin(\omega_r t_2) - \frac{nV_o(t_1+t_3)}{L_m}}{1-\cos\left[\omega_r\left(t_1+t_3\right)\right]} \tag{19}$$

$$P_o = \left[\frac{nV_o}{T_s}\right] * \left[\begin{array}{l}\left(\frac{i_{Ls}(t_0)}{\omega_r}\right)\left(\sin\left(\omega_r\left(t_1+t_3\right)\right) - \left(\omega_r\left(t_1+t_3\right)\right)\right) + \left(V_i - nV_o - \frac{v_{Cs}(t_0)}{\omega_r^2 L_s}\right)\left(1-\cos\left(\omega_r\left(t_1+t_3\right)\right)\right) \\ -\left(V_i - \frac{v_{Cs}(t_0)}{\omega_r^2 L_s}\right)\left(1-\cos\left(\omega_r t_3\right)\right) - \left(\frac{nV_o}{L_m}\right)\left(\frac{t_1^2+t_3^2}{2} + t_1 t_3\right)\end{array}\right] \tag{21}$$

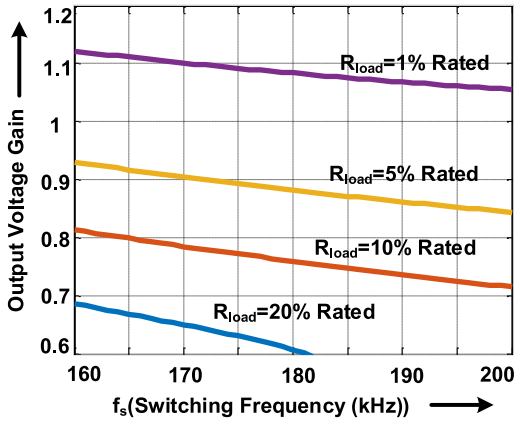


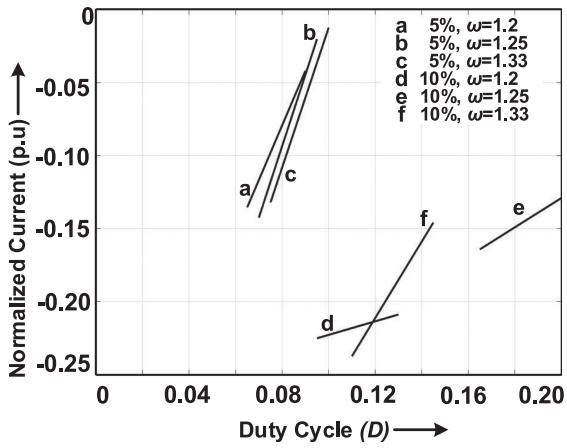

Fig. 7. Voltage gain curve at duty cycle, $D = 0.2$.

conditions below 20% for a constant 380-V output at different $V_{\text{in}}$ of 35 and 40 V, respectively. These graphs imply that the switching frequency can be reduced by varying the duty cycle at light loading conditions. Such analysis assists in choosing the operating point of the $LLC$ resonant converter.

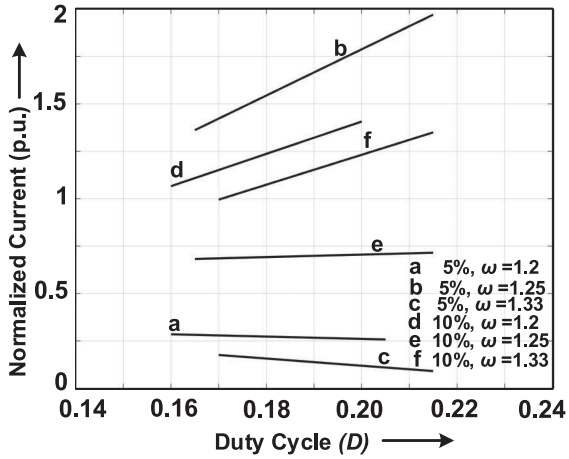
The calculated values were found to be in close agreement with the PSIM model. On the other hand, frequency modulation with a constant duty cycle of $D = 0.5$ will require operation at switching frequencies 4–5 times higher than the series resonant frequency at light load conditions. Since switching losses are significant at a high-frequency operation, reduction in turn-OFF switching losses will be achieved with the decreased switching frequency using this modulation strategy. However, for the constant power output, turn-OFF currents for MOSFETs operating with duty cycle $D$ will increase. Therefore, it is necessary to analyze the turn-OFF currents and determine the operating point that will deliver net positive improvement in a light load efficiency. The proposed technique provides gain less than unity for operation above resonance as shown in Fig. 7 for duty cycle, $D = 0.2$, at light load operation. It exhibits a smooth and monotonic voltage gain switching frequency control characteristic that allows for a simple proportional-integral (PI) controller implementation.

### B. Turn-OFF Currents

The turn-OFF current of leading leg switches was evaluated for three different switching frequencies for 10% and 5% loading conditions. Since variation in duty cycle changes the output voltage gain, the output voltage could vary from 380 V $\pm$20 V for the following analysis. The assumed output voltage variation is a good approximation as ripple voltage in a single-phase grid-connected microinverter system is roughly 5% of the nominal value [33]. Fig. 8(a) shows normalized ($V_{\text{nom}}/P_{\text{nom}}$) turn-OFF current for the low-side switch $Q_2$ with respect to duty cycle, $D$, of the switch $Q_1$. A negative turn-OFF current for the required duty-cycle variation implies true ZVS for a high-side switch $Q_1$. Fig. 8(b) shows the normalized turn-OFF current for the high-side switch $Q_1$ with respect to duty cycle, $D$, of the switch $Q_1$. A positive turn-OFF current ensures that low-side MOSFET $Q_2$ achieves ZVS. Since the lagging leg is already soft switched, the proposed method achieves ZVS for all four switches for an




(a)




(b)

Fig. 8. Normalized turn-OFF current for (a) switch $Q_2$ and (b) switch $Q_1$.

input voltage range of 2:1 (20–40 V) for loading conditions as low as 5%.

### C. Effect of the DC-Bias Current on Transformer Size

Due to the asymmetrical modulation waveshape, even harmonics are induced in the primary circuit with dominant second harmonic content. These harmonics are not present for a symmetrical modulation technique such as variable FM or PSM. The resonant capacitor, $C_r$, blocks the dc component of $v_{ab}$ that prevents resonant inductor core saturation. However, a dc bias exists in the transformer magnetizing current due to the waveform asymmetry. This increase in the magnetizing current assists in achieving ZVS for primary-side MOSFETs. Hence, any asymmetrical modulation technique will require a tradeoff between conduction losses (due to a higher magnetizing current) and switching losses. For the same reason, it is advisable to use the proposed modulation technique at light loads where switching losses dominates.

The dc bias in the transformer magnetizing current will lead to a dc flux bias superimposed on the ac flux swing in the *B–H* curve, which leads to increase in the peak ac flux swing in the transformer core during one half of the switching cycle. If the

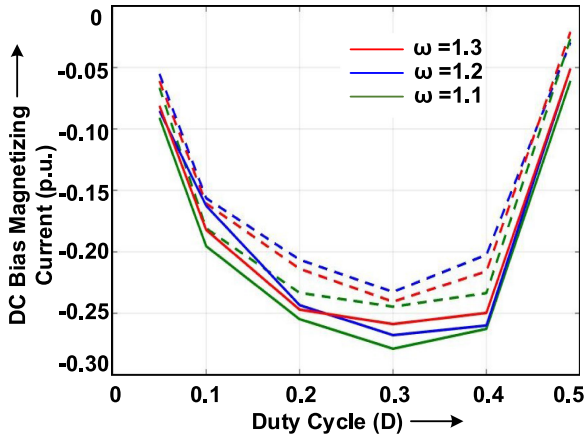



Fig. 9. DC bias magnetizing current for APWM (solid line) and proposed modulation technique (dashed line) at $V_{\text{in\_max}} = 40$ V, $Q = 0.11$ (30% rated load).

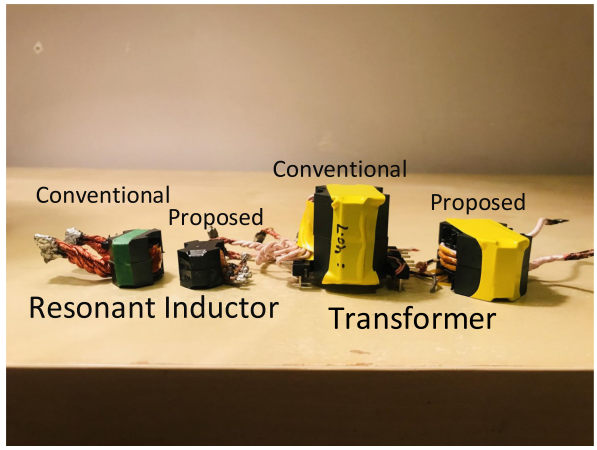



Fig. 10. Magnetics size comparison.

transformer was already operating close to the knee point of the saturation curve, the additional dc flux bias will push the core into saturation. Hence, $\Delta B_{\text{Conv}}$-based transformer needs to be designed for a lower peak flux density to ensure that the extra dc-bias current does not saturate the core. Fig. 9 shows the dc bias current for $V_{\text{in\_max}} = 40$ V at 30% load operation for the APWM and proposed modulation technique. Since the proposed modulation technique exhibits a lower dc bias current than the conventional approach, $\Delta B_{\text{Prop}} > \Delta B_{\text{Conv}}$. Since core loss is limited by saturation, the following equation can be used to calculate area product of transformer.

$$A_p = \frac{L_m \Delta I_{L_m} \left(I_{p\_\text{rms}} + I_{s\_\text{rms}}/n\right)}{\Delta B J K_u} \tag{23}$$

where $I_{p\_\text{rms}}$ and $I_{s\_\text{rms}}$ are the primary and secondary rms currents, respectively, and $n$ represents the transformer turns ratio. $\Delta B$, $J$, and $K_u$ are the flux density swing, current density, and core window utility factor. Since the proposed improved APWM and conventional approach are employed during the medium-light power level operation, the rms current is not the limiting factor for the transformer design. However, for the same current density and turns ratio, $\Delta B_{\text{Conv}} = 0.2$ T and $\Delta B_{\text{Prop}} = 0.3$ T are chosen. From (23), a lower $\Delta B$ eventually requires a higher area product of the transformer. Fig. 10 shows the transformer and resonant inductor core for both techniques.

## V. Loss Analysis

The analysis in previous section did not consider the effect of parasitic capacitances of the system. Fig. 11(a) shows the full-bridge $LLC$ converter with relevant parasitic capacitance. Since, the study of dead-time intervals was to explain the ZVS phenomenon only, they have been excluded from the loss analysis. The key steady-state waveforms under the proposed modulation technique operation, considering effects of parasitic capacitances under light load conditions are shown in Fig. 11(b). Resonant capacitor, $C_s$, acts as a dc-blocking capacitor and prevents the introduction of dc bias in a high-frequency transformer. Voltage across $C_s$, $v_{Cs}$, will be level shifted due to the negative dc voltage blocked across it as shown in Fig. 11(b). Fig. 12 shows the equivalent circuit of the $LLC$ converter considering parasitic capacitance effect during the freewheeling period $t_2 \le t < t_5$. At time instant $t_2$, $L_s$, $L_m$, $C_s$, and $C_{\text{par}}$ start resonating at a resonant frequency $\omega_{r\_\text{par}}$, which is defined in (26). High-frequency oscillation due to resonance of the $LLC$ tank with parasitic capacitances (in the picofarads range) affects $dB/dt$ of the inductor and transformer core and leads to sudden jumps in the flux waveform. $v_{Ls}$ and $v_{Lm}$ can be expressed as

$$v_{Ls}(t) = -L_s i_{Ls}(t_2)\left[\frac{C_{\text{par}}L_m - L_m C_s}{\omega_{r_{\text{par}}} C_{\text{par}} C_s L_m L_s}\right]\cos\left[\omega_{r_{\text{par}}}(t-t_2)\right] - \left[v_{Cs}(t_2) + v_{C_{\text{par}}}(t_2)\right]\sin\left[\omega_{r_{\text{par}}}(t-t_2)\right] \tag{24}$$

$$v_{Lm}(t) = L_s i_{Ls}(t_2)\left[\frac{C_{\text{par}}L_m - L_m C_s}{\omega_{r_{\text{par}}} C_{\text{par}} C_s L_m L_s}\right]\cos\left[\omega_{r_{par}}(t-t_2)\right] - \left[v_{Cs}(t_2) + v_{C_{\text{par}}}(t_2)\right]\sin\left[\omega_{r_{\text{par}}}(t-t_2)\right] \tag{25}$$

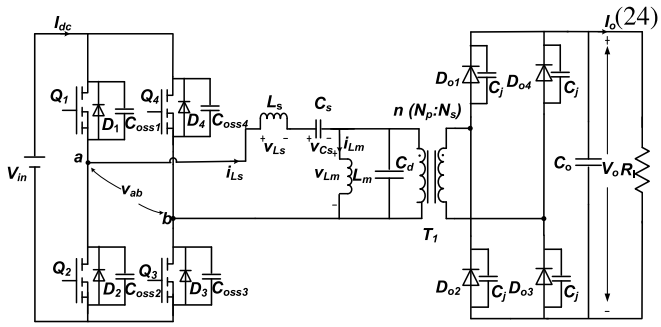
where

$$\omega_{r_{par}} = \sqrt{\frac{L_s C_s + L_m C_{\text{par}}}{L_s C_s L_m C_{\text{par}}}}. \tag{26}$$

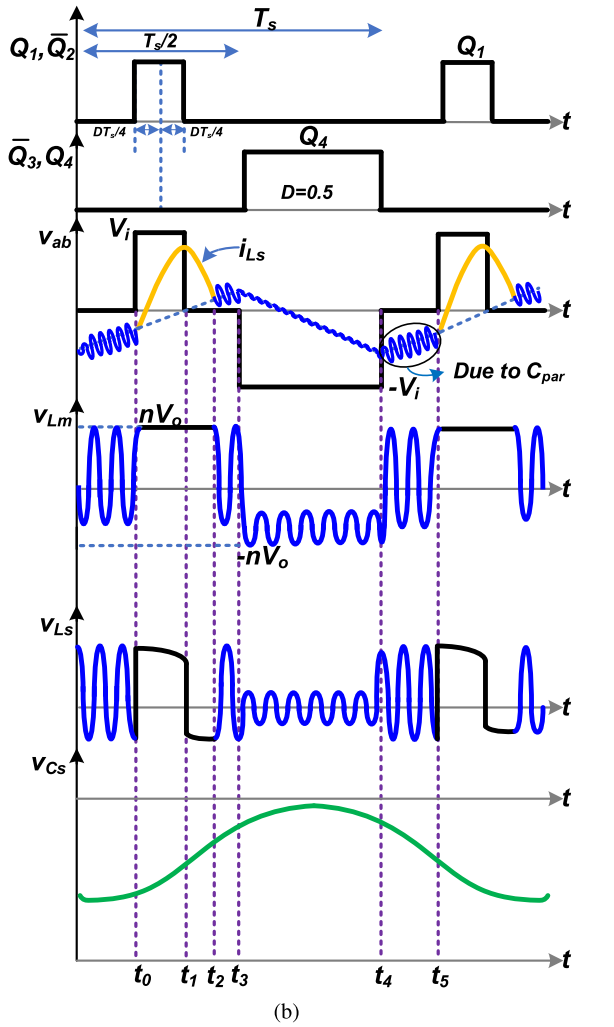
Time-domain equations are solved for each freewheeling period as follows.

*1) Freewheeling Period 3 [$t_2$–$t_3$]:* Due to the absence of a damping negative voltage at $v_{ab}$, the primary current oscillates with high amplitude. It is critical that the current oscillation amplitude is not large, which allows multiple zero crossings of the current before a time instant $t_3$. Such a situation would not guarantee ZVS.

$v_{L_m}$ is reflected to the transformer secondary across the bridge rectifier diode. Since it is assumed that $C_o$ holds the output voltage constant, multiple zero crossings of $v_{L_m}$ during time interval $t_2$–$t_5$ will cause multiple diode switching transitions only if peak amplitude reaches $\pm nV_o$. This phenomenon will increase reverse recovery switching losses. However, in practical scenario, circuit damping might prevent oscillating $v_{L_m}$ waveform from reaching $\pm nV_o$ value multiple times. Hence, the oscillating voltage will cause junction capacitance voltage

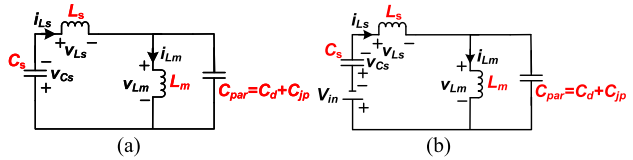



(a)




(b)

Fig. 11. (a) Full-bridge *LLC* converter with parasitic capacitances. (b) Theoretical light loading waveforms considering $C_d$ and $C_j$ for the proposed method.




(a) (b)

Fig. 12. Equivalent $LLC$ circuit considering transformer distributed capacitance ($C_d$) and primary referred rectifier junction capacitance, $C_{jp}$ for (a) freewheeling periods 3 and 5 and (b) freewheeling period 4.

across each diode to charge and discharge, and the current equivalent to leakage values will flow in the secondary circuit.

*2) Freewheeling Period 4 [$t_3$–$t_4$]:* This period begins at time instant $t = t_3$ when $Q_3$ turns OFF, while $Q_4$ is turned ON with ZVS. Expressions for evaluating $v_{Ls}$ and $v_{Lm}$ during this period are given by

$$v_{Ls}(t) = -L_s i_{Ls}(t_3)\left[\frac{C_{\text{par}}L_m - L_m C_s}{\omega_{r_{\text{par}}} C_{\text{par}} C_s L_m L_s}\right]\cos\left[\omega_{r_{\text{par}}}(t-t_3)\right] - \left[V_{in} + v_{Cs}(t_3) + v_{C_{\text{par}}}(t_3)\right]\sin\left[\omega_{r_{\text{par}}}(t-t_3)\right] \tag{27}$$

$$v_{Lm}(t) = L_s i_{Ls}(t_3)\left[\frac{C_{\text{par}}L_m - L_m C_s}{\omega_{r_{\text{par}}} C_{\text{par}} C_s L_m L_s}\right]\cos\left[\omega_{r_{\text{par}}}(t-t_3)\right] - \left[V_{in} + v_{Cs}(t_3) + v_{C_{\text{par}}}(t_3)\right]\sin\left[\omega_{r_{\text{par}}}(t-t_3)\right]. \tag{28}$$

Due to a negative damping voltage $v_{ab} = -V_{\text{in}}$, the resonant current does not demonstrate similar amplitude of current oscillation as in the previous period. Hence, multiple zero crossings are not observed, guaranteeing true ZVS of $Q_4$.

During freewheeling periods, the resonant waveforms of $v_{Lm}$ and $v_{Ls}$ affect $dB/dt$ and the core loss. Hence, selection of MOSFET and rectifier diodes is a critical step toward the final design. The component selection process is explained in detail in [12]. For the study presented in this article, $C_d = 790$ pF and $C_j = 45$ pF are the datasheet values for the transformer and rectifier diode capacitance, respectively.

Based on the analysis performed and the component selection, it is necessary to evaluate the converter design and operating conditions under which the proposed mode of operation is guaranteed. It can be observed that if instantaneous resonant currents $i_{L_s}(t_2)$ and $i_{L_s}(t_3)$ remain greater than zero for the chosen inductance ratio, $K$, for various duty cycle, $D$, the proposed mode of operation exists. Fig. 13 shows the boundary modes for ZVS operation with variation in $K$ and $D$ values with this modulation scheme at different values of $\omega$.

## VI. Optimal Duty-Cycle Calculation

In this section, power loss analysis of a full-bridge $LLC$ resonant converter is performed to find optimal duty ratio and switching frequency values at different light load condition. Major sources of power loss at light load operating conditions include high-frequency transformer loss, resonant inductor loss, and MOSFET switching loss. Magnetic loss per unit volume of the chosen core shape can be computed by using the conventional original Steinmetz equation (OSE) given by

$$P_{\text{core}} = k f^{\alpha} B_{pk}^{\beta}. \tag{29}$$

where $k$, $\alpha$, and $\beta$ are Steinmetz constants, depending on magnetic material characteristics. However, the OSE fails to give accurate core loss result for nonsinusoidal voltage waveforms [34]. The improved generalized Steinmetz equation (iGSE) has been proven to demonstrate the minimum core loss error for a nonsinusoidal arbitrary magnetic flux waveform without any extra parameter requirement apart from the Steinmetz parameters

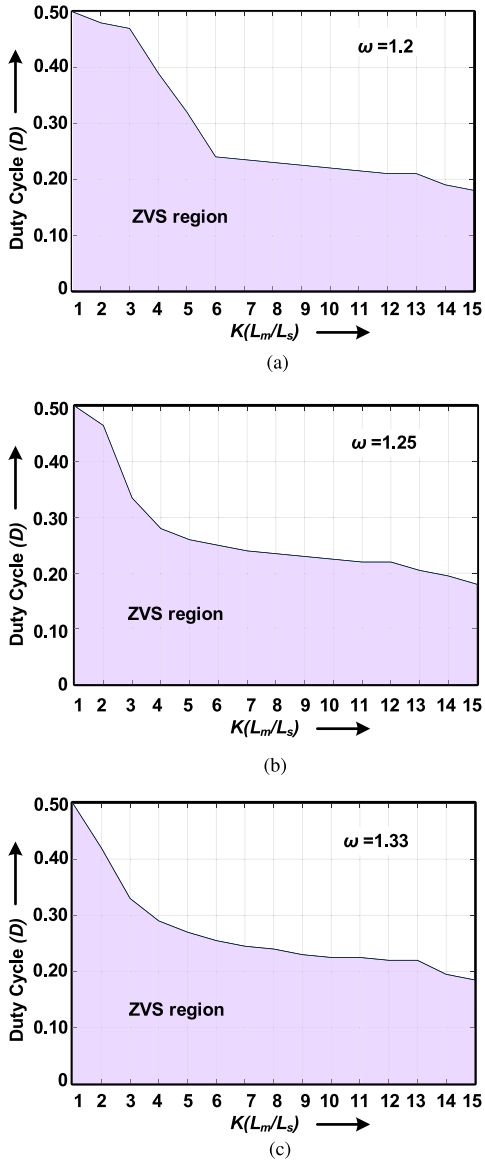



Fig. 13. Boundary modes for ZVS operation under influence of parasitics at (a) $\omega = 1.2$, (b) $\omega = 1.25$, and (c) $\omega = 1.33$.

in a datasheet [35], [36]. For any asymmetric, nonsinusoidal waveform, core loss over one switching cycle can be calculated as

$$P_{\text{core}} = \frac{V_c}{T_s}\int_0^{T_s} k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{30}$$

where $\Delta B$ is peak-to-peak flux density, $dB(t)/dt$ is rate of change of flux density, and $k_i$ coefficient is given by

$$k_i = \frac{\kappa}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \tag{31}$$

However, the iGSE has a severe limitation: it neglects the variation of Steinmetz parameters under the condition when dc bias exists in the magnetizing current waveforms. Therefore, in order to ensure an accurate core loss calculation for the proposed modulation waveform, it is essential to compute the Steinmetz parameters $\alpha$, $\beta$, and $k_i$ over different dc-bias magnetization levels ($H_{\text{dc}}$) and flux density swing ($\Delta B_{L_m}$). A SY-8219 B-H

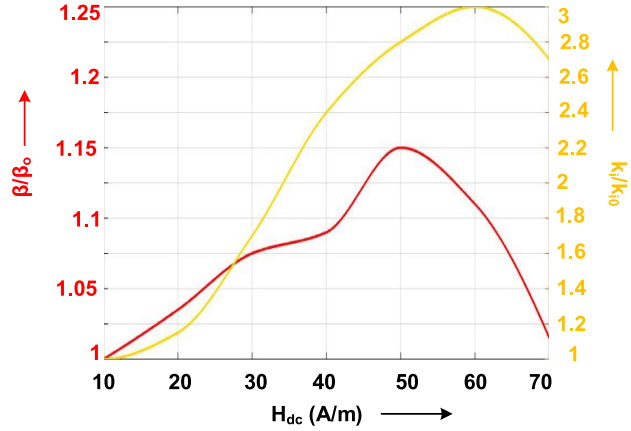



Fig. 14. Variation of Steinmetz parameters $\beta$ and $k_i$ under various $H_{\text{dc}}$ conditions.

analyzer, 5.2-A, 140-V power amplifier (IE-1125B), and a dc source (SY-962, peak dc bias current = 30 A) were employed for the *B–H* hysteresis loop measurement of the transformer core with square-wave input voltage excitation superimposed with a dc bias current (maximum of 4 A for the proposed modulation technique) for the designed air-gapped transformer to calculate ($H_{\text{dc}_{\text{max}}}$). For a maximum switching frequency of 180 kHz, $H_{\text{dc}} = 75$ A/m was observed at $I_{\text{dc}_{\text{max}}} = 4$ A and $\Delta B_{L_m} = 0.1$ T. By fitting the experimental core loss values using a least-square algorithm [37] at $\Delta B_{L_m} = 0.025, 0.05$, and 0.1 T and $f_s = 150$ and 180 kHz, $\alpha = 1.41$ at 150 kHz with $H_{\text{dc}} = 0$ was calculated. Since switching frequency varies between a small range of 150–180 kHz, $\alpha = 1.41$ is a fairly accurate assumption. For various $H_{\text{dc}}$ levels, the power loss curve was a straight line, implying a constant $\alpha = 1.41$. Based on the same methodology, Fig. 14 shows a variation of $\beta$ and $k_i$ normalized with respect to $\beta_0$ and $k_{i0}$, with varying $H_{\text{dc}}$ levels at a fixed $\delta B = 0.1$ T at T = 25° C. Using the Steinmetz parameters at $H_{\text{dc}} = 0$ from manufacturers datasheet, Steinmetz parameters at various $H_{\text{dc}}$ levels can be calculated and used in the iGSE formula for the proposed modulation waveform. Since, both $v_{Lm}$ and $v_{Ls}$ have different nonsinusoidal voltage waveforms during powering ($t_0 \le t < t_2$) and nonpowering ($t_2 \le t < T_s$) periods, (30) can be calculated for each period as follows:

$$P_{\text{pow}} = \frac{V_c}{T_s}\int_0^{t_2} k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{32}$$

$$P_{\text{free}} = \frac{V_c}{T_s}\int_{t_2}^{T_s} k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt. \tag{33}$$

Total core loss over a switching cycle can be found by the following expression:

$$P_{\text{core\_Total}} = P_{\text{pow}} + P_{\text{free}}. \tag{34}$$

### A. *Transformer Core Loss*

Transformer peak-to-peak flux density, $\Delta B_{L_m}$, and rate of change of flux density, $dB_{L_m}/dt$, can be given as

$$\Delta B_{L_m} = \frac{nV_oD}{N_pA_ef_s} \tag{35}$$

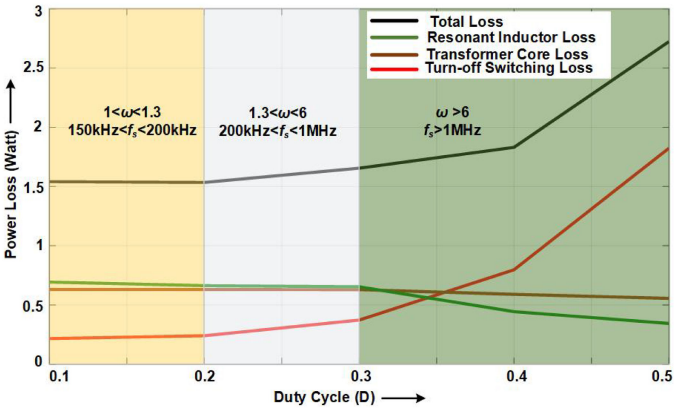



Fig. 15. Power loss as a function of duty cycle for 10% loading condition.

$$\frac{dB_{L_m}(t)}{dt} = \frac{v_{Lm}(t)}{N_p A_e}. \tag{36}$$

It can be seen from Fig. 11(b) that $dB_{L_m}/dt$ is constant with an amplitude equal to $+nV_o$ during powering stages, while it is a sinusoidal waveform with a similar peak amplitude during the freewheeling period. Using frequency modulation, $dB_{L_m}/dt$ will remain constant during the entire switching cycle since $L_m$ stays clamped to $\pm nV_o$. Transformer core loss at 10% loading condition for a fixed output voltage of 380 V at maximum input voltage, $V_{\text{in\_max}} = 40$ V is given in Fig. 15.

### B. External Resonant Inductor Core Loss

Peak-to-peak flux density, $\Delta B_{L_s}$, and the rate of change of flux density, $dB_{L_s}/dt$, of the external inductor can be given as

$$\Delta B_{L_s} = \frac{2L_s I_{pk}}{N_{L_s} A_{L_s}} \tag{37}$$

$$\frac{dB_{L_s}(t)}{dt} = \frac{v_{L_s}(t)}{N_{L_s} A_{L_s}}. \tag{38}$$

Utilizing iGSE, it was observed that inductor core losses decreased with the increasing duty cycle and corresponding switching frequency. Fig. 15 exhibits the trend of power loss over a full range of the duty cycle.

### C. Turn-OFF Switching Loss

Since there exists an overlap between the switch voltage and current during a turn-OFF transition, energy is lost as switching loss. The turn-OFF switching loss for a MOSFET can be given as

$$P_{\text{turn-off}} = \frac{1}{6}\left[I_{\text{turn-off}} - C_{\text{ds}}\frac{V_{\text{in}}}{T_{\text{turn-off}}}\right] T_{\text{turn-off}} f_{\text{sw}} \tag{39}$$

where $T_{\text{turn-off}}$ is defined as

$$T_{\text{turn-off}} = \frac{R_{\text{gs}} Q_{\text{gd}}}{V_{\text{plateau}}} \tag{40}$$

where $R_{\text{gs}}$ is gate resistance, $Q_{\text{gd}}$ is MOSFET gate–drain charge, and $V_{\text{plateau}}$ is the Miller plateau voltage. $i_{L_s}(t_0)$, $i_{L_s}(t_1)$, $i_{L_s}(t_3)$, and $i_{L_s}(t_4)$ are the turn-OFF currents for MOSFET $Q_1$, $Q_2$, $Q_3$, and $Q_4$, respectively. Fig. 15 shows the turn-OFF losses of the $LLC$ converter at 10% loading condition.

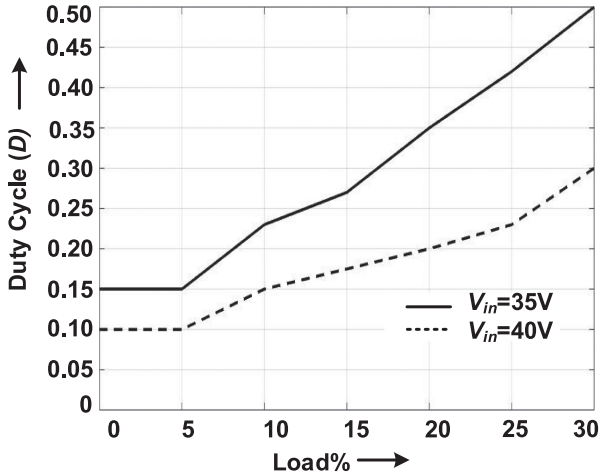



Fig. 16. Optimal duty-cycle calculation for different load conditions at $V_{\text{in}} = 35$ V and $V_{\text{in\_max}} = 40$ V.

### D. Description and Observation

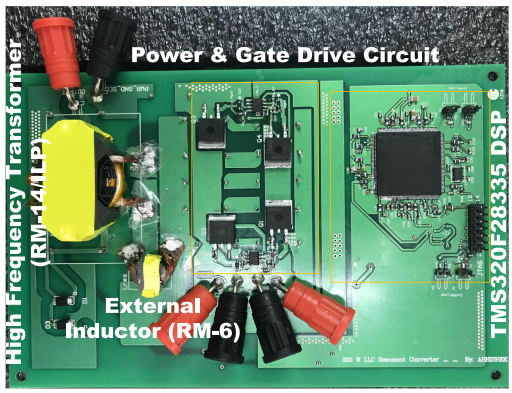
Fig. 15 shows the total power loss with a range of $\omega$ and $D$ required for the ZVS operation with an output voltage equal to 380 V at $V_{\text{in\_max}} = 40$ V at fixed 10% load operation. Increasing duty cycle requires larger switching frequency to regulate the output voltage. It leads to reduction in the operating peak-to-peak flux density, and consequently, core losses for a given output voltage and load power. However, it is difficult to design the high-frequency transformer when operating over such a wide range of switching frequency and fix the optimum peak-to-peak $B$ value for nominal operation. Optimizing the gate drive circuitry layout with the selection of controller IC becomes cumbersome. Using iGSE, core loss calculation below $D = 0.1$ showed aberrant behavior with increase calculated losses. It is hypothesized that this behavior is attributed to high magnitude of higher order harmonics and large $dB/dt$ rate for fixed load power operation at low values of $D$. It is expected that operation at such low values of $D$ would be required for extremely light load conditions below 10%. Experimental verification of the iGSE method over such a wide variation of both switching frequency and peak-to-peak flux density is nonexistent. Thermal limitation on core material losses is not considered in the model, which will have an impact at heavier load conditions. For practical applications, however, it is decided that the upper limit on $D$ and $\omega$ not exceeding 0.2 and 1.3, respectively, will give an optimal tradeoff between magnetic losses and turn-OFF switching losses for 10% load operation. Based on similar analysis, optimal duty-cycle values for minimum power losses are calculated for $V_{\text{in}} = 35$ V and $V_{\text{in\_max}} = 40$ V for different light loads in Fig. 16.

## VII. Experimental Results

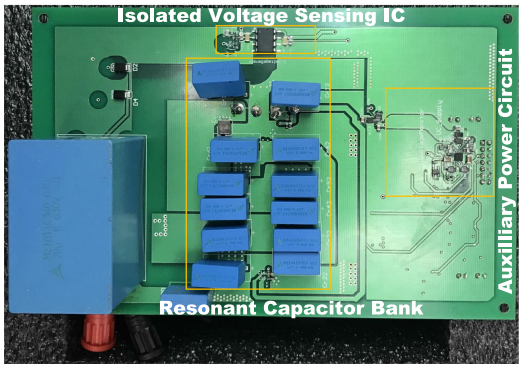
An experimental prototype with design specifications given in Table II has been implemented for performance validation of

TABLE II
DESIGN PARAMETERS

| Parameters | Measured Value |
|---|---|
| Input voltage range | $20-40V$ |
| Output voltage ($V_o$) | $380\pm10V$ |
| Output power ($P_o$) | $300W$ |
| Resonant frequency ($f_r$) | $152.8kHz$ |
| Switching frequency ($f_{sw}$) | $90-180kHz$ |
| External series resonant inductor ($L_s$) | $0.89\mu H$ |
| Leakage inductor | $0.2\mu H$ |
| Series resonant capacitor ($C_s$) | $0.99\mu F$ |
| Rated quality factor | 0.37 |
| Magnetizing inductor ($L_m$) | $6\mu H$ |
| Transformer turns | 1:13 |
| DC bus capacitor | $20\mu F$ |
| Snubber capacitance ($C_{sn}$) | $1nF$ (each MOSFET) |

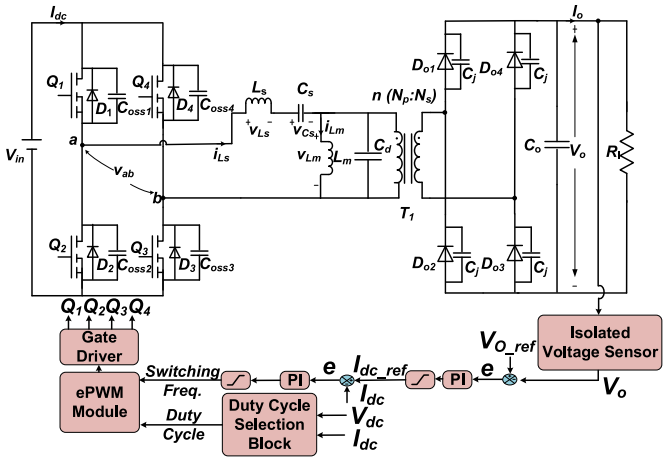



(a)

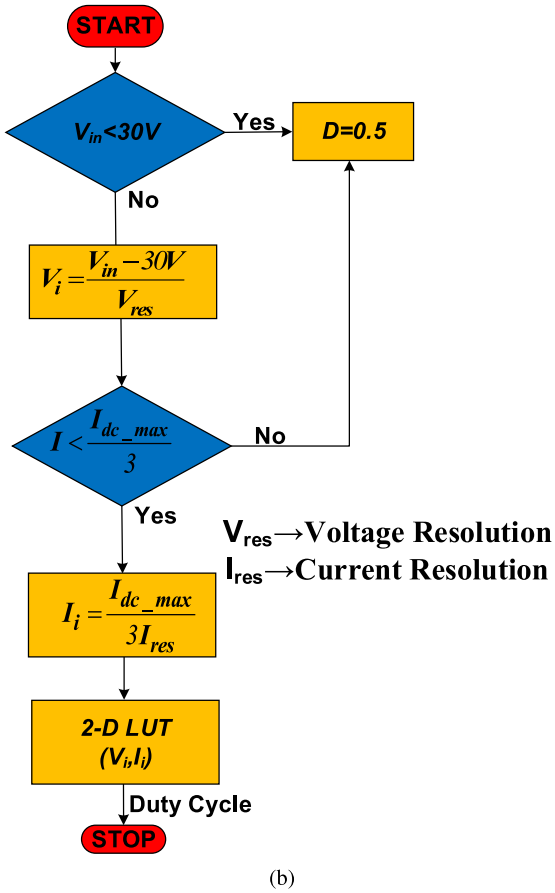



(b)

Fig. 17. Experimental prototype. (a) Top side. (b) Bottom side.




(a)

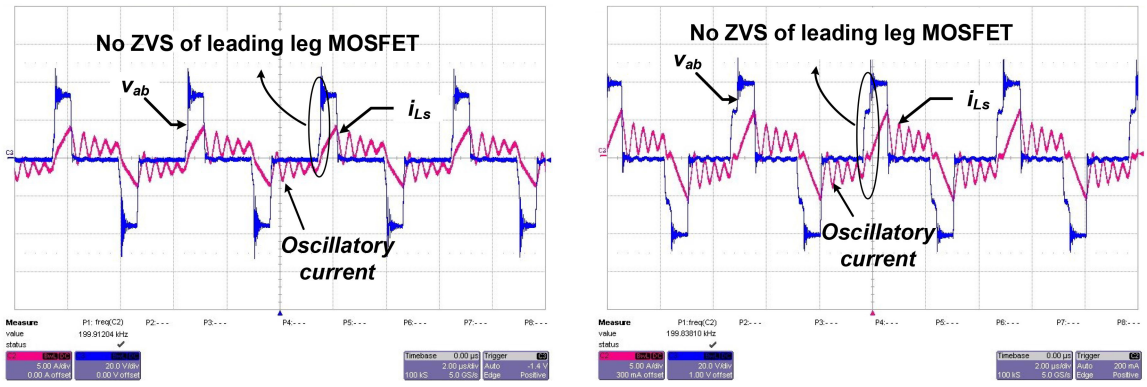



(b)

Fig. 18. (a) *LLC* converter with an adjustable duty-cycle switching frequency control scheme. (b) Duty-cycle selection block flowchart.

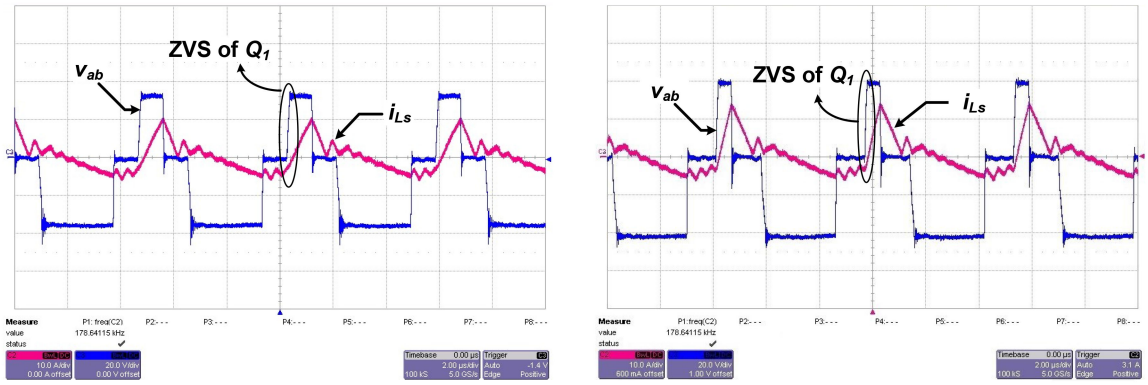
the proposed hybrid modulation technique as shown in Fig. 17. Fig. 18(a) shows the proposed closed-loop control scheme for the hybrid modulation strategy. Two individual control loops for the $LLC$ resonant converter's switching frequency and duty cycle are required to be implemented. TSM320F28335 DSP is used to implement the control structure and generate the required gate signals. Fig. 18(b) shows the logic flowchart of the duty-cycle selection block. Operation below 30-V input voltage requires a variable frequency control only. ZVS and output regulation is guaranteed for the operation between 20 and 30 V input below the resonant frequency [12].

Since operation at resonant frequency guarantees most efficient operation due to the minimum circulating current, at nominal conditions, $\omega=1$ ($f_s=150$ kHz) is chosen for the input voltage $V_{\text{in\_nom}}=30$ V. Converter operation transitions from FM to the proposed adjustable duty-cycle switching frequency




(a) (b)

Fig. 19. Experimental waveforms of phase-shift-modulated input voltage and resonant current at $f_{\text{sw}} = 200$ kHz ($\omega = 1.33$) at 10% load at (a) $V_{\text{in\_max}} = 35$ V and (b) $V_{\text{in\_max}} = 40$ V.




(a) (b)

Fig. 20. Experimental ZVS waveforms of the proposed modulation technique-based input voltage and resonant current at (a) $f_{\text{sw}} = 178$ kHz ($\omega = 1.2$), $D_{\text{eff}} = 0.23$ at $V_{\text{in}} = 35$ V and (b) $f_{\text{sw}} = 178$ kHz ($\omega = 1.2$), $D_{\text{eff}} = 0.15$ at $V_{\text{in\_max}} = 40$ V at 10% load.

TABLE III
COMPARISON OF DIFFERENT LIGHT LOAD MODULATION TECHNIQUES FOR LOW-$Q$ $LLC$ CONVERTER

| Technique | Control Characteristics | ZVS Range | Required $\omega$ & $D$ Control Range |
|---|---|---|---|
| VFM [12] | Monotonic, Not ideal for low-$Q$ | Wide I/P Voltage | Wide $\omega$, Fixed $D$ |
| PSM [12] | Monotonic, Not ideal for low-$Q$ | Narrow I/P Voltage | Narrow $\omega$, Wide $D$ |
| APWM [12] | Non-Monotonic, Not ideal for low-$Q$ | Narrow I/P Voltage | Narrow $\omega$, Wide $D$ |
| Proposed Improved APWM | Monotonic, Ideal for low-$Q$ | Wide I/P Voltage | Narrow $\omega$, Narrow $D$ |

when $\omega > 1$ for operation between 30 and 40 V input when the dc input current becomes 30% of the rated value for this prototype. Control resolution can be selected based on the values of $V_{\text{res}}$ and $I_{\text{res}}$. The preselected optimal duty-cycle values calculated in the previous section are stored in a lookup table for each $V_i$ and $I_i$.

ZVS at worst-case conditions implies ZVS at all possible operating conditions. The ZVS performance at 10% loading condition at two upper input voltages, $V_{\text{in}} = 35$ V and $V_{\text{in\_max}} = 40$ V is tested under the conventional PSM. ZVS of all four MOSFETs is lost under both operating input voltages as shown in Fig. 19(a) and 19(b), respectively. Chances of turning ON leading leg MOSFETs at zero $V_{DS}$ increases if the oscillatory resonant current is at the trough of the waveform just before switching transition. Apart from inability to turn ON leading leg MOSFETs at zero voltages, ZVS of lagging leg MOSFETs also cannot be guaranteed due to multiple zero crossings of the primary resonant current during time interval when $v_{ab} = 0$. Due to multiple zero crossings, the MOSFETs intrinsic antiparallel diode conduction may or may not happen before switch turns ON, leading to uncertainty over the ZVS performance.

Hence, the conventional PSM cannot guarantee true ZVS of a low-$Q$ high-turns-ratio $LLC$ resonant converter for the given input voltage range application within the selected switching frequency range. Such pronounced ringing in the resonant current can be contributed to long intervals of effective zero input voltage tank excitation (forcing function), i.e., $v_{ab} = 0$. This leads to large ripple in the resonant current due to the interaction

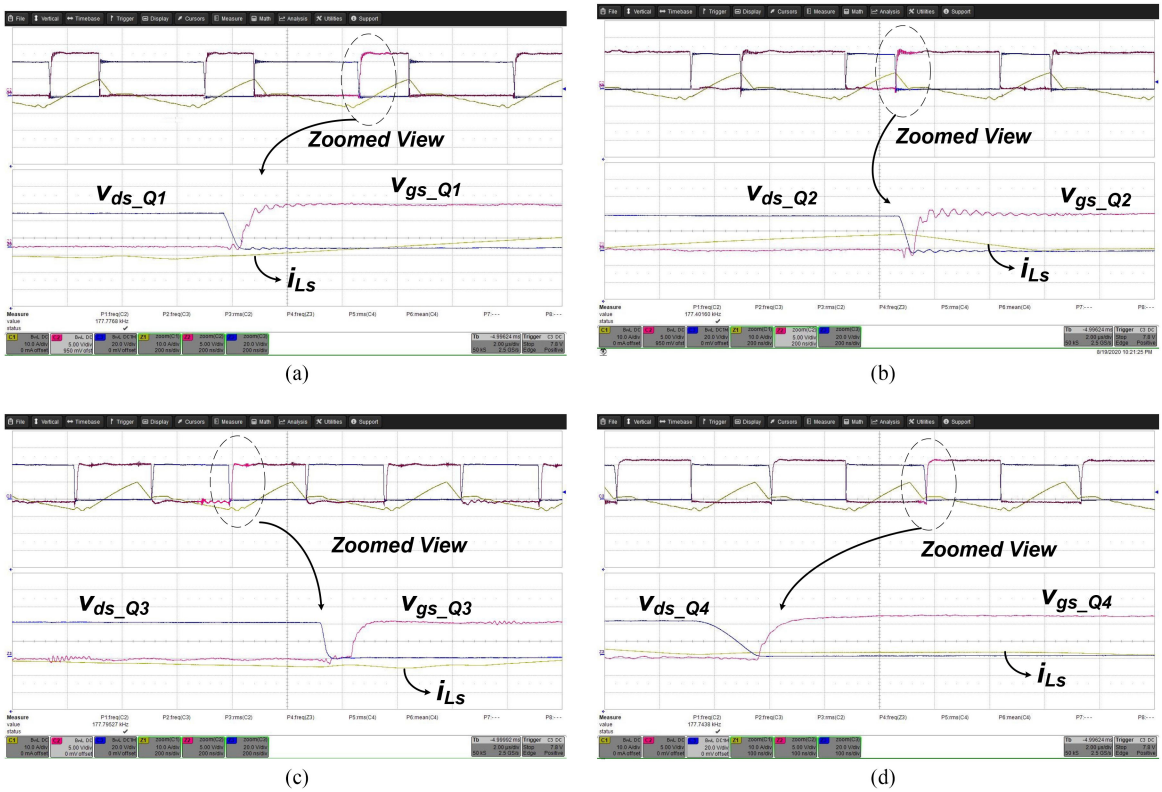



Fig. 21. Experimental $V_{GS}$ and $V_{DS}$ ZVS waveforms at $V_{in\_max}$ of primary MOSFET (a) $Q_1$, (b) $Q_2$, (c) $Q_3$, and (d) $Q_4$ at 10% load.

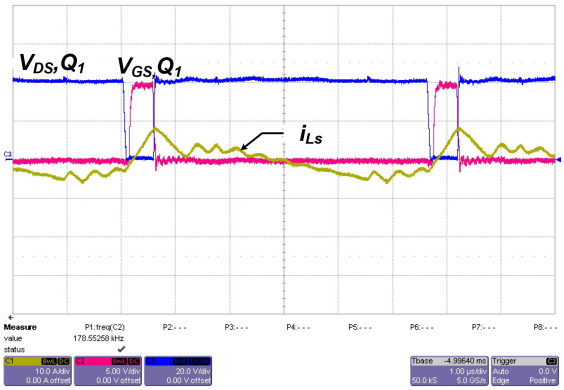



Fig. 22. Experimental $V_{GS}$ and $V_{DS}$ ZVS waveforms at $V_{in\_max}$ of primary MOSFET $Q_1$ at 5% load.

of the $LLC$ resonant tank with distributed capacitance of the high-frequency low-profile transformer and primary reflected junction capacitance of rectifier diodes. Therefore, in order to reduce the probability of losing ZVS due to multiple zero crossings of the resonant current, intervals for which $v_{ab}$ stays zero should be reduced.

In order to compare ZVS performance with the conventional PSM, experimental waveforms for the proposed modulation scheme are taken at the same worst-case operating conditions in Fig. 20(a) and 20(b), respectively. Operation at 35 V requires switching frequency $f_{sw} = 178$ kHz at duty cycle $D = 0.23$, and demonstrates true ZVS of all four primary MOSFET switches in the full-bridge switching network. The proposed modulation method also achieves true ZVS at maximum input voltage $V_{in\_max} = 40$ V with duty cycle $D = 0.15$ and switching frequency $f_{sw} = 178$ kHz. The proposed scheme allows for a smaller time interval when the input H-bridge voltage, $v_{ab}$ stays at 0. Due to the large negative pulse of duty cycle, $D = 0.5$, the current oscillations are damped out. Damping of the resonant current during time period $t_4$–$t_5$ [as per Fig. 11(b)] is observed experimentally as well. Therefore, the proposed modulation scheme guarantees ZVS between 30 and 40 V since there are no multiple zero crossings before switching transition of either high-side ($Q_1$) or low-side ($Q_2$) MOSFET in the leading leg. This ensures that the total MOSFET drain-to-source capacitance $C_{ds}$ once discharged (during turn-ON of MOSFET) does not start charging again due to the reversal of the current direction as observed in the conventional PSM. Consequently, the distributed capacitance is not suddenly discharged from $+nV_o$ to $-nV_o$ due to the small $v_{ab} = 0$ interval. As seen in Fig. 19, this phenomenon is common in the PSM scheme at light loads. The proposed technique eliminates this fundamental drawback observed in the conventional PSM-modulated high-turns-ratio resonant converters. However, the proposed technique exhibits a higher peak current of one MOSFET than PSM but guarantees soft switching of all four primary MOSFETs at light loading conditions for the designed $LLC$ resonant converter unlike PSM in which soft switching depends on the current oscillations due to component parasitics.

Fig. 21 shows the MOSFETs experimental waveforms of drain–source voltage, $V_{DS}$, gate-source voltage, $V_{GS}$, and resonant current, $i_{Ls}$, for all four primary MOSFETs operating under the

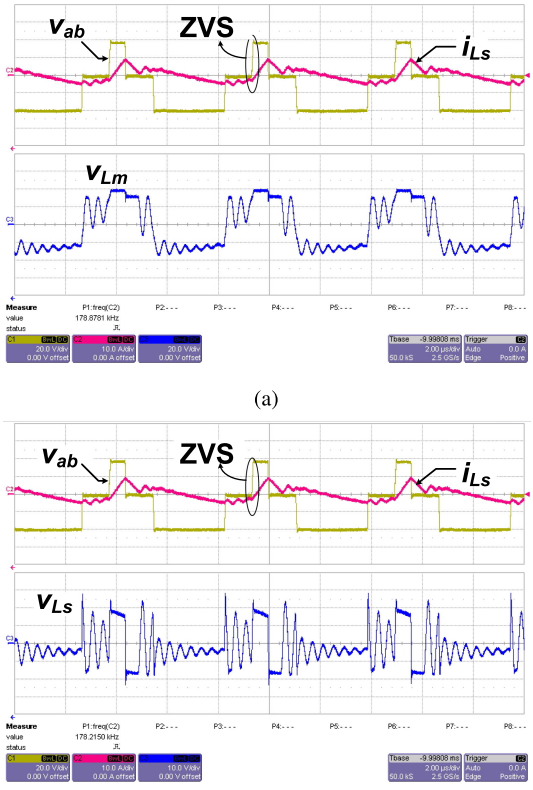



Fig. 23. Experimental waveforms at $V_{\text{in\_max}}$. (a) ZVS of primary MOSFETs at 10% load with primary magnetizing inductance voltage $v_{L_m}$ and (b) resonant inductor voltage, $v_{L_s}$.

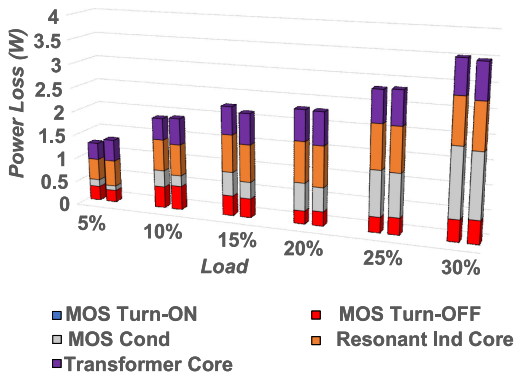



Fig. 24. Loss distribution versus load power for different input voltage.

proposed modulation technique. It was experimentally validated that dead-time requirement for leading leg MOSFETs $Q_1$ and $Q_2$ was higher due to lower turn-OFF current magnitudes during switching transition. Lagging leg MOSFETs $Q_3$ and $Q_4$ had sufficient inductive current during switching transition to ensure ZVS turn-ON. Therefore, true ZVS was experimentally exhibited at operating point of maximum input voltage $V_{\text{in\_max}} = 40$ V at 10% load condition. It was observed that the operating point at extreme light load conditions changed slightly from $D = 0.15$, $f_s = 179$ kHz to $D = 0.23$, $f_s = 177$ kHz. This was a result of duty-cycle oscillation from the PI controller and does not impact the ZVS performance. However, a future study regarding

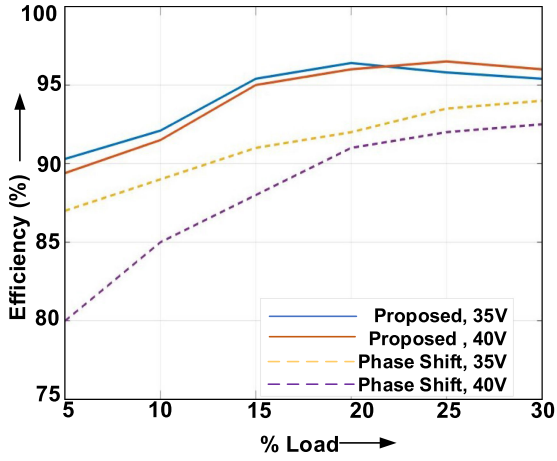



Fig. 25. Efficiency curve.

PI controllers based on small-signal analysis for the improved APWM $LLC$ converter will decrease these oscillations.

Since, the probability of achieving ZVS is least for $Q_1$ (least turn-OFF current of the lagging leg low-side switch $Q_2$), attaining ZVS for $Q_1$, consequently, signifies ZVS for all four primary MOSFETs. Fig. 22 shows the MOSFET drain–source voltage, $V_{\text{DS}}$, and gate–source voltage, $V_{GS}$, waveform for the switch $Q_1$ during the converter operation at $V_{\text{in\_max}} = 40$ V at 5% load operation. All four MOSFETs demonstrate ZVS at turn-ON transition with the proposed modulation scheme. A qualitative comparison of the proposed modulation technique and other modulation schemes for the light load $LLC$ converter performance is given in Table III. It is clear that, out of all the modulation techniques, only the proposed modulation technique can achieve true ZVS for a wide input voltage range with a minimal switching frequency range requirement. Experimental waveforms for $v_{L_m}$ and $v_{L_s}$ are shown in Fig. 23(a) and (b). The experimental loss distribution at $V_{\text{in}} = 35$ V and $V_{\text{in}} = 40$ V is provided in Fig. 24 for various load power operation. With a higher load power operation, the conduction losses dominated the magnetic core losses. MOSFET turn-OFF loss was significant at light loads due to the asymmetrical nature of the proposed modulation technique. Compared to efficiencies shown in a previous work [28], efficiency at 40 V improved by at least 1.5% at 10% load, as shown in Fig. 25, by incorporating the loss analysis in selection of duty cycle and switching frequency. However, at higher loads of 20% and above, where conduction losses become dominant, the efficiency gains were small.

## VIII. Conclusion

This article dealt with analysis of a full-bridge $LLC$ converter operation under a novel hybrid duty-cycle–switching-frequency modulation technique. Unlike existing modulation waveforms, a new asymmetrical modulation waveform applicable to any dc–dc resonant converter is proposed. The proposed modulation waveform is more suitable for attaining ZVS at light load operation in the presence of high parasitic capacitances. It damps out the circulating current arising due to the

interaction of resonant tank elements with converter parasitic capacitances, primarily $C_d$ and $C_j$, eliminating any possibility of multiple zero crossings of the resonant current evident in the conventional PSM. System losses were calculated for the nonideal $LLC$ converter (including effect of parasitics) using time-domain equations as a function of *D*. The existence of a dc bias in the magnetizing current was observed due to the modulation scheme, which should be considered during the transformer design. Preselected optimal duty ratios, which leads to minimum power losses at the light load condition, are selected at the upper input voltage range. Optimal combination of the preselected duty cycle (to achieve ZVS) and the corresponding required switching frequency (to regulate voltage) is selected such that both ZVS and output voltage regulation is obtained at light load conditions. ZVS at an extremely light load of 5% is demonstrated. The proposed modulation technique can be extended to any conventional dc–dc resonant converter topology.

## APPENDIX A
## VARIABLE DEFINITION FOR THE CONSTANT OUTPUT VOLTAGE

This appendix contains variables used for the initial resonant inductor current $i_{Ls}(0)$ and initial resonant capacitor voltage $v_{Cs}(0)$ for the proposed improved APWM technique in Section IV. Variables $\alpha_1$, $\alpha_{21}$, $\alpha_{22}$, and $\alpha_{23}$ have been defined in (A.4)–(A.7). $\alpha_2$ can be expressed as follows:

$$\alpha_2 = \alpha_{21} + \alpha_{22} + \alpha_{23}. \tag{A.1}$$

$\beta_1$ and $\beta_2$ can be expressed as follows:

$$\beta_1 = \frac{\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\left\{1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]\right\}}{Z_0\sqrt{1+K}} + \frac{\sin\left[\omega_r\left(t_1 + t_3\right)\right]\left\{1 - \cos([\omega_{r_1}\left(T_s - t_1 - t_3\right)]\right\}}{Z_0} \tag{A.2}$$

$$\beta_2 = \left\{1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]\right\}\left\{1 + \cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\right\} + \sqrt{1+K}\sin\left[\omega_r\left(t_1 + t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]. \tag{A.3}$$

## APPENDIX B
## VARIABLE DEFINITION FOR CONSTANT OUTPUT POWER EQUATIONS

This appendix contains variable definition for the proposed modulation scheme when analysis of a constant output power, variable output voltage condition is required. Similar to the analysis for the fixed output voltage condition, an iterative function in terms of the unknown time instant $t_3$ is framed as $f_{\text{fixedpower}} = f(t_1 + t_3)$ which has been expressed in (B.1) shown at the top of this page. $\alpha_{1\_V_i}$, $\alpha_{1\_V_o}$, $\alpha_{2\_V_i}$, and $\alpha_{2\_V_o}$ have been are the variables used in $f_{\text{fixedpower}}$. These have been defined in (B.2)–(B.5) shown at the top of this page. It should be noted

$$\alpha_1 = \left[\frac{V_i\sin\left(\omega_r t_3\right)}{Z_0} + \frac{nV_o}{L_m\left\{1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]\right\}}\left(t_1 + t_3\right)\right]\left[\begin{array}{l}1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right] \\ + \left(\frac{1}{\sqrt{1+K}}\right)\sin\left[\omega_r\left(t_1 + t_3\right)\right]\sin\left\{\omega_{r_1}\left[\left(T_s - t_1 - t_3\right)\right]\right\}\end{array}\right] + \frac{nV_o\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]}{Z_0\sqrt{1+K}} - V_i\left[\frac{\sin\left(\omega_r t_3\right)\cos\left\{\omega_{r_1}\left[\left(T_s - t_1 - t_3\right)\right]\right\}}{Z_0} + \frac{\cos\left(\omega_r t_3\right)\sin\left\{\omega_{r_1}\left[\left(T_s - t_1 - t_3\right)\right]\right\} + \sin\left\{\omega_{r_1}\left[\left(t_6 + t_8\right)\right]\right\} - \sin\left(\omega_{r_1} t_8\right)}{Z_0\sqrt{1+K}}\right] \tag{A.4}$$

$$\alpha_{21} = V_i\left[1 + \cos\left(\omega_{r_1} t_8\right) - \cos\left[\omega_{r_1}\left(t_6 + t_8\right)\right] - \cos\left(\omega_r t_3\right)\cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right] + \left(\frac{\omega_r}{\omega_{r_1}}\right)\sin\left(\omega_r t_3\right)\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\right] \tag{A.5}$$

$$\alpha_{22} = V_i\left[\frac{\sin\left(\omega_r t_3\right)}{1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]}\right]\left[\begin{array}{l}\sin\left[\omega_r\left(t_1 + t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right] \\ +\sqrt{1+K}\cos\left[\omega_r\left(t_1 + t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\end{array}\right] \tag{A.6}$$

$$\alpha_{23} = -nV_o\left[\left\{1 - \cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\right\} + \left[\frac{Z_0\left(t_1 + t_3\right)}{L_m\left\{1 - \cos\left[\omega_r\left(t_1 + t_3\right)\right]\right\}}\right] \times \left\{\begin{array}{l}\sin\left[\omega_r\left(t_1 + t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right] \\ +\sqrt{1+K}\cos\left[\omega_r\left(t_1 + t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s - t_1 - t_3\right)\right]\end{array}\right\}\right] \tag{A.7}$$

$$f(t_1+t_3) = P_o - \frac{V_{o\_\text{calc}}}{nT_s}\left[\frac{\alpha_{1\_V_i}\left[2\left[1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right]-\omega_r\left(t_1+t_3\right)\sin\left[\omega_r\left(t_1+t_3\right)\right]\right]}{\beta_1\omega_r^2 L_s}\right.$$
$$- \frac{V_i\left[1+\cos\left(\omega_r t_1\right)-\cos\left(\omega_r t_3\right)-\cos\left[\omega_r\left(t_1+t_3\right)\right]-\omega_r\left(t_1+t_3\right)\sin\left(\omega_r t_3\right)\right]}{\omega_r^2 L_s\left(1-\cos\left(\omega_r\left(t_1+t_3\right)\right)\right)}$$
$$\left. - \frac{V_{o\_\text{calc}}\left(t_1+t_3\right)\left[\sin\left[\omega_r\left(t_1+t_3\right)\right]-\omega_r\left(t_1+t_3\right)\right]}{n\omega_r L_m\left(1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right)+\omega_r\left(\frac{t_1^2}{2}+\frac{t_3^2}{2}+t_1t_3\right)}\right] \tag{B.1}$$

$$\alpha_{1\_V_i} = \frac{V_i\sin\left(\omega_r t_3\right)}{\omega_r L_s\left(1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right)}\left[\left[1-\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]+\frac{1}{1+K}\sin\left[\omega_r\left(t_1+t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right]\right.$$
$$\left. - \left[\frac{1}{Z_0\sqrt{1+K}}\left[\cos\left(\omega_r t_3\right)\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]+\sin\left[\omega_{r_1}\left(t_6+t_8\right)\right]-\sin\left(\omega_{r_1}t_8\right)\right]\right]\right] \tag{B.2}$$

$$\alpha_{1\_V_o} = \frac{t_1+t_3}{nL_m\left(1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right)}\left[1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right.$$
$$+\frac{1}{1+K}\sin\left[\omega_r\left(t_1+t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]$$
$$\left. + \frac{K}{\omega_r\sqrt{1+K}\left(t_1+t_3\right)}\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\left[1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right]\right] \tag{B.3}$$

$$\alpha_{2\_V_i} = V_i\left[\left[1+\cos\left(\omega_{r_1}t_8\right)\right]-\cos\left[\omega_{r_1}\left(t_6+t_8\right)\right]-\cos\left(\omega_r t_3\right)\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right.$$
$$+(1+K)\sin\left(\omega_r t_2\right)\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]$$
$$+\frac{\sin\left(\omega_r t_3\right)}{\left[1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right]}\sin\left[\omega_r\left(t_1+t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]$$
$$\left.+(1+K)\cos\left[\omega_r\left(t_1+t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right] \tag{B.4}$$

$$\alpha_{2\_V_o} = \frac{1-\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]}{n}-\frac{\omega_r\left(t_1+t_3\right)}{nK\left[1-\cos\left[\omega_r\left(t_1+t_3\right)\right]\right]}\left[\sin\left[\omega_r\left(t_1+t_3\right)\right]\cos\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right.$$
$$\left.+(1+K)\cos\left[\omega_r\left(t_1+t_3\right)\right]\sin\left[\omega_{r_1}\left(T_s-t_1-t_3\right)\right]\right] \tag{B.5}$$

that $\beta_1$ and $\beta_2$ variables remain the same as defined in (A.2) and (A.3), respectively, in Appendix A. $V_{o\_\text{calc}}$ is the output voltage at different operating conditions such that the output power is constant (B.6)

$$V_{o\_\text{calc}} = \frac{\alpha_{2\_V_i}\beta_1-\alpha_{1\_V_i}\beta_2}{\alpha_{1\_V_o}\beta_2+\alpha_{2\_V_o}\beta_1}. \tag{B.6}$$

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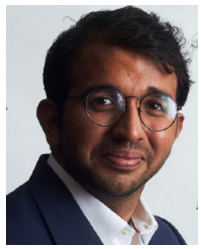

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