Analysis and Suppression of Common-Mode EMI Noise in 1 MHz 380 V-12 V DCX Converter With Low NFoM Devices

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***Abstract*—For the thriving information technology industrial applications, the series resonant converter (SRC) dc transformer (DCX) using integrated printed circuit board (PCB) windings is a preferred candidate because of its high efficiency and high power density characteristics by pushing the frequency to megahertz. However, the planar PCB transformer possesses large interwinding capacitance, which leads to severe common-mode (CM) noise and a large electromagnetic interference filter. Hence, the total volume of the conversion system is still high. In this article, a series inputs and parallel outputs (ISOP) structure for DCX is analyzed and discussed to demonstrate the CM noise reduction with the static point construction method, in which several *dv/dt* static points are constructed. Unlike most of the present suppressing methods, it can maintain high efficiency as well. Additionally, the ISOP structure provides more opportunities for optimizing control strategies to achieve the cancelation effect and further reducing the CM noise by the interleaving within a cell and the interleaving among cells. The excellence of the aforementioned methods is verified by experiments on 1-MHz 380 V–12 V 1.8-kW SRC DCX prototypes with a peak efficiency of 98.3%. The proposed methods ultimately reduce the CM noise by 50 dB.**

***Index Terms*—Cancelation method, common-mode (CM) noise, interleaving, planar transformer, static point construction.**

I. Introduction

With the rapid development of industrial technology, the power consumption of data centers is more and more tremendous. In 2016, global data centers consumed 416 billion kWh, which occupies more than 40% of the total electricity consumption of the U.K. [1]. Even worse, the limited total conversion efficiency in the current data center power architecture leads to a massive waste of electricity, which is caused by both the large loss on the 12 V bus and too many power conversion stages. In order to reduce the substantial power delivering loss in the cable, industry leaders, such as Google and IBM, are implementing a new data center architecture with a higher voltage distribution bus, such as 48 or 380 V instead of 12 V [2]–[8]. A board-mounted dc/dc power module is deemed to be superior since it helps to save an amount of conduction loss caused by the large current in the printed circuit board (PCB) traces of the motherboard. However, it brings higher requirements for power density and efficiency at the same time.

For the consideration of high efficiency, the series resonant converter (SRC) is a preferred candidate because it can run up to megahertz, operating at the fixed neighboring resonant frequency and maximize the efficiency [9]–[11]. For the purpose of improving the power density of the dc/dc converter, the planar PCB transformer is widely adopted in present dc/dc modules. Furthermore, in order to reduce the eddy current and improve the efficiency under megahertz frequency, an interleaved winding structure is quite essential [11]–[15]. However, the planar PCB with interleaved windings has an extremely large interwinding capacitance, which causes a dramatic increase in the common-mode (CM) current in the megahertz converters; and the electromagnetic interference (EMI) filter will be much larger. Many interesting methods have been proposed to reduce CM noise in planar PCB transformers, such as shielding technique, cancelation technique, and balance technique [13]–[23]. The shielding technique is to insert a shielding layer between the adjacent primary windings and secondary windings to block the displacement current flowing through the interwinding capacitance [13]–[15]. Yang *et al*. [13] adopted the shielding method in a hybrid transformer structure, where the primary windings use Litz wire and the secondary windings use PCB, which reduces the CM noise by 13 dB. Yang *et al*. [14] further adopted this shielding method in the *LLC* converter using the matrix transformer with PCB windings, which achieves a 22 dB CM noise attenuation because of a better symmetrical winding structure. Based on the article presented in [14], Fei *et al*. [15] add one of the two shielding layers into the primary windings to improve the efficiency and reduce the CM noise at the same time. However, the shielding method needs additional layers, which makes the structure more complicated, especially for the interleaved PCB

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windings. The cancelation technique includes two types, rearranging the transformer windings or adding more components. For the technique of rearranging the transformer windings, there are several interesting ideas. Paired layers conception is defined in [16] to make the primary and secondary windings with the same *dv/dt* adjacent to each other, and it can be easily adopted by different transformers regardless of the turn ratio, the number of layers, and the material of windings. However, it will increase the loss of the primary windings. A symmetrical transformer and topology with the cancelation technique are constructed in [17], which reduces the CM noise by 20 dB in total. In [18], the primary and the secondary windings are avoided to be overlapped to construct a transformer without interwinding capacitance. The cancelation technique can also be applied to the peripheral topology. In [19], only the position of the components is changed to generate the cancelation effect, and no extra components are needed. Nevertheless, there is a constraint on the suitable types of topology. For the cancelation technique based on the adding components, an auxiliary winding is normally added to generate an opposite current to counteract the original one [20]–[22]. By properly designing the antiphase winding, the CM noise can be reduced by 30 dB in [20]. However, it will bring a large terminal loss for large output current applications. Besides, to achieve a better cancelation effect, compensation capacitors are often needed, which makes the converter more complex and the accuracy of the cancelation is hard to control due to the tolerance of the components [21], [22]. The balance technique is to construct a Wheatstone bridge to neglect the effect of the CM noise. By adding balanced chokes and further coupling the balanced chokes, the CM noise is reduced by 52 dB in [23]. However, the additional chokes will decrease the power density of the converters.

In this article, a static point construction method is adopted to reduce the CM noise, and a series inputs and parallel outputs (ISOP) SRC converter is implemented with the method. Taking the advantage of the ISOP converter, the high-voltage devices are replaced by multiple low-voltage devices to reduce the conduction losses in the SRC converter with megahertz switching frequency [24], as shown in Fig. 1. It has been proved that a peak efficiency of 98.3% can be achieved with a proper design. Furthermore, the ISOP structure reduces the switching transition voltage significantly and brings more possibilities of control mode. Two control strategies are presented in this article to suppress the CM noise further, and they are verified in a 380 V–12 V dc transformer (DCX) prototype. The static point construction method and the initial experimental results are reported in [25]. More details about the optimal control strategies and the experimental results are presented in this article.

II. Analysis of CM Noise in 380 V-12 V DCX Converter

The schematic of half-bridge Synchronized rectifier (SRC) with Line impedance stabilization network (LISN) is shown in Fig. 2. The switching process of devices at high frequency generates large *dv/dt*, which causes severe CM noise. In unregulated SRC, the leakage inductance serves as the resonant inductance L_r, so the L_r distributes inside of the transformer

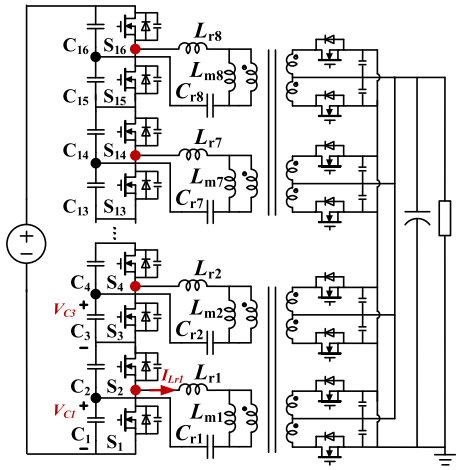


Fig. 1. Schematic of the ISOP converter with low-voltage devices [24].

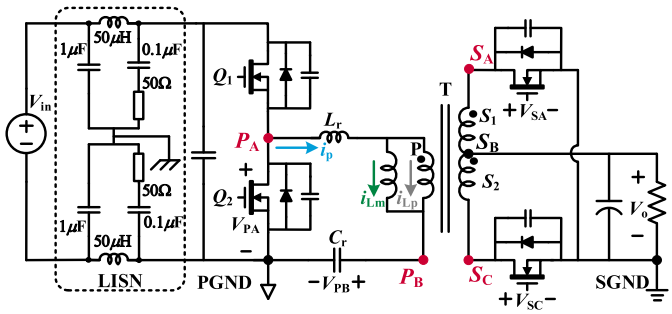


Fig. 2. Half-bridge SRC schematics.

windings actually. Thus, the large *dv/dt* induced on the primary middle point P_A is also on one of the primary winding terminals. On the other hand, the *dv/dt* induced on the drains of two SRs (S_A and S_C) is on one of the secondary winding terminals.

Within the conducting EMI testing frequency range (150 kHz–30 MHz), the input and output capacitances are large enough so that they can be treated as short branches [26], [27]. From Fig. 2, the voltage waveforms V_{PA}, V_{SA}, and V_{SC} are trapezoid waves so that the switching devices can be replaced by the equivalent voltage sources [28]. Then, the equivalent circuit for CM noise analysis can be drawn in Fig. 3(a). For that the resonant capacitor C_r is large, the voltage ripple on it is small, so it has a faint effect on the fundamental frequency of CM noise even under full load. As for the leakage inductance L_r distributed in the windings, when one of the primary switches is ON, the absolute value of the voltage on L_r is the same as the C_r and the phases of them are opposite as the SRC works at the resonant frequency. It is obvious that the effect of L_r on the fundamental frequency of CM is very small during this time. However, during the deadtime when all of the primary switches are OFF, $L_r$will oscillate with the parasitic capacitors of the transformer and the MOSFETs. For the components in this article, the leakage inductance L_r is 10 nH or so and the equivalent parasitic capacitance is smaller than 2 nF. Thus, the oscillation frequency in the deadtime is more than 30 MHz. This oscillation on the leakage inductance also has a faint effect on the

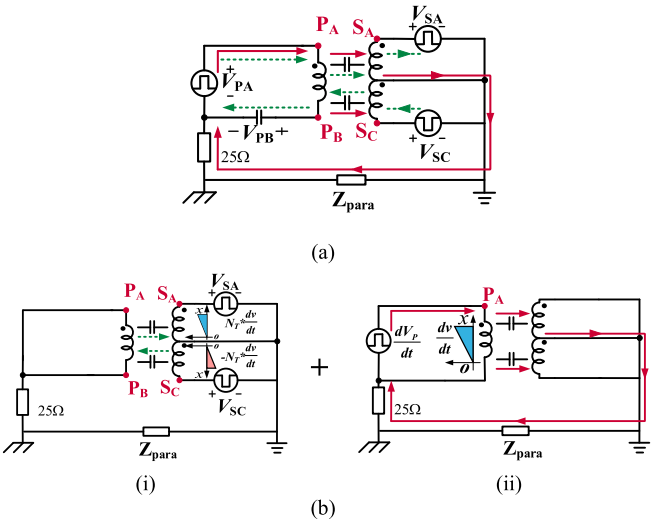


Fig. 3. CM equivalent circuit of half-bridge SRC. (a) Equivalent circuit. (b) Equivalent circuits when considering the primary and secondary noise source separately.

fundamental frequency of CM noise in the proposed structure. Thus, for simplification, L_r and C_r can be neglected when the mainly concentrated frequency for the CM noise is lower than 30 MHz.

Then, using the superposition theorem [28], the effect of each source with large *dv/dt* can be analyzed separately. Thus, the equivalent circuit in Fig. 3(a) can be divided into the equivalent circuit in Fig. 3(b)(i) and (ii). In Fig. 3(b)(i), the two sources on the secondary side, V_{SA} and V_{SC}, are out-of-phase with the same magnitude. Thus, when planar PCB windings are used, the two secondary windings can be arranged on each side of the primary windings, which is exactly what we did in this article. Thus, the $N_T \cdot dv_p/dt$ and the $-N_T \cdot dv_p/dt$ (N_T is the transformer ratio) generated on the two secondary windings will cancel the CM current on the primary windings, as the interwinding capacitances is almost the same when using symmetrical PCB windings. Therefore, in Fig. 3(b)(ii), the *dv/dt* generated by the primary switches becomes the main CM noise in the proposed structure, which is defined as dv_p/dt.

Assuming that the CM noise source induces a linear *dv/dt* distribution on the primary windings, the CM noise path is depicted by the red line in Fig. 3(b)(ii). Since the impedance of the CM noise path is related to the transformer structure, the transformer structure should be detailed at first. For the application with a large output current, the matrix transformer structure is preferred since it can help to increase the output capability by distributing the secondary current among multiple cores and windings [10], [11]. Therefore, four independent transformers are chosen to handle the large output current. In order to compare the CM noise between the SRC converters with high-voltage devices and that with low-voltage devices [24], the transformers are designed to be the same. The simplified system block diagrams are shown in Fig. 4. As the turn ratio *N* of the SRC is 16:1:1, the turns ratio of each transformer is 4:1:1. To achieve high power

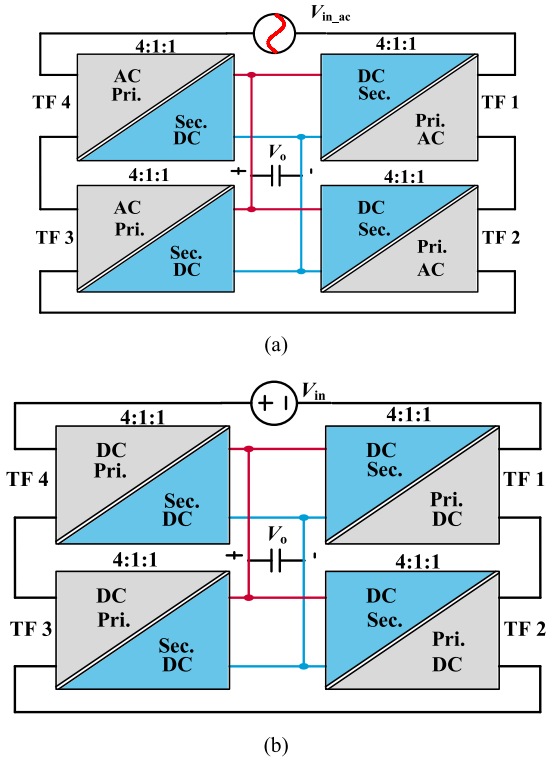


Fig. 4. Simplified system block diagram of the four independent cell circuits. (a) Series connection at a high-frequency terminal with high-voltage switches. (b) Series connection at dc input with low-voltage devices.

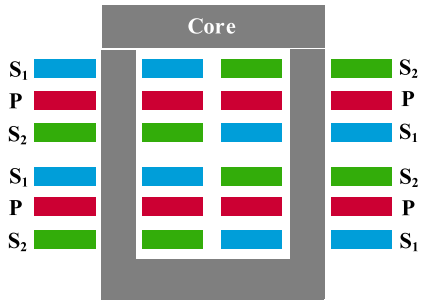


Fig. 5. Structure of each independent transformer.

density, the planar transformer with PCB windings is used. To make full use of the PCB and achieve high efficiency, all the six layers of PCB are used to construct the transformer windings that transfer large current. The winding arrangement of each independent transformer is given in Fig. 5, where *P* represents the primary windings, and S_1 and S_2 represent the center-tapped secondary windings. Fig. 6 shows the layout of all the six layers in each independent transformer, where the same secondary windings in the corresponding position are paralleled, such as S_1 in Layer 1 and S_1 in Layer 4. It can be seen that the windings are fully interleaved and the structure is highly symmetrical, which reduces the eddy current effect and guarantees a similar interwinding capacitance between every two vertically adjacent windings.

In order to calculate the total CM current of the whole transformer, one pair of the adjacent primary and secondary windings

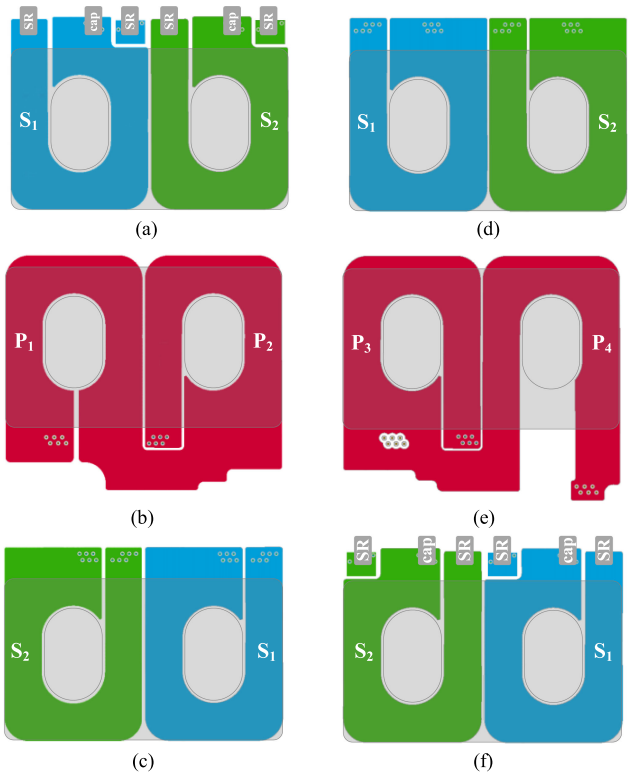


Fig. 6. Six-layer PCB layout for each independent transformer. (a) Layer 1. (b) Layer 2. (c) Layer 3. (d) Layer 4. (e) Layer 5. (f) Layer 6.

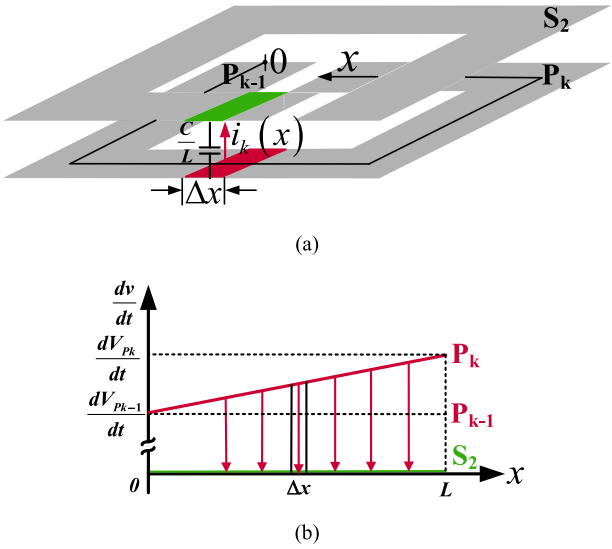


Fig. 7. One pair of the adjacent primary and secondary winding. (a) Physical model. (b) *dv/dt* distribution along windings.

is analyzed as an example. Fig. 7 shows the physical model and the *dv/dt* distribution along the windings, where $P_{k\text{-}1}$ and P_k represent the two terminals of the kth primary turn. Establishing the x-axis along the windings, the CM current through the infinitesimal capacitance at position x is expressed in (1), where the length of one turn is L, and the physical interwinding capacitance of one turn is C. The CM current generated by the kth primary turn is expressed in (2). It is illustrated that the CM

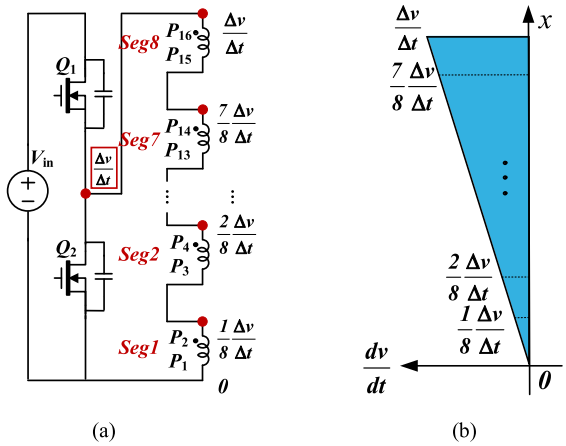


Fig. 8. Distribution of *dv/dt* along primary windings in the conventional SRC DCX. (a) Schematic of the primary side. (b) Distribution of *dv/dt*.

current induced by one primary turn is proportional to the sum of the *dv/dt* on two terminals of the specific primary turn.

$$i_k(x) = \frac{C}{L} \cdot \left[\frac{dV_{P_{k-1}}}{dt} + \left(\frac{dV_{P_k}}{dt} - \frac{dV_{P_{k-1}}}{dt} \right) \cdot \frac{x}{L} \right] \tag{1}$$

$$I_k = \int i_k(x) = C \cdot \frac{1}{2} \cdot \left(\frac{dV_{P_{k-1}}}{dt} + \frac{dV_{P_k}}{dt} \right). \tag{2}$$

Applying this conclusion, the CM current of the whole transformer can be derived. The *dv/dt* distribution on the primary windings is drawn in Fig. 8, where the *dv/dt* generated by the primary middle point is defined as $\Delta v/\Delta t$. According to Fig. 6(b), in order to reduce the vias' losses in PCB windings, two primary turns (P_1 and P_2) are arranged in one layer for a single magnetic core with two magnetic legs, as well as that in Fig. 6(e). For the sake of convenience, the two serial primary turns are defined as one segment, so 16 primary turns can be separated into 8 segments, as shown in Fig. 8(a). Then, the interwinding capacitance between Seg1 in Fig. 6(b) and secondary windings in Fig. 6(a) [or Fig. 6(c)] can be defined as C_{11} (or C_{12}). For that the layout of the windings is symmetrical, it can be assumed that $C_{11} = C_{12} = \cdots = C_{81} = C_{82} = C$ for simplification. Then, the CM current i_{CM} can be calculated as

$$\begin{aligned} I_{\mathrm{CM}} = {} & (C_{11} + C_{12}) \cdot \frac{1}{2} \cdot \left(0 + \frac{1}{8} \frac{\Delta v}{\Delta t} \right) \\ & + \cdots + (C_{81} + C_{82}) \cdot \frac{1}{2} \cdot \left(\frac{7}{8} \frac{\Delta v}{\Delta t} + \frac{\Delta v}{\Delta t} \right) \\ = {} & 8C \frac{\Delta v}{\Delta t} \end{aligned} \tag{3}$$

From (3), the factors that determine the magnitude of CM current are C (physical interwinding capacitance of one turn) and $\Delta v/\Delta t$ (potential change at the primary middle point). This conclusion is consistent with the common sense that the $\Delta v/\Delta t$ generated by the switching points determines the CM current. However, when it comes to the CM noise, a physical quantity in the frequency domain, the conclusion is quite different because

the influence of frequency should also be considered. Applying the Fourier transform, the CM current can be derived in (4), and the magnitude of the fundamental frequency can be expressed in (5). From (5), Δv is a direct factor that influences the $I_{\mathrm{CM(fun)}}$ linearly, but Δt is only in the fraction part, so its impact is not obvious. In general, Δt can be arbitrary, but $\Delta t \cdot f_s$ reflects the duty cycle, which usually varies from 0.05 to 0.25 to guarantee the high efficiency. However, even when it changes from 0.05 to 0.25, the effect it brings to the magnitude of the fundamental frequency is within 1 dB. In conclusion, Δt has a slight impact on the fundamental frequency, but Δv is the determining factor for the fundamental frequency of CM noise. In the design process of the EMI filters, the magnitude of the fundamental frequency for the CM noise is the most important, which means Δv is the key factor in EMI filter design but not the $\Delta v/\Delta t$ anymore. In this case, when trying to suppress CM noise, the best way is to reduce Δv. The details will be elaborated in Section III

$$I_{\mathrm{CM}}(t) = 32C \cdot \Delta v \cdot f_s \cdot \sum_{n=1,3,5\ldots}^{\infty} (-1)^{\frac{n-1}{2}} \frac{\sin(n\pi \cdot \Delta t \cdot f_s)}{n\pi \cdot \Delta t \cdot f_s} \sin(2n\pi f_s t) \tag{4}$$

$$I_{\mathrm{CM(fun)}} = 32C \cdot \Delta v \cdot f_s \cdot \frac{\sin(\pi \cdot \Delta t \cdot f_s)}{\pi \cdot \Delta t \cdot f_s}. \tag{5}$$

III. Low CM Noise Converter With Input Series Topology and Interleaved Control Strategies

According to the distribution *of dv/dt* along windings, as shown in Fig. 8(b), the winding Seg1 in Fig. 8(a), which connects to the source of Q_2, has the smallest *dv/dt*. The source of Q_2 with no *dv/dt* can be defined as a static point. The *dv/dt* increases to the largest as the winding Seg8 is connected to the primary middle point. Actually, the large CM current in the conventional DCX converter is caused by the accumulation of the increasing *dv/dt* distributed along the primary windings.

If all the winding sets of the primary side have the same *dv/dt* distribution as Seg1; in other words, several static points with no *dv/dt* are constructed, the CM current could be significantly suppressed. As the analysis mentioned above, one half-bridge topology owns one static point. In order to construct enough static points, several half-bridge topologies are connected in series. The ISOP structure constructed with enough static points is adopted to reduce the CM noise, and the method is defined as the static point construction method. But in the input series scheme, a large amount of switching devices are needed to construct the ISOP converter. Theoretically, more half-bridge topologies in series lead to smaller CM noise, and the devices with a lower new figure of merit (NFoM) can be used. However, when taking the conduction loss and the total cost into consideration, the number of the half-bridge topology also has a restriction. With proper design, it has been proved that using 16 low-voltage devices instead of two high-voltage devices can achieve higher efficiency [24]. Thus, eight half-bridge topologies with 16 low-voltage devices are chosen to replace the conventional DCX.

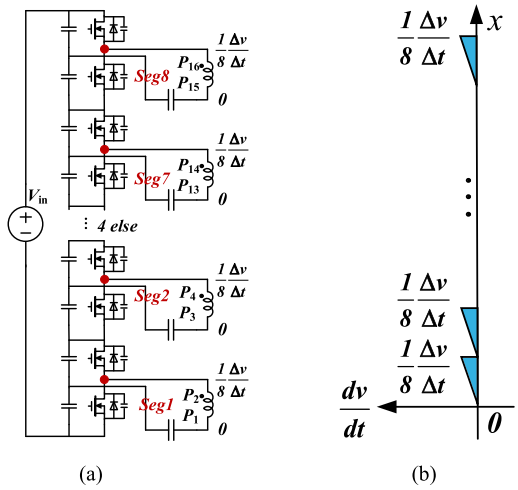


Fig. 9. *dv/dt* distribution along primary winding in ISOP converter. (a) Schematic of the primary side. (b) *dv/dt* distribution.

For the purpose of calculating the CM current in the ISOP converter, the *dv/dt* distribution along the primary windings is given in Fig. 9. As shown in Fig. 9, each half-bridge topology has a static point with no *dv/dt*, so the *dv/dt* generated by the primary windings can be reduced drastically. The total CM current in the ISOP structure is recalculated as $I_{\mathrm{CM}}{}'$ in (6). Compared with (3), the ISOP converter with the static point construction method can reduce the CM current to one-eighth. The predicted CM noise reduction effect Q_{CM} (dB) is expressed in (7). From the calculation result, the reduction of the CM current can be 18 dB

$$I_{\mathrm{CM}}{}' = 8\left[(C_{11}+C_{12}+\cdots+C_{81}+C_{82}) \cdot \frac{1}{2} \cdot \left(0+\frac{1}{8}\frac{\Delta v}{\Delta t}\right)\right] = C \cdot \frac{\Delta v}{\Delta t} \tag{6}$$

$$Q_{\mathrm{CM}} = 20 \cdot \log\left(\frac{i_{\mathrm{CM}}{}'}{i_{\mathrm{CM}}}\right) = -18\ \mathrm{dB}. \tag{7}$$

Since several half-bridge topologies are connected in series, the control strategy of the converter becomes more diverse, which provides more opportunities to suppress the CM noise further. In order to explain the strategies more clearly, two half-bridge topologies that share the same transformer core are defined as a cell in Fig. 10. Two control strategies are proposed here to reduce the CM noise, and their names are the interleaving within an independent magnetic core and the interleaving among different magnetics, respectively. In order to simplify the definition, one magnetic core and corresponding circuits named cell circuit in Fig. 10.

In the previous in-phase control strategy, as shown in Fig. 10(a), two half-bridge topologies in a cell operate at the same time, and the CM current generated by each topology has the same direction. Thus, the CM current of the cell is twice the magnitude of the CM current in one half-bridge topology. In order to construct a cancelation effect, the two topologies in a cell need to operate at the opposite time, and the CM current

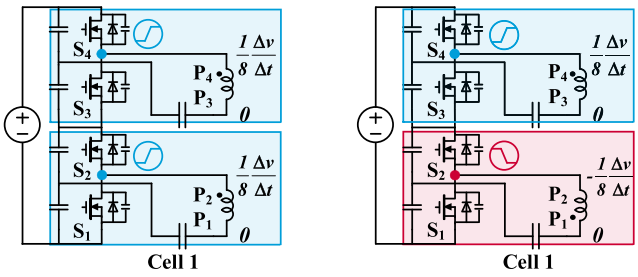


Fig. 10. Schematic comparison of in-phase control and interleaving within a cell control. (a) Cell with in-phase control strategy. (b) Cell with interleaving within a cell control strategy.

generated by them can have the opposite directions with the same magnitude. Thus, the CM current generated by the two topologies in a cell can be counteracted, and the CM noise can be reduced. This control strategy is defined as the interleaving within a cell, and the schematic is shown in Fig. 10(b).

Using the interleaving within a cell strategy, the CM current is recalculated in (8). It can be seen that the CM noise can be reduced to 0 if $C_{11} = C_{12} = \cdots = C_{81} = C_{82} = C$ can be realized. However, the layout of the two topologies in a cell [see Fig. 6(b) and (e)] is not perfectly identical in order to make way for the vias. And there is a slight deviation in the interwinding distance due to the tolerance of the PCB process. Thus, the interwinding capacitance for Fig. 6(b) $(C_{11} + C_{12})$ and (e) $(C_{21} + C_{22})$ is a bit different, so the CM noise cannot be eliminated entirely

$$I_{\mathrm{CM1}} = \left[(C_{11}+C_{12})\cdot\frac{1}{2}\cdot\left(0+\frac{1}{8}\frac{\Delta v}{\Delta t}\right)+(C_{21}+C_{22})\cdot\frac{1}{2}\cdot\left(0-\frac{1}{8}\frac{\Delta v}{\Delta t}\right)\right] + \ldots + \left[(C_{71}+C_{72})\cdot\frac{1}{2}\cdot\left(0+\frac{1}{8}\frac{\Delta v}{\Delta t}\right)+(C_{81}+C_{82})\cdot\frac{1}{2}\cdot\left(0-\frac{1}{8}\frac{\Delta v}{\Delta t}\right)\right]. \quad (8)$$

The other control strategy interleaving among cells is proposed to suppress the CM noise further, and the simplified schematic is shown in Fig. 11. Here, only two cells are drawn to simplify the schematic. The essence of this strategy is to construct a cancelation effect among cells. For example, control the switches in Cells 1 and 4 operating at the opposite time, and so do the switches in Cells 2 and 3. Hence, the CM current generated by these two cells can be counteracted. The CM current with interleaving among cells is expressed in (9). For that the four transformers are integrated into the same PCB, the layout and the interwinding distance of them are almost the same. Therefore, the cancelation effect of this strategy can be much better than that of interleaving within a cell. Furthermore, these two control strategies can be combined to reduce the CM noise, and the cancelation effect within the single cell and among cells can exist at the same time. In this way, the CM noise can

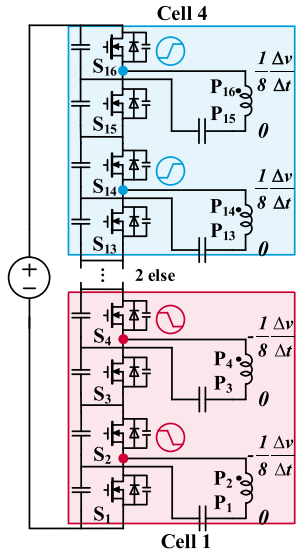


Fig. 11. Schematic of interleaving among cells control strategy.

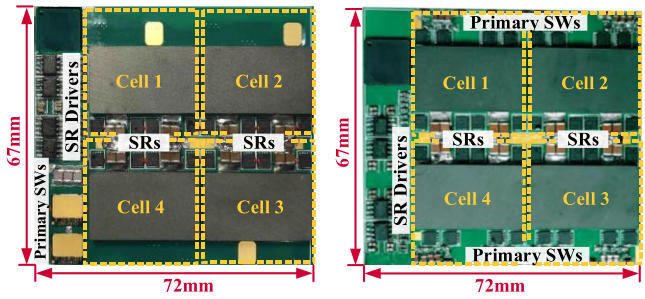


Fig. 12. 380 V–12 V 1 MHz DCX prototypes with about 900 W/in^3. (a) Prototype of the conventional DCX with high-voltage devices. (b) Prototype of the ISOP converter with low-voltage devices.

be the smallest

$$I_{\mathrm{CM2}} = \left[(C_{11}+C_{12})\cdot\frac{1}{2}\cdot\left(0+\frac{1}{8}\frac{\Delta v}{\Delta t}\right)+(C_{21}+C_{22})\cdot\frac{1}{2}\cdot\left(0+\frac{1}{8}\frac{\Delta v}{\Delta t}\right)\right] + \ldots + \left[(C_{71}+C_{72})\cdot\frac{1}{2}\cdot\left(0-\frac{1}{8}\frac{\Delta v}{\Delta t}\right)+(C_{81}+C_{82})\cdot\frac{1}{2}\cdot\left(0-\frac{1}{8}\frac{\Delta v}{\Delta t}\right)\right] \approx 0. \quad (9)$$

IV. Experimental Verifications and Analysis

In order to verify the effect of the static point construction method and the two optimal control strategies, two 380 V–12 V 1 MHz DCX prototypes with a rated output current 150 A are built up. One is constructed with two high-voltage devices using the conventional structure, and the other one is constructed with 16 low-voltage devices using the static point construction method. The two prototypes are shown in Fig. 12(a) and (b),

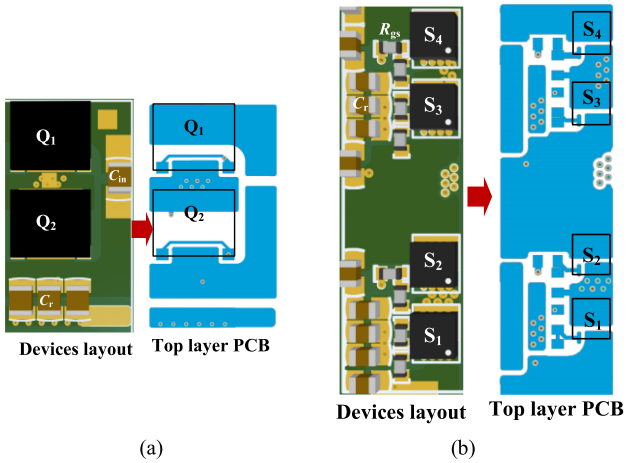


Fig. 13. Layout comparison of primary switching devices. (a) Layout of the conventional DCX. (b) Layout of a single cell in ISOP converter.

TABLE I
KEY PARAMETERS OF TWO 380 V-12 V PROTOTYPES

Parameters of main components	
SRs	BSZ0501NSI
Primary SW	GS66516T / BSZ040N06LS5
C_r / L_r	1.25uF / 14.2nH
L_m	1.8uH
U/I Core / Ratio	DMR51W / 4:1:1
C_{in}	2.2uF/50V
C_o	10uF/50V
PCB	6 Layer/2oz

respectively. The layout of the primary switching devices in the conventional DCX and ISOP converter is given in Fig. 13(a) and (b), respectively. The layout of the transformer windings and the secondary rectifiers are almost the same for these two prototypes. The key parameters of the main components in DCX prototypes are given in Table I.

The experimental waveforms of the conventional DCX under light load are shown in Fig. 14(a). It is obvious that the Zero voltage switching (ZVS) of the primary switches is achieved since the drain-source voltage of the two switches is reduced to zero during the deadtime. The experimental waveforms of a half-bridge topology in the ISOP structure under light load are shown in Fig. 14(b). From this figure, the ZVS ON for all switches is achieved in such a single half-bridge topology. Similarly, all the eight half-bridge topologies in the ISOP converter are guaranteed ZVS operation, and the waveforms are the same as Fig. 14(b). Besides, no matter which optimal control strategy is adopted, the ZVS of each topology is achieved. Fig. 14(c) shows the voltage waveforms of the static points in the ISOP structure (see Fig. 9). It can be seen that the voltage is static even at switching moments. Thus, the static points can be guaranteed and the accumulation of the increasing *dv/dt* along the primary windings can be reduced significantly.

The measured CM noise spectrum of the conventional SRC DCX with high-voltage devices is shown by the dashed black

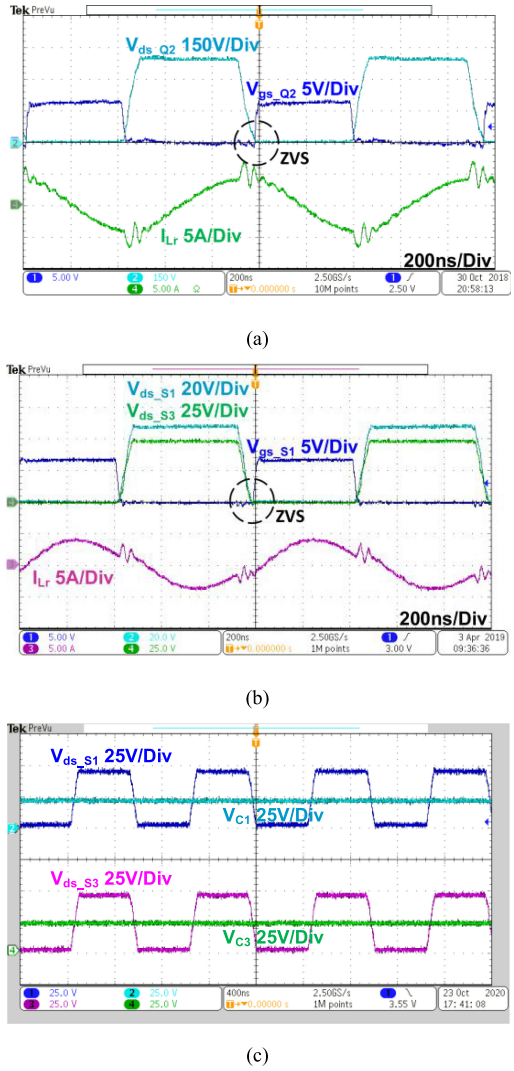
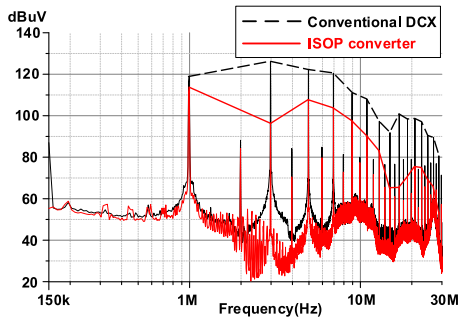


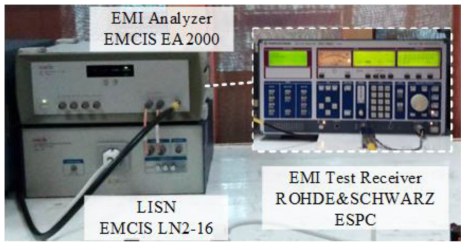
Fig. 14. Experimental waveforms under a light load. (a) Waveforms of the conventional DCX. (b) Key waveforms of a half-bridge topology in the ISOP structure. (c) Voltage waveforms of the static points in the ISOP structure.

envelope curve in Fig. 15(a). Using the static point construction method, the measured CM noise spectrum of the ISOP converter with low-voltage devices is shown by the red envelope curve. Fig. 15(b) shows the method for the EMI measurement. By comparing the two curves in Fig. 15(a), it is evident that the static point construction method reduces the CM noise by 10 dB on fundamental frequency 1 MHz and 20 dB on average within the whole testing frequency range.

When combining the methods of interleaving within one cell and among cells, the CM noise and the CM current can be reduced further, then the measured efficiency of the ISOP converter is given in Fig. 16, where the peak efficiency of the ISOP converter is 98.3% under 40% load. For the prototype with high-voltage GaN devices for which the CM noise of it is too large, the calculated efficiency is shown for comparison, which is a little bit lower than that of the ISOP structure. The cost and loss comparison between the conventional single half-bridge structure and the proposed ISOP structure using 16 switches is



(a)



(b)

Fig. 15. (a) Comparison of the measured CM noise spectrums in the conventional DCX and ISOP converter with static point construction method. (b) EMI measurement method in this article.

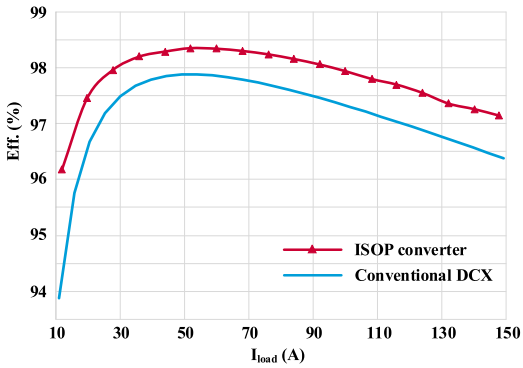
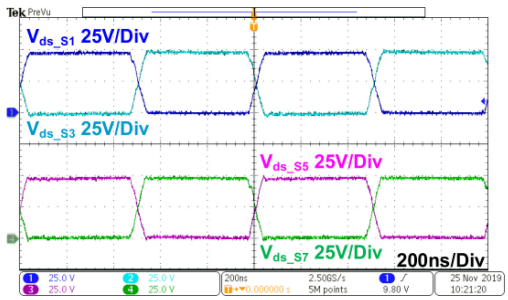


Fig. 16. Measured efficiency of the ISOP converter and the calculated efficiency of the conventional DCX.

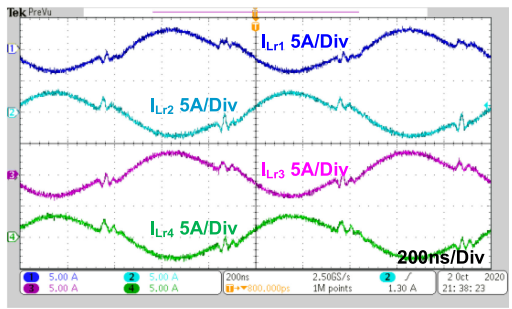
shown in Table II. The equivalent R_{dson} of the primary switches in the ISOP structure is around 32 mΩ for which eight switches conduct the primary current at the same time. Thus, for the high-voltage silicon devices and GaN devices, the R_{dson} is also selected around 32 mΩ for comparison. The isolated gate driver UCC21225A is used for every two switches in a half-bridge. Then, the total cost of the primary switches and the primary drivers can be compared in Table II. As for the conduction loss of the primary switches at full load, it can be seen that owing to the CM current and high NFoM, the conduction loss will be very large when high-voltage silicon devices are used. As for the GaN devices, although the NFoM of them can be reduced compared with that of the high-voltage MOSFETs, the larger temperature coefficient of resistance and the dynamic ON-state resistance should also be considered. Thus, even after considering the driving loss, the ISOP structure can still achieve

TABLE II
COST AND LOSS COMPARISON OF THE PRIMARY SWITCHES AND DRIVERS

	Single half bridge-Si	Single half bridge-GaN	The ISOP SRC
Primary switches	IPT60R035CFD7	GS66516T	BSZ040N06LS5
R_{dson}@25℃	35mΩ	32mΩ	4mΩ
$@1k (Sws)	6.37/pcs	38.45/pcs	0.63/pcs
Number	2	2	16
Cost (with rivers)	13.89$	78.05$	19.26$
Loss (W) @full load	15.3	10.6	5.6
Footprint of primary switches (mm^2)	206.51	137.52	174.24



(a)



(b)

Fig. 17. Waveforms of the interleaving within a cell control strategy.

a higher efficiency under a relatively lower cost. The comparison of the footprint of the primary switches is also given in Table II.

The experimental waveforms of the interleaving within a cell control strategy are shown in Fig. 17. The drain-source voltages of four devices in two cells (Cell 1 and 2) and the resonant currents through $L_{r1} - L_{r4}$ are given as an example to illustrate the operating principle. In Fig. 17(a), V_{ds_S1} and V_{ds_S3} represent the two topologies within the same cell operating at the opposite time, so do V_{ds_S5} and V_{ds_S7}. V_{ds_S1} and V_{ds_S5} represent the two topologies in the same position of different cells operating at the same time, so do V_{ds_S3} and V_{ds_S7}. The operating principle can also be verified by the current, as shown in Fig. 17(b). The circuit parameters among different half bridges are highly consistent and the current distributes evenly among the cells. The effect of the interleaving within a cell control strategy is shown in Fig. 18. The dashed black envelope curve is the CM noise spectrum with in-phase control strategy, which is the same as the red curve in Fig. 15. The solid red envelope

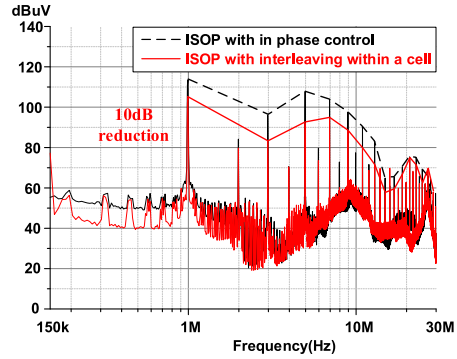


Fig. 18. Comparison of the measured CM noise spectrums with in-phase control strategy and interleaving within a cell control strategy.

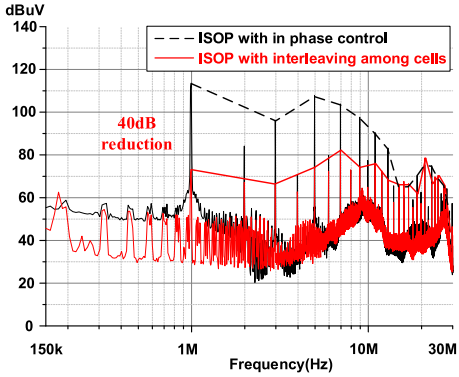


Fig. 20. Comparison of the measured CM noise spectrums with in-phase control strategy and interleaving among cells control strategy.

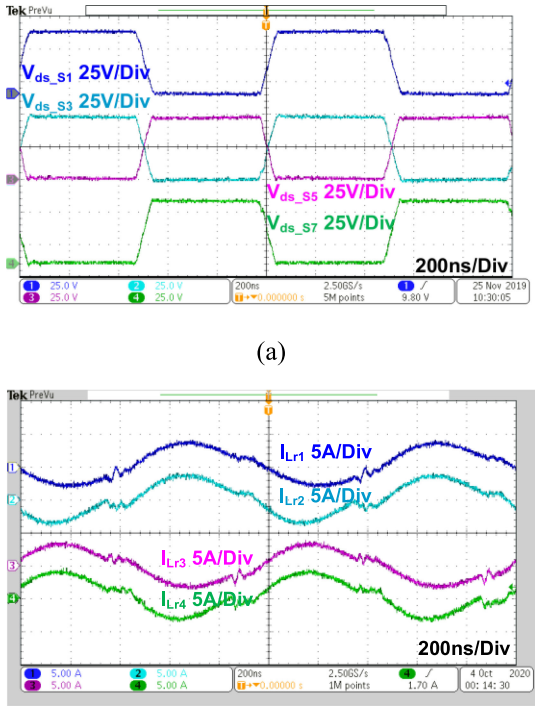


Fig. 19. Waveforms of the interleaving among cells control strategy.

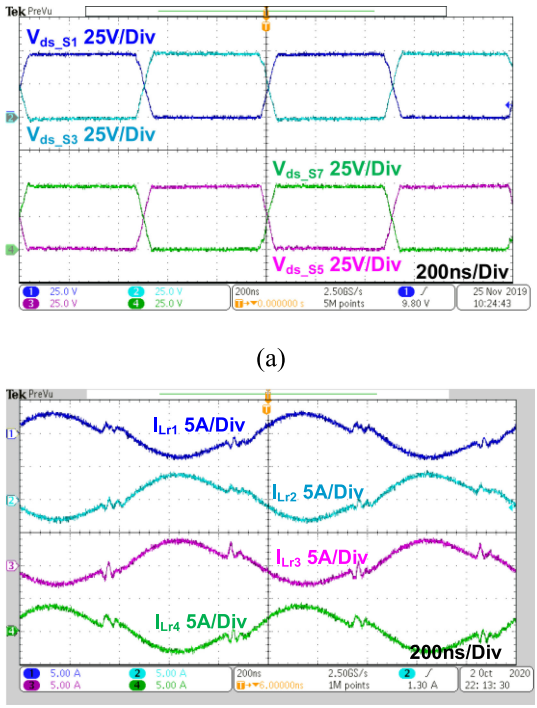


Fig. 21. Experimental waveforms of the combined control strategy.

curve in Fig. 18 is the CM noise spectrum with the interleaving within a cell control strategy. The CM noise can be reduced by 10 dB, as shown in Fig. 18. The suppressing effect is noticeable, but the CM noise is still large.

The experimental waveforms of the interleaving among cells control strategy are shown in Fig. 19. In this control strategy, the V_{ds_S1} and V_{ds_S3} within the same cell operate at the same time, so do V_{ds_S5} and V_{ds_S7}. V_{ds_S1} and V_{ds_S5} in the same position of different cells operate at the opposite time, so do V_{ds_S3} and V_{ds_S7}. The resonant currents through $L_{r1} - L_{r4}$ are also shown in Fig. 19(b). The suppressing effect of the interleaving among cells control strategy is demonstrated in Fig. 20. The dashed black envelope curve is the CM noise spectrum with in-phase control strategy, which is the same as the solid red envelope curve in Fig. 15 and the dashed black envelope curve in Fig. 18. The red envelope curve in Fig. 20 is the CM noise spectrum with the interleaving among cells control strategy. Comparing the two curves in Fig. 20, the CM noise can be reduced by 40 dB.

Comparing the two control strategies, the effect of the interleaving among cells is much better than that of the interleaving within a cell, and it is identical to the analysis mentioned in Section III. Combining the two optimal control strategies, the experimental waveforms are given in Fig. 21. V_{ds_S1} and V_{ds_S3} within the same cell operating at the opposite time, so do V_{ds_S5} and V_{ds_S7}. V_{ds_S1} and V_{ds_S5} in the same position of different cells also operate at the opposite time, so do V_{ds_S3} and V_{ds_S7}. The CM noise spectrums with the combined control strategy

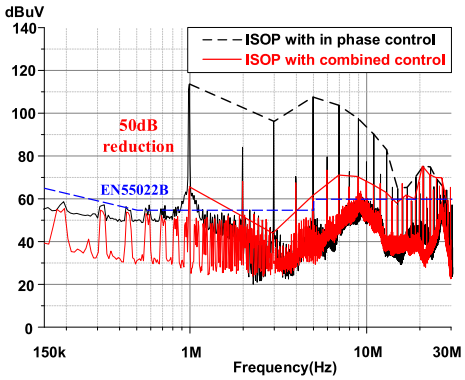


Fig. 22. Comparison of the measured CM noise spectrums with in-phase control strategy and combined control strategy.

are shown in Fig. 22. From Fig. 22, with the combined control strategy, the CM noise can be reduced by 50 dB compared with the in-phase control strategy. However, as the frequency increases to more than 15 MHz, the influence of the parasitic inductance and resistance will be more apparent, which will affect the phase of the CM current and reduce the cancelation effect at such a high frequency. However, for that the design of the EMI filter is mainly decided by the fundamental frequency, the CM noise over 15 MHz will have a small effect. Besides, the final spectrum is almost close to the EMI testing standard EN55022B, and the required EMI filter can be reduced a lot.

V. Conclusion

For 380-V input DCX application, in order to achieve high efficiency and high power density, the switching frequency need to be pushed to megahertz. However, for a conventional half-bridge SRC topology, the CM noise is quite severe under high frequency, which needs a large EMI filter and sacrifices the power density of the conversion system. A static point construction method was adopted in this article to reduce the CM noise at megahertz frequency, and an ISOP converter was implemented with several low-voltage devices. This method reduced the CM noise by 10 dB on fundamental frequency and achieved high efficiency at the same time. Furthermore, two optimal control strategies, interleaving within a cell and among cells, respectively, were adopted to suppress the CM noise. The interleaving within a cell strategy reduced the CM noise by 10 dB, and the interleaving among cells strategy reduced the CM noise by 40 dB. When combining the two optimal strategies, the CM noise was ultimately reduced by 50 dB, and the EMI filter could be quite small.

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