# An Accurate Datasheet-Based Full-Characteristics Analytical Model of GaN HEMTs for Deadtime Optimization

Zhiyuan Qi, *Student Member, IEEE*, Yunqing Pei, *Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Kangping Wang, *Member, IEEE*, Mengyu Zhu, *Student Member, IEEE*, Cheng Zhao, *Student Member, IEEE*, Qingshou Yang, *Student Member, IEEE*, and Yongmei Gan, *Member, IEEE*

***Abstract*—The gallium nitride high electron mobility transistors (GaN HEMTs) are a superior candidate for the new-generation power electronics systems with higher efficiency and power density. However, due to the unique reverse characteristics, the reverse voltage drop of GaN HEMTs is much higher than that of diode. The deadtime loss in GaN-based bridge converters will be comparable to switching losses if the deadtime is not optimized. To optimize the deadtime for higher efficiency, this article proposes an accurate analytical model of GaN HEMTs, including circuit's parasitic inductances, the nonlinear capacitances, the unique reverse characteristics, etc. Taking a GaN-based synchronous buck converter as the example, the proposed model is realized, which fully uses the datasheet to avoid additional experiments. In order to accurately measure the switching current for validation, a novel parasitics-based current measurement method is proposed. The proposed model is verified by simulation in LTspice and experiment, and good agreement is shown. Based on the accurate analytical model, the deadtime is optimized for different load currents to improve the efficiency within the full load range. Compared with the fixed deadtime of 15 ns, the increase of efficiency can be up to 8%. This work will promote the high-frequency application of GaN HEMTs.**

***Index Terms*—Analytical model, deadtime optimization, gallium nitride high electron mobility transistors (GaN HEMTs), parasitics-based current measurement.**

## I. Introduction

It IS well acknowledged that high efficiency and high power density are two key drivers and metrics for the advancement of power conversion technologies. For the silicon (Si) power devices have developed to its theoretical limit, it is difficult and almost impossible to further improve the power density and efficiency by using Si devices [1]–[3]. The emergence of gallium nitride high electron mobility transistors (GaN HEMTs), as the representative of wide bandgap power devices, can break through the bottleneck [4]. Compared with Si and silicon carbide (SiC) materials, GaN material has higher electron mobility, higher saturated electron velocity, and higher electric breakdown field [5], as shown in Fig. 1. Due to these material superiorities, GaN devices can achieve smaller ON-state resistance and smaller gate charge than Si and SiC counterparts with comparable voltage and current capabilities, which means better conduction and switching performance. Therefore, GaN devices are more suitable for high frequency applications. By using GaN HEMTs, the switching frequency can be pushed up to multi megahertz easily, which is good for the increase of power density.

However, on the one hand, when operating at such high switching frequency, the switching losses start to dominate the overall losses and become the limiting factor to further increase switching frequency [1], [6]. On the other hand, GaN HEMTs have unique reverse characteristics, which make the reverse voltage drop of GaN HEMTs much higher than that of diode. The deadtime loss in GaN-based bridge converters will be comparable to switching losses if the deadtime is not optimized. To have a deep insight into the switching process and optimize the deadtime for higher efficiency, an accurate model of GaN HEMTs is highly required.

Basically, there are three types of models, i.e., physics-based model, behavior model, and analytical model [7]– [12]. The physical model can achieve very close simulation results to experimental results, but it is very time-consuming and needs many parameters related to device fabrication [7], [9], [13], [14]. The widely used model is the behavior model because it has good tradeoff between the accuracy and the simulation time. However, it is not suitable for massive data processing [9], [13]. Relatively, the analytical model is the fastest and suitable for data processing, but the major challenge to improve the accuracy should be addressed. This article will focus on proposing an accurate and rapid analytical model for GaN HEMTs. So far, there have been some analytical models of GaN HEMTs presented [3], [6], [15]–[17], but most of them are modified from the models

Manuscript received August 25, 2020; revised November 2, 2020; accepted December 5, 2020. Date of publication December 11, 2020; date of current version March 5, 2021. This work was supported in part by the Science and Technology Plan of Guangdong Province, China, under Grant 2017B010112002, in part by the Key-Area Research and Development Program of Guangdong Province, China, under Grants 2020B010173001 and 2020B010170001, and in part by the Power Electronics Science and Education Development Program of Delta Group under Grant DREG2019007. Recommended for publication by Associate Editor W. Cao. *(Corresponding author: Laili Wang.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: mambaqizhy@stu.xjtu.edu.cn; peiyq@mail.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; wangkangping@stu.xjtu.edu.cn; zmy3118104006@stu.xjtu.edu.cn; zhaocheng3117@stu.xjtu.edu.cn; qs_yang@stu.xjtu.edu.cn; ymgan@mail.xjtu.edu.cn).

Color versions of one or more of the figures in this article are available online at https://doi.org/10.1109/TPEL.2020.3044083.

Digital Object Identifier 10.1109/TPEL.2020.3044083

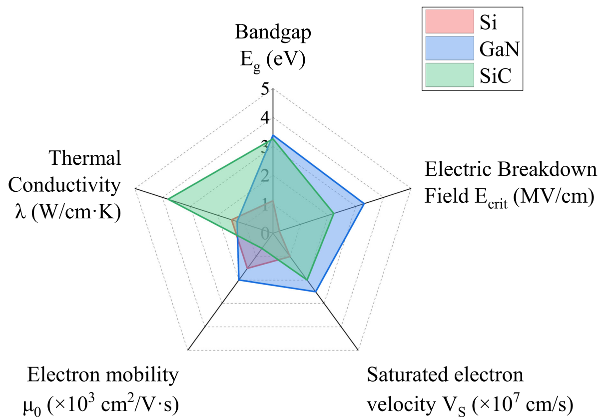



Fig. 1. Comparison of Si, GaN, and SiC properties.

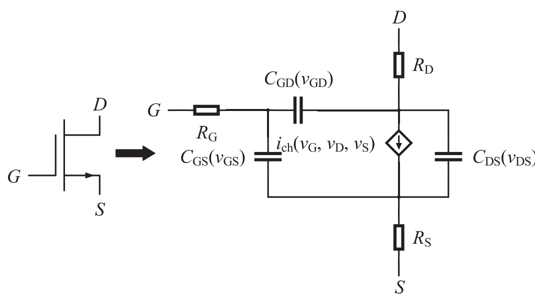



Fig. 2. Equivalent circuit schematic of GaN HEMTs' device-level model.

of MOSFETs [12], [13], [18]–[31], which are not suitable for GaN HEMTs. In order to realize an accurate analytical model of GaN HEMTs, circuit's parasitic inductances, the nonlinear capacitances, and the unique reverse characteristics of GaN HEMTs should be considered [9].

However, in the existing analytical models of GaN HEMTs, the nonlinear capacitances are usually achieved directly from datasheet, which cannot reflect the real nonlinearity of the parasitic capacitances. It is because of the gate-to-source capacitance of GaN HEMTs being strongly affected by gate-to-source voltage, but the nonlinear capacitances in datasheet are with regard to drain-to-source voltage. In order to achieve the nonlinearity of gate-to-source capacitance with regard to gate-to-source voltage, some additional experiments are conventionally needed [32], which is not expected for engineers and designers. To avoid additional experiments, the datasheet needs to be fully used. Besides the curve of nonlinear capacitances in datasheet, the curve of gate charge can also be used, and then some derivations are required. For simplification, a Schottky diode is usually used to replace the synchronous switch in the existing analytical models of GaN HEMTs [3], [6]. But actually, GaN HEMTs have unique reverse characteristics as mentioned above. When operating reversely, GaN HEMTs are controlled by gate-to-drain voltage instead of gate-to-source voltage. However, the driving signal is usually applied between gate terminal and source terminal. During the deadtime, GaN HEMTs operate at weak active region, resulting in a higher reverse voltage drop than the voltage drop of diode. The power losses during deadtime can be comparable to switching losses if the deadtime is not optimized. Therefore, the deadtime needs to be optimized for higher efficiency by considering the unique reverse characteristics of GaN HEMTs. Besides, either a constant transconductance or only the transfer characteristics in datasheet is conventionally used to model the *I-V* characteristics of GaN HEMTs, affecting the accurate prediction of the switching process. To improve the accuracy, both the transfer characteristics and the output characteristics need to be used to model the *I-V* characteristics.

According to the above analysis, this article will fully use the datasheet to model the *I-V* characteristics and *C-V* characteristics of GaN HEMTs without any additional experiments, and further propose an accurate analytical model of GaN HEMTs, including circuit's parasitic inductances, the nonlinear capacitances, the unique reverse characteristics, etc. Based on the proposed model, the deadtime will be optimized to improve efficiency by revealing the impact of deadtime on power losses. The rest of this article is organized as follows. In Section II, the device-level modeling process of GaN HEMTs is described in detail. Based on the device-level model, detailed circuit-level model is built in Section III, the switching process is discussed in depth by dividing it into four phases. In Section IV, a parasitics-based current measurement method is proposed, and the verification of the proposed model is carried out by simulation and experiment. Then, based on the presented model, the power losses are decomposed. In Section V, in order to improve the efficiency, the deadtime is optimized for different load currents. Finally, in Section VI, the conclusion and the next working plan are given out.

## II. Device-Level Modeling of GaN HEMTs

The modeling process in this article is divided into two steps, i.e., the device-level model of GaN HEMTs and the circuit-level model. In this section, the device-level model of GaN HEMTs is presented in detail. Fig. 2 shows the schematic of GaN HEMTs' device-level model. It can be seen that there are no differences between the model of GaN HEMTs and Si MOSFET from the aspect of the schematic. In the model, there are three nonlinear capacitances, i.e., gate-source capacitance $C_{\rm GS}(v_{\rm GS})$, gate-drain capacitance $C_{\rm GD}(v_{\rm GD})$, drain-source capacitance $C_{\rm DS}(v_{\rm DS})$, and a voltage-controlled current source $i_{\rm ch}(v_{\rm G}, v_{\rm D}, v_{\rm S})$ representing channel current. But, the *I-V* characteristics and *C-V* characteristics of GaN HEMTs are quite different from Si MOSFETs, which will be carefully modeled below. The GaN HEMTs EPC2015C is taken as the example to demonstrate the modeling process. The technique of extracting image data and curve fitting is used to fully extract the information of datasheet, and some derivations are carried out to achieve the accurate analytical model of GaN HEMTs without any additional experimental measurements.

### A. *Modeling of GaN HEMTs' I-V Characteristics*

As mentioned above, the reverse characteristics of GaN HEMTs are unique, which means different *I-V* characteristics from power MOSFETs. For power MOSFETs, as long as the value of the gate-to-source voltage is higher than threshold voltage,

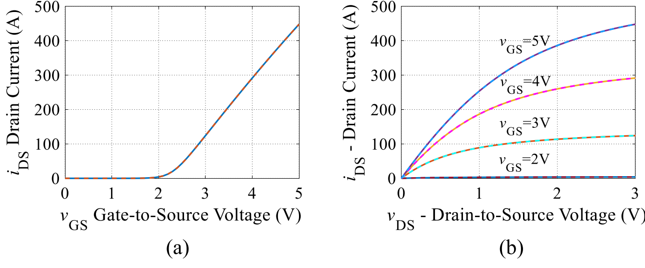



Fig. 3. Fitted curves of EPC2015C's *I-V* characteristics (solid line: curves from datasheet, dash line: fitted curves). (a) Transfer characteristics. (b) Output characteristics.

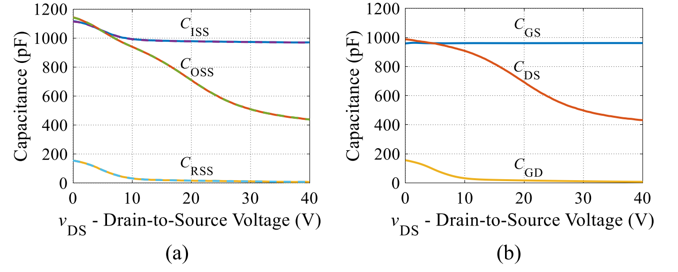



Fig. 4. (a) Fitted curves of $C_{\mathrm{ISS}}$, $C_{\mathrm{OSS}}$, and $C_{\mathrm{RSS}}$ versus $v_{\mathrm{DS}}$ (solid line: curves from datasheet, dash line: fitted curves). (b) Derived curves of $C_{\mathrm{GS}}$, $C_{\mathrm{DS}}$, and $C_{\mathrm{GD}}$ versus $v_{\mathrm{DS}}$.

the channel will conduct current no matter the drain-to-source voltage is positive or negative. For the GaN HEMTs, it has a symmetrical structure, which can be regarded as a parallel-pair of two power MOSFETs in opposite directions [33]. When drain-to-source voltage is positive, the channel current is controlled by gate-to-source voltage; but when drain-to-source voltage is negative, the channel current is controlled by gate-to-drain voltage. This results in the unique reverse characteristics of GaN HEMTs, which has great influence on the power loss during deadtime between top switch and bottom switch in half-bridge circuit.

The same as power MOSFETs, the operation of GaN HEMTs can also be divided into three regions under the positive drain-to-source voltage or negative drain-to-source voltage, i.e., cutoff region, active region, and ohmic region. Conventionally, the cutoff region is treated as an ideal OFF-state without any current flowing through, and the ohmic region is treated as the absolute ON-state without voltage drop across drain and source terminals. Besides, a constant transconductance is often used to describe the dependence of channel current on gate-to-source voltage in active region. In this article, no assumption for simplification is made, the output characteristics and transfer characteristics are both used into the modeling of the *I-V* characteristics.

The *I-V* characteristics reflecting the steady behavior of GaN HEMTs can be described by (1) as follows:

$$i_{\mathrm{ch}} = \begin{cases} f_1(v_{\mathrm{GS}}), \text{ if } v_{\mathrm{DS}} > v_{\mathrm{GS}} - v_{\mathrm{th}} \geq 0 \\ \quad \text{or } v_{\mathrm{DS}} > 0 > v_{\mathrm{GS}} - v_{\mathrm{th}} \\ f_2(v_{\mathrm{GS}}, v_{\mathrm{DS}}), \text{ if } v_{\mathrm{GS}} - v_{\mathrm{th}} > v_{\mathrm{DS}} \geq 0 \\ -f_3(v_{\mathrm{GD}}), \text{ if } -v_{\mathrm{DS}} > v_{\mathrm{GD}} - v_{\mathrm{th}} \geq 0 \\ \quad \text{or } -v_{\mathrm{DS}} > 0 > v_{\mathrm{GD}} - v_{\mathrm{th}} \\ -f_4(v_{\mathrm{GD}}, -v_{\mathrm{DS}}), \text{ if } v_{\mathrm{GD}} - v_{\mathrm{th}} > -v_{\mathrm{DS}} > 0 \end{cases} \tag{1}$$

where $v_{\mathrm{GS}}$, $v_{\mathrm{GD}}$, $v_{\mathrm{DS}}$, and $v_{\mathrm{th}}$ are the gate-to-source voltage, gate-to-drain voltage, drain-to-source voltage, and threshold voltage, respectively. $f_1(v_{\mathrm{GS}})$, $f_2(v_{\mathrm{GS}}, v_{\mathrm{DS}})$, $f_3(v_{\mathrm{GD}})$, and $f_4(v_{\mathrm{GD}}, -v_{\mathrm{DS}})$ are the functions of channel current in different regions.

With regard to the function $f_1(v_{\mathrm{GS}})$, since $v_{\mathrm{DS}} > v_{\mathrm{GS}} - v_{\mathrm{th}} \geq 0$ or $v_{\mathrm{DS}} > 0 > v_{\mathrm{GS}} - v_{\mathrm{th}}$, it means that the GaN HEMTs operate in forward active region or forward cutoff region. Hence, the transfer characteristics curve is used to obtain $f_1(v_{\mathrm{GS}})$. The transfer characteristics curve can be well fitted by using linear-interpolant method, as shown in Fig. 3(a), and the obtained fitting function is $f_1(v_{\mathrm{GS}})$. When $v_{\mathrm{GS}} - v_{\mathrm{th}} > v_{\mathrm{DS}} \geq 0$, GaN HEMTs fully conduct and locate in the forward ohmic region, the output characteristics curve is used to obtain $f_2(v_{\mathrm{GS}}, v_{\mathrm{DS}})$. By using linear lowess fitting method with a span of 1%, the output characteristics curve is well fitted, as shown in Fig. 3(b), and the obtained fitting function is $f_2(v_{\mathrm{GS}}, v_{\mathrm{DS}})$. As aforementioned, GaN HEMTs have symmetrical structure, and thus symmetrical working characteristics. Therefore, $f_3(v_{\mathrm{GD}})$ and $f_4(v_{\mathrm{GD}}, -v_{\mathrm{DS}})$ can be achieved just by changing $v_{\mathrm{GS}}$ and $v_{\mathrm{DS}}$ in $f_1(v_{\mathrm{GS}})$ and $f_2(v_{\mathrm{GS}}, v_{\mathrm{DS}})$ to $v_{\mathrm{GD}}$ and $-v_{\mathrm{DS}}$.

### *B. Modeling of GaN HEMTs' C-V Characteristics*

An accurate modeling of *C-V* characteristics can precisely describe the dynamic behavior of GaN HEMTs, thus can achieve a precise description of the switching process. Generally, the datasheet just gives out the curves of input capacitance $C_{\mathrm{ISS}}$, output capacitance $C_{\mathrm{OSS}}$, and reverse capacitance $C_{\mathrm{RSS}}$ with regard to $v_{\mathrm{DS}}$, which can be obtained by curve fitting, as shown in Fig. 4(a). By using (2)–(4), the curves of $C_{\mathrm{GS}}$ , $C_{\mathrm{GD}}$, and $C_{\mathrm{DS}}$ with regard to $v_{\mathrm{DS}}$ are achieved, as shown in Fig. 4(b). It can be seen that the derived $C_{\mathrm{GS}}$ is almost constant versus $v_{\mathrm{DS}}$, that is why it is usually treated as a constant in conventional analytical models [6], [12], [13], [22], [26], [27], [32]. However, the fact is that the three interelectrode capacitances are just related to their respective applied voltage. For example, $C_{\mathrm{GS}}$ is related to $v_{\mathrm{GS}}$ strongly [7], [19], [34]–[41], $C_{\mathrm{GD}}$ and $C_{\mathrm{DS}}$ are actually related to $v_{\mathrm{GD}}$ and $v_{\mathrm{DS}}$, respectively. What is more, as the structure of GaN HEMTs is symmetrical, so the three nonlinear capacitances are also symmetrical with regard to their respective voltage. In order to achieve accurate model of *C-V* characteristics, the datasheet needs to be fully used, and some derivations are necessary.

$$C_{\mathrm{ISS}} = C_{\mathrm{GS}} + C_{\mathrm{GD}} \tag{2}$$

$$C_{\mathrm{RSS}} = C_{\mathrm{GD}} \tag{3}$$

$$C_{\mathrm{OSS}} = C_{\mathrm{DS}} + C_{\mathrm{GD}} \tag{4}$$

With regard to the nonlinear capacitance $C_{\mathrm{DS}}$ ($v_{\mathrm{DS}}$), it can be obtained by simply subtracting (3) from (4). For the nonlinear capacitance $C_{\mathrm{GD}}$ ($v_{\mathrm{GD}}$), as the measurement of *C-V* curves in datasheet is under the condition of $v_{\mathrm{GS}} = 0$ V [42], so $v_{\mathrm{DS}} = v_{\mathrm{DG}}$, thus $C_{\mathrm{GD}}$ ($v_{\mathrm{GD}}$) can also be obtained. For the nonlinear capacitance $C_{\mathrm{GS}}$ ($v_{\mathrm{GS}}$), it cannot be obtained directly from the *C-V* curves in datasheet. Therefore, this article also

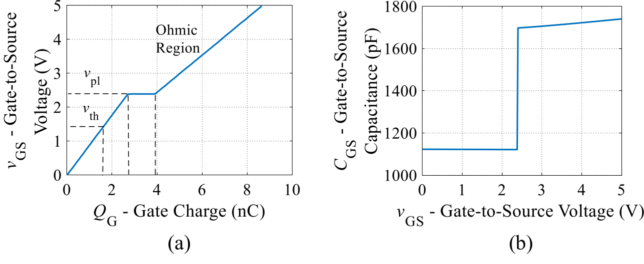



Fig. 5. Derivation of $C_{GS}-v_{GS}$ curve from the $v_{GS}-Q_G$ curve in datasheet. (a) The $v_{GS}$ - $Q_G$ curve. (b) The derived $C_{GS}$ - $v_{GS}$ curve.

uses the $Q_G$-$v_{GS}$ curve in datasheet into the derivation of $v_{GS}$-dependent $C_{GS}$. It should be noted that the curve of $Q_G$-$v_{GS}$ reflects the turn-ON process of GaN HEMTs. With the driving current flowing into the gate terminal of GaN HEMTs, $C_{GS}$ charges and $C_{GD}$ discharges, thus the gate-to-source voltage rises. There is no current flowing through the channel until $v_{GS}$ is higher than threshold voltage $v_{th}$, then the channel current rises continuously until the current of output inductor. During this current-increasing period, $v_{DS}$ remains to be 20 V, $C_{GS}(v_{GS})$ during this range can be obtained from (5). Then, it starts to enter the voltage-decreasing stage when $v_{GS}$ remains constant, which is so-called Miller platform. During this stage, $C_{GS}$ keeps constant. After that, when $v_{DS}$ drops to smaller than $v_{GS-}v_{th}$, GaN HEMTs fully conducts and locates in ohmic zone, and $C_{GS}(v_{GS})$ can be calculated by using (6). Based on the above method, the curve of $C_{GS-}v_{GS}$ is obtained as shown in Fig. 5. It can be seen that there is a sudden change at the Miller platform voltage $v_{pl}$, which exactly verifies why $C_{GS}$ cannot be treated as a constant. Through the above process, an accurate device-level model of GaN HEMTs is built.

$$\frac{\mathrm{d}Q_G}{\mathrm{d}v_{GS}} = \frac{\mathrm{d}Q_{GS}}{\mathrm{d}v_{GS}} + \frac{\mathrm{d}Q_{GD}}{\mathrm{d}v_{GS}} = \frac{\mathrm{d}Q_{GS}}{\mathrm{d}v_{GS}} + \frac{\mathrm{d}Q_{GD}}{\mathrm{d}\left(v_{GD}+20\right)}$$
$$= \frac{\mathrm{d}Q_{GS}}{\mathrm{d}v_{GS}} + \frac{\mathrm{d}Q_{GD}}{\mathrm{d}v_{GD}} = C_{GS}\left(v_{GS}\right) + C_{GD}\left(20-v_{GS}\right) \tag{5}$$

$$\frac{\mathrm{d}Q_G}{\mathrm{d}v_{GS}} = \frac{\mathrm{d}Q_{GS}}{\mathrm{d}v_{GS}} + \frac{\mathrm{d}Q_{GD}}{\mathrm{d}v_{GS}}$$
$$\approx \frac{\mathrm{d}Q_{GS}}{\mathrm{d}v_{GS}} + \frac{\mathrm{d}Q_{GD}}{\mathrm{d}v_{GD}} = C_{GS}\left(v_{GS}\right) + C_{GD}\left(v_{GD}\right). \tag{6}$$

## III. Circuit-Level Modeling of GaN HEMTs Based on a Synchronous Buck Converter

Based on the built device-level model of GaN HEMTs, this section takes a GaN-based synchronous buck converter as the example to derive the circuit-level model. The specifications of the synchronous buck converter are shown in Table I. In order to describe the switching behavior of GaN HEMTs as actually as possible, the decoupling capacitors $C_{in}$ and almost all the related parasitic inductances are considered into circuit-level model. $V_{dc}$ represents the voltage of the input filter capacitors, which is almost constant. Fig. 6 (a) shows the schematic of the synchronous buck converter with main parasitic inductances,

TABLE I
Specifications of the Synchronous Buck Converter

| | |
|---|---|
| Input Voltage | 12 V |
| Output Voltage | 3.3 V |
| Output Current | 10 A |
| Switching Frequency | 1 MHz |
| Switching Device | EPC2015C |
| Output inductance | 1uH |

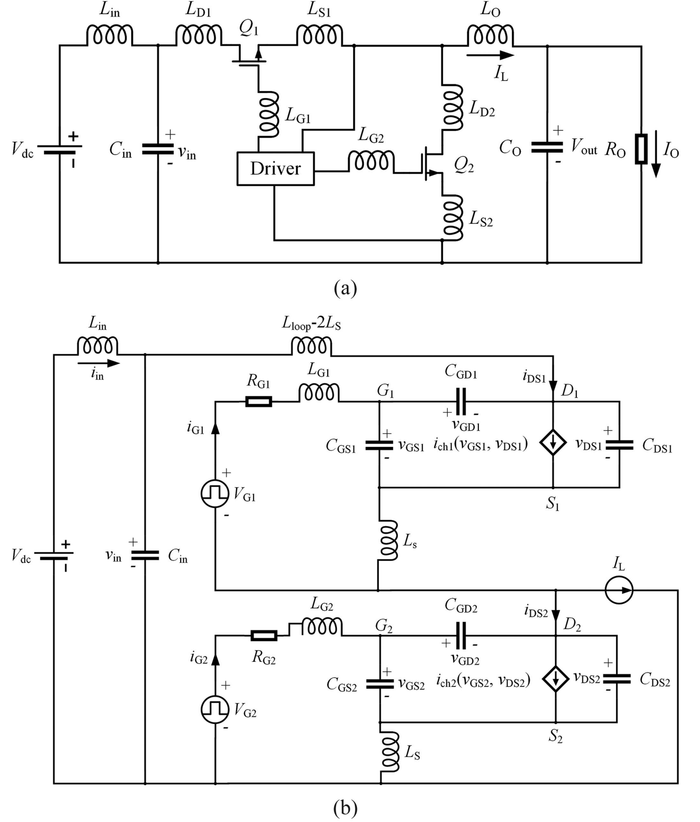



Fig. 6. (a) Schematic of synchronous buck converter with main parasitic inductances. (b) Schematic of the obtained circuit-level model.

including $L_{in}$, $L_{G1}$, $L_{D1}$, $L_{S1}$, $L_{G2}$, $L_{D2}$, and $L_{S2}$. By substituting the device model of GaN HEMTs into the circuit, the circuit-level model can be obtained as shown in Fig. 6(b). The power loop inductance $L_{loop}$ is the sum of $L_{D1}$, $L_{S1}$, $L_{D2}$, and $L_{S2}$. In the model, $L_{S1}$ and $L_{S2}$ are replaced by $L_S$, which is about 80 pH [43]. Considering the actual current of load inductor in synchronous buck converter, the current of load inductor $I_L$ is modeled as a current source with triangle waveform as shown in Fig. 7.

Then, based on the Kirchhoff voltage law and Kirchhoff current law, the voltage equations and current equations of both the power loop and two driving loops can be derived for the circuit-level model, as listed in (7)–(16). The variables used in the model are defined in Table II. There are ten state variables and ten equations in the model, so the unique solution exists. However, since the interelectrode capacitances are nonlinear

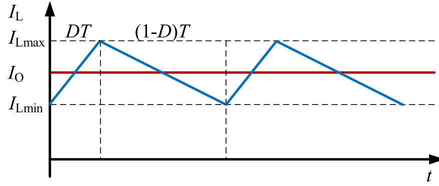



Fig. 7. Current waveform of load inductor.

TABLE II
DEFINITIONS OF CIRCUIT PARAMETERS IN PROPOSED MODEL

| | | | |
|---|---|---|---|
| DC bus voltage | $V_{dc}$ | Drain current of bottom switch | $i_{DS2}$ |
| Voltage across $C_{in}$ | $v_{in}$ | Channel current of top switch | $i_{ch1}$ |
| Top switch's driving voltage | $V_{G1}$ | Channel current of bottom switch | $i_{ch2}$ |
| Bottom switch's driving voltage | $V_{G2}$ | Parasitic inductance from $V_{dc}$ to $C_{in}$ | $L_{in}$ |
| Gate-to-source voltage of top switch | $v_{GS1}$ | Gate resistance of top switch | $R_{G1}$ |
| Gate-to-drain voltage of top switch | $v_{GD1}$ | Gate resistance of bottom switch | $R_{G2}$ |
| Drain-to-source voltage of top switch | $v_{DS1}$ | Parasitic inductance of top switch's driving loop | $L_{G1}$ |
| Gate-to-source voltage of bottom switch | $v_{GS2}$ | Parasitic inductance of bottom switch's driving loop | $L_{G2}$ |
| Gate-to-drain voltage of bottom switch | $v_{GD2}$ | Common source inductance | $L_S$ |
| Drain-to-source voltage of bottom switch | $v_{DS2}$ | Parasitic inductance of power loop | $L_{loop}$ |
| Driving current of top switch | $i_{G1}$ | Parasitic resistance of power loop | $R_{loop}$ |
| Driving current of bottom switch | $i_{G2}$ | Current of the output inductance | $I_L$ |
| Drain current of top switch | $i_{DS1}$ | Current through $L_{in}$ | $i_{in}$ |

about their respective applied voltage, the algebraic solution cannot be obtained. The iteration calculation method is required to solve the proposed analytical model. What is more, solving the power electronics problems is often a stiff problem, so the ode15s function in MATLAB is employed to solve the stiff model.

$$V_{G1} = v_{GS1} + R_{G1}i_{G1} + (L_{G1} + L_S)\frac{di_{G1}}{dt} + L_S\frac{di_{DS1}}{dt} \tag{7}$$

$$\begin{aligned} i_{G1} &= C_{GS1}\cdot\frac{dv_{GS1}}{dt} + C_{GD1}\cdot\frac{dv_{GD1}}{dt} \\ &= C_{ISS1}\cdot\frac{dv_{GS1}}{dt} - C_{GD1}\cdot\frac{dv_{DS1}}{dt} \end{aligned} \tag{8}$$

$$\begin{aligned} i_{DS1} &= i_{ch1} + C_{DS1}\cdot\frac{dv_{DS1}}{dt} - C_{GD1}\cdot\frac{dv_{GD1}}{dt} \\ &= i_{ch1} + C_{OSS1}\cdot\frac{dv_{DS1}}{dt} - C_{GD1}\cdot\frac{dv_{GS1}}{dt} \end{aligned} \tag{9}$$

$$\begin{aligned} v_{in} &= v_{DS1} + v_{DS2} + R_{loop}i_{DS1} + L_S\left(\frac{di_{G1}}{dt} + \frac{di_{G2}}{dt}\right) \\ &\quad + L_{loop}\frac{di_{DS1}}{dt} \end{aligned} \tag{10}$$

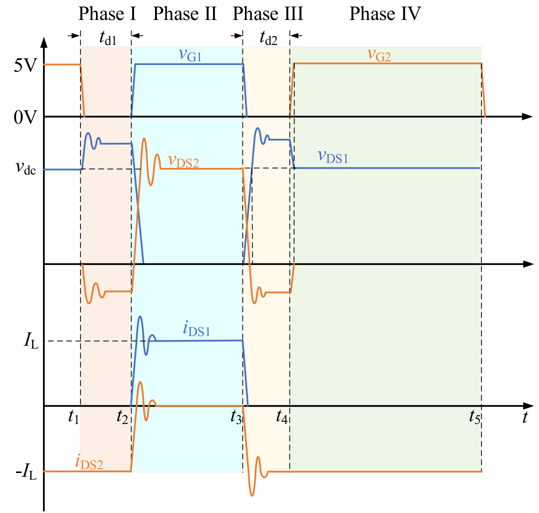



Fig. 8. Schematic of main waveforms during a switching period.

$$V_{G2} = v_{GS2} + R_{G2}i_{G2} + (L_{G2} + L_S)\frac{di_{G2}}{dt} + L_s\frac{di_{DS2}}{dt} \tag{11}$$

$$i_{G2} = C_{ISS2}\cdot\frac{dv_{GS2}}{dt} - C_{GD2}\cdot\frac{dv_{DS2}}{dt} \tag{12}$$

$$i_{DS2} = i_{ch2} + C_{OSS2}\cdot\frac{dv_{DS2}}{dt} - C_{GD2}\cdot\frac{dv_{GS2}}{dt} \tag{13}$$

$$I_L = i_{DS1} - i_{DS2} \tag{14}$$

$$V_{dc} = v_{in} + L_{in}\frac{di_{in}}{dt} \tag{15}$$

$$i_{in} = i_{DS1} + C_{in}\cdot\frac{dv_{in}}{dt}. \tag{16}$$

For ease of solving the proposed model, (7)–(16) are rearranged into the form of (17) as follows:

$$\frac{dX}{dt} = AX + B \tag{17}$$

where $X = [v_{GS1}\ i_{G1}\ v_{GS2}\ i_{G2}\ v_{DS1}\ v_{DS2}\ i_{DS1}\ i_{DS2}\ i_{in}\ v_{in}]^T$, A and B are given in the Appendix.

In order to calculate the proposed analytical model, the initial state should be set carefully. As the synchronous buck converter is taken as the example in this article, so this article sets the ON state of bottom switch as the initial state which can help to improve the accuracy of calculation. At the initial state, the bottom switch $Q_2$ fully conducts the current from source terminal to drain terminal, and $v_{DS2}$ is negative. At this time, $i_{ch2}$ is actually controlled by $v_{GD2}$. Then, as shown in Fig. 8, this article divides a full switching period into four phases for calculation, i.e., the deadtime phase before top switch turning ON (from $t_1$ to $t_2$), the top switch turning-ON and conducting phase (from $t_2$ to $t_3$), top switch turning-OFF phase (from $t_3$ to $t_4$), and the bottom switch turning-ON and conducting phase (from $t_4$ to $t_5$). According to the calculation process shown in Fig. 9, the four subprocesses are calculated in turn, during which each phase starts at the end state of the previous phase.

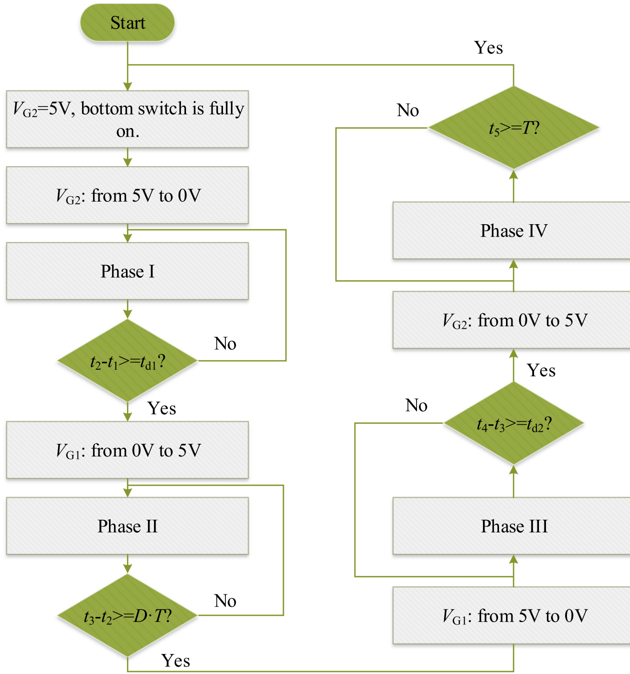



Fig. 9. Calculation process of the proposed analytical model of GaN HEMTs.

### *A. Phase I: Deadtime Phase Before Top Switch Turning on*

The arrival of bottom switch's turn-OFF signal at $t_1$ indicates the start of this phase. And $v_{\rm GS2}$ decreases as $V_{\rm G2}$ drops from 5 to 0 V. At the beginning, $Q_2$ is still fully ON, $-v_{\rm DS2}$ is negligible, so $v_{\rm GD2}$ is approximately equal to $v_{\rm GS2}$, and decreases with the decrease of $v_{\rm GS2}$, so does $-i_{\rm ch2}$. Due to the presence of parasitic inductance, $i_{\rm DS2}$ does not change immediately, the difference $i_{\rm ch2} - i_{\rm DS2}$ will charge $C_{\rm OSS2}$ reversely to increase $-v_{\rm DS2}$. The decrease of $v_{\rm GD2}$ and the increase of $-v_{\rm DS2}$ will result in the relationship $v_{\rm GD2} - v_{\rm th} <= -v_{\rm DS2}$, which means $Q_2$ starts to operate at the active region. When $v_{\rm GS2}$ drops to almost zero, $v_{\rm GD2}$ is equal to $-v_{\rm DS2}$, and $-v_{\rm DS2}$ does not increase any more. This process will last till the turn-ON signal of top switch arrives. During this process from $t_1$ to $t_2$, the value of $-v_{\rm DS2}$ is related to the channel current, and is usually much higher than the voltage drop of diode. For the GaN HEMTs EPC2015C operating at 10 A, the value of $-v_{\rm DS2}$ is about 2.16 V. It will bring a large power loss during this phase, which is called the deadtime loss before top switch turns ON. Therefore, the deadtime $t_{\rm d1} = t_2 - t_1$ needs to be carefully optimized.

### *B. Phase II: Top Switch Turning-on and Conducting Phase*

At the time $t_2$, the turn-ON signal of top switch $Q_1$ comes, and this stage starts. Due to the excitation of driving voltage $V_{\rm G1}$ jumping from 0 to 5 V, $v_{\rm GS1}$ will increase. When $v_{\rm GS1}$ increases to higher than $v_{\rm th}$, the channel of $Q_1$ is turned ON and starts to conducts current. As $v_{\rm GS1}$ increases, $i_{\rm ch1}$ increases. Because of the presence of parasitic inductance, $i_{\rm DS1}$ does not change immediately. The current difference $i_{\rm ch1} - i_{\rm DS1}$ will discharge $C_{\rm OSS1}$, which leads to the decrease of $v_{\rm DS1}$ and further the increase of $i_{\rm DS1}$. Then, $-i_{\rm DS2}$ will decrease due to the relationship of $-i_{\rm DS2} = -(i_{\rm DS1} - I_{\rm L})$. The decrease of the $-i_{\rm DS2}$ causes the difference $i_{\rm DS2} - i_{\rm ch2}$, which discharges $C_{\rm OSS2}$ reversely. Then, $-v_{\rm DS2}$ and $v_{\rm GD2}$ decrease, and $-i_{\rm ch2}$ decreases accordingly. With the further increase of $v_{\rm GS1}$, when it increases to a value that makes the current $i_{\rm DS1}$ reach to $I_{\rm L}$, it means that $I_{\rm L}$ is completely commutated from $Q_2$ to $Q_1$. But the increase of $i_{\rm DS1}$ still continues, and the difference $i_{\rm DS1} - I_{\rm L}$ will charge $C_{\rm OSS2}$ to increase $v_{\rm DS2}$. Meanwhile, as $v_{\rm GS1}$ increases, $v_{\rm DS1}$ decreases due to the discharge of $C_{\rm OSS1}$ by $i_{\rm ch1} - i_{\rm DS1}$. When $v_{\rm DS1}$ is close to zero, the top switch $Q_1$ is fully turned ON. After that, the parasitic inductance of power loop $L_{\rm loop}$ will resonate with $C_{\rm OSS2}$ to result in the current oscillation of $Q_1$ and voltage oscillation of $Q_2$. With the arrival of turn-OFF signal of $Q_1$ at $t_3$, this phase ends.

### *C. Phase III: Top Switch Turning-off Phase*

This phase starts with the arrival of top switch's turn-OFF signal at $t_3$, and $v_{\rm GS1}$ starts to fall down. With the decrease of $v_{\rm GS1}$, $i_{\rm ch1}$ decreases. Due to the presence of parasitic inductance, $i_{\rm DS1}$ does not change immediately, the difference $i_{\rm DS1} - i_{\rm ch1}$ will charge $C_{\rm OSS1}$ to increase $v_{\rm DS1}$. Then, a voltage across parasitic inductance is caused to reduce $i_{\rm DS1}$, thus a reverse current through bottom switch $-i_{\rm DS2}$ increases due to the relationship $-i_{\rm DS2} = -(i_{\rm DS1} - I_{\rm L})$. Generally, the turn-ON signal of $Q_2$ is not applied before $Q_1$ is completely turned OFF. Therefore, $-i_{\rm DS2}$ is used to discharge $C_{\rm OSS2}$, which reduces $v_{\rm DS2}$. For $Q_1$, it will turn into the active region from ohmic region when $v_{\rm GS1} - v_{\rm th} <= v_{\rm DS1}$, and the channel will be turned OFF when $v_{\rm GS1} < v_{\rm th}$. For $Q_2$, $v_{\rm DS2}$ will reduce to zero and then increase reversely. Since $v_{\rm GS2}$ is zero, $v_{\rm GD2}$ is approximately to $-v_{\rm DS2}$, it increases with the reverse charge of $C_{\rm OSS2}$. When $v_{\rm GD2} >= v_{\rm th}$, the channel of $Q_2$ is turned ON. The reverse charging process will continue until $v_{\rm GD2}$ reaches to an enough high value so that the current $-i_{\rm DS2}$ can absolutely flow through the channel. Accordingly, the source-to-drain voltage $-v_{\rm DS2}$ does not increase any more. As $Q_2$ is operating at the weak active region, $-v_{\rm DS2}$ is usually much higher than the voltage drop of diode. When the turn-ON signal of $Q_2$ comes at $t_4$, this phase ends. The duration of this phase $t_4 - t_3$ is another deadtime $t_{\rm d2}$, which also needs to be carefully optimized.

### *D. Phase IV: Bottom Switch Turning-on and Conducting Phase*

When the turn-ON signal of $Q_2$ arrives at $t_4$, the turn-ON process of $Q_2$ starts. With the increase of $v_{\rm GS2}$, $v_{\rm GD2} = v_{\rm GS2} + v_{\rm SD2}$ increases, then $i_{\rm ch2}$ increases, which will be larger than $-i_{\rm DS2}$. The extra current will discharge $C_{\rm OSS2}$ reversely to leading $Q_2$ from active region into ohmic region. When $-v_{\rm DS2}$ is close to zero, $Q_2$ is fully turned ON. Then the parasitic inductance of power loop $L_{\rm loop}$ will resonate with $C_{\rm OSS1}$ to cause the oscillation of waveform. This phase ends with the arrival of bottom switch's turn-OFF signal at $t_5$.

Through the calculation process shown in Fig. 9, the proposed model can be calculated accurately by using MATLAB, thus the switching waveforms during a full switching period can be obtained.

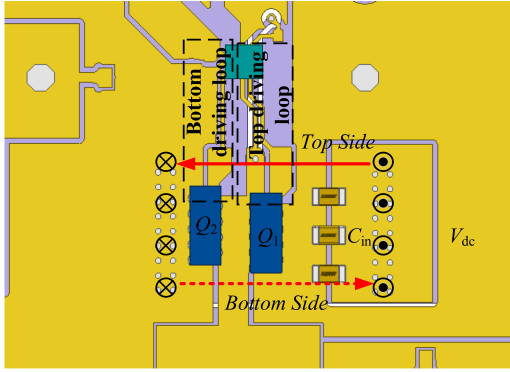



Fig. 10. Simulation model in Ansys Q3D Extractor.

TABLE III
EXTRACTION OF THE CIRCUIT'S PARASITIC INDUCTANCES

| | Parasitic inductance (nH) |
|---|---|
| Power loop $L_{loop}$ | 1.76 |
| Top driving loop $L_{G1}$ | 3.98 |
| Bottom driving loop $L_{G2}$ | 3.41 |
| $V_{dc}$-to-$C_{in}$ inductance $L_{in}$ | 1.33 |

## IV. Verification and Discussions of the Proposed Analytical Model

In this section, the proposed analytical model of GaN HEMTs will be verified. Before this, the parasitic inductances need to be extracted for simulating the actual circuit. Therefore, Ansys Q3D Extractor was utilized to extract the parasitic inductances. In order to achieve accurate parasitic inductances, the simulation model was obtained by first exporting the actual layout of printed circuit board (PCB) in Altium Designer to the specific format of ODB++, and then using Ansys SIwave to convert the ODB++ files to the files readable by Q3D Extractor, as shown in Fig. 10. The simulation frequency was set to 100 MHz representing high frequency oscillation, then the parasitic inductances were extracted as listed in Table III. As mentioned above, the common source inductance $L_S$ of EPC2015C is about 80 pH. The decoupling capacitor $C_{in}$ is 0.3 $u$F, consisting of three 0.1 $u$F ceramic capacitors in parallel. With the extracted parasitic inductances, the switching process during a full switching period can be accurately calculated by using the proposed analytical model.

### A. Simulation Verification by LTspice

LTspice is widely used for the simulation of power electronics circuits, the behavior model used in LTspice can achieve very close results to experiment. Hence, the simulation verification by LTspice was firstly carried out, in which the device model of EPC2015C is provided by manufacturer. The load current is 5 A, and the deadtimes $t_{d1}$ and $t_{d2}$ are both set to 30 ns. The simulation results by the proposed model are compared with the simulation results by LTspice in Fig. 11. We can see that the simulation waveforms by the proposed model are consistent with the simulation waveforms by LTspice.

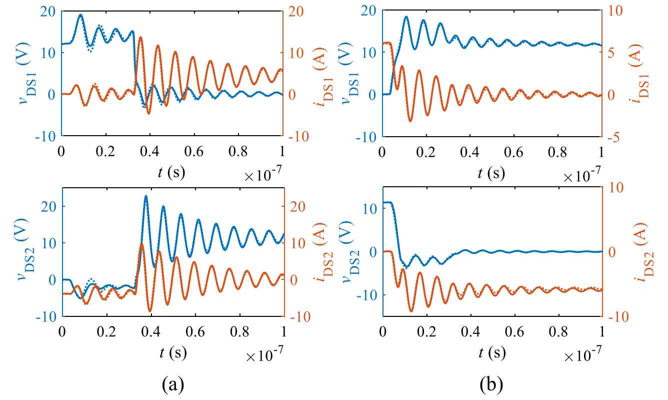



Fig. 11. Switching waveforms comparison between the proposed model and LTspice at the load current of 5 A (solid line: proposed model, dotted line: LTspice). (a) Phase I and phase II. (b) Phase III and phase IV.

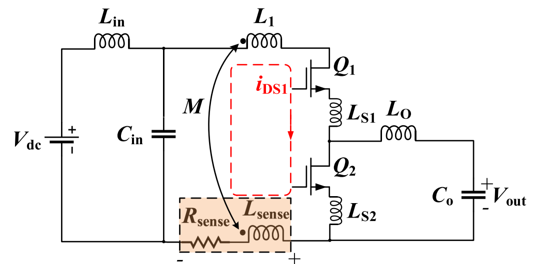



Fig. 12. Schematic of synchronous buck converter with sensing trace.

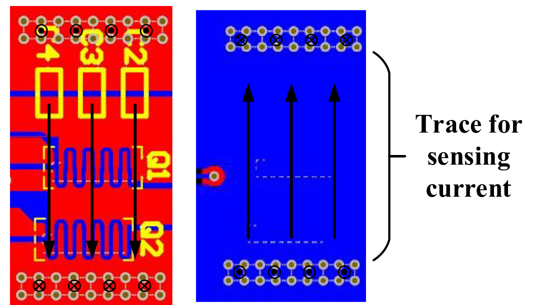



Fig. 13. Designed sensing trace for current measurement in PCB.

### B. Parasitics-Based Current Measurement Method

In order to measure the switching currents accurately in experimental verification, a novel high-bandwidth current measurement method based on the parasitics of PCB's trace was proposed. As shown in Figs. 12 and 13, the trace from the source terminal of $Q_2$ to the ground terminal of decoupling capacitors was used as the sensing trace, whose parasitic inductance is $L_{sense}$, and parasitic resistance is $R_{sense}$. The mutual inductance between the sensing trace and the rest trace in power loop is $M$. The current through the sensing trace is the $i_{DS1}$, and it exists the following relationship between $i_{DS1}$ and the voltage across the sensing trace $v_{sense}$.

$$v_{sense} = R_{sense}\ i_{DS1} + (L_{sense} - M)\frac{di_{DS1}}{dt}. \quad (18)$$

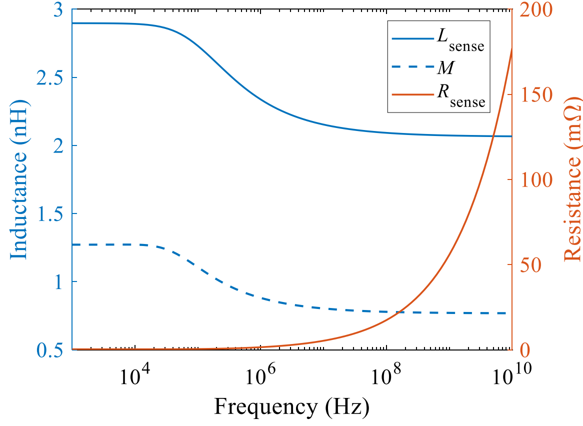



Fig. 14. Extracted parasitics of sensing trace by Ansys Q3D Extractor.

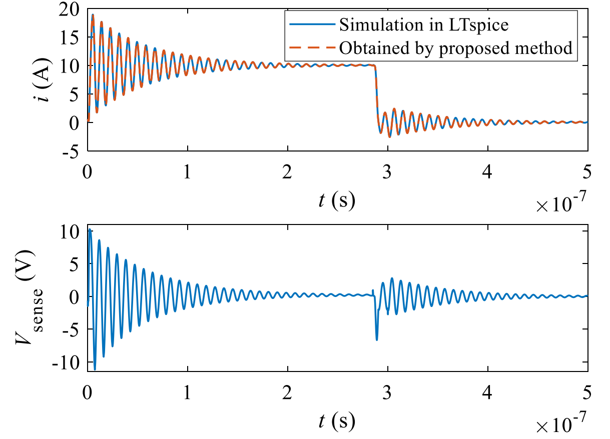



Fig. 15. Verification of the proposed parasitics-based current measurement method by LTspice.

The key is to derive the switching current $i_{DS1}$ and $i_{DS2}$ from the measured $v_{sense}$ in . As we know, a periodic function can be represented by an infinite series of sine and cosine functions, which is the so-called Fourier series. Hence, $i_{DS1}$ can be written as

$$i_{DS1} = I_0 + \sum_{k=1}^{\infty} I_k \sin(k\omega t + \varphi_k) \tag{19}$$

where $\omega = 2\pi f$ and $f$ is the switching frequency.

By using (18), $v_{sense}$ can be written as

$$\begin{aligned} v_{sense} &= R_0 I_0 + \sum_{k=1}^{\infty} R_k I_k \sin(k\omega t + \varphi_k) \\ &\quad + \sum_{k=1}^{\infty} k\omega L_k I_k \cos(k\omega t + \varphi_k) \\ &= R_0 I_0 + \sum_{k=1}^{\infty} Z_k I_k \sin(k\omega t + \varphi_k + \varphi_z) \end{aligned} \tag{20}$$

where $R_k = R_{sense}(kf)$, $L_k = L_{sense}(kf) - M(kf)$, $Z_k = \sqrt{R_k{}^2 + (k\omega L_k)^2}$ ,and $\varphi_z = \operatorname{atan}(\frac{k\omega L_k}{R_k})$.

From (19) and (20), $i_{DS1}$ can be derived from the measured $v_{sense}$, and thus $i_{DS2} = I_L - i_{DS1}$ can be obtained. In order to obtain the frequency-dependent $R_k$ and $L_k$, the frequency characteristics of $L_{sense}$, $R_{sense}$, and $M$ were extracted by using Ansys Q3D Extractor, as shown in Fig. 14. The proposed current measurement method was verified by simulation in LTspice. From Fig. 15, we can see that it shows good agreement between the derived current and the current by simulation. Benefitting from the consideration of the frequency characteristics of sensing trace, the proposed parasitics-based current measurement can realize very high bandwidth, which is very suitable for the measurement of high frequency switching current.

### C. Experimental Verification

In order to verify the proposed analytical model of GaN HEMTs, an experimental protype of 12-3.3 V synchronous buck converter based on EPC2015C was built, as shown in Fig. 16.

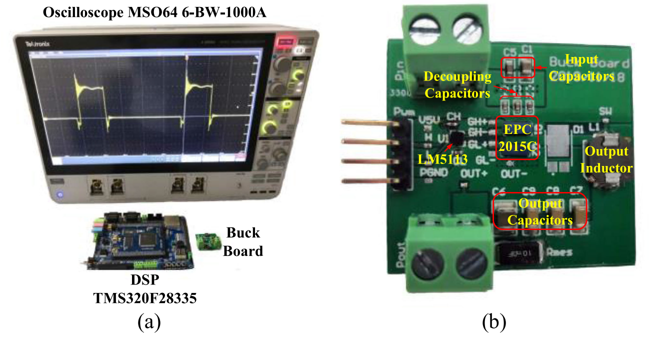



Fig. 16. (a) Experiment setup for validating the proposed analytical model. (b) 12-3.3 V synchronous buck converter.

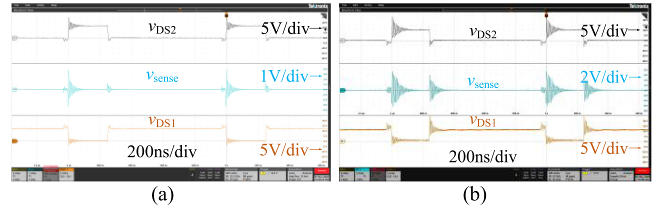



Fig. 17. Measured waveforms at different load current. (a) 2A. (b) 10A.

The converter operates at the switching frequency of 1 MHz. The PWM signals for gate driver LM5113 are generated by DSP TMS320F28335, the deadtimes $t_{d1}$ and $t_{d2}$ are both set to about 30 ns. The 1-GHz high-bandwidth oscilloscope MSO64 6-BW-1000A and passive voltage probe TPP1000 from Tektronix were used to accurately measure the switching waveforms.

Through the experiment, the waveforms of $v_{DS1}$, $v_{DS2}$, and $v_{sense}$ at the load current of 2 and 10 A were measured, as shown in Fig. 17. Based on the proposed current measurement method, $i_{DS1}$ and $i_{DS2}$ were derived from the measured $v_{sense}$. Then, the experimental waveforms of $v_{DS1}$, $v_{DS2}$, $i_{DS1}$, and $i_{DS2}$ were replotted in Figs. 18 and 19 to be compared with the switching waveforms by the proposed model. Benefitting from the consideration of the nonlinear capacitances and the unique reverse characteristics of GaN HEMTs, and almost all the parasitic inductances of circuit into the proposed analytical

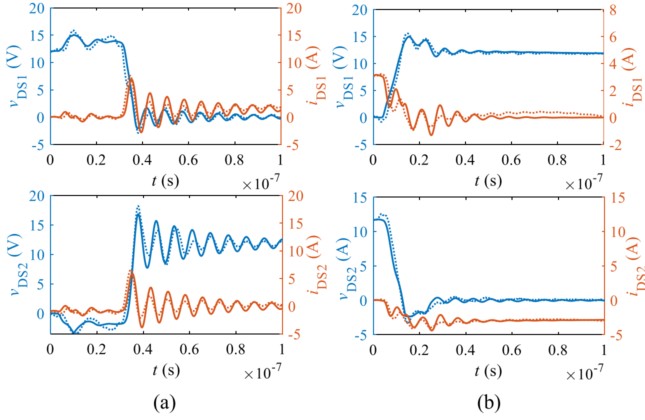



Fig. 18. Switching waveforms comparison between the proposed model and experiment at the load current of 2 A (solid line: proposed model, dotted line: experiment). (a) Phase I and II. (b) Phase III and IV.

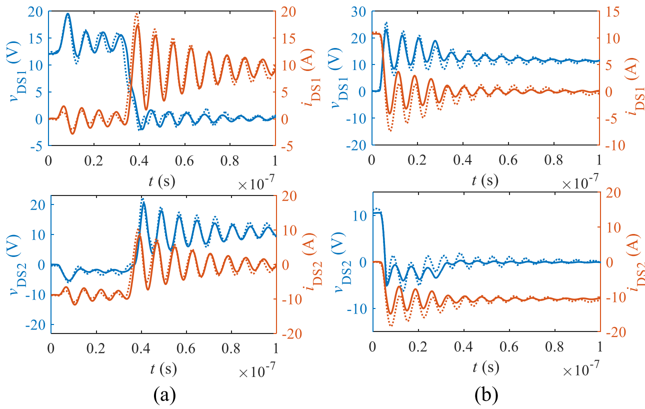



Fig. 19. Switching waveforms comparison between the proposed model and experiment at the load current of 10 A (solid line: proposed model, dotted line: experiment). (a) Phase I and II. (b) Phase III and IV.

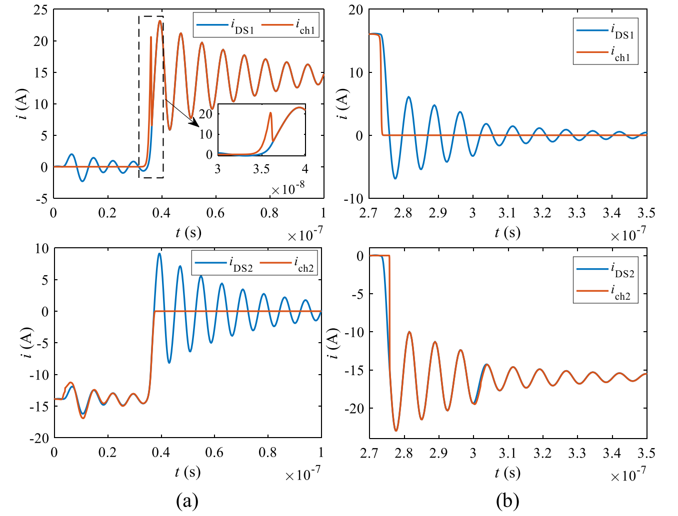



Fig. 20. Derived channel currents by the proposed model at the load current of 15 A. (a) Phase I and II. (b) Phase III and IV.

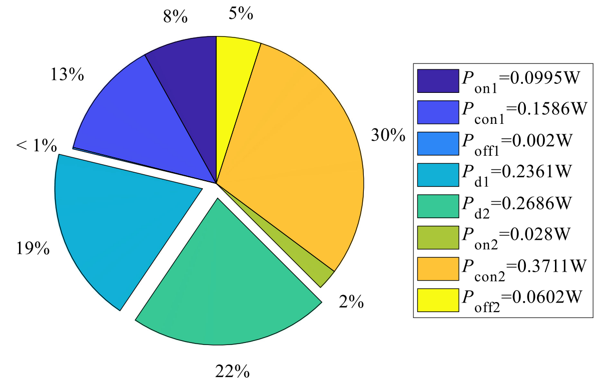



Fig. 21. Decomposition of power losses related to GaN HEMTs.

model, the simulation results during the full switching period show good agreement with the experimental results. The error between the simulation results and experimental results can be attributed to the following two reasons. First, the experimental results are highly related to the designed measuring points, the complicated parasitics in actual circuit can have great influence on the measurement results. Second, the temperature effect was not considered in the proposed analytical model, while the junction temperature has serious and complex influence on the operation of switching devices. Nevertheless, the accuracy of the proposed analytical model of GaN HEMTs was verified, thus we can have accurate evaluation of the power losses.

### *D. Decomposition of Power Losses Based on the Proposed Analytical Model*

Conventionally, the power losses of switching devices are calculated by integrating the product of drain-to-source voltage and drain current, as shown in (21). It is not quite exact due to the presence of the output capacitance. It is more accurate by using (22) to calculate the power losses of switching devices. As the channel current is usually unmeasurable, so (21) is still widely used for calculation power losses of switching devices.

$$P_{\text{loss}} = f \cdot \int i_{\text{DS}} \cdot v_{\text{DS}} \text{d}t \tag{21}$$

$$P_{\text{loss}} = f \cdot \int i_{\text{ch}} \cdot v_{\text{DS}} \text{d}t. \tag{22}$$

In this article, the channel current can be calculated accurately, as shown in Fig. 20, so the power losses of switching devices can be accurately evaluated by using (22). Based on the proposed model, power losses of top switch and bottom switch are calculated at the load current of 10 A, including the turn-ON loss of top switch $P_{\text{on1}}$, conduction loss of top switch $P_{\text{con1}}$, turn-OFF loss of top switch $P_{\text{off1}}$, turn-ON loss of bottom switch $P_{\text{on2}}$, conduction loss of bottom switch $P_{\text{con2}}$, turn-OFF loss of bottom switch $P_{\text{off2}}$, deadtime loss before top switch turning ON $P_{\text{d1}}$, and the deadtime loss after top switch turning OFF $P_{\text{d2}}$. Then, the calculated power losses are plotted in Fig. 21, which shows that the deadtime losses $P_{\text{d1}}$ and $P_{\text{d2}}$ are 0.2361 and 0.2686 W, respectively, accounting for significant proportions of the total power loss (19% and 22%, respectively). Therefore, it is very necessary to optimize the deadtimes to reduce deadtime losses and improve efficiency.

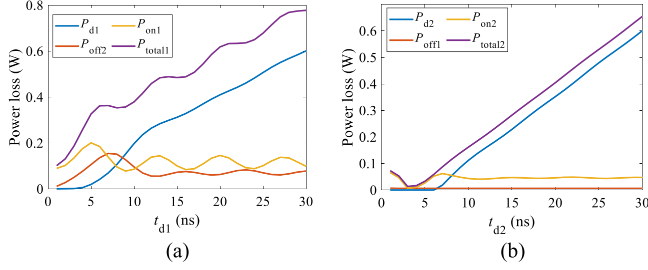



Fig. 22. Effects of deadtime $t_{d1}$ and $t_{d2}$ on power losses at the load current of 10 A. a) The effects of deadtime $t_{d1}$. (b) The effects of deadtime $t_{d2}$.

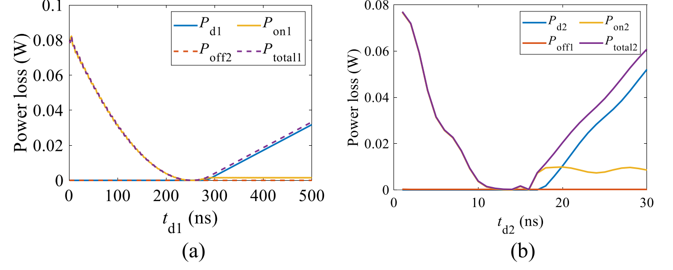



Fig. 23. Effects of deadtime $t_{d1}$ and $t_{d2}$ on power losses at the load current of 1 A. (a) The effects of deadtime $t_{d1}$. (b) The effects of deadtime $t_{d2}$.

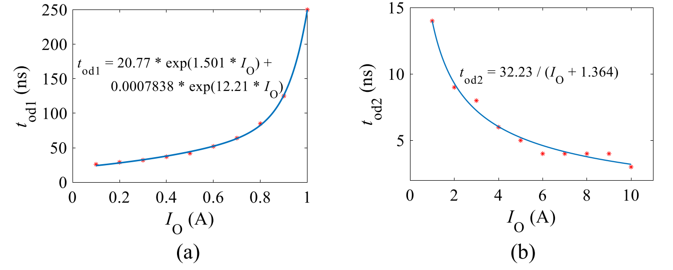



Fig. 24. Curve of optimal deadtime $t_{od1}$ and $t_{od2}$ versus load current $I_O$. (a) $t_{od1}$ vs. $I_O$. (b) $t_{od2}$ vs. $I_O$.

## V. Optimization of Deadtime

As mentioned above, due to the large reverse voltage of GaN HEMTs, the power losses during deadtime can account for significant proportions in the total power loss. It is very important to optimize the deadtime for higher efficiency. The two aforementioned deadtimes $t_{d1}$ and $t_{d2}$ can not only affect the deadtime losses, but also affect the other losses. Moreover, different load currents can have great impact on the selection of the deadtime because different load currents make different voltage changing rate during the switching transient. If the deadtime is too large, it can cause significant power loss during deadtime. If the deadtime is too short, it may cause short-through between top switch and bottom switch, which can also result in large power loss. Therefore, based on the proposed model, this section focuses on the optimization of the deadtime with the consideration of the load current's effect.

It can be easily understood that the deadtime $t_{d1}$ only affects $P_{d1}$, $P_{on1}$, and $P_{off2}$, while $t_{d2}$ only affects $P_{d2}$, $P_{off1}$, and $P_{on2}$. Fig. 22 shows the effects of $t_{d1}$ and $t_{d2}$ on power losses at the load current of 10 A. From Fig. 22(a), we can see that $P_{d1}$ increases as $t_{d1}$ increases while $P_{on1}$ and $P_{off2}$ have an oscillation with the increase of $t_{d1}$. The frequency of the oscillation is related to the resonance between parasitic inductance $L_{loop}$ and the output capacitance of GaN HEMTs $C_{OSS}$. Overall, the effect of $t_{d1}$ on $P_{total1}$, i.e., the sum of $P_{d1}$, $P_{on1}$, and $P_{off2}$, is mainly decided by $P_{d1}$, and in direct proportion to $t_{d1}$. However, if the load current $I_O$ is smaller than a value $I_{limit}$, as shown in (23), $I_L$ will have negative value and flow through $Q_1$ reversely to discharge $C_{OSS1}$, which reduces $v_{DS1}$ before $Q_1$ is turned ON, so $P_{on1}$ is reduced. With the increase of $t_{d1}$, $P_{on1}$ gets smaller, so does $P_{total1}$. When $v_{DS1}$ reduces to zero, the ZVS of $Q_1$ is achieved, and the continuous increase of $t_{d1}$ will charge $C_{OSS1}$ reversely to increase $-v_{DS1}$, so $P_{on1}$ and $P_{total1}$ are increased, the $t_{d1}$ when $v_{DS1}$ is zero is the optimal, as shown in Fig. 23(a). From Figs. 22(b) and 23(b), we can see that with the increase of $t_{d2}$, $P_{d2}$ does not change at the beginning until a value after which it increases almost linearly. With regard to $P_{on2}$, it decreases at beginning until a value after which it starts to increase, and then turns to flat. There is an optimal deadtime of $t_{d2}$ to realize minimum $P_{on2}$. It can be explained as follows. If $t_{d2}$ is too small, the turn-ON signal of bottom switch will arrive before top switch is turned OFF. Since $v_{DS2}$ is still positive, a large channel current will be caused, which increases $P_{on2}$. With the increase of $t_{d2}$, $v_{DS2}$ is smaller when the turn-ON signal of bottom switch comes, so $P_{on2}$ is smaller. If $v_{DS2}$ is zero when the turn-ON signal of bottom switch comes, $P_{on2}$ is smallest. The value of $t_{d2}$ is optimal. If we increase $t_{d2}$ further, $v_{DS2}$ will turn to negative before the turn-ON signal comes, $P_{on2}$ will increase slightly. When $-v_{DS2}$ is high enough to make $I_L$ flow through the channel absolutely, the continuous increase of $t_{d2}$ will no longer increase $P_{on2}$. As for $P_{off1}$, it is not affected by $t_{d2}$. The result is that there is an optimal $t_{d2}$ to make the sum of $P_{d2}$, $P_{off1}$, and $P_{on2}$ minimum.

$$I_{limit} = \frac{V_{dc}\,(1-D)\,DT}{L_O} \approx 1.2\text{ A}. \tag{23}$$

According to the above analysis, $t_{d1}$ should be as short as possible if $I_O$ is higher than $I_{limit}$. In this article, $t_{d1}$ is set to 3 ns if $I_O$ is higher than $I_{limit}$. But if $I_O$ is lower than $I_{limit}$, there is an optimal $t_{d1}$. The effect of $t_{d1}$ under different load currents below $I_{limit}$ is investigated, the optimal values of $t_{d1}$ under different currents below $I_{limit}$ are obtained as shown in Fig. 24(a). The smaller $I_O$ makes larger negative peak of $I_L$ to accelerate the discharge of $C_{OSS1}$, so the required optimal deadtime $t_{od1}$ is smaller. As for $t_{d2}$, the optimal value exists within full load range, so the effect of $t_{d2}$ under different load currents is also invesgated, the optimal values of $t_{d2}$ under different load currents are obtained in Fig. 24(b). Since larger $I_O$ charges or discharges the output capacitance faster, the optimal deadtime $t_{od2}$ is smaller with the increase of $I_O$. Then, the comparison between the optimized deadtime and the fixed deadtime is conducted, $t_{d1}$ and $t_{d2}$ are both fixed to 5, 10, and 15 ns, respectively. As shown in Fig. 25, through the optimization control of $t_{d1}$ and $t_{d2}$ under different load currents, the efficiency within full load range can be improved obviously. Compared with the fixed deadtime of 15 ns, the increase of efficiency can be up to 8%.

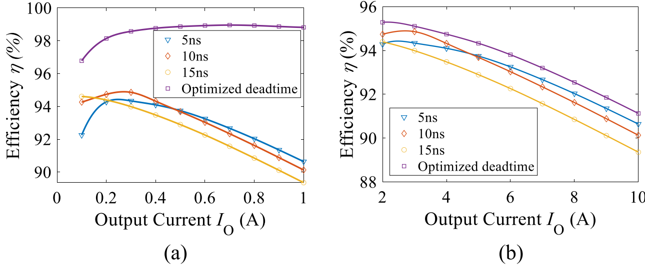



Fig. 25. Comparison of efficiency between the optimized deadtime and fixed deadtime. (a) $I_{\mathrm{O}} < I_{\mathrm{limit}}$. (b) $I_{\mathrm{O}} > I_{\mathrm{limit}}$.

## VI. Conclusion

In order to optimize the deadtime for higher efficiency, this article proposes an accurate analytical model of GaN HEMTs, including circuit's parasitic inductances, the nonlinear capacitances, the unique reverse characteristics, etc. The proposed analytical model fully uses the datasheet to avoid additional experiments. A 12-3.3 V synchronous buck converter based on EPC2015C is taken as the example to build the analytical model. The proposed model is first verified by simulation in LTspice. For experimental verification, a novel parasitics-based current measurement method is proposed, which is verified by simulation in LTspice. Then, the proposed analytical model of GaN HEMTs is verified by experiments, and good agreement is demonstrated. Based on the accurate analytical model, the deadtimes are optimized for different load currents to improve the efficiency within the full load range. Compared with the fixed deadtime of 15 ns, the increase of efficiency can be up to 8%. In the future work, on the basis of the proposed analytical model of GaN HEMTs in this article, we will investigate the effects of circuit's parasitic inductances and driving resistances on the switching losses and voltage overshoot, to provide guidance for engineers to optimize the circuit's parameters.

## Appendix

As mentioned in Section III, the circuit-level model is written into the form of the state-space equation

$$\frac{\mathrm{d}X}{\mathrm{d}t} = \mathrm{A}X + \mathrm{B} \tag{A1}$$

where $X = [v_{\mathrm{GS1}}\ i_{\mathrm{G1}}\ v_{\mathrm{GS2}}\ i_{\mathrm{G2}}\ v_{\mathrm{DS1}}\ v_{\mathrm{DS2}}\ i_{\mathrm{DS1}}\ i_{\mathrm{DS2}}\ i_{\mathrm{in}}\ v_{\mathrm{in}}]^T$. According to (7)–(16)

$$\mathrm{A} = \begin{bmatrix} 0 & a_1 & 0 & 0 & 0 & 0 & a_2 & 0 & 0 & 0 \\ a_3 & a_4 & a_5 & a_6 & a_7 & a_8 & a_9 & 0 & 0 & a_{10} \\ 0 & 0 & 0 & a_{11} & 0 & 0 & a_{12} & 0 & 0 & 0 \\ a_{13} & a_{14} & a_{15} & a_{16} & a_{17} & a_{18} & a_{19} & 0 & 0 & a_{20} \\ 0 & a_{21} & 0 & 0 & 0 & 0 & a_{22} & 0 & 0 & 0 \\ 0 & 0 & 0 & a_{23} & 0 & 0 & a_{24} & 0 & 0 & 0 \\ a_{25} & a_{26} & a_{27} & a_{28} & a_{29} & a_{30} & a_{31} & 0 & 0 & a_{32} \\ a_{33} & a_{34} & a_{35} & a_{36} & a_{37} & a_{38} & a_{39} & 0 & 0 & a_{40} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & a_{41} \\ 0 & 0 & 0 & 0 & 0 & 0 & a_{42} & 0 & a_{43} & 0 \end{bmatrix} \tag{A2}$$

$$\mathrm{B} = \begin{bmatrix} b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & b_7 & b_8 & b_9 & 0 \end{bmatrix}^T \tag{A3}$$

where

$$a_1 = \frac{C_{\mathrm{OSS1}}}{C_{\mathrm{ISS1}} \cdot C_{\mathrm{OSS1}} - {C_{\mathrm{GD1}}}^2} \tag{A4}$$

$$a_2 = \frac{C_{\mathrm{GD1}}}{C_{\mathrm{ISS1}} \cdot C_{\mathrm{OSS1}} - {C_{\mathrm{GD1}}}^2} \tag{A5}$$

$$a_3 = \frac{-\left[(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\right]}{(L_{\mathrm{G1}} + L_{\mathrm{S}})\,(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\,(L_{\mathrm{G1}} + L_{\mathrm{G2}} + 2L_{\mathrm{S}})} \tag{A6}$$

$$a_4 = R_{\mathrm{G1}} a_3 \tag{A7}$$

$$a_5 = a_{13} = \frac{-{L_{\mathrm{S}}}^2}{(L_{\mathrm{G1}} + L_{\mathrm{S}})\,(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\,(L_{\mathrm{G1}} + L_{\mathrm{G2}} + 2L_{\mathrm{S}})} \tag{A8}$$

$$a_6 = R_{\mathrm{G2}}\ a_5 \tag{A9}$$

$$a_7 = a_8 = \frac{L_{\mathrm{S}}\,(L_{\mathrm{G2}} + L_{\mathrm{S}})}{(L_{\mathrm{G1}} + L_{\mathrm{S}})\,(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\,(L_{\mathrm{G1}} + L_{\mathrm{G2}} + 2L_{\mathrm{S}})} \tag{A10}$$

$$a_9 = R_{\mathrm{loop}}\ a_7 \tag{A11}$$

$$a_{10} = -a_7 \tag{A12}$$

$$a_{11} = \frac{C_{\mathrm{OSS2}}}{C_{\mathrm{ISS2}} \cdot C_{\mathrm{OSS2}} - {C_{\mathrm{GD2}}}^2} \tag{A13}$$

$$a_{12} = \frac{C_{\mathrm{GD2}}}{C_{\mathrm{ISS2}} \cdot C_{\mathrm{OSS2}} - {C_{\mathrm{GD2}}}^2} \tag{A14}$$

$$a_{14} = R_{\mathrm{G1}}\ a_{13} \tag{A15}$$

$$a_{15} = \frac{-\left[(L_{\mathrm{G1}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\right]}{(L_{\mathrm{G1}} + L_{\mathrm{S}})\,(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\,(L_{\mathrm{G1}} + L_{\mathrm{G2}} + 2L_{\mathrm{S}})} \tag{A16}$$

$$a_{16} = R_{\mathrm{G2}}\ a_{15} \tag{A17}$$

$$a_{17} = a_{18} = \frac{L_{\mathrm{S}}\,(L_{\mathrm{G1}} + L_{\mathrm{S}})}{(L_{\mathrm{G1}} + L_{\mathrm{S}})\,(L_{\mathrm{G2}} + L_{\mathrm{S}})\, L_{\mathrm{loop}} - {L_{\mathrm{S}}}^2\,(L_{\mathrm{G1}} + L_{\mathrm{G2}} + 2L_{\mathrm{S}})} \tag{A18}$$

$$a_{19} = R_{\mathrm{loop}}\ a_{18} \tag{A19}$$

$$a_{20} = -a_{17} \tag{A20}$$

$$a_{21} = \frac{C_{\mathrm{GD1}}}{C_{\mathrm{ISS1}} \cdot C_{\mathrm{OSS1}} - {C_{\mathrm{GD1}}}^2} \tag{A21}$$

$$a_{22} = \frac{C_{\mathrm{ISS1}}}{C_{\mathrm{ISS1}} \cdot C_{\mathrm{OSS1}} - {C_{\mathrm{GD1}}}^2} \tag{A22}$$

$$a_{23} = \frac{C_{\mathrm{GD2}}}{C_{\mathrm{ISS2}} \cdot C_{\mathrm{OSS2}} - {C_{\mathrm{GD2}}}^2} \tag{A23}$$

$$a_{24} = \frac{\mathrm{C_{ISS2}}}{\mathrm{C_{ISS2}} \cdot \mathrm{C_{OSS2}} - \mathrm{C_{GD2}}^2} \quad \text{(A24)}$$

$$a_{25} = a_{33} = \frac{L_\mathrm{S}\left(L_\mathrm{G2} + L_\mathrm{S}\right)}{\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\left(L_\mathrm{G1} + L_\mathrm{G2} + 2L_\mathrm{S}\right)} \quad \text{(A25)}$$

$$a_{26} = a_{34} = R_\mathrm{G1}\ \ a_{25} \quad \text{(A26)}$$

$$a_{27} = a_{35} = \frac{L_\mathrm{S}\left(L_\mathrm{G1} + L_\mathrm{S}\right)}{\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\left(L_\mathrm{G1} + L_\mathrm{G2} + 2L_\mathrm{S}\right)} \quad \text{(A27)}$$

$$a_{28} = a_{36} = R_\mathrm{G2}\ \ a_{27} \quad \text{(A28)}$$

$$a_{29} = a_{30} = a_{37} = a_{38} = \frac{-\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)}{\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\left(L_\mathrm{G1} + L_\mathrm{G2} + 2L_\mathrm{S}\right)} \quad \text{(A29)}$$

$$a_{31} = a_{39} = R_\mathrm{loop}\ \ a_{29} \quad \text{(A30)}$$

$$a_{32} = a_{40} = -a_{29} \quad \text{(A31)}$$

$$a_{41} = -\frac{1}{L_\mathrm{in}} \quad \text{(A32)}$$

$$a_{42} = -\frac{1}{C_\mathrm{in}} \quad \text{(A33)}$$

$$a_{43} = -a_{42} \quad \text{(A34)}$$

$$b_1 = \frac{-C_\mathrm{GD1} i_\mathrm{ch1}}{\mathrm{C_{ISS1}} \cdot \mathrm{C_{OSS1}} - \mathrm{C_{GD1}}^2} \quad \text{(A35)}$$

$$b_2 = \frac{\left[\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\right]V_\mathrm{G1} + L_\mathrm{S}^2 V_\mathrm{G2} + L_\mathrm{S}^3 \frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t}}{\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\left(L_\mathrm{G1} + L_\mathrm{G2} + 2L_\mathrm{S}\right)} \quad \text{(A36)}$$

$$b_3 = \frac{-C_\mathrm{GD2}\left(I_\mathrm{L} + i_\mathrm{ch2}\right)}{C_\mathrm{ISS2} \cdot C_\mathrm{OSS2} - C_\mathrm{GD2}^2} \quad \text{(A37)}$$

$$b_4 = \frac{L_\mathrm{S}^2 V_\mathrm{G1} + \left[\left(L_\mathrm{G1} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\right]V_\mathrm{G2} + \left[\left(L_\mathrm{G1} + L_\mathrm{S}\right)L_\mathrm{loop}L_\mathrm{S} - L_\mathrm{S}^3\right]\frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t}}{\left(L_\mathrm{G1} + L_\mathrm{S}\right)\left(L_\mathrm{G2} + L_\mathrm{S}\right)L_\mathrm{loop} - L_\mathrm{S}^2\left(L_\mathrm{G1} + L_\mathrm{G2} + 2L_\mathrm{S}\right)} \quad \text{(A38)}$$

$$b_5 = \frac{-C_\mathrm{ISS1} i_\mathrm{ch1}}{C_\mathrm{ISS1} \cdot C_\mathrm{OSS1} - C_\mathrm{GD1}^2} \quad \text{(A39)}$$

$$b_6 = \frac{-C_\mathrm{ISS2}\left(I_\mathrm{L} + i_\mathrm{ch2}\right)}{C_\mathrm{ISS2} \cdot C_\mathrm{OSS2} - C_\mathrm{GD2}^2} \quad \text{(A40)}$$

$$b_7 = \frac{-(L_\mathrm{G1}+L_\mathrm{S})L_\mathrm{S}^2 \frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t} - L_\mathrm{S}(L_\mathrm{G2}+L_\mathrm{S})V_\mathrm{G1} - L_\mathrm{S}(L_\mathrm{G1}+L_\mathrm{S})V_\mathrm{G2}}{(L_\mathrm{G1}+L_\mathrm{S})(L_\mathrm{G2}+L_\mathrm{S})L_\mathrm{loop} - L_\mathrm{S}^2(L_\mathrm{G1}+L_\mathrm{G2}+2L_\mathrm{S})} \quad \text{(A41)}$$

$$b_8 = \frac{-L_\mathrm{S}(L_\mathrm{G2}+L_\mathrm{S})V_\mathrm{G1} - L_\mathrm{S}(L_\mathrm{G1}+L_\mathrm{S})V_\mathrm{G2}}{(L_\mathrm{G1}+L_\mathrm{S})(L_\mathrm{G2}+L_\mathrm{S})L_\mathrm{loop} - L_\mathrm{S}^2(L_\mathrm{G1}+L_\mathrm{G2}+2L_\mathrm{S})} - \frac{\left[(L_\mathrm{G1}+L_\mathrm{S})(L_\mathrm{G2}+L_\mathrm{S})L_\mathrm{loop} - L_\mathrm{S}^2(L_\mathrm{G2}+L_\mathrm{S})\right]\frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t}}{(L_\mathrm{G1}+L_\mathrm{S})(L_\mathrm{G2}+L_\mathrm{S})L_\mathrm{loop} - L_\mathrm{S}^2(L_\mathrm{G1}+L_\mathrm{G2}+2L_\mathrm{S})} \quad \text{(A42)}$$

$$b_9 = \frac{V_\mathrm{dc}}{L_\mathrm{in}} \quad \text{(A43)}$$

where

$$\frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t} = \begin{cases} \frac{V_\mathrm{dc}(1-D)}{L_\mathrm{O}}, 0 \le t\ \le DT \\ \frac{-D \cdot V_\mathrm{dc}}{L_\mathrm{O}}, DT\ < t\ \le T \end{cases}, 0 \le D\ \le 1. \quad \text{(A44)}$$

## References


[1] X. C. Huang, Q. Li, Z. Y. Liu, and F. C. Lee, “Analytical loss model of high voltage GaN HEMT in cascode configuration,” *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2208–2219, May 2014.

[2] R. L. Xie, H. X. Wang, G. F. Tang, X. Yang, and K. J. Chen, “An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration,” *IEEE Trans. Power Electron.,* vol. 32, no. 8, pp. 6416–6433, Aug. 2017.

[3] D. Han and B. Sarlioglu, “Deadtime effect on GaN-Based synchronous boost converter and analytical model for optimal deadtime selection,” *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 601–612, Jan. 2016.

[4] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, “Modeling of wide bandgap power semiconductor devices–Part I,” *IEEE Trans. Electron. Devices,* vol. 62, no. 2, pp. 423–433, Feb. 2015.

[5] E. A. Jones, F. Wang, and D. Costinett, “Review of commercial GaN power devices and GaN-based converter design challenges,” *IEEE J. Emerg. Sel. Top. Power Electron.,* vol. 4, no. 3, pp. 707–719, Sep. 2016.

[6] K. P. Wang, X. Yang, H. C. Li, H. Ma, X. J. Zeng, and W. J. Chen, “An analytical switching process model of low-voltage eGaN HEMTs for loss calculation,” *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 635–647, Jan. 2016.

[7] F. M. Yigletu, S. Khandelwal, T. A. Fjeldly, and B. Iniguez, “Compact charge-based physical models for current and capacitances in AlGaN/GaN HEMTs,” *IEEE Trans. Electron. Devices,* vol. 60, no. 11, pp. 3746–3752, Nov. 2013.

[8] H. Li, X. R. Zhao, W. Z. Su, K. Sun, T. Q. Zheng, and X. J. You, “Nonsegmented PSpice circuit model of GaN HEMT with simulation convergence consideration,” *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 8992–9000, Nov. 2017.

[9] R. Yuancheng, X. Ming, Z. Jinghai, and F. C. Lee, “Analytical loss model of power MOSFET,” *IEEE Trans. Power Electron.,* vol. 21, no. 2, pp. 310–319, Mar. 2006.

[10] D. Cucak *et al.*, “Physics-based analytical model for input, output, and reverse capacitance of a GaN HEMT with the field-plate structure,” *IEEE Trans. Power Electron.,* vol. 32, no. 3, pp. 2189–2202, Mar. 2017.

[11] M. Turzynski and W. J. Kulesza, “A simplified behavioral MOSFET model based on parameters extraction for circuit simulations,” *IEEE Trans. Power Electron.,* vol. 31, no. 4, pp. 3096–3105, Apr. 2016.

[12] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, “Datasheet driven silicon carbide power MOSFET model,” *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2220–2228, May 2014.

[13] S. K. Roy and K. Basu, “Analytical estimation of turn on switching loss of SiC MOSFET and Schottky diode pair from datasheet parameters,” *IEEE Trans. Power Electron.,* vol. 34, no. 9, pp. 9118–9130, Sep. 2019.

[14] S. K. Roy and K. Basu, “Analytical model to study hard turn-off switching dynamics of SiC mosfet and Schottky diode pair,” *IEEE Trans. Power Electron.,* vol. 36, no. 1, pp. 861–875, Jan. 2021.

[15] Y. J. Xin *et al.*, “Analytical switching loss model for GaN-based control switch and synchronous rectifier in low-voltage buck converters,” *IEEE J. Emerg. Sel. Top. Power Electron.,* vol. 7, no. 3, pp. 1485–1495, Sep. 2019.

[16] Y. F. Shen, H. Wang, Z. Shen, F. Blaabjerg, and Z. Qin, “An analytical turn-on power loss model for 650-V GaN eHEMTs,” in *Proc. Thirty-3rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 913–918.

[17] Y. Zhang, C. Chen, T. Liu, K. Xu, Y. Kang, and H. Peng, “A high efficiency model-based adaptive dead-time control method for GaN HEMTs considering nonlinear junction capacitors in triangular current mode operation,” *IEEE J. Emerg. Sel. Top. Power Electron.,* vol. 8, no. 1, pp. 124–140, Mar. 2020.

[18] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.,* vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[19] C. Salcines, I. Kallfass, H. Kakitani, and A. Mikata, "Dynamic characterization of the input and reverse transfer capacitances in power MOSFETs under high current conduction," in *Proc. Apec 2016 31st Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2969–2972.

[20] I. Castro *et al.*, "Analytical switching loss model for superjunction MOSFET with capacitive nonlinearities and displacement currents for DC-DC power converters," *IEEE Trans. Power Electron.,* vol. 31, no. 3, pp. 2485–2495, Mar. 2016.

[21] L. Aubard, G. Verneau, J. C. Crebier, C. Schaeffer, and Y. Avenas, "Power MOSFET switching waveforms: An empirical model based on a physical analysis of charge locations," in *Proc. 2002 IEEE 33rd Annu. IEEE Power Electron. Specialists Conf. Proc.*, 2002, pp. 1305–1310.

[22] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: An improved analytical losses model," *IEEE Trans. Power Electron.,* vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[23] J. S. Glaser and D. Reusch, "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.,* 2016, pp. 1–8.

[24] K. N. Chen, Z. M. Zhao, L. Q. Yuan, T. Lu, and F. B. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET," *IEEE Trans. Electron Devices,* vol. 62, no. 2, pp. 333–338, Feb. 2015.

[25] R. Q. Li, Q. H. Zhu, and M. J. Xie, "A new analytical model for predicting *dv/dt*-induced low-side MOSFET false turn-on in synchronous buck converters," *IEEE Trans. Power Electron.,* vol. 34, no. 6, pp. 5500–5512, Jun. 2019.

[26] J. Brown, "Modeling the switching performance of a MOSFET in the high side of a non-isolated buck converter," *IEEE Trans. Power Electron.,* vol. 21, no. 1, pp. 3–10, Jan. 2006.

[27] Y. L. Xiong, S. Sun, H. W. Jia, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.,* vol. 24, no. 1–2, pp. 525–531, Jan./Feb. 2009.

[28] C. C. McAndrew and J. J. Victory, "Accuracy of approximations in MOSFET charge models," *IEEE Trans. Electron Devices,* vol. 49, no. 1, pp. 72–81, Jan. 2002.

[29] V. Dimitrov, P. Goranov, and D. Hvarchilkov, "An analytical approach to model the switching losses of a power MOSFET," in *Proc. 2016 IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 928–933.

[30] S. Eskandari, K. Peng, B. Tian, and E. Santi, "Accurate analytical switching loss model for high voltage SiC MOSFETs includes parasitics and body diode reverse recovery effects," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1867–1874.

[31] J. J. Wang, H. S. H. Chung, and R. T. H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.,* vol. 28, no. 1, pp. 573–590, Jan. 2013.

[32] A. Endruschat, C. Novak, H. Gerstner, T. Heckel, C. Joffe, and M. Marz, "A universal SPICE field-effect transistor model applied on SiC and GaN transistors," *IEEE Trans. Power Electron.,* vol. 34, no. 9, pp. 9131–9145, Sep. 2019.

[33] Efficient Power Conversion Corporation. "Circuit simulations using EP-C device models," [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/Circuit_Simulations_Using_Device_M-odels.pdf

[34] A. X. Zhang *et al.*, "Analytical modeling of capacitances for GaN HEMTs, including parasitic components," *IEEE Trans. Electron. Devices,* vol. 61, no. 3, pp. 755–761, Mar. 2014.

[35] Y. H. Jia, Y. H. Xu, Z. Wen, Y. Q. Wu, and Y. X. Guo, "Analytical gate capacitance models for large-signal compact model of AlGaN/GaN HEMTs," *IEEE Trans. Electron. Devices,* vol. 66, no. 1, pp. 357–363, Jan. 2019.

[36] H. Gerstner, A. Endruschat, T. Heckel, C. Joffe, B. Eckardt, and M. Marz, "Non-linear input capacitance determination of WBG power FETs using gate charge measurements," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 247–253.

[37] S. Aamir Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Capacitance modeling in dual field-plate power GaN HEMT for accurate switching behavior," *IEEE Trans. Electron. Devices,* vol. 63, no. 2, pp. 565–572, Feb. 2016.

[38] X. X. Cheng, M. Li, and Y. Wang, "Physics-based compact model for AlGaN/GaN MODFETs with close-formed I-V and C-V characteristics," *IEEE Trans. Electron. Devices,* vol. 56, no. 12, pp. 2881–2887, Dec. 2009.

[39] G. Amarnath, R. Swain, and T. R. Lenka, "Modeling and simulation of 2DEG density and intrinsic capacitances in AlInN/GaN MOSHEMT," *Int. J. Numer. Modeling-Electron. Netw. Devices Fields,* vol. 31, no. 1, pp. 1–8, Jan./Feb. 2018.

[40] J. Waldron and T. P. Chow, "Physics-based analytical model for high-voltage bidirectional GaN transistors using lateral GaN power HEMT," in *Proc. 25th Int. Symp. Power Semicond. Devices IC's*, 2013, pp. 213–216.

[41] F. K. M. U. O. Keysan, "Investigation of turn-on and turn-off characteristics of enhancement-mode GaN power transistors," in *Proc. 20th Eur. Conf. Power Electron. Appl.*, 2018, pp. P.1–P.9.

[42] Efficient Power Conversion Corporation. "EPC2015C-Enhancement Mode Power transistor," EPC2015C datasheet, 2020. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2015C_ datasheet.pdf

[43] D. Reusch, D. Gilham, Y. P. Su, and F. C. Lee, "Gallium nitride based 3D integrated non-isolated point of load module," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 38–45.

**Zhiyuan Qi** (Student Member, IEEE) was born in Henan Province, China, in 1989. He received the B.S. and M.S. degrees in electrical engineering and automation from Harbin Engineering University, Harbin, China, in 2012 and 2015, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include the packaging and integration of wide-bandgap power semiconductors and high-frequency power conversion technologies.

**Yunqing Pei** (Member, IEEE) was born in 1969. He received the B.S. and M.S. degrees in electrical engineering, and the Ph.D. degree in power electronics from Xi'an Jiaotong University, Xi'an, China, in 1991, 1994, and 1999, respectively.

He was a Faculty Member with Xi'an Jiaotong University, where he is currently a Professor. From 2006 to 2007, he was a Visiting Scholar with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University. His research interests include the high-power inverters, switch-mode power supply, and converters in distributed generation systems.

**Laili Wang** (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Electrical Engineering Department, Queen.s University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Canada. In 2017, he joined as a Full Professor with Xi'an Jiaotong University. His research interests include package and integration, wireless power transfer, and energy harvesting.

Dr. Wang is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Vice Chair of the Technical Committee of Power Conversion Systems and Components (TC2) in PELS, the Co-Chair of the System Integration and Application in International Technology Roadmap for Wide Bandgap Power Semiconductor (ITRW), and the Chair of the IEEE CPSS and PELS Joint Chapter in Xi'an, China.

**Kangping Wang** (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012 and 2018, respectively.

From 2016 to 2017, he was with the Department of ePOWER, Electrical and Computer Engineering, Queen.s University, Canada, as a Visiting Scholar. Since 2018, he has been an Associate Professor with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China. His research interests include high-frequency power conversion technology, and application and integration technology of wide-bandgap devices.

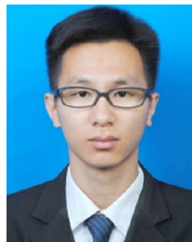
Dr. Wang was the recipient of the Best Paper Award of the International Conference on Power Electronics – ECCE Asia in 2019.

**Mengyu Zhu** was born in 1997. She received the B.S. degree in electrical engineering and automation from the China University of Mining and Technology, Xuzhou, China, in 2018. She is currently working toward the M.S. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

Her research interests include gate drive technologies of wide-bandgap semiconductors, design of high-power high-voltage power converters, high-temperature semiconductor packaging technology, and high-temperature converter.

**Cheng Zhao** (Student Member, IEEE) was born in Shanxi, China, in 1996. He received the B.S. degree in electrical engineering from Jilin University, Changchun, China, in 2017. He is currently working toward the Ph.D. degree in electronic and electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include packaging and applications of power semiconductor devices and parallel operation of SiC MOSFETs.



**Qingshou Yang** was born in Hebei, China, in 1993. He received the B.S. and M.S. degrees in electrical engineering and automation from Yanshan University, Qinhuangdao, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include application of wide-bandgap devices and power electronic integration.

**Yongmei Gan** was born in 1971. She received the B.S. degree and the M.S. degree in control engineering from the Xi'an University of Technology, Xi'an, China, in 1993 and 1996, respectively, and the Ph.D. degree in control theory and control engineering from Northwestern Polytechnical University, Xi'an, China, in 1999.

Since 2000, she has been with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, where she is currently an Associate Professor. From 2008 to 2009, she was a Visiting Scholar with the Electrical and Computer Engineering, University of Toronto. Her research interests include package and integration, energy harvesting, and supervisory control of discrete-event systems.