A Novel Three-Phase Dual-Output Neutral-Point-Clamped Three-Level Inverter

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***Abstract*—A novel topology of a three-phase dual-output neutral-point-clamped three-level inverter (DO-NPC-TLI) is proposed. DO-NPC-TLI can achieve two groups of ac voltage outputs with adjustable frequency and amplitude. We describe the topology in detail. The proposed topology is based on a neutral-point-clamped three-level inverter (NPC-TLI). A total of eight switches and six clamping diodes are added to the NPC-TLI to form the new topology, and then analyze the working principle of the circuit. With the consideration of neutral point voltage balance, a modulation strategy combining the time-sharing modulation idea and virtual space vector pulsewidth modulation (VSVPWM) is proposed. In order to simplify the complicated calculation process of VSVPWM, a carrier-based PWM based on VSVPWM is proposed. All of the duty ratios are used to calculate the modulation waves of DO-NPC-TLI. The driving signals of switches are generated by comparing the modulation waves with a carrier. The modulation strategy mentioned above is verified by the experiment. The correctness of the experimental results illustrates the effectiveness of the modulation strategy and the feasibility of the proposed topology.**

***Index Terms*—Carrier-based pulsewidth modulation (CBPWM), dual-output (DO), netural-point-clamped (NPC), three-level-inverter (TLI), virtual space vector pulsewidth modulation (VSVPWM).**

I. Introduction

DUAL-AC motor drive systems are now developing in emerging industries, such as electric vehicles [1], [2], railway traction, wind power generation, and power-assisted ships [3]. The dual-output inverter is the key part. Each individual motor can be driven by a separate inverter. As the number of motors increases, so does the number of inverters, which makes it necessary to consider the size, cost, and other issues. Therefore, the proposed nine-switch inverter (NSI) replaces the use of two independent two-level inverters [4], [5], and this topology reduces the number of switches, size, and the cost. However, its switching devices need to withstand a higher voltage, not suitable for the high-voltage application. Its application is limited to some extent. Therefore, multilevel inverters are proposed.

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Compared with the traditional two-level inverters, multilevel inverters have significant advantages [6], [7]. The main advantage of the multilevel inverters is that the quality of voltage waveform is improved. And by increasing the number of switching devices, they jointly withstand the dc voltage and reduce the voltage withstood of each switching device [8]. In addition, the harmonic distortion of the output voltage is reduced and the efficiency of the inverter is improved. Multilevel inverters are usually applied in high-power and large-capacity occasions [9]. Therefore, the multilevel inverters can be chosen to use for better application in the field of dual-ac motor drive.

Bhattacharya *et al.* [10] used two groups of independent three-level inverters to drive the motor. But the number of switches of three-level inverters is already more than that of two-level inverters. Despite the superior performance, the size and cost are also increased. A three-level dual-output inverter is proposed in [11]. But the inverter has a limitation of the switching mode due to its topology. The neutral point voltage is difficult to balance. Therefore, an alternative three-level dual-output inverter is proposed in this article. On the basis of the topology of neutral-point-clamped three-level inverter (NPC-TLI), which is widely used [12], eight switches and six clamping diodes are added to form a new topology, namely the proposed dual-output neutral-point-clamped three-level inverter (DO-NPC-TLI).

For the modulation strategy, the topology proposed in [10] is two groups of independent inverters, each group of which can be modulated separately by space vector pulsewidth modulation (SVPWM) for three-level inverters. Haruna and Hoshi [11] proposed the sinusoidal pulsewidth modulation (SPWM) for the simplified three-level dual-output topology. In order to improve the modulation index, the zero-sequence voltage is required with the SPWM. And the neutral point voltage balance is not considered. Moreover, the output-phase voltage has a larger dc voltage offset. Although the modulation strategy has been proposed, due to the lack of research in this area, the strategy can be used to refer is very few. However, NSI was proposed earlier, so its modulation strategy has been mature and can be used for reference. In [13], SVPWM applied to NSI has been proposed. A pulsewidth modulation (PWM) period is evenly divided into two segments. In the former half period, inverter 1 is modulated directly by SVPWM, while inverter 2 works in a zero vector state. In the latter half period, the situation is just opposite to the former half period, that is, in a PWM period, two groups of inverters can work alternately. SVPWM can improve the utilization of dc voltage and its technology is mature. Therefore, a new modulation strategy for the three-level

dual-output inverter is proposed by combining the time-sharing modulation idea of NSI with three-level SVPWM. Gupta and Khambadkone [14] show a three-level SVPWM modulation strategy based on the rectangular coordinate system. This modulation strategy is widely used because of being simple to control and its high-voltage utilization rate. However, NPC-TLI has the problem of neutral point voltage balance [15] and DO-NPC-TLI also has the same problem. Only the SVPWM modulation strategy cannot solve the problem. Therefore, other modulation strategies need to be considered. Chen *et al.* [16] and Wang *et al.* [17] propose a method of injecting zero-sequence voltage to balance the neutral point voltage but it is difficult to calculate the zero-sequence voltage. Song *et al.* [18] propose an idea of using the allocation factor on the basis of SVPWM by adjusting the action time of positive and negative short vectors. The neutral point potential fluctuation can be improved but cannot be completely suppressed [19]. Jiang *et al.* [20]–[22] propose a VSVPWM modulation strategy. The basic idea of this strategy is that new virtual vectors are synthesized by using medium vectors and short vectors. The current at the neutral point of each new vector is zero during the operation time. Accordingly, there is no effect on the neutral point voltage. Then, a VSVPWM modulation method for DO-NPC-TLI is proposed by combining the idea of time-sharing modulation and three-level VSVPWM.

However, during the calculation of the VSVPWM modulation strategy, there are a lot of trigonometric functions in duty ratios, which are complex. In addition, the judgment of sections and its subsections needs to be made, and the switching sequences of each sector need to be listed, which is a complicated process. In order to simplify the process of the calculation, a CBPWM based on VSVPWM is proposed, using switching sequences and duty ratios to calculate modulation waves. The expressions of modulation waves are simple and regular, which no longer contain the calculation of trigonometric functions. After comparing modulation waves with the triangular carrier wave, the desired driving signals of each switch can be obtained through a logical operation. The implementation of CBPWM simplifies the VSVPWM modulation algorithm to a great extent.

In order to have a better application in the field of dual-ac motor drive system, DO-NPC-TLI is proposed. It can achieve two groups of three-level ac outputs with adjustable amplitude and frequency. The structure of this article is as follows. Section II introduces the topology and the working principle of DO-NPC-TLI. Section III introduces the VSVPWM modulation strategy for DO-NPC-TLI and CBPWM by the VSVPWM modulation strategy. The experimental results are provided in Section IV. Finally, Section V offers the conclusion.

II. Topology and Working Principle of DO-NPC-TLI

A. Topology of DO-NPC-TLI

The topology of DO-NPC-TLI is shown in Fig. 1, which is adding eight switches and six clamping diodes on the basis of topology of NPC-TLI to form a new dual-output topology of DO-NPC-TLI. Each phase has six switches and four clamping diodes, respectively, defined as S_{x1}–S_{x6} and D_{x7}–D_{x10}, where "x" mentioned in the following part is all $x \in \{a, b, \text{and } c\}$. In addition, two switches S_{o1} and S_{o2} are directly connected to the

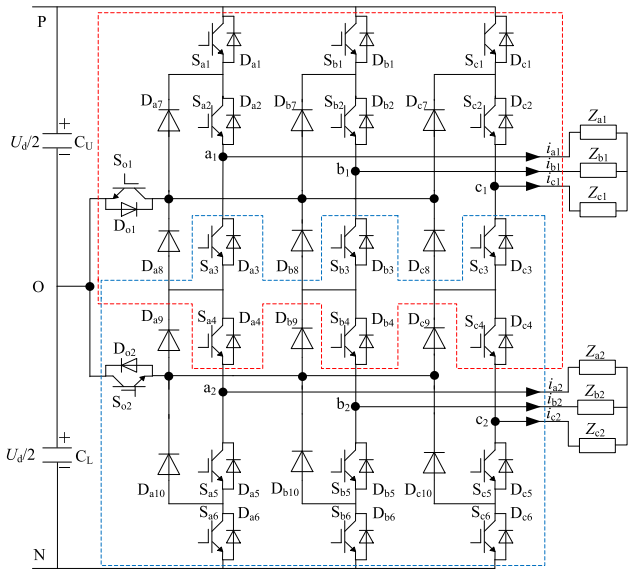

Fig. 1. Topology of DO-NPC-TLI.

capacitors on the dc side. Switches S_{x1}–S_{x4}, clamping diodes $D_{x7} - D_{x8}$, and switch S_{o1} constitute inverter 1 with three-phase ac voltage outputs u_{a1}, u_{b1}, and u_{c1}, as shown in the red dotted box. Switches S_{x3}–S_{x6}, clamping diodes $D_{x9} - D_{x10}$, and switch S_{o2} constitute inverter 2 with three-phase ac voltage outputs u_{a2}, u_{b2}, and u_{c2}, as shown in the blue dotted box. Switches S_{x3} and S_{x4} are the public switches of two inverters.

According to the content mentioned above, DO-NPC-TLI requires 20 switches and 12 diodes, i.e., one less switch and 12 more diodes than the topology in [11].

B. Working Principle

The circuit has two working modes. Mode 1 is that inverter 1 works in an effective working state and mode 2 is that inverter 2 works in an effective working state.

Mode 1: Inverter 1 is effective. Switches S_{x5} and S_{x6} of each phase and switch S_{o1} are in the ON state and switch S_{o2} is in the OFF state. At this time, three phases of inverter 2 are connected to the negative bus (state *N*), which means that inverter 2 outputs *NNN*, a zero vector. Each phase has three working states, respectively, state *P*, *O*, and *N*, corresponding to output voltage $+U_d/2$, 0, and $-U_d/2$. Taking phase *a* as an example, three working states of phase *a* are shown in Fig. 2(a)–(c).

As shown in Fig. 2(a), switches S_{a1} and S_{a2} are in the ON state. Whether the current flows from the circuit to the load (as shown by the red arrow) or from the load to the circuit (as shown by the blue arrow), at this time, the potential of output terminal a_1 is equal to the potential of point *P* and the output voltage is $+U_d/2$.

As shown in Fig. 2(b), switches S_{a2} and S_{a3} are in the ON state, and the potential of output terminal a_1 is equal to the potential of point *O*, and the output voltage is zero. It is in this state that there is one more switch ON than the other two states. Therefore, in this working state, the switch loss is indeed more than the other

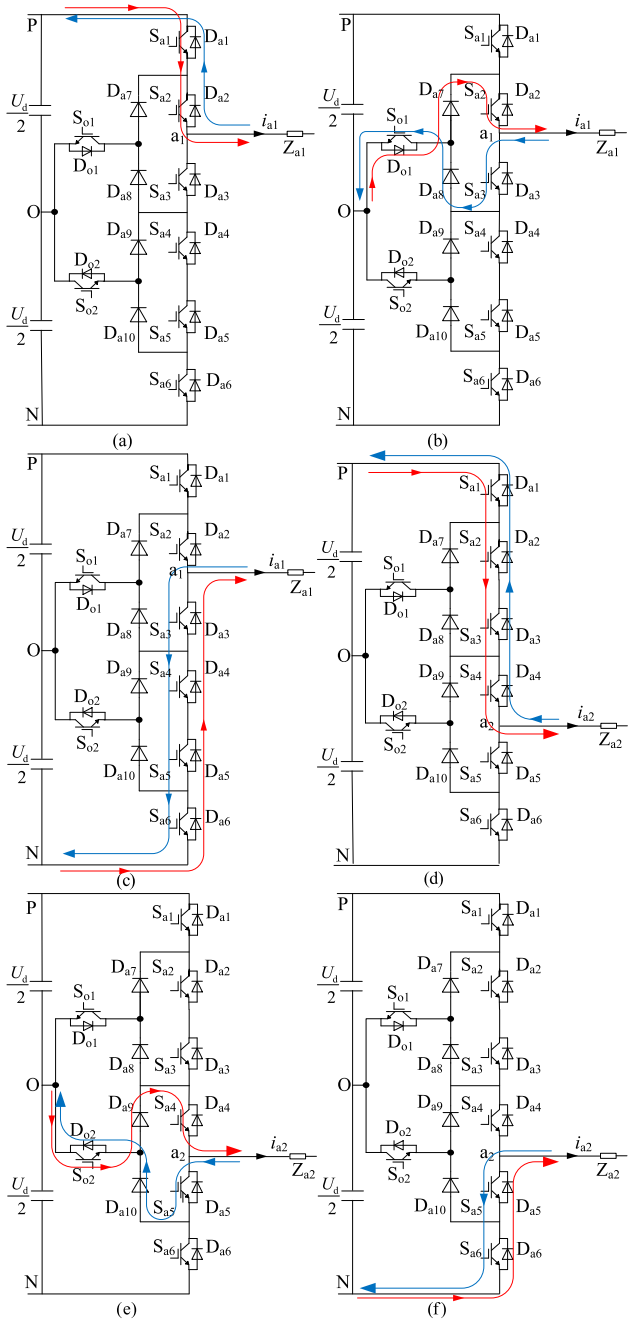

Fig. 2. Working states of modes 1 and 2.

two states. And compared with the topology in [11], the switch loss is actually slightly higher at the same switching frequency.

As shown in Fig. 2(c), switches S_{a3} and S_{a4} are in the ON state, and the potential of output terminal a_1 is equal to the potential of point N, and the output voltage is -U_d/2. Phases b and c are the same as phase a.

Mode 2: Inverter 2 is effective. Switches S_{x1} and S_{x2} of each phase and switch S_{o2} are in the ON state, and switch S_{o1} is in the OFF state. At this time, the three phases of inverter 1 are connected to the positive bus (state P), which means that inverter 1 outputs PPP, a zero vector. Each phase has three working states, respectively, P, O, and N, corresponding to output voltage $+U_d$/2, 0, and -U_d/2.

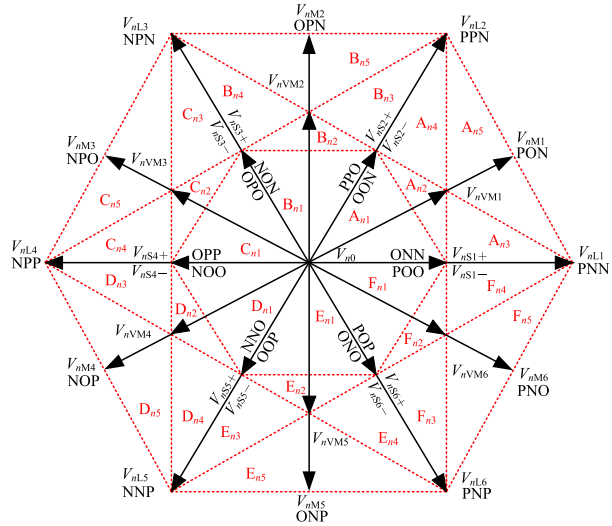

Fig. 3. Virtual space vector diagram of inverter n.

Taking phase a as an example, the working principles of the three working states of phase a are shown in Fig. 2(d)–(f). The working principle of the working states in mode 2 is the same as mode 1. The results of the analysis mentioned above are listed in Table I.

According to this working mode, inverters 1 and 2 need to work alternately in one cycle. When inverter 1 is in the working state, inverter 2 outputs 0; when inverter 2 is in the working state, inverter 1 outputs 0. The total modulation index of the two inverters is 1. With one cycle divided into two, the maximum modulation index of each inverter is 0.5, which is also a disadvantage of this topology.

According to the analysis of the above-mentioned six working states, the voltage stress of switches and clamping diodes can be obtained. Take switch S_{a1} as an example, its voltage stress is 0, U_d/2 or U_d/4, U_d/2, 0, 0, and 0 respectively. The max voltage stress of switch S_{a1} is U_d/2. The analysis of other switches and clamping diodes is the same as S_{a1}. The results are all given in Table II. The topology in [11] is also analyzed for its voltage stress and it is known that one of the switches is required to withstand the voltage of U_d. As for the current stress, switches S_{x2} and S_{x5} bear the greatest current stress. The selection of the integral switching devices should be based on the specific situation and take the one with the greatest current stress as the reference.

III. Strategy of DO-NPC-TLI

A. VSVPWM Strategy

Inverters 1 and 2 work alternately in a switching cycle to obtain two groups of three-phase ac outputs. As given in Table I, each phase of inverter n (all "n" mentioned in the following part are $n\in\{1,2\}$) has three states, P, O, and N. Fig. 3 shows a virtual space vector diagram of inverter n, which is made up of 27 states. The output terminal in each state has different connection modes with the dc side and each connection mode corresponds to a space vector, respectively [23].

TABLE I
RELATIONSHIP BETWEEN THE WORKING STATE AND THE SWITCHING STATE

Mode	Effective inverter	Working state	S_{o1}	S_{o2}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	Output voltage
Mode 1	Inverter 1	P	ON	OFF	ON	ON	OFF	OFF	ON	ON	$+U_d/2$
		O	ON	OFF	OFF	ON	ON	OFF	ON	ON	0
		N	ON	OFF	OFF	OFF	ON	ON	ON	ON	$-U_d/2$
Mode 2	Inverter 2	P	OFF	ON	ON	ON	ON	ON	OFF	OFF	$+U_d/2$
		O	OFF	ON	ON	ON	OFF	ON	ON	OFF	0
		N	OFF	ON	ON	ON	OFF	OFF	ON	ON	$-U_d/2$

TABLE II
VOLTAGE STRESS

Switch	S_{o1}	S_{o2}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}
Voltage stress	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$
Diode	D_{x7}	D_{x8}	D_{x9}	D_{x10}				
Voltage stress	$U_d/2$	$U_d/2$	$U_d/2$	$U_d/2$				

TABLE III
CLASSIFICATION OF SPACE VECTORS

Classification	Voltage vector
Zero vector	V_{n0}
Medium vector	$V_{n\mathrm{M1}}\ V_{n\mathrm{M2}}\ V_{n\mathrm{M3}}\ V_{n\mathrm{M4}}\ V_{n\mathrm{M5}}\ V_{n\mathrm{M6}}$
Large vector	$V_{n\mathrm{L1}}\ V_{n\mathrm{L2}}\ V_{n\mathrm{L3}}\ V_{n\mathrm{L4}}\ V_{n\mathrm{L5}}\ V_{n\mathrm{L6}}$
Positive short vector	$V_{n\mathrm{S1+}}\ V_{n\mathrm{S2+}}\ V_{n\mathrm{S3+}}\ V_{n\mathrm{S4+}}\ V_{n\mathrm{S5+}}\ V_{n\mathrm{S6+}}$
Negative short vector	$V_{n\mathrm{S1-}}\ V_{n\mathrm{S2-}}\ V_{n\mathrm{S3-}}\ V_{n\mathrm{S4-}}\ V_{n\mathrm{S5-}}\ V_{n\mathrm{S6-}}$
Virtual medium vector	$V_{n\mathrm{VM1}}\ V_{n\mathrm{VM2}}\ V_{n\mathrm{VM3}}\ V_{n\mathrm{VM4}}\ V_{n\mathrm{VM5}}\ V_{n\mathrm{VM6}}$

From Fig. 3, the virtual space vector diagram of inverter n is divided into six sections. It is labeled as sections A_n–F_n. Each section is redivided into five subsections, which is labeled as subsections A_{n1}–F_{n5}. The specific classification of space vectors is given in Table III.

As described in [24], zero vectors and large vectors have no effect on the neutral point voltage balance. Therefore, when constructing virtual space vectors, zero vectors and large vectors keep the modulus and direction of original vectors unchanged. Short vectors always appear in pairs and each short vector always appears in pairs as a positive or a negative vector. And the two short vectors are equivalent when the reference voltage vector is synthesized but their effects on the neutral point voltage are opposite, which can offset each other. Therefore, redefined short vectors are reconstructed by using the property of short vectors. New virtual medium vectors are composed of two short vectors and medium vectors. According to (1), new vectors satisfy. According to the content mentioned above and taking vectors in section *Bn* as an example, the following equation can be obtained:

$$\begin{cases} V_{nS2} = (V_{nS2+} + V_{nS2-})/2 \\ V_{nS3} = (V_{nS3+} + V_{nS3-})/2 \\ V_{nVM2} = (V_{nS2+} + V_{nM2} + V_{nS3+})/3 \end{cases}. \tag{1}$$

According to (1), it can be seen that the reconstructed short vectors are composed of a positive short vector and a negative short vector, each account for half. The virtual medium vectors are composed of two short vectors and one medium vector, each accounting for one third.

Assuming that the reference output voltages of inverter n can be described as (2), where U_{mn}, ω_n, and φ_n are the amplitude, angular frequency, and initial phase angle of the output three-phase voltages of inverter n, respectively

$$\begin{bmatrix} u_{a-\mathrm{ref}n} \\ u_{b-\mathrm{ref}n} \\ u_{c-\mathrm{ref}n} \end{bmatrix} = U_{mn} \begin{bmatrix} \cos(\omega_n t + \varphi_n) \\ \cos(\omega_n t + \varphi_n - 2\pi/3) \\ \cos(\omega_n t + \varphi_n + 2\pi/3) \end{bmatrix}. \tag{2}$$

The reference output voltage vector of inverter n can be described as follows:

$$\mathbf{U}_{\mathrm{ref}n} = \frac{2}{3}(u_{a-\mathrm{ref}n} + u_{b-\mathrm{ref}n}e^{j\frac{2\pi}{3}} + u_{c-\mathrm{ref}n}e^{j\frac{4\pi}{3}}) \tag{3}$$

where $U_{\mathrm{ref}n}$ is the reference output voltage vector of inverter n.

The virtual space vector diagrams of sections B_1 and B_2 are given in Fig. 4. The method of selecting basic vectors involved in the synthesis of the reference voltage is still to follow the principle of the nearest three vectors. Three fundamental vectors nearest to the reference voltage are used to synthesize it. Taking subsection B_{n1} as an example. When $U_{\mathrm{ref}n}$ is located in B_{n1}, V_{n0}, V_{nS2}, and V_{nS3} are chosen to synthesize $U_{\mathrm{ref}n}$. By the principle of volt–second balance, the equation is as follows:

$$\begin{cases} U_{\mathrm{ref}n} = V_{nS2}d_{11} + V_{nS3}d_{12} + V_{n0}d_{13} \\ 1 = d_{n1} + d_{n2} + d_{n3} \end{cases}. \tag{4}$$

Duty ratios can be obtained from (4). Table IV lists the equations of duty ratios in section B_n. d_{n1}, d_{n2}, and d_{n3} are the duty ratios corresponding to three effective vectors in each subsections of the inverter n.

After the duty ratios calculation, the switching sequences and dwell time of each vector need to be listed. The switching sequences of VSVPWM is not unique. Moreover, when the mode changes (Mode 1 to 2 or Mode 2 to1), the problem of voltage jump and the following CBPWM need to be considered. After analyzing further, the optimized switching sequences are shown in Fig. 5 (circled by the green dotted box), which shows the detail of two inverters working alternately in one switching cycle. The

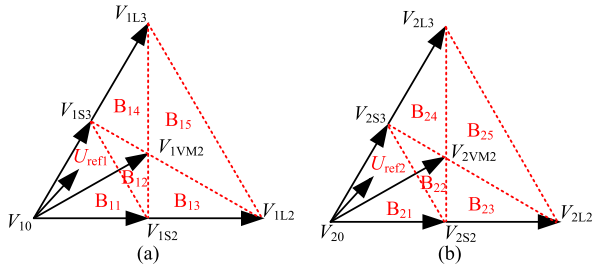

Fig. 4. Virtual space vector diagrams of sections B_1 and B_2. (a) Section B_1 of inverter 1. (b) Section B_2 of inverter 2.

TABLE IV
DUTY RATIOS OF SECTION B_n

Bn	d_{n1}	d_{n2}	d_{n3}
B_{n1}	$2\sqrt{3}U_{refn}\sin(\theta_n+\pi/3)/U_d$	$2\sqrt{3}U_{refn}\sin(\theta_n-\pi/3)/U_d$	$1-2\sqrt{3}U_{refn}\sin\theta_n/U_d$
B_{n2}	$6U_{refn}\sin(\pi/6-\theta_n)/U_d-2$	$2-6U_{refn}\sin(\pi/6+\theta_n)/U_d$	$6\sqrt{3}U_{refn}\sin\theta_n/U_d-3$
B_{n3}	$6U_{refn}\sin(\pi/6-\theta_n)/U_d+2$	$3\sqrt{3}U_{refn}\sin(\theta_n-\pi/3)/U_d$	$3U_{refn}\sin(\pi/6+\theta_n)/U_d-1$
B_{n4}	$3\sqrt{3}U_{refn}\sin(\theta_n+\pi/3)/U_d$	$2-6U_{refn}\sin(\pi/6+\theta_n)/U_d$	$3U_{refn}\sin(\theta_n-\pi/6)/U_d-1$
B_{n5}	$3U_{refn}\sin(\pi/6+\theta_n)/U_d-1$	$3U_{refn}\sin(\theta_n-\pi/6)/U_d-1$	$3-3\sqrt{3}U_{refn}\sin\theta_n/U_d$

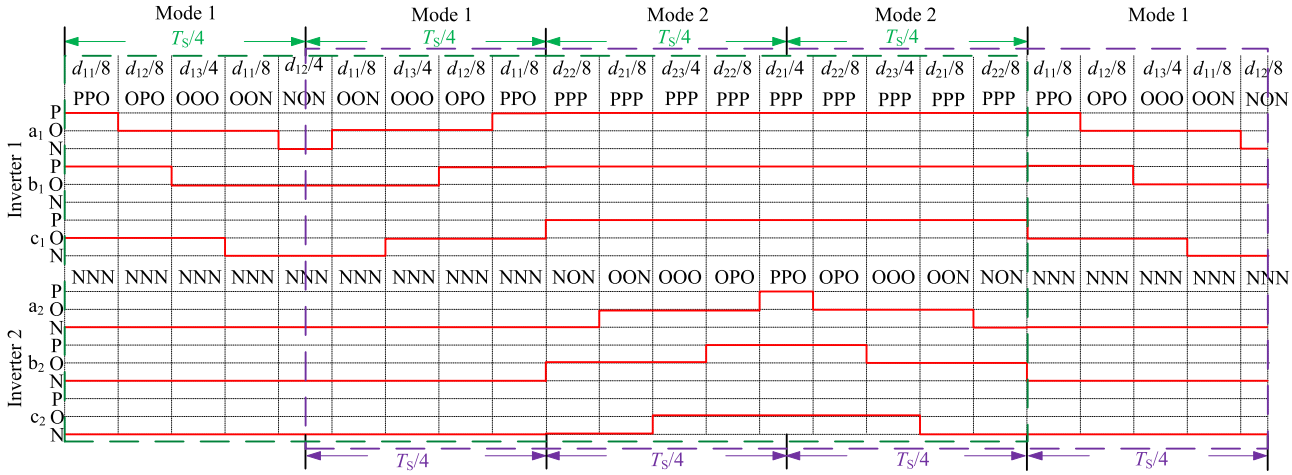

Fig. 5. Switching sequences and dwell time in a switching cycle.

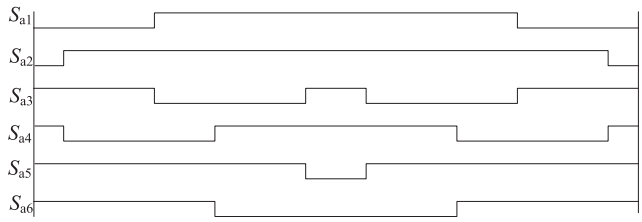

Fig. 6. Driving signal of switches of phase *a* in the switching cycle.

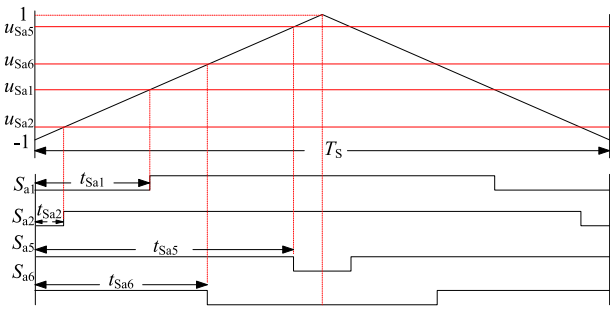

Fig. 7. Driving signals and modulation waves of each switch of phase *a*.

content mentioned above is all of the process of VSVPWM for DO-NPC-TLI.

B. CBPWM Strategy

The VSVPWM modulation strategy needs to identify which sections and subsections the reference voltage is located in and needs to list the switching sequences and dwell time of each subsection. There are a lot of trigonometric functions in the calculation process of duty ratios and the equation derivation is too complex. Therefore, a CBPWM based on VSVPWM is proposed.

As CBPWM requires the symmetrical arrangement of switching sequences, move the switching sequences of the first one-fourth cycle of Fig. 5 to the end of the entire cycle so the switching sequences for CBPWM can be obtained (as circled by the purple dotted box in Fig. 5). In the former half cycle, inverter 1 works for the one-fourth cycle first, followed by inverter 2 for the one-fourth cycle. According to the principle of symmetry, in the later half period, inverter 2 works first, and then inverter 1

TABLE V
SUMMARY OF EQUATIONS

	OOOPP	NOOOP	NNOOO
u_{Sx1}	$(u_{min1}-u_{max1})/U_d$	$(u_{min1}-u_{mid1})/U_d$	0
u_{Sx2}	1	$(u_{max1}-u_{mid1})/U_d-1$	$(u_{max1}-u_{min1})/U_d-1$
u_{Sx5}	$(u_{min2}-u_{max2})/U_d$	$(u_{min2}-u_{mid2})/U_d$	1
u_{Sx6}	0	$(u_{max2}-u_{mid2})/U_d$	$(u_{max2}-u_{min2})/U_d-1$

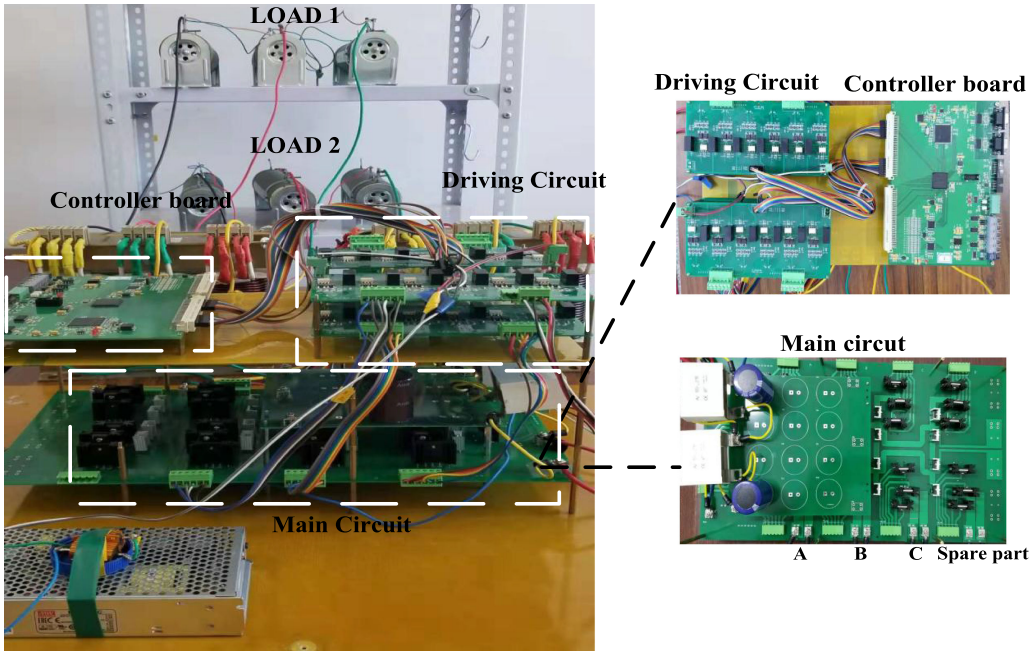

Fig. 8. Photograph of the experimental prototype.

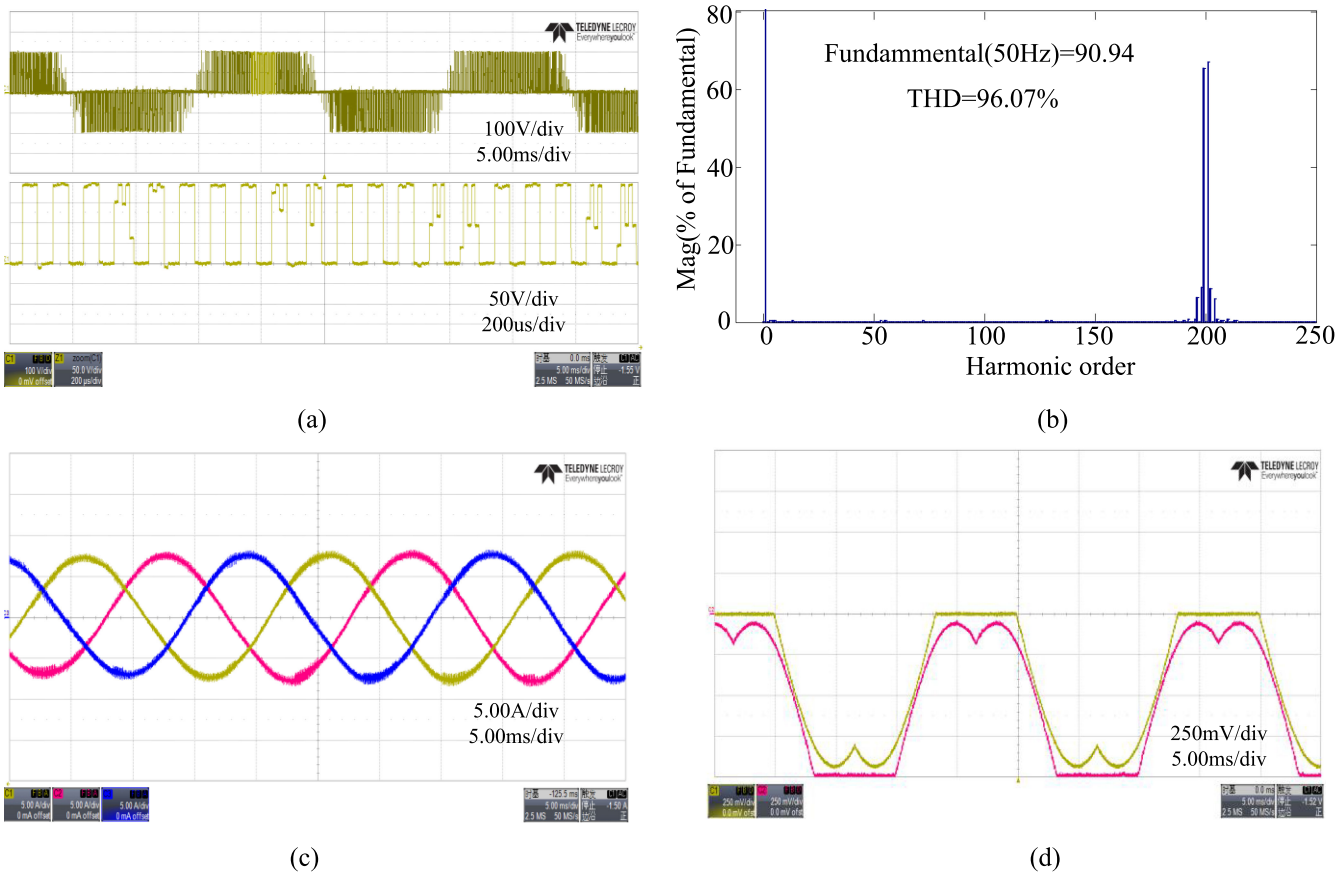

Fig. 9. Experimental waveforms of inverter 1. (a) Output line-to-line u_{ab1} and zoom of u_{ab1}. (b) FFT of u_{ab1}. (c) Output three-phase current i_{abc1}. (d) Modulation waveforms of S_{a1} and S_{a2}.

TABLE VI
EXPERIMENTAL PARAMETERS

Symbol	Description	Value
U_{d}	DC voltage	200 V
C_{U} / C_{L}	upper / lower capacitor	470 μF
f_1	output voltage frequency 1	50 Hz
f_2	output voltage frequency 2	60 Hz
U_{ref1}	output reference voltage 1	55 V
U_{ref2}	output reference voltage 2	55 V
R_n	Load n resistances	6 Ω
L_n	Load n inductances	10 mH
f_{s}	switching frequency	10 kHz

TABLE VII
PARAMETERS OF PMSM AND DC GENERATOR

PMSM	Value	DC generator	Value
Rated power	0.55 Kw	Rated power	0.6 Kw
Rated voltage	220 V	Rated voltage	220 V
Rated current	1 A	Rated current	3.8 A
Rated speed	1500 r/min	Rated speed	1500 r/min
Rated frequency	50 Hz	Excitation current	0.28 A
Pole	2	Excitation voltage	220 V

works. Then according to switching states in Table I, the driving signals of six switches of phase a can be obtained, which are shown in Fig. 6. Analyzing further, driving signals S_{a3} and S_{a4} can be obtained by the logical operations of S_{a1}, S_{a2}, S_{a5}, and S_{a6}. According to Fig. 6, the following equation can be obtained:

$$\begin{aligned} S_{a3} &= \overline{S_{a1}} \cdot S_{a5} + S_{a1} \cdot \overline{S_{a5}} \\ S_{a4} &= \overline{S_{a2}} \cdot S_{a6} + S_{a2} \cdot \overline{S_{a6}}. \end{aligned} \tag{5}$$

Therefore, it is only necessary to calculate the modulation waves of switches S_{a1}, S_{a2}, S_{a5}, and S_{a6}.

Fig. 7 shows a detailed illustration of CBPWM. In Fig. 7, the carrier wave is an isosceles triangular wave. Its period is the same as the modulation cycle and the amplitude varies from -1 to 1. It can be derived as

$$u_{\mathrm{tri}} = \begin{cases} \frac{4}{T_S}t - 1, 0 \le t \le \frac{T_S}{2} \\ -\frac{4}{T_S}t + 3, \frac{T_S}{2} \le t \le T_S \end{cases}. \tag{6}$$

During the half switching cycle, at the change time of switching state, a vertical line is drawn and intersects the carrier at a point. A parallel line is drawn at this point, which corresponds to the modulated wave of each switch.

According to the content mentioned above and Fig. 7, the equations of time interval t_{Sa1}, t_{Sa2}, t_{Sa5}, and t_{Sa6} are as follows:

$$\begin{cases} t_{Sa1} = \left(\frac{d_{12}}{8} + \frac{d_{11}}{8} + \frac{d_{13}}{4} + \frac{d_{12}}{8}\right) \cdot T_S \\ t_{Sa2} = \frac{d_{12}}{8} \cdot T_S \\ t_{Sa5} = \frac{T_S}{4} + \left(\frac{d_{22}}{8} + \frac{d_{21}}{8} + \frac{d_{23}}{4} + \frac{d_{22}}{8}\right) \cdot T_S \\ t_{Sa6} = \frac{T_S}{4} + \frac{d_{22}}{8} \cdot T_S \end{cases}. \tag{7}$$

By substituting (7) into (6), modulation waves u_{Sa1}, u_{Sa2}, u_{Sa5}, and u_{Sa6} can be obtained

$$\begin{cases} u_{Sa1} = \frac{(u_{\min 1} - u_{\mathrm{mid}1})}{U_d} \\ u_{Sa2} = \frac{(u_{\max 1} - u_{\mathrm{mid}1})}{U_d} - 1 \\ u_{Sa5} = \frac{(u_{\min 2} - u_{\mathrm{mid}2})}{U_d} \\ u_{Sa6} = \frac{(u_{\max 2} - u_{\mathrm{mid}2})}{U_d} \end{cases}. \tag{8}$$

The same principle can be obtained for phase b and c. The derivation process of other subsections is the same as the content mentioned above. It can be concluded that all subsections of the section can obtain the same expressions of modulation waves. So only the modulation waves in subsection X_{n1} ($X \in \{\mathrm{A}–\mathrm{F}\}$) needed to be calculated.

Analyzing further, each phase of inverter n has only three kinds of switching sequences in a switching cycle. The specific switching sequences are listed in the first row of Table V. Because the CBPWM is symmetric, only half-cycle switching sequences are given. From the half cycle in Fig. 5, the effective working states of inverters 1 and 2 are the same in each one-fourth cycle. So the switching sequences are represented by only five states. According to the equation derivation, no matter which phase of a, b, and c, as long as corresponding to three switching sequences, the expressions of modulation waves are all the same. Table V gives the summary of equations. For example, in the above-mentioned analysis, the switching states of phase a are shown in Fig. 6. Based on Fig. 5, the switching sequences are *NOOOP* in the one-fourth cycle. The expressions of modulation waves [see (8)] can correspond to the equations given in Table V.

In (8) and Table V

$$\begin{aligned} u_{\max n} &= \max(u_{a-\mathrm{ref}n}, u_{b-\mathrm{ref}n}, u_{c-\mathrm{ref}n}) \\ u_{\mathrm{mid}n} &= \mathrm{mid}(u_{a-refn}, u_{b-\mathrm{ref}n}, u_{c-\mathrm{ref}n}) \\ u_{\min n} &= \min(u_{a-\mathrm{ref}n}, u_{b-\mathrm{ref}n}, u_{c-\mathrm{ref}n}). \end{aligned} \tag{9}$$

According to the content mentioned above, the carrier modulation does simplify VSVPWM to a large extent.

IV. EXPERIMENTAL RESULTS

To validate the proposed topology DO-NPC-TLI and its modulation strategy, the experimental platform is setup in the

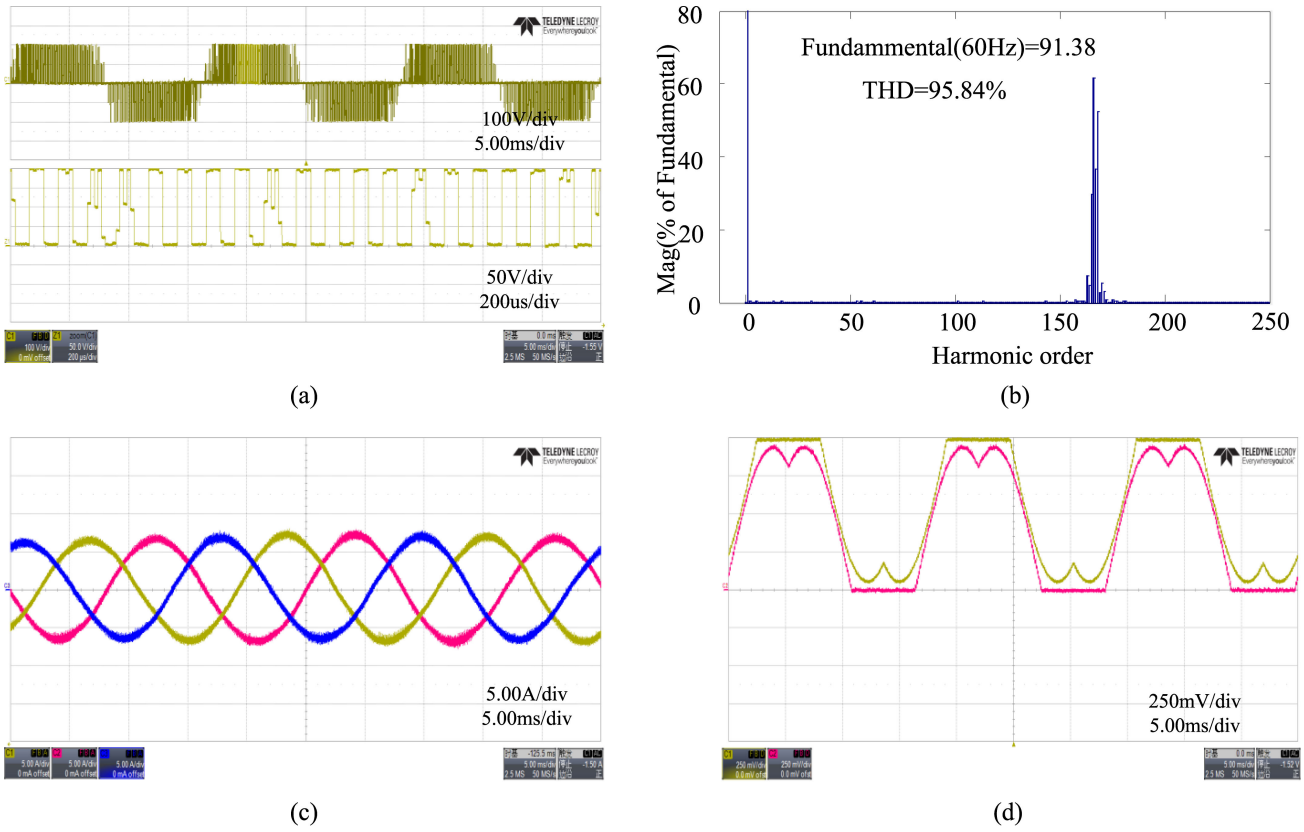

Fig. 10. Experimental waveforms of inverter 2. (a) Output line-to-line u_{ab2} and zoom of u_{ab2}. (b) FFT of u_{ab2}. (c) Output three-phase current i_{abc2}. (d) Modulation waveforms of S_{a5} and S_{a6}.

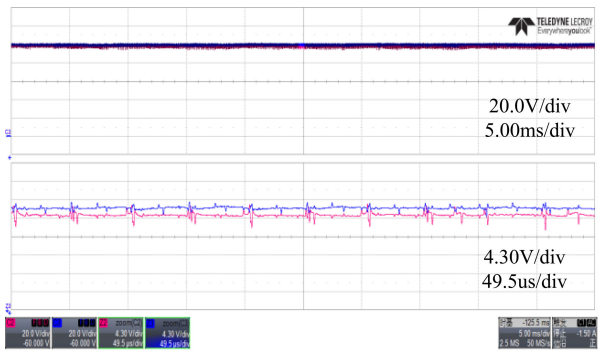

Fig. 11. Waveforms of the neutral point voltage.

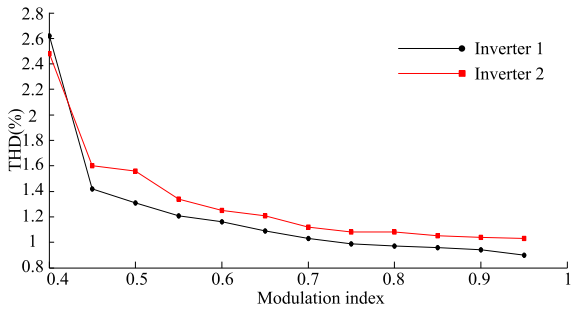

Fig. 13. THD of inverter n (THD is calculated to the tenth harmonic).

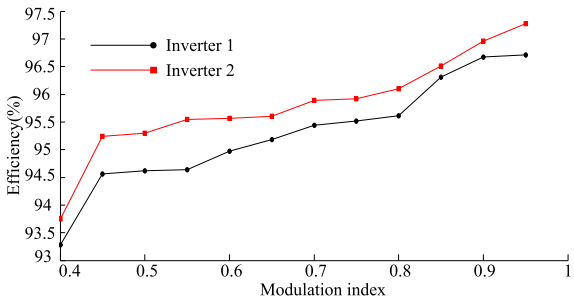

Fig. 12. Conversion efficiency of the inverter.

laboratory, as shown in Fig. 8. The prototype consists of a controller board, main circuit, driver circuit, and two groups of three-phase loads. The controller board that executes the control program includes a high-performance DSP TMS320F28335 and a field-programmable gate array EP4CE115F23I7N. The frequency of the triangular carrier signal is set as 10 kHz. The experimental parameters are given in Table VI. The type of power MOSFET is AUIRFSL6535. The type of clamping diode is IDP15E60.

The experimental results of inverter 1 are shown in Fig. 9. The amplitude of reference voltage is 55 V and the frequency is 50 Hz. Fig. 9(a) shows the waveforms of the output line-to-line

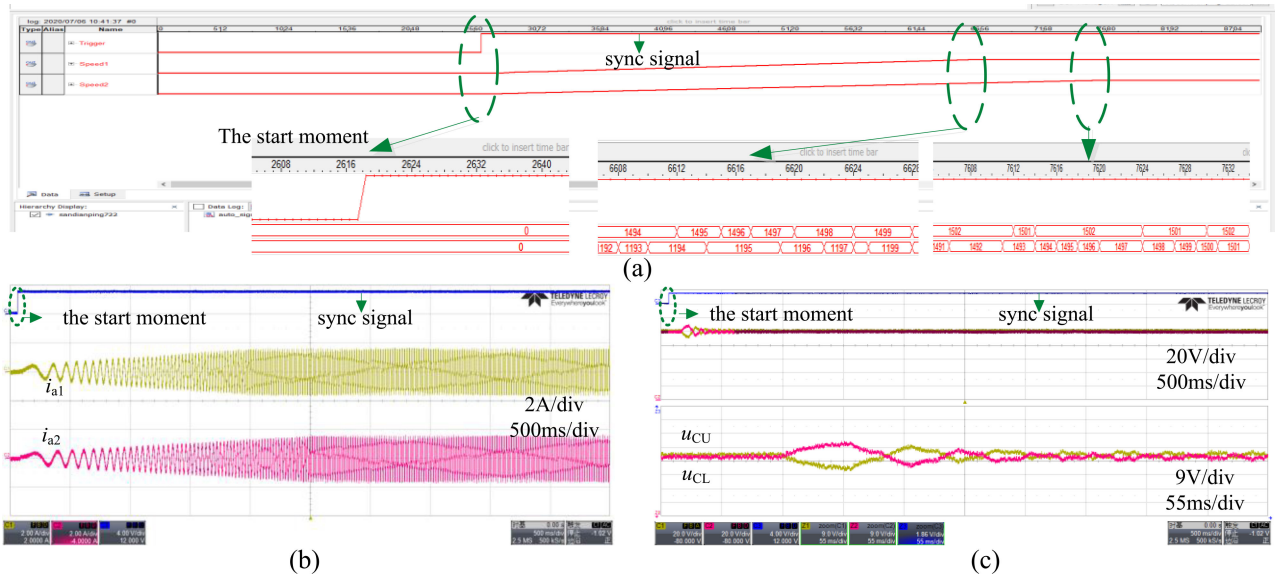

Fig. 14. Experimental waveforms of case 1. (a) Speed of motors 1 and 2. (b) Stator currents of i_{a1} and i_{a2}. (c) Neutral point voltage.

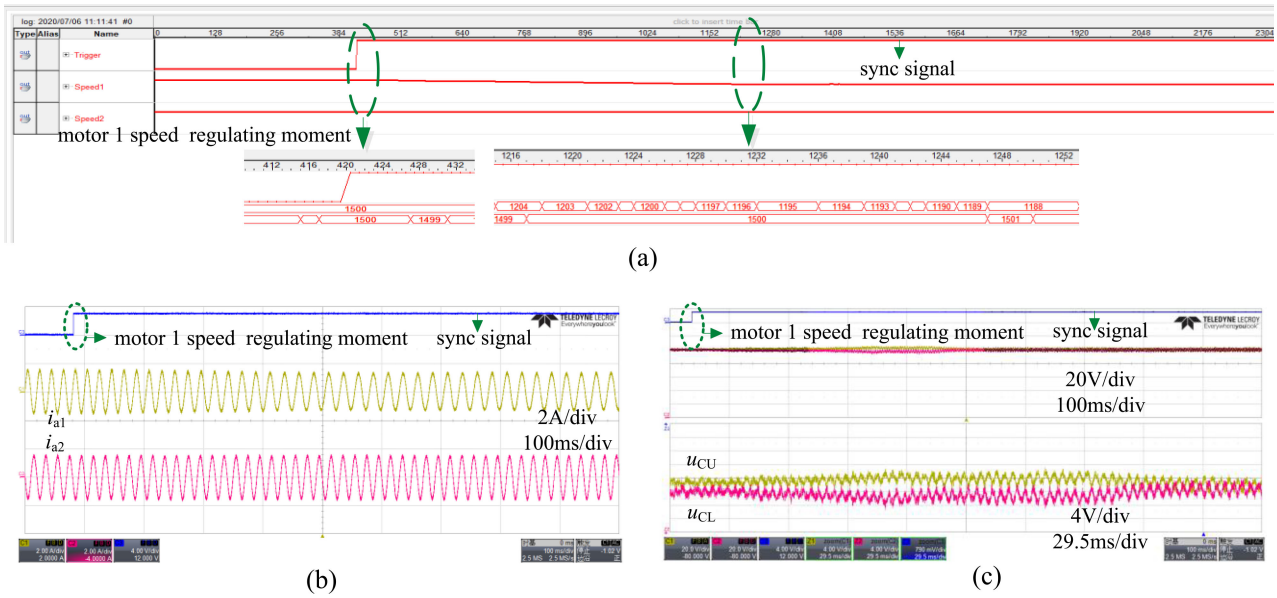

Fig. 15. Experimental waveforms of case 2. (a) Speed of motors 1 and 2. (b) Stator currents of i_{a1} and i_{a2}. (c) Neutral point voltage.

voltage u_{ab1} and the zoom of u_{ab1}. It can be seen that the line-to-line voltage waveform is the pulse wave, the maximum instantaneous value is 200 V, which is equal to the value of the dc voltage, and there are three voltage values of 0, 100, and 200 V. The fast Fourier transform (FFT) analysis of u_{ab1} is shown in Fig. 9(b), the value of the fundamental wave is about 90.94 V, and the theoretical value of line voltage u_{ab1} is 95.26 V. The output voltage amplitude is consistent with the desired value, and the harmonics are mainly distributed near the switching frequency and its multiples, there is no low-order harmonics. Fig. 9(c) is the three-phase load output phase currents of inverter 1, the frequency is 50 Hz, and the waveforms are three-phase symmetrical sinusoidal waveforms, which indirectly prove that the output voltage does not contain low-order harmonics. The theoretical value of the three-phase current is 8.12 A, the current value obtained by the experiment is about 8 A, and the actual value is close to the expected value. Fig. 9(d) shows the modulation waveforms of S_{a1} and S_{a2}. The value of the modulation wave is only related to the three-phase reference voltage of inverter 1. The changes of inverter 2 have no effect on the modulation waveforms of S_{a1} and S_{a2}. And the modulation waves are not the conventional sine wave, which changes in periodically. The cycle is the same as inverter 1.

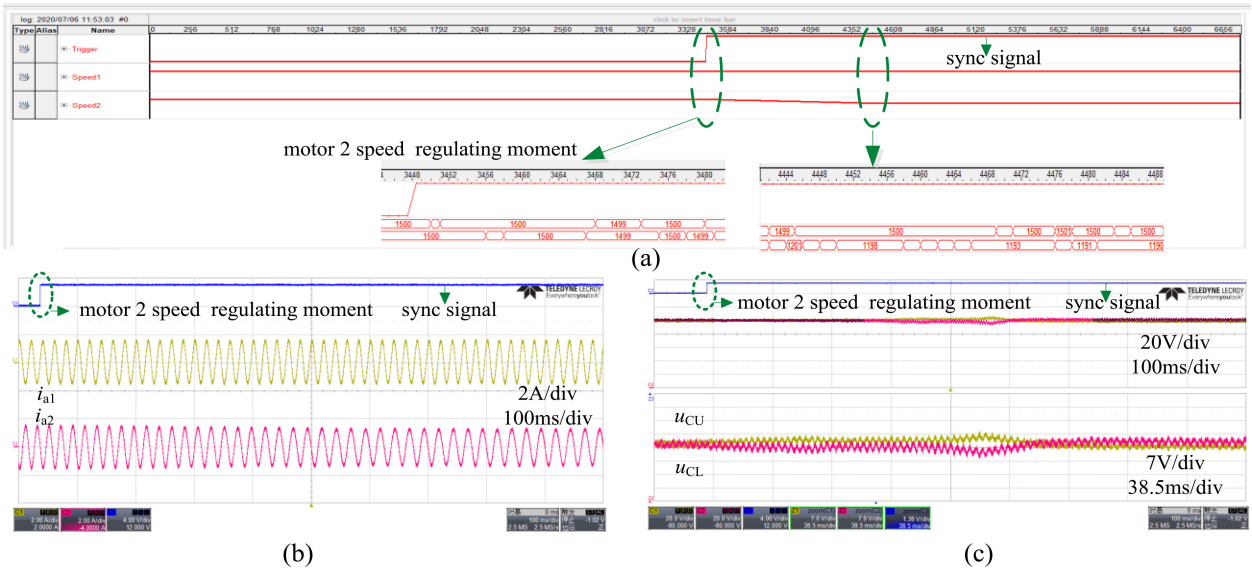

Fig. 16. Experimental waveforms of case 3. (a) Speed of motors 1 and 2. (b) Stator currents of i_{a1} and i_{a2}. (c) Neutral point voltage.

The experimental results of inverter 2 are shown in Fig. 10. The amplitude of the reference voltage is 55 V and the frequency is 60 Hz. The line voltage u_{ab1} has no low-order harmonics, the three-phase load output phase currents of inverter 2 are symmetrical sinusoidal waveforms, and the frequency is 60 Hz. The values of the line-to-line voltage and currents are close to the expected value, respectively.

Fig. 11 shows the waveform of the neutral point voltage on the dc side of the circuit. The upper waveform is the voltage values of two capacitors in the dc side and the lower waveform is the zoom of the upper waveform. The neutral point voltage basically keeps balanced and the dc voltage is 200 V. Each capacitor is continuously charged and discharged and is stable at about 100 V.

The waveform under one modulation index is selected in the experiment but Figs. 12 and 13 show the conversion efficiency and the total hormonic distortion (THD) of the inverter with different modulation indexes. From Fig. 12, with the increase of the modulation index, the influence of the loss of the tube voltage drop on the output voltage decreases, so the conversion efficiency increases. And in Fig. 13, when the modulation index is less than 0.5, it is equivalent to two effective vectors to synthesize the output voltage, which is equivalent to a two-level inverter. When the modulation index is greater than 0.5, it is a three-level inverter. As the number of levels increases, the THD of the output voltage decreases. And the overall THD of the output voltage is low.

In order to verify the working condition of DO-NPC-TLI when the load changes, two groups of motor loads are driven. Each motor load is that a permanent magnet synchronous motor (PMSM) drives a dc generator. Two groups of motors are, respectively, called motor 1 and motor 2. The parameters of PMSM and dc generator are given in Table VII. Experiments are divided into three cases. Case 1 is the soft-start process of two groups of motors. Case 2 is that after a stable operation of two groups of motors, the speed of motor 1 is regulated, while that of motor 2 is maintained. Case 3 is that the speed of motor 2 is regulated, while that of motor 1 is maintained. And in order to display experimental results synchronously, the waveform at the top of each figure is a synchronous signal.

Under the constant *V/f* control, the soft-start time of motors 1 and 2 is set to 2 s and 2.5 s, respectively. The experimental results of case 1 are shown in Fig. 14. Fig. 14(a) shows the speed of two motors with the tool "SingalTap II Logic Analyzer" in Quartus II (sample time 0.5 ms). The speed of two motors rises smoothly after starting. Motors 1 and 2 reach the synchronous speed at about 2 s and 2.5 s, respectively. The speed fluctuates slightly due to the open-loop control. Fig. 14(b) shows the stator currents of i_{a1} and i_{a2}, which reach the rated value slowly within the respective setting time. Fig. 14(c) shows the neutral point voltage on the dc side. Each capacitor voltage fluctuates about 9 V during the soft-start process. After two motors operate stably, two capacitor voltages return to the equilibrium state.

The experimental results of case 2 are shown in Fig. 15. The speed of two motors, stator currents of i_{a1} and i_{a2}, and the neutral point voltage on the dc side are shown in Fig. 15(a)–(c). Two motors operate stably before the speed regulating of motor 1 is triggered. Then the instruction frequency of motor 1 is changed from 50 to 40 Hz within 0.4 s. The speed of motor 1 and stator current i_{a1} change smoothly and each capacitor voltage fluctuates about 5 V. After about 0.4 s, the speed of motor 1 changes to about 1200 r/min. The frequency of i_{a1} changes to 40 Hz and its amplitude decreases accordingly. Two capacitor voltages return to the equilibrium state, while the speed of motor 2 remains at a stable synchronous speed during the speed regulating.

The experimental results of case 3 are shown in Fig. 16. Then the instruction frequency of motor 2 is changed from 50 to 40 Hz within 0.5 s. The speed regulating process is similar to case 2.

V. Conclusion

In this article, a new topology DO-NPC-TLI is proposed, which can realize two groups of three-phase ac outputs through two common switches of each phase. A VSVPWM modulation strategy with a time-sharing modulation ideal is proposed for the new topology, which solves the problem of the neutral point voltage balance and realizes the modulation of the circuit. In order to simplify VSVPWM, a CBPWM by VSVPWM is proposed. CBPWM does not have the calculation of trigonometric functions and does not need the judgment of subsections. The calculation process is simple. The modulation strategy is verified by the experiment. The correctness of the experimental results shows the feasibility of the circuit and the effectiveness of the modulation strategy.

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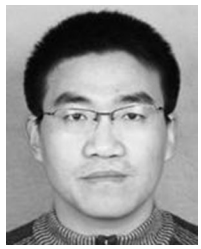

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