A Novel Bond Wire Fault Detection Method for IGBT Modules Based on Turn-on Gate Voltage Overshoot

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***Abstract*—Bond wire degradation is one of the most common failure modes for wire-welded packaging insulated-gate bipolar transistor (IGBT) modules. This article proposes a novel bond wire detection method based on IGBT turn-ON gate voltage overshoot. The degree of bond wires lift-off will change the stray inductance of the gate charge loop circuit, and therefore has a strong influence on turn-ON gate voltage overshoot before miller platform, which can be used as an effective bond wire fault indicator. A double pulse test platform is built to verify the resolution and sensitivity of the proposed precursor for bond wire degradation. The dependences on bus voltages, load currents, junction temperatures are discussed and tested. The experimental results show that the gate turn-ON voltage overshoot of IGBT increases with the increasing severity of bond wire faults, which agrees with the theoretical analysis. The proposed turn-ON gate voltage overshoot-based method has a high sensitivity for identifying bond wire fault at the incipient stage. It offers an effective technique for detecting bond wire degradation for practical applications.**

***Index Terms*—Condition monitoring (CM), failure mechanism, fault detection, insulated gate bipolar transistor (IGBT), power semiconductor devices, prognosis, reliability.**

I. Introduction

POWER electronic converters are widely used in industry [1]. Power semiconductor devices are not only the key components of the power electronic converter but also one of the most fragile parts of the converter [2]. The failure rate of power electronic devices among all converter failure types is 31% [2], which is the highest of all failure types. Insulated-gate bipolar transistor (IGBT) is one of the most widely used power electronic devices and key components of converters [3]. IGBT accounts for the largest proportion of all power electronic devices [2]. The reliability monitoring of IGBT modules in operation is of great significance for avoiding catastrophic failures of most power electronic converters. IGBTs typically operate in high-speed switching mode, and they suffer from frequent fluctuations of thermal [4] and electromagnetic stresses, which lead to fatigue and the aging of IGBT modules [5], [6]. The degradation of bond wires is one of the most prominent fault types in wire welding packaging IGBT modules [7].

The detection of IGBT bond wires has been attracting great research interest. Many bond wires monitoring methods have been proposed in the literature. These methods can be classified into three classes according to the type of signals used, namely voltage-based methods, current-based methods, and other signal-based methods.

The first class is the voltage-based methods. The voltage signal is usually easy to measure. Bond wire fault detecting methods based on voltage drop have also been proposed [8]–[12]. However, the method based on the voltage drop has little sensitivity when the bond wire faults are minor. The resolution is too low to identify when the load is light. Further, Singh *et al.* [10] proposed a bond wire degradation monitoring method based on the inflection point voltage, which can rule out the influence of IGBT junction temperature variations. However, the measurement is required at a fixed current, which is difficult to be practical *in situ* monitoring technique because the IGBT current frequently varies with the load condition in practical applications. Kexin *et al.* [13] investigates two aspects of IGBT characteristics, the gate–emitter voltage during turn-ON process and collector-emitter voltage during the turn-OFF process. But, it did not consider the influence of bus voltage, IGBT current, and IGBT temperature variations. Lehmann *et al.* [14] proposed an online bond wire detection method by adding sensing wires and resistors in the packaging and monitoring its voltage. However, it needs to modify the internal wire layout of the IGBT module, which is unpractical and too complicated.

The second class is the current-based methods. It has been proposed that short-circuit current is sensitive to bond wires failures [15], [16]. However, this method requires the gate-drive voltage to vary, which adds complexity to the drive circuit in applications, and regular short-circuit monitoring would disrupt the normal operation of converters. Approaches based on the gate signal of IGBT have drawn great attention because the gate signal can be easily measured on-line. The dynamic differences of gate turn-ON and turn-OFF current with bond wire failures have been studied in [17]. However, the experiments present in [17] indicate that the bond wire lift-off has little influence on the gate turn-ON and turn-OFF currents.

The third class is other signal-based methods, including time, resistance, transfer characteristic, etc. Gate Miller platform duration can also be used to evaluate the aging of IGBT bond wires

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[18], but it still has a disadvantage of low sensitivity with minor bond wire faults. A recursive least squares algorithm is used to estimate the collector-emitter resistance RCE and monitor the condition of bond wires [19]. The results presented in [19] indicates that there is nearly no difference between a healthy condition and one bond wire lift-off condition. Therefore, this method also cannot detect minor bond wire faults. Transfer characteristic is also studied in [20], which is independent of temperature variations via the cross points with saturation current under various gate voltages. However, the method is invasive and needs to interrupt the normal operation.

In this article, a novel method based on turn-ON gate voltage overshoot before Miller platform is proposed to detect IGBT bond wire failures. It is noninvasive and does not require modification to the driver control. It is shown in experimental results that even a slight bond wire cracking fault can be detected with high resolution. It is effective for bond wire fault detection for IGBT modules at the incipient stage. This method has great potential for state monitoring of IGBT modules in practical applications.

The rest of the article is organized as follows. In Section II, the internal structure of IGBT is presented. The gate voltage overshoot $V_{\mathrm{g\_p}}$ is analyzed in detail. The calculation of stray emitter inductance is discussed to explain the effect of bond wire fault. In Section III, the experiment setup and results are presented, and the validity of the proposed method is verified at various operation conditions. The benchmark values of $V_{\mathrm{g\_p}}$ with fault-free IGBT are calibrated for practical considerations. Two existing methods are also tested for comparison. Moreover, the practical implementation for gate voltage overshoot V_{g_p} measuring is discussed. Finally, Section IV summarizes the conclusion extracted from theoretical analysis and experimental validation.

II. Turn-on Gate Voltage Overshoot as Precursor

A. Bond Wire Stray Parameters

Middle-power and high-power IGBT modules are generally based on wire-welded packaging, which using some high-purity aluminum bond wires for internal connection. The considered IGBT modules are encapsulated by chips, copper substrates, heat dissipation base plates, lead terminals, glue, shell, etc. For Infineon FF300R12ME4 considered, for instance, this module includes three IGBT chips and three freewheeling diode (FWD) chips. The internal structure of FF300R12ME4 and the serial number marked of each bond wire are shown in Fig. 1.

The fluctuation of temperature causes different materials to face different levels of thermal stress. Long-term stress accumulation can lead to fatigue and degradation of bond wires, which may then lead to the failure of IGBT modules. The emitters of IGBT models have the largest current density and current fluctuation, which makes the bond wires of emitter more fragile than other components. For FF300R12ME4 considered, its emitter has six aluminum bond wires. The stray inductance and resistance of those bond wires exist in the gate charge loop circuit. Fig. 2 shows a distributed parameter diagram of the gate loop circuit, which includes the internal bond wires.

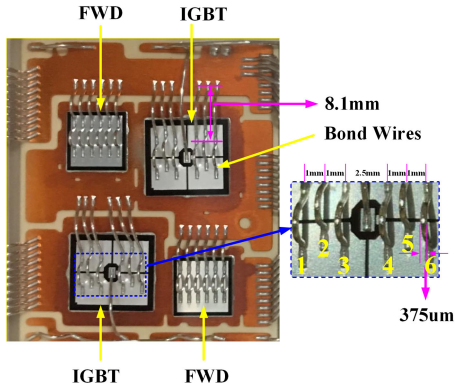

Fig. 1. Internal structure of IGBT and the serial number marked of each bond wire.

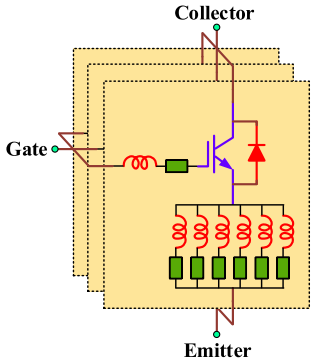

Fig. 2. Distributed parameters of IGBT considering the emitter bond wires.

According to Gu [21], the partial inductance of bond wire consists of partial self-inductance and mutual-inductance. The parasitic self-inductance L_{s} of one aluminum bond wire can be determined by

$$L_{\mathrm{s}} = 2 \cdot 10^{-1} \cdot l \cdot [\ln(4 \cdot 10^{3} \cdot \frac{l}{d}) - 0.75] \tag{1}$$

where l stands for the length of the bond wire (in millimeters) and d stands for the diameter of the bond wire (in nanometers).

The parasitic mutual-inductance M of one aluminum bond wire can be determined by

$$M = 0.19685 \cdot d \left[\ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{l} - \left(\frac{s}{2l}\right)^{2} \right]. \tag{2}$$

where s stands for the distance between two bond wire centers (in millimeters).

For multiple bond wires, the mutual-inductance is caused by the magnetic coupling of multiple bond wires. For the internal structure of FF300R12ME4 shown in Fig. 1, the bond wires have a length of 8.1 mm and a diameter of 375 μm. Each chip has 6 bond wires connected with the copper busbar. Therefore, the parasitic inductance L_{i} of bond wire i is the addition of self-inductance L_{s_i} of bond wire i and mutual-inductances M_{ij}

TABLE I
PARASITIC INDUCTANCE L_i (IN NANOHENRY) OF BOND WIRE i FOR FAULT-FREE IGBT MODULE

No. of the bond wire	1	2	3	4	5	6	The parasitic inductance L_i
1	6.10	3.04	2.11	1.21	1.03	0.88	14.37
2	3.04	6.10	3.04	1.46	1.21	1.03	15.87
3	2.11	3.04	6.10	1.84	1.46	1.21	15.76
4	1.21	1.46	1.84	6.10	3.04	2.11	15.76
5	1.03	1.21	1.46	3.04	6.10	3.04	15.87
6	0.88	1.03	1.21	2.11	3.04	6.10	14.37

between bond wire i and bond wire j

$$L_{\mathrm{i}} = L_{\mathrm{s\_i}} + \sum_{j=1}^{j=6} M_{\mathrm{ij}} (j \neq i). \tag{3}$$

The self-inductance L_{s_i} of bond wire i and mutual-inductances M_{ij} between bond wire i and bond wire j can be calculated according to (1) and (2). Hence, the parasitic inductance L_i (in nanohenry) of bond wire i is calculated and given in Table I.

The total stray inductance of one chip is 2.55 nH, which is the result of a parallel connection of six inductances. For multichip IGBT module, the stray emitter inductance is determined by parallel connection of parasitic inductances of multiple chips.

The parasitic resistance $R_{\mathrm{p\_A}}$ of one aluminum bond wire can be determined by

$$R_{\mathrm{P\_A}} = 2.83 \cdot 10^{-8} \cdot \frac{4l}{\pi d^2}. \tag{4}$$

where l stands for the length of the bond wire and d stands for the diameter of the bond wire.

For the emitter bond wires of IGBT, the paralleled chips have a symmetrical structure. Therefore, the equivalent resistance R_{e} of the internal emitter of IGBTs can be determined by

$$R_{\mathrm{e}} = \frac{R_{\mathrm{p\_A}}}{3 \cdot n}. \tag{5}$$

where n represents the number of effective bond wires.

B. Gate Voltage Overshoot V_{g_p}

The gate driver voltage v_g, gate driver current i_g, collector voltage v_{ce} and collector current i_{c} waveforms of IGBT during a turn-ON transient are shown in Fig. 3.

In Fig. 3, V_{bus} is the dc bus voltage. I_L is the stable load current, which flows through the collector of IGBT after the turn-ON process. When the gate voltage increases to gate threshold voltage V_{g_th} at t_1, the IGBT collector current i_{c} begins to increase. In the period of $(t_1 - t_2)$, i_{c} increases to I_L with a high current change rate $\frac{di_{\mathrm{c}}}{dt}$. In the period of $(t_2 - t_3)$, FWD of another arm has a reverse recovery process, so i_{c} continues to increase rapidly.

Theoretically speaking, the gate voltage overshoot V_{g_p} depends on the parasitic inductance and resistance of drive loop parameters. Considering the fault-free FF300R12ME4, the equivalent gate driver loop circuit is shown in Fig. 4.

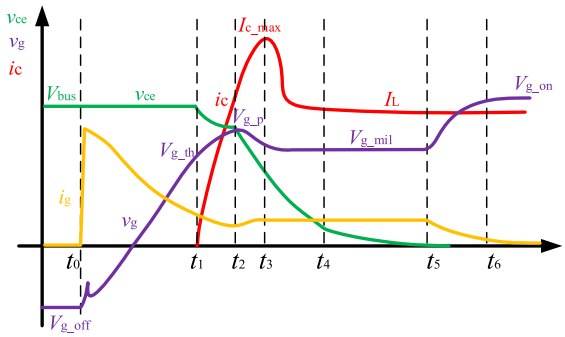

Fig. 3. Waveforms of IGBT turn-ON transient.

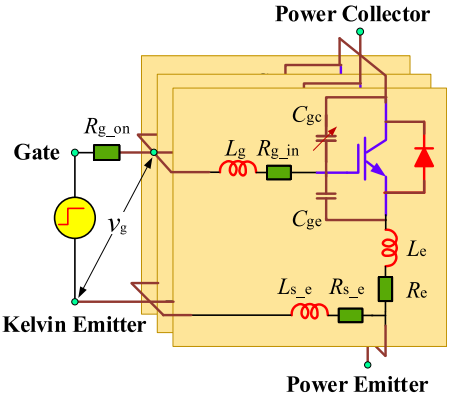

Fig. 4. Equivalent gate driver loop circuit of IGBT.

During the period of $(t_1 - t_3)$, the current change rate $\frac{di_{\mathrm{c}}}{dt}$ would reach to more than 1000 A/us [22], [23], and it induces an induced voltage across the parasitic inductance L_{e} of IGBT emitter bond wires. Besides, there is a voltage drop when i_{c} flows across the resistance R_{e} of emitter bond wires. Similarly, the gate current change rate $\frac{di_{\mathrm{g}}}{dt}$ would produce induced voltage because of the parasitic inductance of the IGBT gate loop. The gate current i_g would produce voltage drop because of the parasitic resistance of the IGBT gate loop. With the marks in Fig. 4, V_{g_p} is determined by

$$\begin{aligned} V_{g\_p} = {} & V_{g\_\mathrm{th}} + i_g \left(R_{g\_\mathrm{in}} + R_e + R_{s\_e}\right) \\ & + i_c R_e + \left(L_g + L_{\mathrm{e}} + L_{s\_e}\right) \frac{di_g}{dt} + L_e \frac{di_c}{dt} \end{aligned} \tag{6}$$

where V_{g_th} is the IGBT turn-ON threshold voltage, which is the gate voltage bias starting to induce an inversion layer creating a channel between collector and emitter of IGBT so the collector current starts to increase. The parasitic inductance and resistance of one single bond wire can be calculated according to (1) and (4). Considering a typical operating condition (400 V, 120 A), the physical and electrical parameters and values of the drive loop can be acquired. Hence, each terms of (6) can be calculated and they are shown below.

It can be observed in Table II that the voltage on a parasitic inductance induced by a current change rate $\frac{di_{\mathrm{c}}}{dt}$ dominates the gate voltage overshoot V_{g_p}. The other three items can be

TABLE II
PHYSICAL AND ELECTRICAL PARAMETERS OF DRIVE LOOP AND CORRESPONDING TERMS OF (6)

Physical parameters and value		Electrical parameters and value		Corresponding product terms and their value	
$R_{g\_in}+R_e+R_{s\_e}$	12.96 mΩ	i_g	0.28A	$i_g\cdot(R_{g\_in}+R_e+R_{s\_e})$	0.0036V
R_e	0.116mΩ	i_c	120A	$i_c\cdot R_e$	0.0139V
$L_g+L_e+L_{s\_e}$	39.15nH	$\frac{di_g}{dt}$	$5\cdot10^5 A/s$	$(L_g+L_e+L_{s\_e})\cdot\frac{di_g}{dt}$	0.0196V
L_e	2.55nH	$\frac{di_c}{dt}$	$13\cdot10^8 A/s$	$L_e\cdot\frac{di_c}{dt}$	3.315V

TABLE III
PARASITIC INDUCTANCE L_i (IN NANOHENRY) OF BOND WIRE i FOR IGBT MODULE WITH ONE BOND WIRES ONE CUT-OFF

No. of the bond wire	1	2	3	4	5	The parasitic inductance L_i
1	6.10	3.04	2.11	1.21	1.03	13.48
2	3.04	6.10	3.04	1.46	1.21	14.85
3	2.11	3.04	6.10	1.84	1.46	14.55
4	1.21	1.46	1.84	6.10	3.04	13.65
5	1.03	1.21	1.46	3.04	6.10	12.84

TABLE IV
PARASITIC INDUCTANCE L_i (IN NANOHENRY) OF BOND WIRE i FOR IGBT MODULE WITH TWO BOND WIRES CUT-OFF

No. of the bond wire	1	2	3	4	The parasitic inductance L_i
1	6.10	3.04	2.11	1.21	12.46
2	3.04	6.10	3.04	1.46	13.63
3	2.11	3.04	6.10	1.84	13.08
4	1.21	1.46	1.84	6.10	10.61

TABLE V
PARASITIC INDUCTANCE L_i (IN NANOHENRY) OF BOND WIRE i FOR IGBT MODULE WITH THREE BOND WIRES CUT-OFF

No. of the bond wire	1	2	3	The parasitic inductance L_i
1	6.10	3.04	2.11	11.24
2	3.04	6.10	3.04	12.17
3	2.11	3.04	6.10	11.24

TABLE VI
PARASITIC INDUCTANCE L_i (IN NANOHENRY) OF BOND WIRE i FOR IGBT MODULE WITH FOUR BOND WIRES CUT-OFF

No. of the bond wire	1	2	The parasitic inductance L_i
1	6.10	3.04	9.13
2	3.04	6.10	9.13

neglected. Therefore, with parasitic emitter inductance linked to the derivative of the collector current linked to the currents, the gate voltage overshoot V_{g_p} can be simplified into

$$V_{g\_p}=V_{g\_\mathrm{th}}+L_e\frac{di_c}{dt}. \tag{7}$$

According to the analysis and (7), if IGBT has no load current, the IGBT would not have gate voltage overshoot in the turn-ON transient. In order to verify this analysis, a gate voltage measurement during IGBT turn-ON transient with no load current is conducted and shown in Fig. 5.

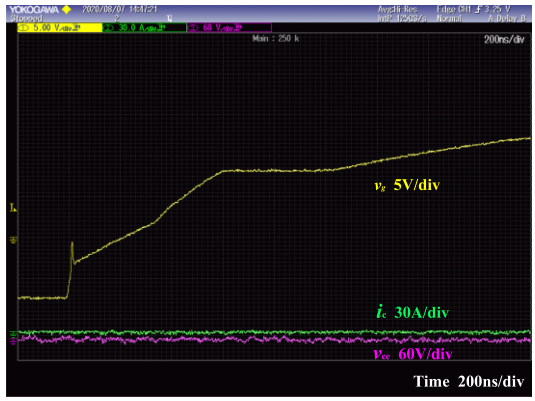

Fig. 5. Gate voltage during IGBT turn-ON transient with no load current.

Fig. 5 indicates that the gate voltage overshoot does not exist when the load current i_c is 0. This agrees with (7).

C. Influence of Operating Parameters on V_{g_p}

The influence of operating parameters on V_{g_p} will be discussed as follows. According to [24], V_{g_th} can be determined by

$$V_{g\_\mathrm{th}}=V_{\mathrm{FB}}+2\cdot\psi_B(T)+\frac{\sqrt{4\varepsilon_s e_0 N_A\psi_B(T)}}{C_{\mathrm{I}}}. \tag{8}$$

In (8), ε_s is the permittivity of the semiconductor, e_0 is the elementary charge, C_{I} is the unit-area isolation capacitance, T is the IGBT junction temperature, and N_{A} is the acceptor impurity concentration. All these parameters are essentially independent of temperature [24]. V_{FB} is the flatband voltage, which is closely related to the temperature T and bus voltage V_{bus} [22]. ψ_B is the Fermi level from the intrinsic Fermi level, which is determined as follows [24]:

$$\psi_B(T)=\frac{k\cdot T}{e_0}\cdot\ln\left(\frac{N_A}{n_i(T)}\right). \tag{9}$$

In (9), n_{i} is the intrinsic carrier concentration, which is influenced by the IGBT junction temperature T. k is the Boltzmann constant.

On the other hand, the turn-ON current change rate $\frac{di_c}{dt}$ can be determined as [23], [25]

$$\frac{di_c}{dt}=\frac{dv_g}{dt}\cdot G_m=\frac{dv_g}{dt}\cdot\left[\frac{1}{1-\alpha_{\mathrm{PNP}}(T)}\right]\cdot\times\left[\mu_n\cdot C_{\mathrm{ox}}\cdot\frac{W}{L}\cdot(v_g-v_{g\_\mathrm{th}})\right]. \tag{10}$$

G_m is the transconductance, α_{PNP} is the gain of the inherent bipolar transistor, which is related to temperature T, $\frac{W}{L}$ is the ratio between the width and the length of the MOS channel, and C_{ox} is the oxide capacitance. According to [25], the turn-ON current change rate $\frac{di_c}{dt}$ rises with the increasing of both bus voltage V_{bus} and load current I_L, and it decreases with the increase of IGBT junction temperature T.

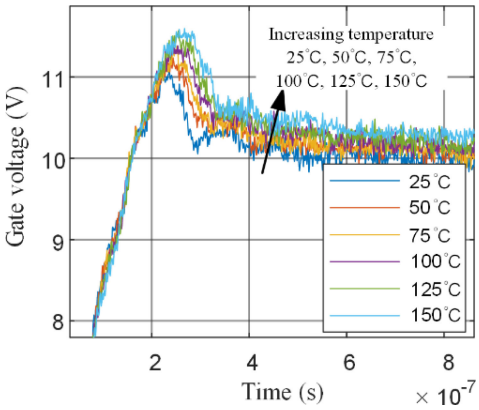

Fig. 6. Gate voltages during turn-ON transient via various temperatures.

Therefore, the gate voltage overshoot V_{g_p} can be determined as

$$V_{g\_p} = V_{\mathrm{FB}}\left(T, V_{\mathrm{bus}}\right) + 2 \cdot \frac{k \cdot T}{e_0} \cdot \ln\left(\frac{N_A}{n_i\left(T\right)}\right) + \frac{\sqrt{4\varepsilon_s e_0 N_A \left(\frac{k \cdot T}{e_0} \cdot \ln\left(\frac{N_A}{n_i(T)}\right)\right)}}{C_{\mathrm{I}}} + L_e \cdot \frac{dv_g}{dt} \cdot \left[\frac{1}{1 - \alpha_{\mathrm{PNP}}\left(T\right)}\right] \cdot \left[\mu_n \cdot C_{\mathrm{ox}} \cdot \frac{W}{L} \cdot \left(v_g - v_{g\_\mathrm{th}}\right)\right]. \quad (11)$$

Equation (11) indicates that the gate voltage overshoot V_{g_p} is affected by dc bus voltage V_{bus}, load current I_{L}, IGBT junction temperature T, and IGBT stray emitter inductance.

To illustrate the effect of different parameter variations, a group of simulations under 400 V and 120 A is conducted. The gate voltages during turn-ON transient via various temperatures are acquired by oscilloscope and redrawn by MATLAB, which is shown in Fig. 6.

Fig. 6 shows that there is a positive relationship between the gate voltage overshoot V_{g_p} and IGBT junction temperature T.

Those experimental results further explain (11), and they are consistent with the theoretical analysis. The calibration on I_L, V_{bus}, and T as benchmark values will be introduced in Section III-D.

D. Analysis of Parasitic Inductance With Bond Wire Fault

This article aims to provide a precursor for IGBT bond wire degradation. Next, the effect of different severities of bond wires lift-off will be discussed.

When one bond wire fails, for instance, no. 6, the update stray inductance of the other five valid bond wire is described in Table III.

The total stray inductance of one chip is 2.77nH, which is the result of the parallel connection of the remaining five inductances. Similarly, for two bond wires lift-off, the total stray inductance of one chip is described in Table IV.

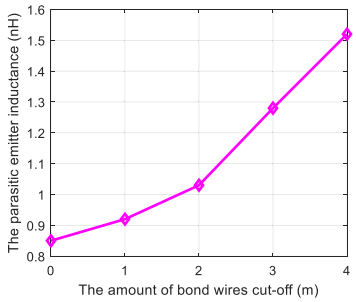

Fig. 7. Relationship between L_{e} with the amount of cut-off bond wires m.

TABLE VII
INCREMENT AND THE PERCENTAGE CHANGE OF V_{g_p} WITH VARIOUS DEGREES OF BOND WIRES LIFT-OFF

Amount of bond wires lift-off	The stray emitter inductance	Increment of stray inductance	Increment of bond wire induced voltage	The percentage change of $V_{\mathrm{g\_p}}$
0	0.85 nH	0 nH	0 V	0.00%
1	0.92 nH	0.07 nH	0.108 V	0.97%
2	1.03 nH	0.18 nH	0.267 V	2.39%
3	1.28 nH	0.43 nH	0.648 V	5.81%
4	1.52 nH	0.67 nH	1.009 V	9.05%

The total stray inductance of one chip is 3.08 nH, which is the result of the parallel connection of the remaining four inductances. Similarly, for three bond wires lift-off, the total stray inductance of one chip is described in Table V.

The total stray inductance of one chip is 3.85 nH, which is the result of the parallel connection of the remaining three inductances. Similarly, for four bond wires lift-off, the total stray inductance of one chip is described in Table VI.

The total stray inductance of one chip is 4.57 nH, which is the result of the parallel connection of the remaining two inductances.

In practical application, the stray emitter inductance of the IGBT module is determined by three parallel chips. Therefore, the stray emitter inductance is one-third of the above stray inductance of one chip.

The quantitative relation curves between stray emitter inductance L_{e} with the amount of cut-off bond wires m are shown in Fig. 7.

Fig. 7 indicates that parasitic inductance L_{e} of emitter rises with the increase of the number of bond wires cut-off, m, which can be potentially used as bond wire fault precursor.

According to the change of stray emitter inductance and (7), the theoretical value of the percentage change of V_{g_p} can be calculated. With an operating condition, 600 V bus voltage, 150 A collector voltage, and 100 °C temperature, the gate voltage overshoot V_{g_p} of fault-free IGBT is 11.15 V. Besides, the turn-ON transient process $\frac{di_c}{dt}$ is about $1.5 \cdot 10^9$ A/s (The results are shown in Fig. 12). Hence, the increment and the percentage change of V_{g_p} with various degrees of bond wires lift-off are calculated and given in Table VII.

Under typical operating condition, the calculating theoretical approximate results of the percentage change of V_{g_p} with

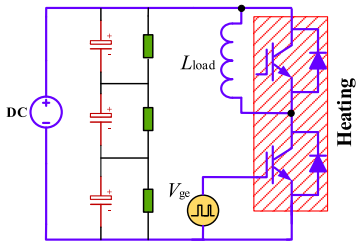

Fig. 8. Schematic diagram of double pulse test.

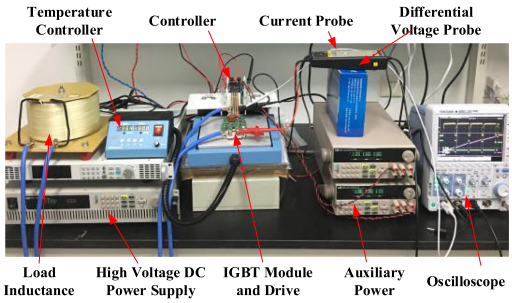

Fig. 9. Double pulse power test platform.

various bond wires cut-off are 0.97%, 2.39%, 5.81%, and 9.05%, which are a typical set of values. The specific threshold values for detecting bond wire in the practical application can be acquired more accurately via experiment testing.

According to the analysis above, the turn-ON gate voltage overshoot V_{g_p} before Miller duration can effectively reflect bond wire lift-off faults. The calibration of benchmark values of fault-free IGBT on I_{L}, V_{bus}, and T will be introduced in Section III for consideration in practical industrial application.

III. Experimental Setup and Results

A. Experimental Setup

In order to verify the theory and feasibility of this method, a double pulse power test platform is built. The schematic diagram of the experimental platform is shown in Fig. 8. The photograph of the experimental platform is shown in Fig. 9.

In Fig. 8, the lower IGBT is used for the bond wires cut-off test. Gate of lower IGBT is controlled by a double pulse generating controller, while the upper IGBT is always kept blocking.

The instruments consisted of the platform are shown as following. The device under test (DUT) is *FF300R12ME4* of *Infineon*. It consists of an independent bridge arm and includes two IGBTs. The external gate resistor is set as 20 Ω, which enables an accurate measurement of the Miller plateau duration illustrated in [18] for comparison. The load inductance of double-pulse is 1.5 mH. The bus capacitances are three B43703A5129M000 connecting in series. The final capacity is 4000 μF, and it is used to store energy for supplying current to the load inductor and relieving stress in the high voltage dc source supply. In order to balance the voltages of three capacitances, each capacitance parallel with a resistor of 500 kΩ for voltage balance.

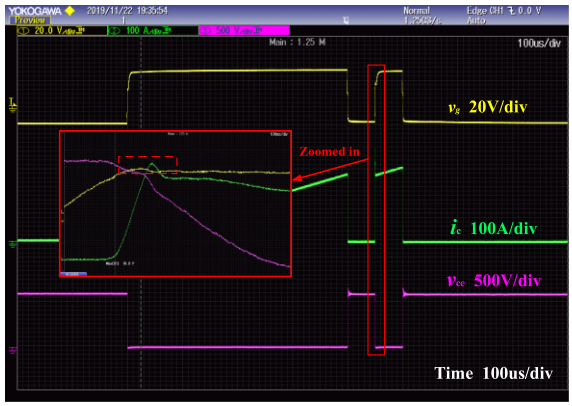

Fig. 10. v_g, v_{ce}, and i_{c} waveforms under double pulse test (the turn-ON transient zoomed-in).

The bus voltage is set by a high voltage dc source IT6726V, which has an accuracy of set value with 0.04%. The double pulse generating controller is conducted by TMS320F28335 and programed by CCS6.0. The pulse duration is set by a keyboard and displayed through digital tubes. The main measuring instrument is high-precision multichannel digital oscilloscope DLM2034, which has a bandwidth of 350 MHz and a sampling rate of 2.5 GS/s. High-frequency current probe CP9060S is a Rogowski Coil with a bandwidth of 30 MHz and a precision of 2%. Auxiliary power supply IT6322A with high-precision and high-resolution of 1 mV. The high-voltage differential probe is 700924 of Yokogawa, which has a bandwidth of 100 MHz and a measuring range of ±1400 V.

This test platform can conduct double-pulse experiments without self-heating. The test current is regulated by the duration of the first pulse. The voltage is controlled by the bus voltage set. The temperature of the DUT can be controlled by the heating aluminum board. Fig. 10 shows a group of typical waveforms including gate driver voltage v_{g}, collector voltage v_{ce} and collector current i_{c} under double pulse test. The V_{bus} is 600 V, and T is 100 °C.

In Fig. 10, yellow waveform of CH1 is gate driver voltage v_g, which has an overshoot before the Miller platform. This overshoot V_{g_p} will be demonstrated by experimental results.

In the test platform developed for bond wire diagnostics and prognostics of IGBT power modules, bond wire faults of DUT, *FF300R12ME4*, are generated by cutting off the emitter bond wires of three paralleled chips one by one (up to four bond wires in a six-wired IGBT). There are three reasons for this arrangement. The first is to focus the attention on emitter bond wire faults because it is the most prominent fault types in wire welding packaging IGBT modules [7], while the diagnosis of gate bond wire degradation is meaningless since the fault of one gate bond wire is catastrophic. The second is that the emitter bond wire fault of one chip would increase the current of other chips and make their emitter bond wires more vulnerable, leading to more severe failures. The third is to shorten the duration of experimental tests by cutting off bond wires [9], [11], [15], rather than long term aging process.

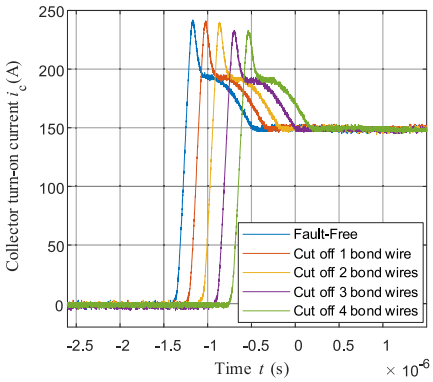

Fig. 11. i_c waveforms of turn-ON transient.

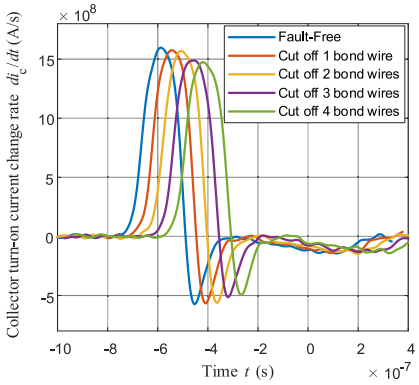

Fig. 12. Turn-ON transient $\frac{di_c}{dt}$ of different bond wires faults.

B. Turn-on Current Change Rate Experimental Results

According to (7), the turn-ON gate voltage overshoot V_{g_p} has a close relationship with turn-ON transition collector current change rate $\frac{di_c}{dt}$. Therefore, to study $\frac{di_c}{dt}$ with various bond wire cut-off condition, the turn-ON transition collector currents of each bond wire faulty condition are measured and compared with the healthy state of the DUT are shown in Fig. 11, which displays the collector current i_c waveforms of fault-free and different cut-off number of emitter bond wires ($V_{\rm bus}$ = 600 V, T = 100 °C, and I_L= 150A).

Fig. 11 indicates that when the bond wires are cut-off, the collector current peak values decrease slightly in comparison with the fault-free condition. The collector current change rate $\frac{di_c}{dt}$ can be obtained by differential calculation of data in Fig. 11. To filter the noise components of Fig. 11, differential calculation of the turn-ON transient current data is performed with 500 quantitate points averaged. The turn-ON transient $\frac{di_c}{dt}$ with filtering the noise component of a healthy and different cut-off number of emitter bond wires are shown in Fig. 12 ($V_{\rm bus}$= 600 V, T = 100 °C, and I_L= 150A).

In Fig. 12, the turn-ON transient current change rate $\frac{di_c}{dt}$ is nearly about 1500 A/μs with a duration of 0.1μs. Furthermore, Fig. 12 indicates that turn-ON current change rate $\frac{di_c}{dt}$ is slightly influenced by the bond wire faults. When the bond wires fault happens, the turn-ON transient process $\frac{di_c}{dt}$ have a slight decline.

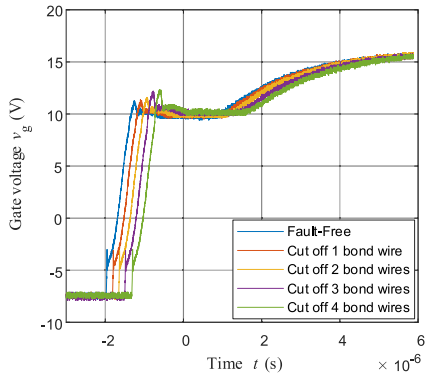

Fig. 13. v_g at different amount of bond wires cut-off.

This is because the bond wire cut-off makes the communication loop circuit inductance increase and the current transient rate decrease. With bond wires cut-off varying from one to four, the current change rate $\frac{di_c}{dt}$ decrease from $1.597 \cdot 10^9$ to $1.575 \cdot 10^9$, $1.569 \cdot 10^9$, $1.488 \cdot 10^9$, and $1.475 \cdot 10^9 A/s$. The percentage changes are -1.38%, -1.75%, -6.83%, and -7.64%. Combined with (7), it can be indicated that if the turn-ON gate voltage overshoot V_{g_p} rises with the increase of the bond wires cut-off, it must be caused by the increase of parasitic inductance L_e of the emitter bond wire.

C. Experimental Results of V_{g_p}

In order to illustrate v_g under different bond wire status, a series of experiments are conducted. The $\rm V_{g\_p}$ would be recorded in different temperatures, collector-emitter voltages and collector currents with various bond wire cut-off conditions. The experimental data are saved in the oscilloscope, and after the test, they are exported to the computer and replotted by MATLAB. The gate voltage v_g waveforms of healthy and different cut-off number of emitter bond wires are shown in Fig. 13 ($V_{\rm bus}$= 600 V, T = 100 °C, and I_L= 150A).

As observed in Fig. 13, the gate voltage overshoot V_{g_p} before Miller duration increases with the increment of the number of bond wires cut-off. Considering the influence of $V_{\rm bus}$, I_L, and T on $V_{\rm g\_p}$, additional experimental validations are conducted under various operating conditions. The experimental results are shown in Fig. 14 ($V_{\rm bus}$= 600 V, I_L= 150A), Fig. 15 ($V_{\rm bus}$= 600 V, T = 100 °C), Fig. 16 (I_L= 150A, T = 100 °C), respectively.

Figs. 14–16 show that turn-ON gate voltage overshoot V_{g_p} increases with the number of bond wires lift-off. The curves of those three figures have a similar trend as in Fig. 7. Besides, the trend of V_{g_p} is consistent with the theoretical value with the difference of more than 1.5 V between healthy and four bond wires lift-off in comparison to 0.16 V of ON-state voltage reported in [9]. It's worth noting that V_{g_p} increases significantly when only one bond wire is cut-off. This characteristic is critical for early bond wire fault detection.

In order to define the degree of bond wire degradation, the ratios expressed as percentage change are calculated. Percentage change of V_{g_p} is the different ratio of precursor

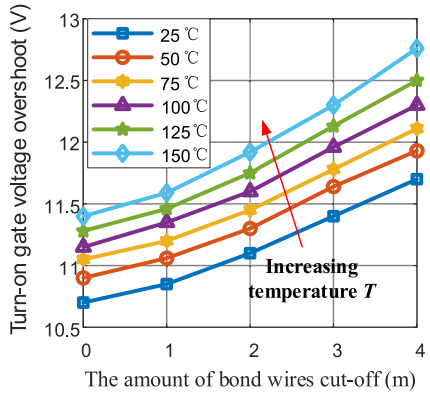

Fig. 14. V_{g_p} at different T($V_{\rm bus}$= 600 V and I_L= 150A).

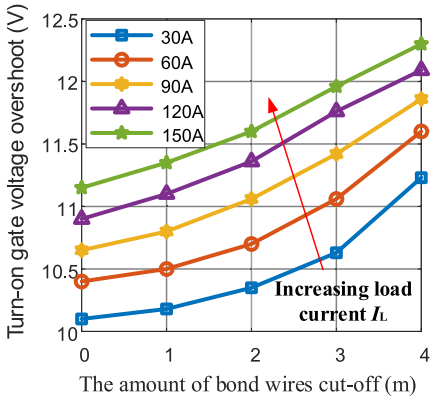

Fig. 15. V_{g_p} at different $I_{\rm L}$($V_{\rm bus}$= 600 V and T = 100 °C).

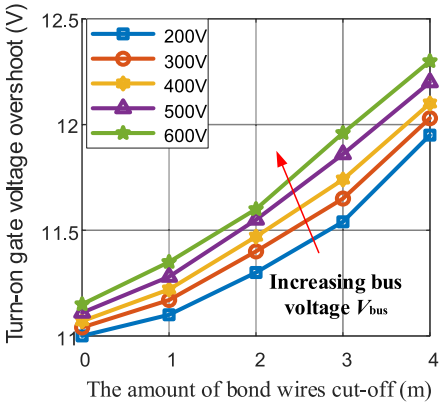

Fig. 16. V_{g_p} at different $V_{\rm bus}$(I_L= 150A and T = 100 °C).

parameter measured with actual device compared with the V_{g_p} benchmark value of the fault-free DUT. The percentage changes of V_{g_p} with various bond wires cut-off and multiple temperatures ($V_{\rm bus}$ = 600 V and I_L = 150 A) are shown in Fig. 17.

Fig. 17 indicates that the percentage change of V_{g_p} varies with temperatures. This agrees with the theoretical analysis in Section II. Moreover, the quantitate percentage change of V_{g_p}

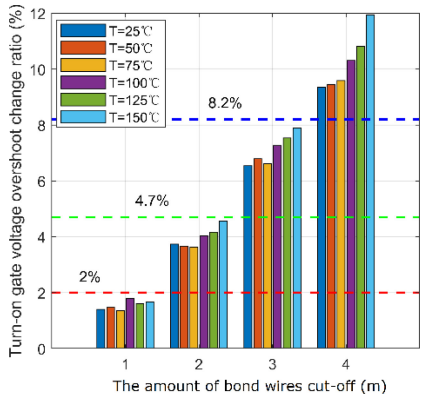

Fig. 17. Percentage changes of V_{g_p} with various bond wires cut-off ($V_{\rm bus}$= 600 V and I_L= 150 A).

data in Fig. 17 show the threshold values of the turn-ON gate voltage overshoot by 2%, 4.7%, 8.2% to 12% for four bond wire cut-off conditions. Besides, the percentage change of V_{g_p} with various $V_{\rm bus}$ (200–600 V) and I_L(30–150 A) are tested. The threshold values of the turn-ON gate voltage overshoot are also 2%, 4.7%, 8.2% to 12% for four bond wire cut-off conditions. The reason for this gradual increase in judgment threshold value is convinced to be caused by the rise of IGBT parasitic inductance. Those results are consistent with the analysis presented in Section II.

It can be summarized from the above data and analysis that the threshold used for degradation degree identification of bond wires based on the turn-ON gate voltage overshoot can be acquired by experiments.

D. Calibration on I_L, $V_{\rm bus}$, and T as Benchmark

For practical considerations of the implementation, the turn-ON gate voltage overshoot of the healthy baselines of the brand new IGBT modules should be obtained from measurements and are later used as the benchmark for predicting bond wire degradation in practical applications.

Based on theoretical analysis and data shown in Figs.14–16, the turn-ON gate voltage overshoot V_{g_p} has dependencies on I_L, $V_{\rm bus}$, and T. Moreover, it can be observed that there is a positive correlation between the turn-ON gate voltage overshoot V_{g_p} and the operating status parameter I_L, $V_{\rm bus}$, and T. Therefore, the fitting is conducted to determine the correlation between V_{g_p} and operation condition variations for calibration as a standard value.

The experimental results of the gate voltage overshoot V_{g_p} at different IGBT junction temperatures and the corresponding linear fitting curves are shown in Fig. 18 ($V_{\rm bus}$= 600 V and I_L= 150 A).

As shown in Fig. 18, the relationship between V_{g_p} with T is quite linear. Besides, the gate voltage overshoot V_{g_p} under various load currents and bus voltages are studied and fitted. The relationships between I_L and $V_{\rm bus}$ are still linear. The fitting

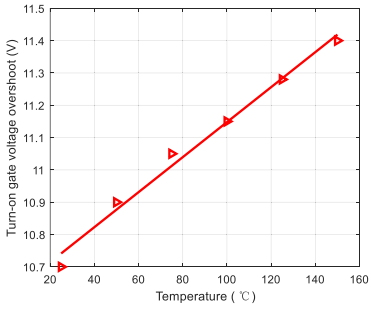

Fig. 18 . V_{g_p} at different T ($V_{\rm bus}$= 600 V and I_L= 150A).

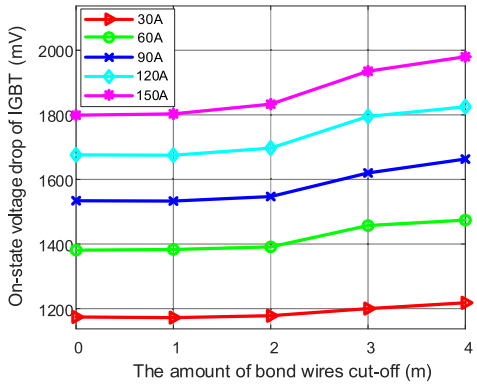

Fig. 19. ON-state voltage drops with different bond wire faults.

results of the benchmark value can be calibrated and expressed as

$$V_{g\_p}= 0.0054 \cdot T + 0.0004 \cdot V_{\rm bus} + 0.0087 \cdot I_{\rm c} + 9.074. \tag{12}$$

With this calibration of the benchmark value, the percentage change can be obtained by the comparing actual V_{g_p} with benchmark value. The degree of bond wire fault can then be identified by the corresponding threshold value.

E. Experiments of Existing Methods

Some existing methods have been proposed and studied. To further verify the superiority of the proposed method. Two existing bond wire degradation monitoring methods are investigated and used as a comparison. They are bond wire diagnosis based on ON-state voltage [8]–[12] and bond wire diagnosis based on the Miller plateau duration [18].

1) Bond Wire Diagnosis Based on ON-State Voltage: The ON-state voltage-based method of bond wire diagnosis is widely studied [8]–[12]. An online ON-state voltage monitoring circuit is utilized for measurement [26]. In order to simulate the practical operating temperature environment, the junction temperature is heated to 100 °C. The ON-state voltage drops with different bond wire faults are shown in Fig. 19.

Fig. 19 indicates that the ON-state voltage drops have an increment with the degradation of bond wires. The sensitivity and resolution are dependent on the load current. Besides, when

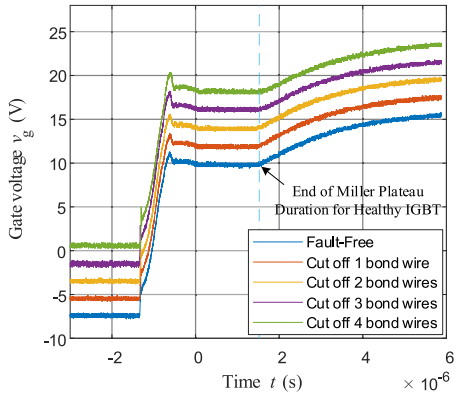

Fig. 20. Miller plateaus of turn-ON transient process with different bond wire faults.

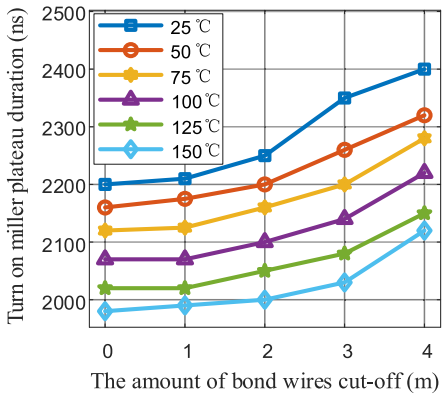

Fig. 21. Miller plateau durations with various bond wire faults at 600 V and 150 A.

the bond wire degradation is not too serious, for instance, the one or two bond wires are cut-off, there is a tiny difference in the on-state voltage drops. Especially when the load current is below 90A, there is little distinction in their on-state voltage drops.

2) Bond Wire Diagnosis Based on the Miller Plateau Duration: The work in [18] proposes a bond wire diagnosis method based on the Miller plateau duration. This method is also used as a comparison. The bus voltage is 600 V, the collector current is 150 A, and the temperature is 100 °C, the Miller plateaus of turn-ON transient process with different bond wire faults are shown in Fig. 20.

As shown in Fig. 20, the Miller plateau duration has a slight increase with the bond wire cut-off. More experiments are conducted for comparisons. In the experiment, the starting point of Miller plateau is the moment of the gate voltage overshoot V_{g_p} [18]. The experiment results of Miller plateau duration at 600 V and 150 A with different junction temperatures and various bond wire faults are shown in Fig. 21.

Fig. 21 indicates the Miller plateau duration has an increment about 150 μs when four bond wires are cut-off. However, it still has a drawback of low resolution between fault-free and

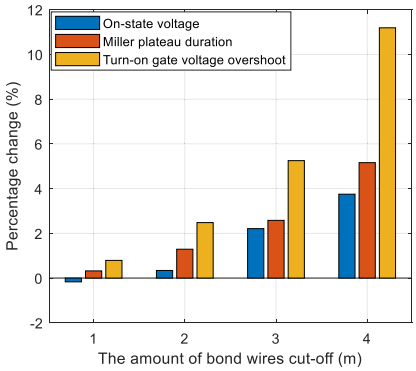

Fig. 22. Percentage changes of three fault indicators compared to baseline with load current 30 A.

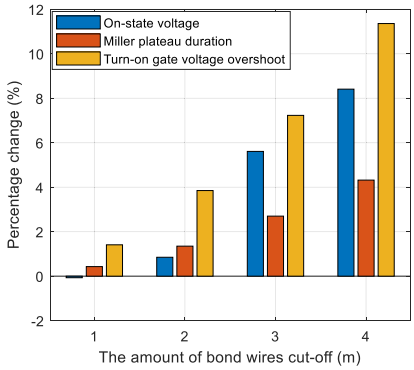

Fig. 23. Percentage changes of three fault indicators compared to baseline with load current 90 A.

one bond wire cut-off condition. In practical application, the measurement circuitry proposed in [18] is difficult for high-frequency applications.

F. Comparisons With Existing Methods

The turn-ON gate voltage overshoot proposed in this article is compared with the existing precursor parameters, including on-state voltage, Miller plateau duration under the same operating condition. The percentage changes of different methods with various cut-off bond wires are presented in Figs. 22 –24. The temperature is set as 100 °C, which is close to the practical online operating temperature environment. The bus voltage is 600 V. Figs. 22–24 are the quantitate percentage change with load current 30, 90, and 150 A, respectively.

Percentage change of turn-ON gate voltage overshoot is obviously larger than that of ON-state voltage, and miller plateau duration when the bond wires lift-off is 1 or 2. For ease of description, we define that one or two wires lift-off can be regarded as "slight fault" and three-plus wires lift-off is "serious fault." This means a slight fault can be distinguished with higher discrimination using the method proposed. For serious fault, the method proposed has superiority compared with the Miller plateau duration-based method. The turn-ON gate voltage overshoot has a higher resolution than the ON-state voltage for 30 and 90 A, while their resolutions are similar for 150 A.

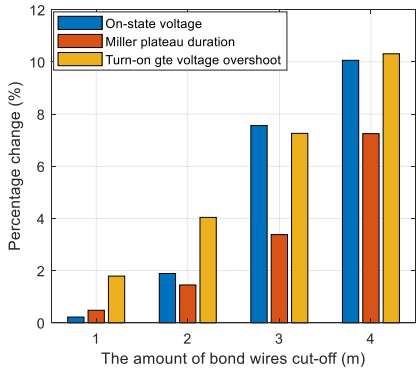

Fig. 24. Percentage changes of three fault indicators compared to baseline with load current 150 A.

TABLE VIII
COMPARISON OF THREE PRECURSORS FOR BOND WIRE DEGRADATION

Bond wire precursor	Sensitivity with a slight fault	Sensitivity with a serious fault
Turn-on gate voltage overshoot proposed	High	High
On-state voltage [9]	Low	Varies with current
Miller plateau duration [18]	Low	Middle

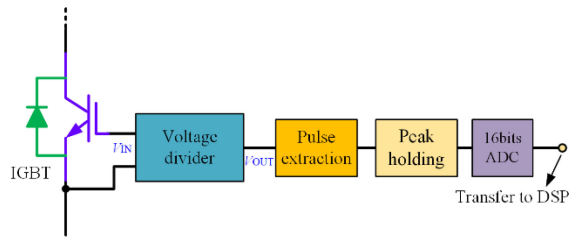

Fig. 25. Signal acquisition and processing scheme for the gate voltage overshoot V_{g_p} during turn-ON transient.

Therefore, the turn-ON gate voltage overshoot-based method for bond wire degradation has higher resolution as an initial bond wire fault indicator, compared with ON-state voltage, Miller plateau duration. The comparison of three precursors for bond wire degradation is summarized and given in Table VIII.

Above experimental results are conducted with a gate resistor of 20 Ω. In fact, the results are similar with smaller gate resistor for instance the recommended resistor by the datasheet can generate similar results in practical application. It is because the percent change of the gate voltage overshoot V_{g_p} mainly depends on the difference of stray inductance of various bond wire fault rather than the collector current change rate, which is influenced by the gate resistor.

G. Measurement Implementation Discussion

A practical measurement implementation for measuring the turn-ON gate voltage overshoot V_{g_p} will be discussed in this section. The scheme of the measurement technique is shown in Fig. 25.

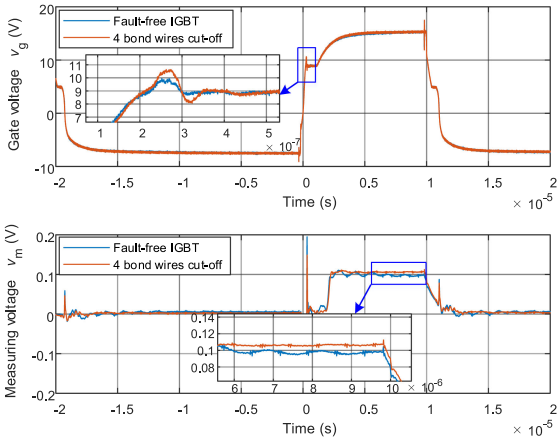

Fig. 26. Signal acquisition results for the gate voltage overshoot V_{g_p} with various IGBT bond wire conditions.

The voltage between the gate and emitter of IGBT is acquired by a voltage divider circuit. The output of the voltage divider circuit is connected with the pulse extraction circuit, which extracts the narrow pulse including the turn-ON gate voltage overshoot V_{g_p}. Then, the peak holding circuit [27]–[29] keeps the peak value of a narrow pulse. The output of the peak holding circuit is adapted to be digitized in a fast 16 bits analog/digital converter (ADC). The measurement ADC is a 16bit +5 V device with resolution of 0.08 mV. During tests, an increase of approximately 100 mV in V_{g_p} has been observed after bond wire is lift-off. Hence, the turn-ON gate voltage overshoot V_{g_p} can be obtained by the microprocessor (DSP or MCU) with high accuracy. With the measuring implementation discussed above, the gate resistor is set as 10 Ω for simulating the practical application and the experiments are conducted. The voltage V_{g_p} of fault-free IGBT and IGBT with four bond wires are monitored and shown in Fig. 26.

Fig. 26 indicates that the increment of gate voltage overshoot V_{g_p} from fault-free IGBT to IGBT with four bond wires cut-off is 700 mV, which can be detected by measuring v_m.

With the temperature, bus voltage, and load current, the turn-ON gate voltage overshoot V_{g_p} benchmark of the fault-free condition can be calculated. Comparing the real V_{g_p} with the benchmark value of V_{g_p}, the percentage change can be calculated, and the IGBT state can be reported as fault-free, slight degradation or serious fault. Finally, whether load reduction or IGBT replacement can be adopted according to the IGBT state report.

IV. Conclusion

In this article, a novel method of using turn-ON gate voltage overshoot for bond wire failure identification has been proposed with theoretical analysis and experimental validation presented. The change of the parasitic inductance can reflect the lift-off of the bond wires. As a result, the turn-ON gate voltage overshoot is proposed as a fault indicator, which can effectively indicate bond wire lift-off faults. The failure of bond wires increases the gate turn-ON voltage overshoot of IGBT modules. The calibration of benchmark value for the dependency of turn-ON gate voltage overshoot V_{g_p} on I_L, $V_{\rm bus}$, and T has been discussed for practical considerations. Besides, the turn-ON gate voltage overshoot-based method for bond wire degradation has higher resolution as an initial bond wire fault indicator, compared with ON-state voltage or Miller plateau duration-based methods, which are commonly used. A practical measurement implementation has also been discussed in this article. It has been shown that the proposed method is effective for early bond wire fault detection and healthy management of IGBT modules.

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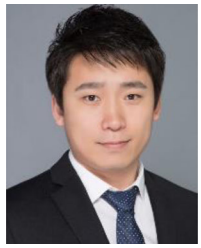

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