A Novel Bidirectional Isolated DC-DC Converter With High Voltage Gain and Wide Input Voltage

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***Abstract*—This article proposes a novel bidirectional isolated dc–dc converter with high voltage gain and wide input voltage, which can be applied to bidirectional power conversion systems. The proposed topology is composed of a bidirectional buck-boost converter and a forward-flyback converter; it has the advantage of higher voltage gain and has continuous current characteristic of the low-side port in step-up and step-down mode. In addition, the proposed topology also has the function of leakage inductance energy recovery, which can improve the efficiency of the converter, reduce the voltage surges on switches, and have the characteristics of zero voltage switching on certain switches. Finally, this paper implements a 500-W bidirectional dc–dc converter to verify the feasibility of the proposed topology. The low-side voltage of the proposed topology is 24, 48, and 55 V; the maximum efficiency in step-up mode are 94.2%, 95.6% and 96.9%, and the maximum efficiency are 92.6%, 94.2% and 94.5% in the step-down mode, respectively.**

***Index Terms*—Bidirectional dc–dc converter, forward-flyback converter, high voltage conversion ratio, zero voltage switching (ZVS).**

I. Introduction

AS TECHNOLOGICAL development and standards of living continue to improve, all kinds of works have more dependent on electricity. Varieties of works are also actively thinking about more efficient scheme of electric power supply and reducing power supply costs because of the rise of environmental protection consciousness. In recent years, demand response [1]–[3] and smart grid [4]–[6] are the hottest topics.

With the popularity of electric scooters, in order to increase the convenience of changing batteries, electric scooter battery exchange station systems are also gradually increasing. If we can combine electric scooter exchange station systems with demand response and a smart grid, using big data [7]–[9] to analyze the battery exchange quantity of each electric scooter battery exchange station, and feed part of battery into the dc bus to assist power plants during peak times, as shown in Fig. 1.

When in off-peak times, the dc bus recharges to batteries of electric scooter battery exchange station systems, it can balance peak and off-peak periods of electricity use and reduce the burden on power plants and renewable energy.

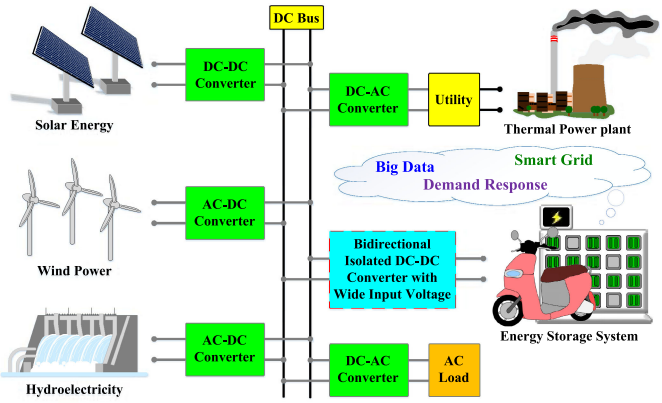

Fig. 1. Configuration of diversified energy system with electric scooter battery exchange station.

As the complexity increases of power transmission systems, the traditional unidirectional converters are no longer enough for use. A bidirectional dc–dc converter can achieve bidirectional power transmission in the same topology, e.g., energy storage systems, uninterruptible power systems, and kinetic energy recovery system for electric vehicles; it can effectively reduce the number of components, increase the power density and reduce production costs. The novel bidirectional dc–dc converters which just designed for higher conversion efficiency, power conversion ratio, stability and lower cost have also sprung up.

There are novel isolated bidirectional dc–dc converters which are improved from the traditional flyback converter [10], [11]. The technology of leakage energy recovery [12]–[14] is adopted, and the conversion efficiency can be improved.

The isolated bidirectional resonant dc–dc converters [15], [16] which were based on a basic bidirectional *LLC* resonant converter. In [15], the drawback of the complex control in the traditional bidirectional *LLC* converter is improved. The zero voltage switching (ZVS) [17]–[19] and ZCS [20]–[22] technology is used in this topology to increase conversion efficiency. In [16], a new control scheme is proposed. All switches in this topology can have the advantage of soft switching; the switching losses can be reduced greatly.

Bidirectional dc–dc converters [23]–[25] which have an inductor are used to reduce the low-side current ripple. The main circuit of the topology [23] consists of the voltage doubler

Manuscript received July 9, 2020; revised October 6, 2020 and November 14, 2020; accepted December 15, 2020. Date of publication December 24, 2020; date of current version March 5, 2021. Recommended for publication by Associate Editor M. Tavakoli Bina. *(Corresponding author: Yu-En Wu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2020.3045986.

Digital Object Identifier 10.1109/TPEL.2020.3045986

circuit, the low-side inductor combined with the transformer to increase power density. In order to reduce the current ripple, the *LC* filters are added to the voltage ports. In [24], this topology is improved by the traditional Ćuk [26], [27] converter, and it features ZVS technology. An isolated bidirectional dc–dc converter [25] is derived by a half bridge converter, full bridge converter, and a center-tapped transformer [28]–[30]. The switching signals are achieved by a complementary pulsewidth modulation (PWM) signal and a hybrid phase-shift control scheme; it can reduce the root mean square current and achieve ZVS of switch within the secondary side, there are the advantages that the conduction loss, the switching loss, and the current stress are reduced of this topology.

Novel bidirectional interleaved converters [31], [32] which comprise two buck-boost bidirectional converters [33] to reduce the current ripple on low-side significantly. In [31], it employs switched capacitor technology to transfer the voltage to achieve a higher voltage conversion ratio. In [32], different from the traditional *LLC* converters which is controlled by fixed frequency and only needs to adjust duty ratio to achieve the function of power regulation, it is easier to control in this topology. All switches in this topology have ZVS; the switching loss can be reduced.

In [34], a full-bridge dual active bridge (FBDAB) converter and a half-bridge dual active bridge (HBDAB) converter are introduced. These topologies can be used for bidirectional transmission in larger power, but the control is more complex in these topologies.

Compared with traditional nonisolated converters, the novel isolated converters [35]–[39] can achieve higher voltage gain by adjusting the turns ratio of transformers. On the other hand, the isolated converters do not establish a direct current flow path between the power source and the load; it can achieve galvanic isolation and improve the safety of equipment [40]–[42]. Therefore, the isolated converters are often used in applications that require isolate electromagnetic interference (EMI) [43]–[46], such as precision equipment and measuring instruments. If the energy of leakage inductance [47]–[49] of the transformer is not processed well, it may reduce the conversion efficiency significantly due to the voltage spikes. If the situation becomes serious, it will damage semiconductor components.

II. Circuit Architecture and Operation Principle

A novel bidirectional isolated dc–dc converter is proposed in this article, as shown in Fig. 2(a). The definitions of components are summarized in the followings. V_H and V_L are the high voltage side and the low voltage side power ports, respectively. There are switches S_1 to S_6 in the proposed topology, the parasitic capacitances C_{S1} to C_{S6} and body diodes D_{S1} to D_{S6} are the parasitic components of switches S_1 to S_6, respectively. The capacitors C_1 to C_3, an inductor L_1 and a transformer are also parts of the proposed topology. The transformer is composed of leakage inductance $L_{\mathrm{lk}\,1}$ and $L_{\mathrm{lk}\,2}$, magnetizing inductance L_{m1} and an ideal transformer (N_2 / N_1).

The operation principle and operation mode of the proposed topology in step-up mode and step-down mode will be analyzed.

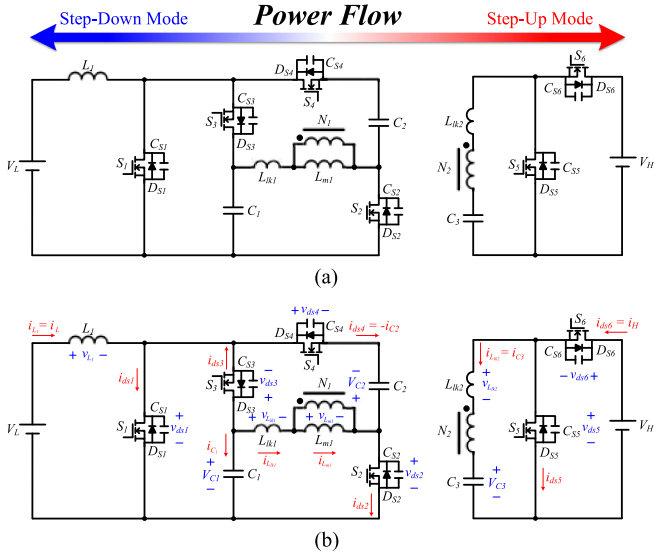

Fig. 2. (a) Proposed bidirectional isolated dc–dc converter. (b) Definition for equivalent circuit diagram of proposed topology.

The voltage polarity and current direction of components in proposed topology is defined, which is shown in Fig. 2(b). Furthermore, all magnetic components are operated in CCM. In order to simplify the analysis of the operation principle, several assumptions need to be made as follows.

1) All the parasitic effects and internal resistance are not considered, which are operated at high frequencies.
2) Assuming switches and parasitic diodes of switches are ideal, and the parasitic capacitance is considered.
3) Assume that the capacitance values C_1, C_2 and C_3 are infinite.
4) Leakage inductance values $L_{\mathrm{lk}\,1}$ and $L_{\mathrm{lk}\,2}$ are much lower than the magnetizing inductance L_{m1}.

A. Step-Up Mode

In step-up mode, the operating signal is a complementary signal composed of two sets of signals; v_{gs1} and v_{gs2} are one set of signals while v_{gs3} and v_{gs4} are another set of signals. The signal of S_5 and S_6 are in OFF state. The key waveforms of the proposed topology in step-up mode are shown in Fig. 3. It can be divided into five operation modes in an operating cycle, as shown in Fig. 4(a)–(e).

1) Mode 1 [t_0~t_1]

At the beginning of this mode at the time $t = t_0$, all switch signals are in OFF state. The capacitor C_1 is charged by the low voltage side V_L and the inductor L_1. The leakage inductance $L_{\mathrm{lk}\,1}$ extracts the energy from the parasitic capacitance C_{S2} of the switch S_2 to achieve ZVS and charges the parasitic capacitance C_{S4} of the switch S_4 until the switch S_4 is turned OFF. The energy of the magnetizing inductance L_{m1} is conducted to the high voltage side V_H by the ideal transformer and via the switch S_6, and the electric charges of the parasitic capacitor C_{S6} on the switch S_6 are removed. The current of the body diode D_{S5} on the switch S_5 gradually drops to zero, the switches S_1 and S_2

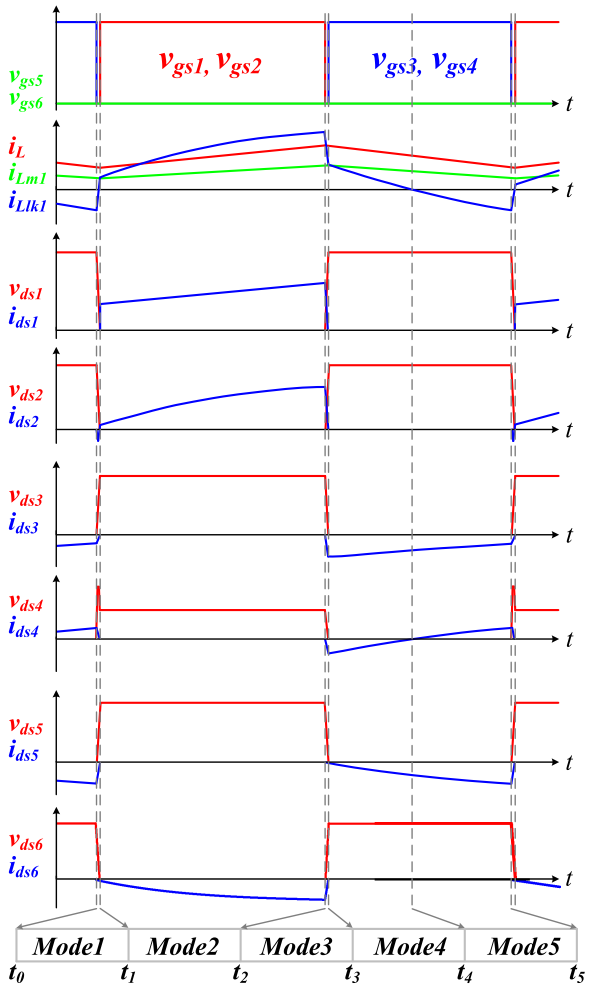

Fig. 3. Key waveforms of proposed topology in step-up mode.

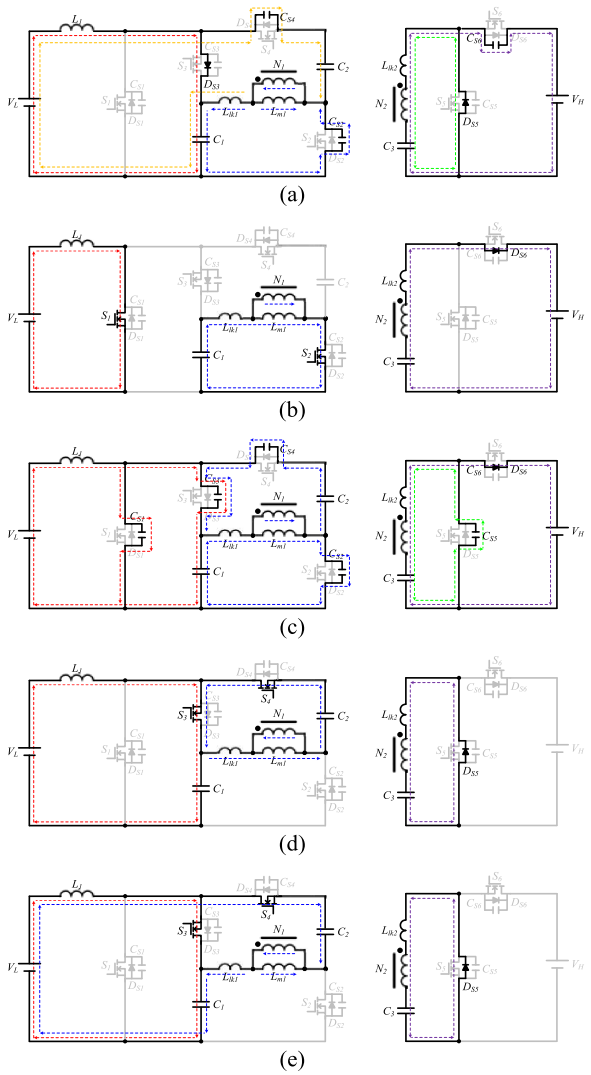

Fig. 4. Equivalent circuit diagram of in step-up mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

are turned ON, and mode 1 ends. The equivalent circuit of mode 1 is shown as Fig. 4(a).

2) Mode 2 [t_1~t_2]

The switch signals v_{gs1} and v_{gs2} are in ON state and the switch signals v_{gs3} and v_{gs4} are in OFF state, while the interval begins at the time $t = t_1$. The low voltage side V_L supplies energy to inductor L_1, and the capacitor C_1 releases energy to magnetizing inductance L_{m1} and leakage inductance $L_{\mathrm{lk}\,1}$. The energy of the capacitor C_1 is transmitted through the ideal transformer and via the body diode D_{S6} of the switch S_6 to the high voltage side V_H with the capacitor C_3. While all switches are turned OFF, mode 2 ends. The equivalent circuit of mode 2 is shown as Fig. 4(b).

3) Mode 3 [t_2~t_3]

At the beginning of this mode at the time $t = t_2$, all switch signals are in OFF state. The parasitic capacitances C_{S1} and C_{S2} of the switches S_1 and S_2 storage energy until the switches S_1 and S_2 are in OFF state. The electric charges from the parasitic capacitances C_{S3} and C_{S4} of the switches S_3 and S_4 are extracted and have the efficacy of ZVS. The capacitor C_1 continuously conducts energy passes the ideal transformer to the high voltage side V_H with the capacitor C_3. The body diode D_{S6} of switch S_6 is conducting until the current is zero. While the switch signals v_{gs3} and v_{gs4} are in ON state, mode 3 ends. The equivalent circuit of mode 3 is shown as Fig. 4(c).

4) Mode 4 [t_3~t_4]

In mode 4 begins at the time $t = t_3$, the switch signals v_{gs1} and v_{gs2} are in OFF state and the switch signals v_{gs3} and v_{gs4} are in ON state, the low voltage side V_L and the inductor L_1 release energy to the capacitor C_1 via the switch S_3. The magnetizing inductance L_{m1} releases energy to the capacitor C_3 through the ideal transformer and via the body diode D_{S5} of the switch S_5. The leakage inductance $L_{\mathrm{lk}\,1}$ releases energy to the capacitor C_2 until the current is zero, and mode 4 ends. The equivalent circuit of mode 4 is shown as Fig. 4(d).

5) Mode 5 [t_4~t_5]

At time $t = t_4$, the switch signals are the same as the previous mode in this time interval. The energy of the capacitor C_1 is stored continuously by the low voltage side V_L and the inductor L_1. The capacitor C_3 stores energy by the magnetizing inductance L_{m1} through the ideal transformer and via the body

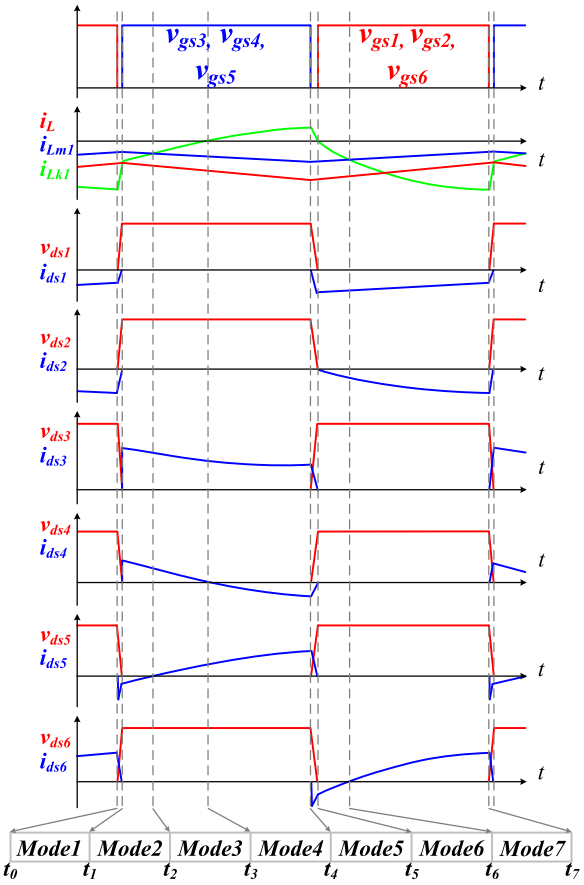

Fig. 5. Key waveforms of proposed topology in the step-down mode.

diode D_{S5} of the switch S_5. The capacitor C_2 releases energy to leakage inductance $L_{\mathrm{lk}\,1}$ until all switches are turned OFF, and mode 5 is end. The equivalent circuit of mode 5 is shown as Fig. 4(e).

B. Step-Down Mode

In step-down mode, the operating signal is also a complementary signal composed of two sets of signals, v_{gs1}, v_{gs2}, and v_{gs6} are one set of signals, and v_{gs3}, v_{gs4}, and v_{gs5} are another set of signals. The key waveforms of the proposed topology in step-down mode are shown in Fig. 5. It can be divided into seven operation modes in an operating cycle, as shown in Fig. 6(a)–(g).

6) Mode 1 [t_0~t_1]

Mode 1 begins at the time $t = t_0$ and all switch signals are in OFF state. The high voltage side V_H charges the parasitic capacitance C_{S6} to make the switch S_6 turned OFF. At this time, a negative current draws the electric charges on the parasitic capacitance C_{S5} of the switch S_5 to achieve ZVS. The energy of capacitor C_1 is stored by the leakage inductance $L_{\mathrm{lk}\,1}$. The inductor L_1 releases energy to the low voltage side V_L. While the switch signals v_{gs3}, v_{gs4} and v_{gs5} are in ON state, Mode 1 ends. The equivalent circuit of mode 1 is shown as Fig. 6(a).

7) Mode 2 [t_1~t_2]

The switch signals v_{gs1}, v_{gs2}, and v_{gs6} are in OFF state and the switch signals v_{gs3}, v_{gs4}, and v_{gs5} are in ON state, while the

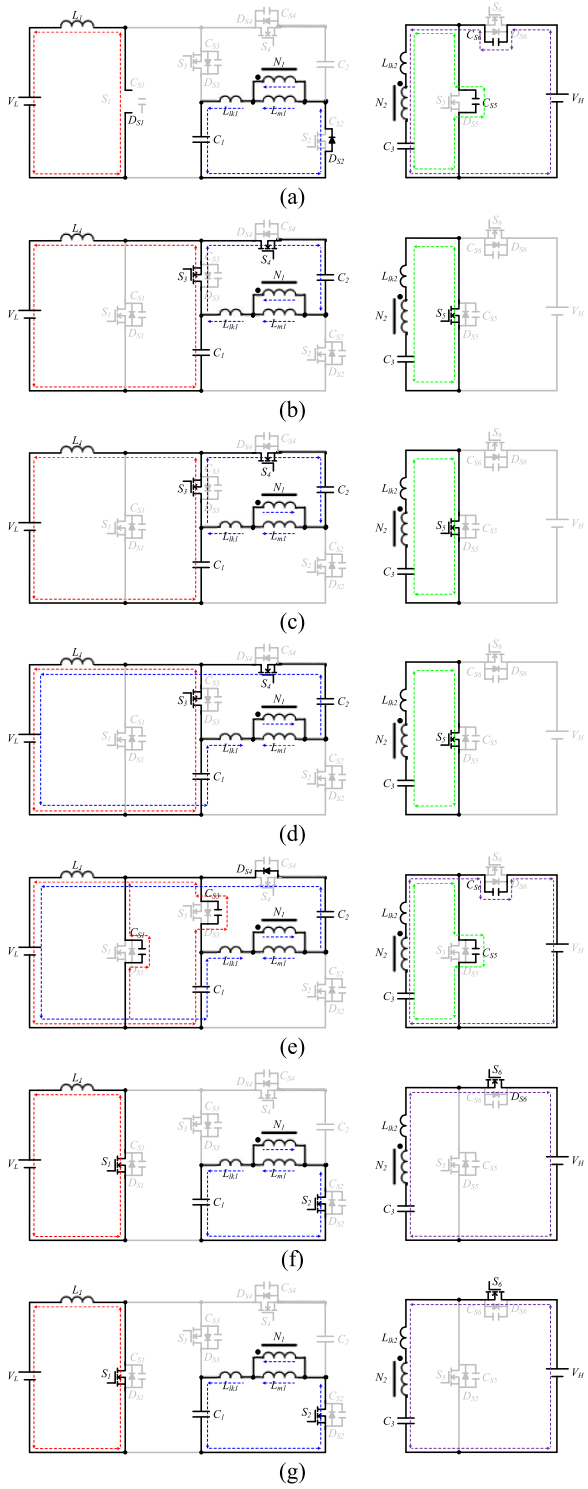

Fig. 6. Equivalent circuit diagram of in the step-down mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7.

interval begins at the time $t = t_1$. The leakage inductance $L_{\mathrm{lk}\,2}$ releases energy to the capacitor C_3 until the current of leakage inductance $L_{\mathrm{lk}\,2}$ is zero. The capacitor C_2 releases energy to the magnetizing inductance L_{m1} and the leakage inductance $L_{\mathrm{lk}\,1}$. The capacitor C_1 releases energy to the inductor L_1 and the low

voltage side V_L, mode 2 ends. The equivalent circuit of mode 2 is shown as Fig. 6(b).

8) Mode 3 [t_2~t_3]

At the beginning of this mode at the time $t = t_2$, the switch signals are the same as the previous mode. The capacitor C_3

Releases energy to the magnetizing inductance L_{m1} via the ideal transformer. The energy of inductor L_1 and the low voltage side V_L is stored by the capacitor C_1. While the current of the leakage inductance $L_{\mathrm{lk}\,1}$ is zero, mode 3 ends. The equivalent circuit of mode 3 is shown as Fig. 6(c).

9) Mode 4 [t_3~t_4]

At time $t = t_3$, the switch signals are also the same as the previous mode in this interval. The energy of magnetizing inductance L_{m1} is stored by the capacitor C_3 via the ideal transformer continuously. The capacitor C_2 is in energy storage state, the capacitor C_1 also releases energy to the inductor L_1 and the low voltage side V_L. While all switches are turned OFF, mode 4 ends. And, the equivalent circuit of mode 4 is shown as Fig. 6(d).

10) Mode 5 [t_4~t_5]

In mode 5 begins at the time $t = t_4$, all switch signals are in OFF state. The leakage inductance $L_{\mathrm{lk}\,2}$ draws off the electric charges from the parasitic capacitor C_{S6} of the switch S_6 to achieve ZVS. The leakage inductance $L_{\mathrm{lk}\,2}$ also charges the parasitic capacitance of the switch S_5 until the switch S_5 is turned OFF. When the parasitic capacitors C_{S3} and C_{S4} are fully charged, the switches S_3 and S_4 are turned OFF. The inductor L_1 begins to release energy to the low voltage side V_L, mode 5 ends. The equivalent circuit of mode 5 is shown as Fig. 6(e).

11) Mode 6 [t_5~t_6]

At time $t = t_5$, the switch signals v_{gs1}, $v_{gs2,}$ and v_{gs6} are in ON state and the switch signals v_{gs3}, v_{gs4}, and v_{gs5} are in OFF state. The current of the leakage inductance $L_{\mathrm{lk}\,2}$ is continuously recharged to the high voltage side V_H until the current is zero. The magnetizing inductance L_{m1} releases energy to the capacitor C_1. The inductor L_1 continues to release energy to the low voltage side V_L, mode 6 ends. The equivalent circuit of mode 6 is shown as Fig. 6(f).

12) Mode 7 [t_6~t_7]

At the beginning of this mode at the time $t = t_6$, all switch signals are the same as the previous mode. The high voltage side V_H starts to release energy to the capacitor C_3 and it also releases energy to the capacitor C_1 via the ideal transformer. The magnetizing inductance L_{m1} releases energy to capacitor C_1, too. The low voltage side V_L is in energy storage state by the inductor L_1. While all switch signals are in OFF state, mode 7 ends. The equivalent circuit of mode 7 is shown as Fig. 6(g).

III. Steady-State Analysis

While analyzing the circuit, the analysis is operated in CCM. The switching period is T_S, the signals v_{gs1} and v_{gs2} are turned ON for time D_1T_S and turned OFF for time $(1 - D_1)T_S$, in step-up mode. In step-down mode, the signals v_{gs1}, v_{gs2} and v_{gs6} are turned ON for time D_6T_S and turned OFF for time $(1 - D_6)T_S$, the while switching period is T_S. The following assumptions need to be made when the proposed topology is analyzed.

1) All components are ideal, the internal resistance and parasitic effects are neglected.

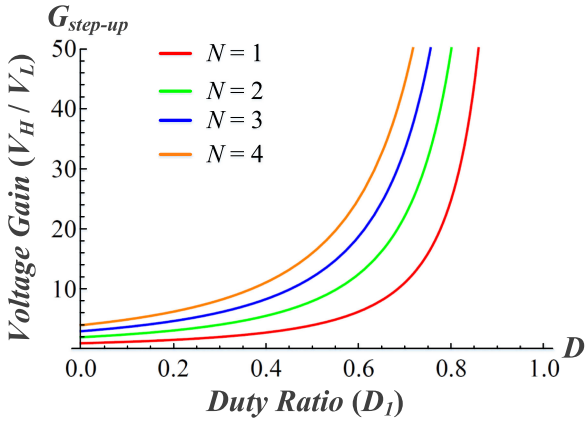

Fig. 7. Voltage gain of the proposed topology in the step-up mode.

2) The capacitance of all capacitors is infinite, making the voltage of capacitors constant.
3) The leakage inductance of the transformer is ignored.
4) The circuit operation modes are ignored that occur in a short time.
5) For easier calculation, the ideal transformer is represented by $N = \frac{N_2}{N_1}$, and N is defined as transformer turns ratio.

A. Step-Up Mode

1) Voltage Gain Analysis: In order to derive the relationship between V_H and V_L, the relationship between V_{C1}, V_{C2}, V_{C3}, and V_L must be derived, respectively. The voltage of C_1 can be obtained as

$$V_{C1} = \frac{1}{1 - D_1} V_L. \tag{1}$$

The voltage of C_3 can be obtained as

$$V_{C3} = \frac{ND_1}{1 - D_1} V_{C1} = \frac{ND_1}{(1 - D_1)^2} V_L. \tag{2}$$

Referring to the step-up mode of mode 5, the leakage inductance is ignored in the equivalent circuit. The voltage of V_{C2} can be written by

$$V_{C2} = \frac{1}{N} V_{C3} = \frac{D_1}{(1 - D_1)^2} V_L. \tag{3}$$

V_H is the sum of the voltage induced by V_{C1} via the turns ratio N and V_{C3}, it can be expressed as

$$V_H = NV_{C1} + V_{C3}. \tag{4}$$

The voltage gain in step-up mode $G_{step\text{-}up}$ can be derived as

$$G_{\mathrm{step-up}} = \frac{V_H}{V_L} = \frac{N}{(1 - D_1)^2}. \tag{5}$$

According to (5), the relationship between the voltage gain in step-up mode $G_{\mathrm{step\text{-}up}}$, the duty ratio D_1 and the turns ratio N is shown in Fig. 7.

2) Voltage Stress Analysis of Components: According to the equivalent circuit during D_1T_S, the voltage across S_3 is V_{C1}, and the voltage across S_4 is the sum of V_{C1} and V_{C2}. The voltage

stress on S_5 is V_H. The voltage stress on S_3, S_4 and S_5 can be expressed as

$$V_{S3,\text{stress}} = V_{C1} = \frac{1}{1-D_1}V_L = \frac{1-D_1}{N}V_H \tag{6}$$

$$V_{S4,\text{stress}} = V_{C1} + V_{C2} = \frac{1}{(1-D_1)^2}V_L = \frac{1}{N}V_H \tag{7}$$

$$V_{S5,\text{stress}} = V_H = \frac{N}{(1-D_1)^2}V_L. \tag{8}$$

On the basis of the equivalent circuit during $(1-D_1)T_S$. The voltage stress on S_1 is V_{C1}. The voltage across S_2 is the sum of V_{C1} and the voltage induced by the turns ratio N from V_{C3}. And the voltage across S_6 is V_H. The voltage across S_1, S_2 and S_6 can be determined as

$$V_{S1,\text{stress}} = V_{C1} = \frac{1}{1-D_1}V_L = \frac{1-D_1}{N}V_H \tag{9}$$

$$V_{S2,\text{stress}} = V_{C1} + \frac{V_{C3}}{N} = \frac{1}{(1-D_1)^2}V_L = \frac{1}{N}V_H \tag{10}$$

$$V_{S6,\text{stress}} = V_H = \frac{N}{(1-D_1)^2}V_L. \tag{11}$$

3) Magnetic Components Design: The magnetic components of the proposed topology are designed in CCM, the maximum current of L_1 and L_{m1} can be written by

$$i_{L1,\max} = I_{L1,\text{avg}} + \frac{\Delta i_{L1}}{2} \tag{12}$$

$$i_{Lm1,\max} = I_{Lm1,\text{avg}} + \frac{\Delta i_{Lm1}}{2}. \tag{13}$$

The minimum current of L_1 and L_{m1} can be given by

$$i_{L1,\min} = I_{L1,\text{avg}} - \frac{\Delta i_{L1}}{2} \tag{14}$$

$$i_{Lm1,\min} = I_{Lm1,\text{avg}} - \frac{\Delta i_{Lm1}}{2}. \tag{15}$$

The current Δi_{L1} and $I_{L1,\text{avg}}$ can be determined by

$$\Delta i_{L1} = \frac{v_{L1}}{L_1}D_1T_S = \frac{(1-D_1)^2D_1}{L_1f_sN}V_H \tag{16}$$

$$I_{L1,\text{avg}} = I_L = \frac{N}{(1-D_1)^2}I_H. \tag{17}$$

The current Δi_{Lm1} and $I_{Lm1,\text{avg}}$ can be determined by

$$\Delta i_{Lm1} = \frac{v_{Lm1}}{L_{m1}}D_1T_S = \frac{(1-D_1)D_1}{L_{m1}f_sN}V_H \tag{18}$$

$$\Delta i_{Lm1} = \frac{v_{Lm1}}{L_{m1}}D_1T_S = \frac{(1-D_1)D_1}{L_{m1}f_sN}V_H. \tag{19}$$

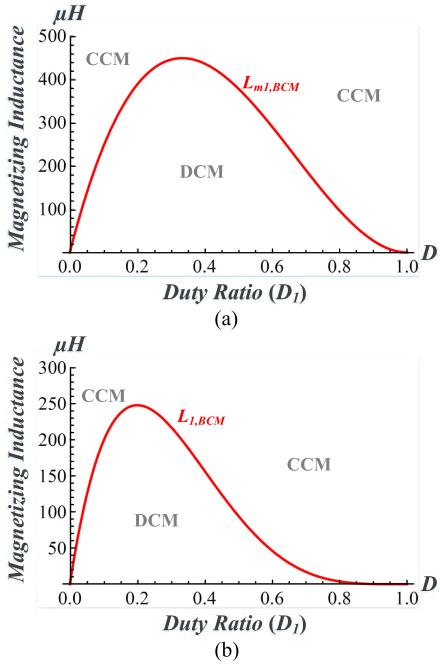

Fig. 8. (a) Curve of $L_{1,\text{BCM}}$ in the step-up mode. (b) Curve of $L_{m1,\text{BCM}}$ in the step-up mode.

Because the magnetic components are designed in CCM, the currents $i_{L1,\min}$ and $i_{Lm1,\min}$ must be greater than zero. While the magnetic components are operated in boundary conduction mode (BCM), the current $i_{L1,\min}$ and $i_{Lm1,\min}$ is equal to zero. Substituting (16) and (17) into (14), the currents $i_{L1,\min}$ can be expressed as

$$I_{L1,\min} = 0 = \frac{N}{(1-D_1)^2}I_H - \frac{(1-D_1)^2D_1}{2L_1f_sN}V_H. \tag{20}$$

Substituting (18) and (19) into (15), the currents $i_{Lm1,\min}$ can be obtained as

$$I_{Lm1,\min} = 0 = \frac{N}{1-D_1}I_H - \frac{(1-D_1)D_1}{2L_{m1}f_sN}V_H. \tag{21}$$

Sorting out (20) and (21), the formulas that L_1 and L_{m1} operated in BCM can be determined by

$$L_{L1,\text{BCM}} = \frac{(1-D_1)^4D_1}{2f_sN^2}\frac{V_H}{I_{H,\text{BCM}}} \tag{22}$$

$$L_{m1,\text{BCM}} = \frac{(1-D_1)^2D_1}{2f_sN^2}\frac{V_H}{I_{H,\text{BCM}}}. \tag{23}$$

There are several design parameters of magnetic components in step-up mode. For instance, the turns ratio N is 2.1, the switching frequency f_s is 40kHz, the high voltage side V_H is 400 V and the current of high voltage side I_H is 0.375 A.

Substituting the above parameters into the (22), the curve of L_1 operated in BCM can be plotted, as shown in Fig. 8(a). When the value of L_1 is greater than the curve in BCM, L_1 is operated in CCM; it is operated in DCM conversely.

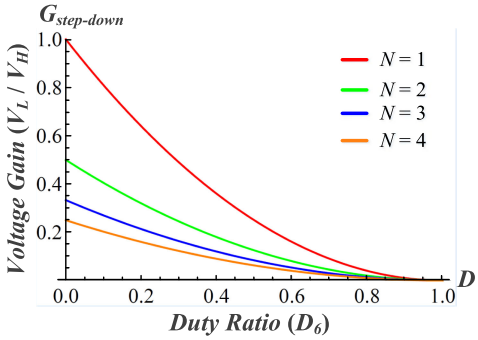

Fig. 9. Voltage gain of the proposed topology in the step-down mode.

Similarly, substituting the above parameters into the (23), the curve of L_{m1} operated in BCM can be plotted, as shown in Fig. 8(b). When the value of L_{m1} is greater than the curve in BCM, L_1 is operated in CCM; otherwise it is operated in DCM.

B. Step-Down Mode

1) Voltage Gain Analysis: To derive the relationship between V_L and V_H, the voltage of C_1 and C_3 can be obtained as

$$V_{C3} = D_6 V_H \tag{24}$$

$$V_{C1} = \frac{1-D_6}{ND_6} V_{C3} = \frac{1-D_6}{N} V_H. \tag{25}$$

The relationship between V_{C1} and V_L can be written by

$$V_{C1} = \frac{1}{1-D_6} V_L. \tag{26}$$

Referring to the step-down mode of mode 4, the leakage inductance is ignored in the equivalent circuit. The voltage of V_{C2} can be written by

$$V_{C2} = \frac{1}{N} V_{C3} = \frac{D_6}{N} V_H. \tag{27}$$

Finally, substituting (25) into (26), the voltage gain in step-down mode $G_{\text{step-down}}$ can be derived as

$$G_{\text{step-down}} = \frac{V_L}{V_H} = \frac{(1-D_6)^2}{N}. \tag{28}$$

According to (28), the relationship between the voltage gain in step-down mode $G_{\text{step-down}}$, the duty ratio D_6 and the turns ratio N is shown in Fig. 9.

2) Voltage Stress Analysis of Components: On the basis of the equivalent circuit during D_6T_S. The voltage stress on S_3 is V_{C1}, and the voltage across S_4 is V_{C2}. V_H is the voltage stress on S_5. The voltage across S_3, S_4, and S_5 can be obtained as

$$V_{S3,\text{stress}} = V_{C1} = \frac{1-D_6}{N} V_H = \frac{1}{1-D_6} V_L \tag{29}$$

$$V_{S4,\text{stress}} = V_{C2} = \frac{D_6}{N} V_H = \frac{D_6}{(1-D_6)^2} V_L \tag{30}$$

$$V_{S5,\text{stress}} = V_H = \frac{N}{(1-D_6)^2} V_L. \tag{31}$$

According to the equivalent circuit during (1-D_6)T_S. The voltage across S_1 is V_{C1}. The voltage stress on S_2 is the sum of V_{C1} and the voltage induced by the turns ratio N from V_{C3}. The voltage across S_6 is V_H. The voltage across S_1, S_2 and S_6 can be expressed as

$$V_{S1,\text{stress}} = V_{C1} = \frac{1-D_6}{N} V_H = \frac{1}{1-D_6} V_L. \tag{32}$$

$$V_{S2,\text{stress}} = V_{C1} + V_{C2} = \frac{1}{N} V_H = \frac{1}{(1-D_6)^2} V_L \tag{33}$$

$$V_{S6,\text{stress}} = V_H = \frac{N}{(1-D_6)^2} V_L. \tag{34}$$

3) Magnetic Components Design: The maximum current of L_1 and L_{m1} can be given by

$$i_{L1,\max} = I_{L1,\text{avg}} + \frac{\Delta i_{L1}}{2} \tag{35}$$

$$i_{Lm1,\max} = I_{Lm1,\text{avg}} + \frac{\Delta i_{Lm1}}{2}. \tag{36}$$

The minimum current of L_1 and L_{m1} can be written by

$$i_{L1,\min} = I_{L1,\text{avg}} - \frac{\Delta i_{L1}}{2} \tag{37}$$

$$i_{Lm1,\min} = I_{Lm1,\text{avg}} - \frac{\Delta i_{Lm1}}{2}. \tag{38}$$

The current Δi_{L1} and $I_{L1,\text{avg}}$ can be determined by

$$\Delta i_{L1} = \frac{v_{L1}}{L_1} D_6 T_S = \frac{D_6}{L_1 f_s} V_L \tag{39}$$

$$I_{L1,\text{avg}} = I_L. \tag{40}$$

The current Δi_{Lm1} and $I_{Lm1,\text{avg}}$ can be determined by

$$\Delta i_{Lm1} = \frac{v_{Lm1}}{L_{m1}} D_6 T_S = \frac{D_6}{(1-D_6) L_{m1} f_s} V_L \tag{41}$$

$$I_{Lm1,\text{avg}} = (1-D_6) I_L. \tag{42}$$

The magnetic components are operated in BCM, the current $i_{L1,\min}$ and $i_{Lm1,\min}$ is equal to zero. Substituting (39) and (40) into (37), the currents $i_{L1,\min}$ can be obtained as

$$I_{L1,\min} = 0 = I_L - \frac{D_6}{2L_1 f_s} V_L. \tag{43}$$

Substituting (41) and (42) into (38), the currents $i_{Lm1,\min}$ can be expressed as

$$I_{Lm1,\min} = 0 = (1-D_6) I_L - \frac{D_6}{2(1-D_6) L_{m1} f_s} V_L. \tag{44}$$

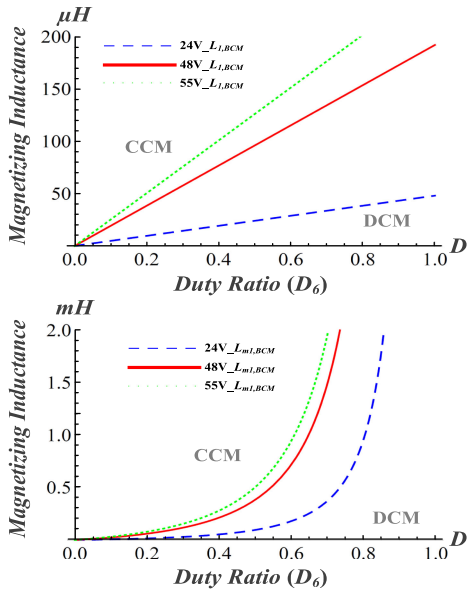

Fig. 10. (a) Curve of $L_{1,\mathrm{BCM}}$ in the step-down mode. (b) Curve of $L_{m1,\mathrm{BCM}}$ in the step-down mode.

While (3.59) and (3.60) are sorted out, the formulas that L_1 and L_{m1} operated in BCM can be expressed as

$$L_{1,\mathrm{BCM}} = \frac{D_6}{2f_s}\frac{V_L}{I_{L,\mathrm{BCM}}} \tag{45}$$

and

$$L_{m1,\mathrm{BCM}} = \frac{D_6}{2(1-D_6)^2 f_s}\frac{V_L}{I_{L,\mathrm{BCM}}}. \tag{46}$$

There are several design parameters of magnetic components in step-down mode. For instance, the switching frequency f_s is 40 kHz, the low voltage side V_L is 24, 48, and 55 V and the current of low voltage side I_L is 6.25, 3.125, and 2.727 A, respectively.

Substituting the above parameters into the (45), the curve of L_1 operated in BCM can be plotted, as shown in Fig. 10(a). While the value of L_1 is greater than the curve in BCM, L_1 is operated in CCM; otherwise it is operated in DCM.

Similarly, substituting the above parameters into the (46), the curve of L_{m1} can be plotted in BCM, as shown in Fig. 10(b). When the value of L_{m1} is greater than the curve in BCM, L_1 is operated in CCM; it is operated in DCM contrarily.

C. Soft Switching Condition

The ZVS is the technique to achieve soft-switching for both the main and the clamp switches, which can avoid the energy losses of parallel capacitors and reduce the energy losses of switches.

In order to achieve the ZVS of the main switch, the energy of the leakage inductance should be larger than the energy in the parallel capacitor while the switch is in OFF state. The relationship can be express as

$$\frac{1}{2}L_{lk}{I_{lk}}^2 \geq \frac{1}{2}C_{\mathrm{oss}}{V_{\mathrm{SW,stress}}}^2. \tag{47}$$

TABLE I
ELECTRICAL SPECIFICATIONS OF THE PROPOSED TOPOLOGY

Parameter	Specification
High-side power P_H	500 W
Low-side power P_L	500 W
High-side voltage V_H	400 V
Low-side voltage V_L	24 V ~ 55 V
Switching frequency f_s	40 kHz
Power switches S_1 and S_3	IRFP4568PbF
Power switches S_2 and S_4	IXFH170N25X3
Power switches S_5 and S_6	IXFH50N50P3
Inductor L_1	100 μH
Magnetizing inductance L_{m1}	390 μH
Leakage inductance L_{lk1}	4.85 μH
Leakage inductance L_{lk2}	20.7 μH
Capacitor C_1	100 μF
Capacitor C_2	47 μF
Capacitor C_3	10 μF
Turns ratio N	2.1

If the switch achieves the ZVS effect, the condition of (47) must be satisfied, and the dead time must be larger than a quarter of the resonance period, it can be obtained as

$$\mathrm{Deadtime} \geq \frac{2\pi}{4}\sqrt{C_{\mathrm{oss}}L_{lk}}. \tag{48}$$

According to datasheets of the switches in proposed topology, the capacity in parasitic capacitances of switches C_{S1} and C_{S3} is 997 pF, the capacity of C_{S2} and C_{S4} is 2.3 nF, and the capacity of C_{S5} and C_{S6} is 540 pF.

In the step-up mode, the switches S_2 and S_4 have ZVS, and the switches S_5 and S_6 have ZVS in step-down mode. In order to calculate the dead time, the capacity in parasitic capacitances of switches is defined as 2.3 nF and 540 pF in step-up mode and step-down mode, respectively. According to (48), the dead time in step-up mode and step-down mode is around 168 and 163 ns, respectively.

IV. DESIGN AND EXPERIENTIAL RESULT

The voltage of battery is commonly used in the market is around 48 V, and the voltage of dc bus is about 400 V. Therefore, the main design parameters are that the low-side voltage V_L is 48 V and the high-side voltage V_H is 400 V. The magnetic components of the proposed topology are designed in the step-up mode. The magnetic components are designed at 30% of full load in BCM, where I_H is 0.375 A. According to (37), the current $i_{L1,\mathrm{min}}$ must be zero in BCM, and the current $I_{L1,\mathrm{avg}}$ is 3.126 A. The current Δi_{L1} is about 6.25 A.

According to the voltage stress on each component, the components can be selected appropriately. Moreover, the electrical specifications of the proposed topology are given in Table I. The prototype of the proposed bidirectional isolated dc–dc converter is shown in Fig. 11, the microcontroller is dsPIC30F4011and the type of controller is PI controller.

In Fig. 12(a)–(f), there are key waveforms for measurements of the low voltage side at 48 V in step-up mode at full load sequentially. In Fig. 12(a), there are the complementary signals of v_{gs1} and v_{gs3} and the measured waveforms of the inductor L_1

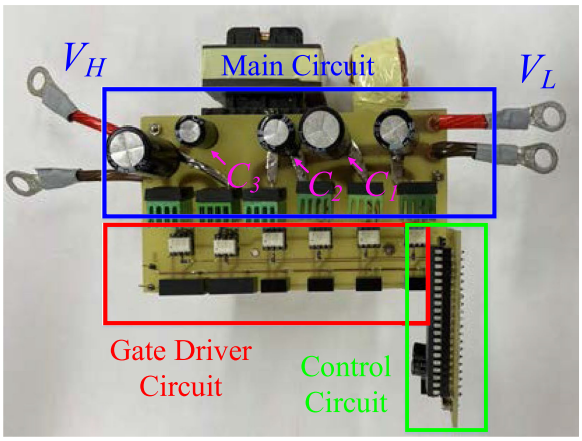

Fig. 11. Photograph of the proposed topology.

and the leakage inductance $L_{\mathrm{lk}\,1}$. The measured waveforms of the v_{ds} and i_{ds} of the switches S_1 and S_3 are shown in Fig. 12(b). In Fig. 12(c), there are the measured waveforms of the v_{ds} and i_{ds} of switches S_2 and S_4. The measured current waveforms i_{ds2} and i_{ds4} show that the switches S_2 and S_4 have ZVS in the step-up mode. There are the measured waveforms of the v_{ds} and i_{ds} of switches S_5 and S_6, as shown in Fig. 12(d). Fig. 12(e) is the measured waveforms of the voltage of the capacitors C_1, C_2, and C_3 and V_H of the proposed topology. In order to show achieved soft switching condition, the measured waveforms in one switching cycle of the v_{ds} and i_{ds} of the switches S_2 and S_4 are shown in Fig. 12(f).

The key waveforms for measurements of the low voltage side at 48 V in step-down mode at full load sequentially are shown in Fig. 13(a)–(e). In Fig. 13(a), there are the complementary signals of v_{gs1} and v_{gs3} and the measured waveforms of the inductor L_1 and the leakage inductance $L_{\mathrm{lk}\,1}$. Fig. 13(b) are the measured waveforms of the v_{ds} and i_{ds} of switches S_1 and S_3. There are the measured waveforms of the v_{ds} and i_{ds} of switches S_2 and S_4, as shown in Fig. 13(c). In Fig. 13(d), there are the measured waveforms of the v_{ds} and i_{ds} of switches S_5 and S_6. The switches S_5 and S_6 have ZVS. Fig. 13(e) is the measured waveforms of the voltage of the capacitors C_1, C_2, C_3, and V_L of the proposed topology and the low voltage side V_L. During measurement, the low voltage side V_L is maintained 48 V sequentially. In Fig. 13(f), the measured waveforms in one switching cycle of the v_{ds} and i_{ds} of the switches S_5 and S_6 are presented to show achieved soft switching condition.

Fig. 14 shows the conversion efficiency of the proposed topology in step-up mode. The highest conversion efficiency appears to be 94.2% at 400 W and the conversion efficiency is 93% at full load, while the low voltage side is 24 V. When the low voltage side is 48 V, the highest conversion efficiency point is 95.6% at 400 W; the conversion efficiency is 95.4% at full load. The highest efficiency point is 400 W the conversion efficiency 96.9%, and the full load efficiency is 95.4%, when the low voltage side is 55 V. In step-up mode, the duty ratios are 0.65, 0.5 and 0.47 while the low-side voltage of the proposed topology is 24, 48, and 55 V.

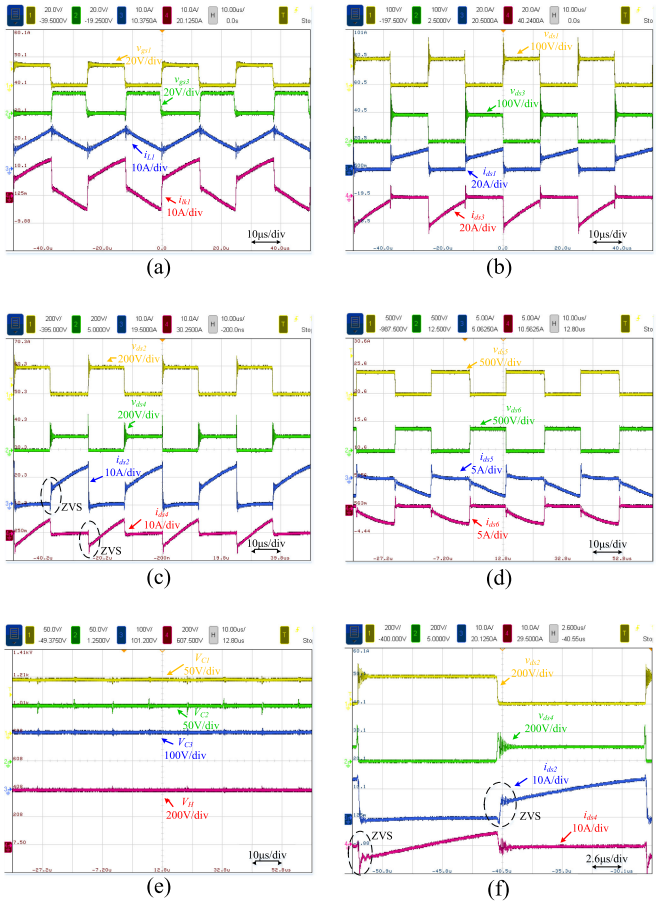

Fig. 12. Experimental results of proposed topology in the step-up mode at full load of 500 W, when V_L is 48 V. (a) Waveforms of v_{gs1}, v_{gs3}, i_{L1} and $i_{\mathrm{lk}\,1}$. (b) v_{ds} and i_{ds} of S_1 and S_3. (c) v_{ds} and i_{ds} of S_2 and S_4, (d) v_{ds} and i_{ds} of S_5 and S_6. (e) Voltage of C_1, C_2, C_3, and V_H. (f) v_{ds} and i_{ds} of S_2 and S_4 in one switching cycle.

The conversion efficiency of the proposed topology in the step-down mode is shown in Fig. 15. When the low voltage side is 24 V, the highest conversion efficiency point is 92.6% at 400 W and full load. The highest conversion efficiency point appears to be 94.2% at 300 and 400 W and the conversion efficiency is 94.1% at full load, while the low voltage side is 48 V. When the low voltage side is 55 V, the highest conversion efficiency point is 94.5% at 300 W; the conversion efficiency is 93.8% at full load. While the low-side voltage of the proposed topology is 24, 48, and 55 V, the duty ratios are 0.6, 0.45 and 0.42 in the step-down mode.

In Fig. 16(a) and (b), the V_L is 48 V. The step variation of output load of proposed topology in step-up mode and step-down mode, while the output load is step changed between half load and full load. It can be seen that the output voltage (V_H/V_L) is very stable and is not greatly affected by load changes. Fig. 17 shows the losses break down analysis of the proposed topology while V_L is 48 V in step-up mode and step-down mode, and the output load operated under in full load. It can be seen from the figure that the power loss of inductors and capacitors accounts for more than 60%.

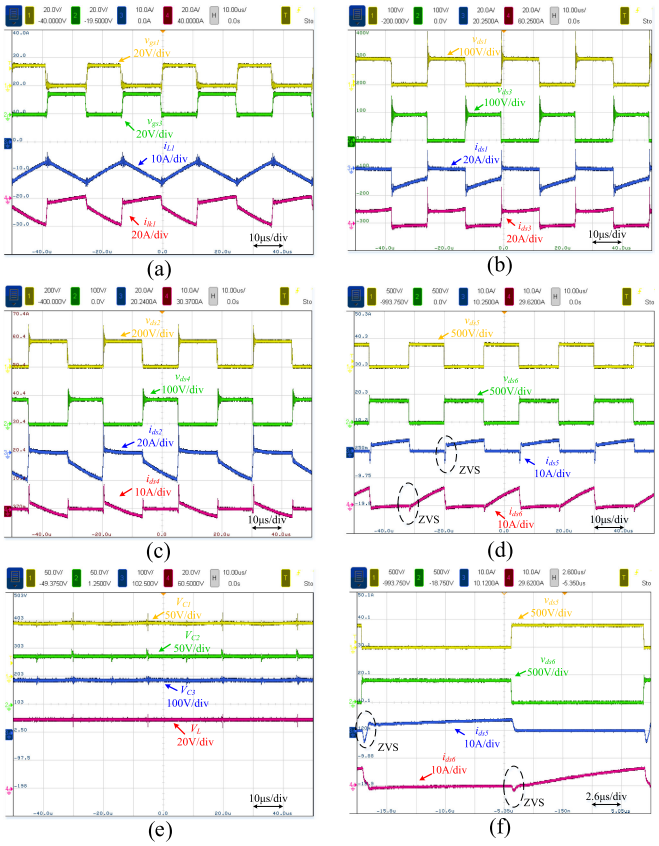

Fig. 13. Experimental results of proposed topology in the step-down mode at full load of 500 W, when V_L is 48 V. (a) Waveforms of v_{gs1}, v_{gs3}, i_{L1}, and $i_{\mathrm{lk}\,1}$. (b) v_{ds} and i_{ds} of S_1 and S_3. (c) v_{ds} and i_{ds} of S_2 and S_4. (d) v_{ds} and i_{ds} of S_5 and S_6. (e) Voltage of C_1, C_2, C_3, and V_L. (f) v_{ds} and i_{ds} of S_5 and S_6 in one switching cycle.

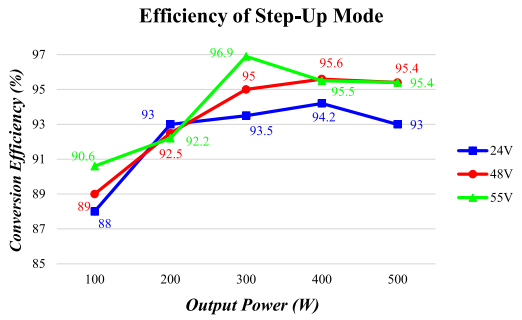

Fig. 14. Efficiency curves of proposed topology in the step-up mode.

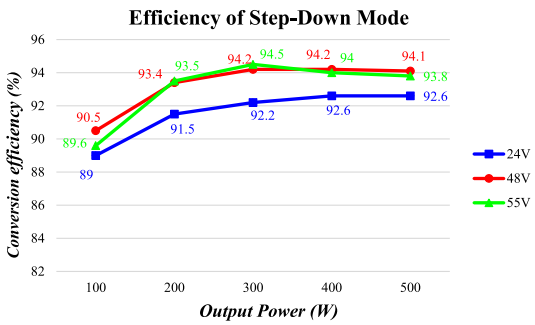

Fig. 15. Efficiency curves of proposed topology in the step-down mode.

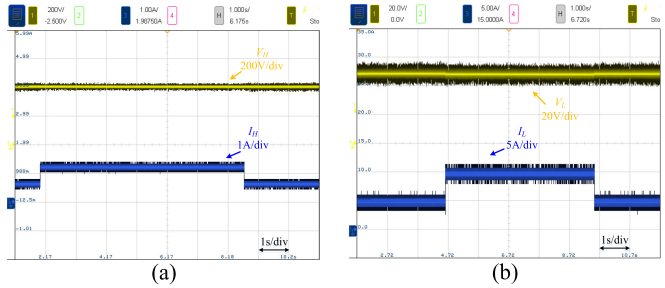

Fig. 16. Step variation of output load of the proposed topology. (a) Step-up mode. (b) Step-down mode.

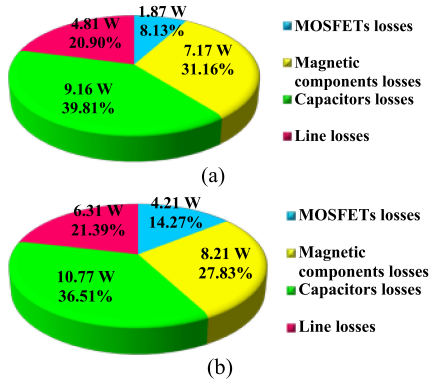

Fig. 17. Losses break down analysis of the proposed topology. (a) Step-up mode. (b) Step-down mode.

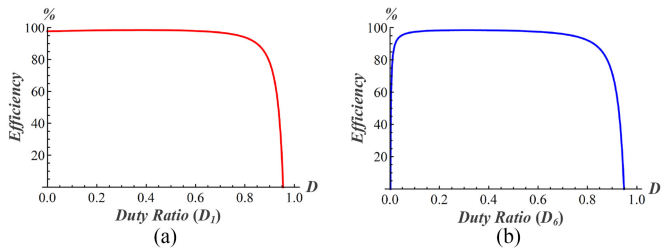

Fig. 18. Efficiency curve of the proposed topology versus duty ratio. (a) Step-up mode. (b) Step-down mode.

In Fig. 18(a) and (b), the efficiency curve of the proposed topology versus duty ratio in the step-up mode and step-down mode, while V_L is 48 V. The resistances of the magnetic components are 30 mΩ; the equivalent series resistances of the capacitors are 50 mΩ; the $R_{ds(\mathrm{on})}$ of S_1 and S_3 are 4.8 mΩ, S_2 and S_4 are 7.4 mΩ, and S_5 and S_6 are 125 mΩ and the body diodes of switches are 1 V.

In order to verify the performance and understand the advantages and disadvantages of the proposed topology. There are the comparisons with different novel bidirectional converters in terms of component counts, cost, complexity of PWM signals, current ripple, etc. In Table II, the comparison with other bidirectional converters [11], [16], [25], [32], and [34] are summarized. In Table III, the maximum voltage stress comparison with related literatures on bidirectional converter in high voltage side and low voltage side, respectively.

TABLE II
COMPARISON OF RELATED LITERATURES ON BIDIRECTIONAL CONVERTERS

	Converter in [11]	Converter in [16]	Converter in [25]	Converter in [32]	Converter in [34] FBDAB	Converter in [34] HBDAB	Proposed Converter
$G_{step\text{-}up}$ (V_H/V_L)	$\frac{2ND}{1-D}$	(49)	$\frac{N}{D}$	$\frac{N}{1-D}$	$\frac{N}{1-2D}$	$\frac{N}{2(1-2D)}$	$\frac{N}{(1-D_6)^2}$
$G_{step\text{-}down}$ (V_L/V_H)	$\frac{D}{2N(1-D)}$	(50)	$\frac{D}{N}$	$\frac{1-D}{N}$	$\frac{1-2D}{N}$	$\frac{2(1-2D)}{N}$	$\frac{(1-D_6)^2}{N}$
MOSFETs	4	8	6	8	8	4	6
Inductors	1	1	4	3	1	1	1
Transformers	2	1	1	1	1	1	1
Capacitors	4	1	4	3	1	5	3
Diodes	6	0	0	0	0	0	0
Cost	Normal	Low	High	High	High	High	Normal
PWM control signals	Normal	Normal	Complex	Normal	Complex	Complex	Normal
Current ripple of V_L	Large	Large	Normal	Small	Large	Large	Normal
Output power	400 W	1 kW	1 kW	260 W	1 kW	1 kW	500 W
Isolated	*Yes*	*Yes*	*Yes*	*Yes*	*Yes*	*Yes*	*Yes*

TABLE III
VOLTAGE STRESS COMPARISON OF RELATED LITERATURES ON BIDIRECTIONAL CONVERTERS

	Maximum voltage stress across switches on low voltage side V_L		Maximum voltage stress across switches on high voltage side V_H	
	In step-up mode	In step-down mode	In step-up mode	In step-down mode
Converter in [11]	$\frac{1}{2ND}V_H$	$\frac{1}{D}V_L$	$\frac{1}{2D}V_H$	$\frac{N}{D}V_L$
Converter in [25]	$\frac{D}{(1-D)N}V_H$	$\frac{1}{1-D}V_L$	V_H	$\frac{N}{D}V_L$
Converter in [32]	$\frac{1}{N}V_H$	$\frac{1}{1-D}V_L$	V_H	$\frac{N}{1-D}V_L$
Converter in [34] FBDAB	$\frac{1-2D}{N}V_H$	V_L	V_H	$\frac{N}{1-2D}V_L$
Converter in [34] HBDAB	$\frac{2(1-2D)}{N}V_H$	V_L	V_H	$\frac{N}{2(1-2D)}V_L$
Proposed Converter	$\frac{1}{N}V_H$	$\frac{1}{(1-D_6)^2}V_L$	V_H	$\frac{N}{(1-D_6)^2}V_L$

A novel bidirectional *LLC* resonant converter was proposed in [16]. The voltage gain in step-up mode of [16] can be express as

$$\frac{1}{\sqrt{\left(\frac{kx^2+x^2-1}{kx^2}\right)^2 - 2Q\tan\Phi\frac{(x^2-1)(kx^2+x^2-1)}{kx^3}+\frac{Q^2(x^2-1)^2}{\cos\Phi^2x^2}}}. \tag{49}$$

The voltage gain in step-down mode of [16] can be written by

$$\sqrt{\left(\frac{kx^2+x^2-1}{kx^2}\right)^2 - 2Q\tan\Phi\frac{(x^2-1)(kx^2+x^2-1)}{kx^3}+\frac{Q^2(x^2-1)^2}{\cos\Phi^2x^2}}. \tag{50}$$

In Fig. 19(a) and (b), the voltage gain of the proposed converter is higher which compared with other bidirectional converters in the step-up mode and step-down mode, respectively. The voltage gain in [34] is the highest, but the duty is limited. To be fair, the comparison under the case of turns ratio $N = 2.1$.

There are the comparisons of conversion efficiency about the proposed topology with the topology proposed in [11], [16], [25], [32], and [34] in step-up mode and step-down mode, respectively, as shown in Figs. 20 and 21. In order to make the voltage gain of the proposed topology close to the references,

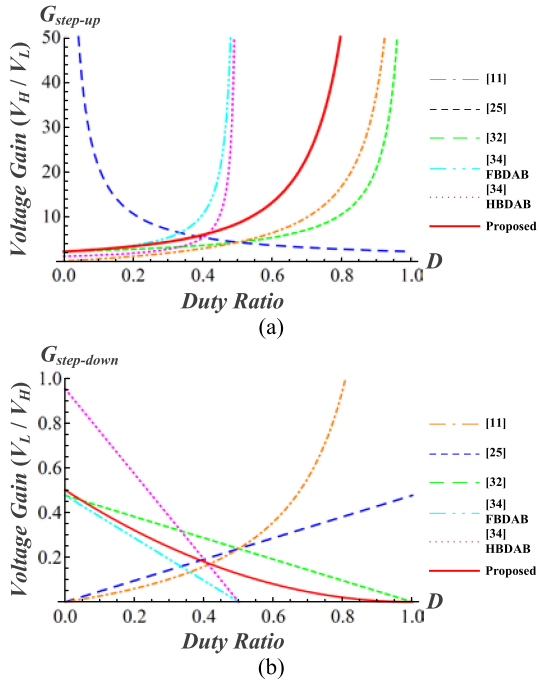

Fig. 19. Comparison of the voltage gain. (a) Step-up mode. (b) Step-down mode.

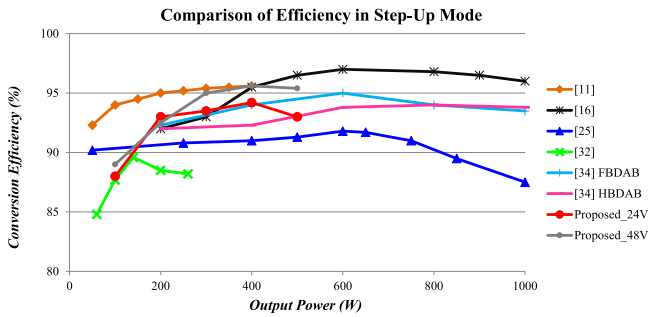

Fig. 20. Comparison of efficiency in the step-up mode.

which are compared, the conversion efficiency of low voltage side 24 V is adopted in the proposed topology. In terms of overall conversion efficiency, the best is in [16], the voltage conversion ratio, which was measured, is much lower than another related literatures. The related situations also occurred in [34], the conversion efficiency is higher, but the SiC MOSFETs switches were used, the component cost is quite high. While the low-voltage side of the proposed converter is 48 V, the highest point of the conversion efficiency measured in step-up mode is comparable to the topology in [11]. The conversion efficiency is not low in [25], but the components are increased. Compared with the proposed topology, it is slightly inferior. In [32], although all switches have ZVS in this topology. The conduction loss on components is increased because there are many components, and conversion efficiency is not high.

Overall, the conversion efficiency of the converter which was proposed in this article has a good performance in both step-up

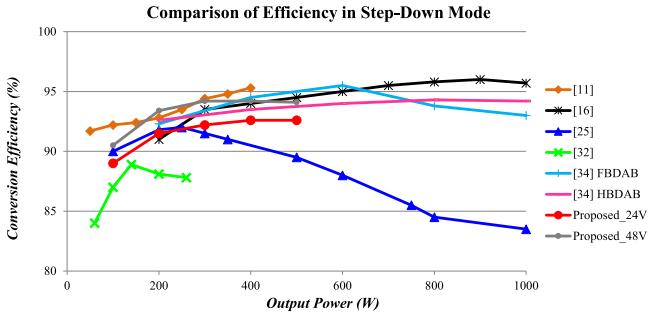

Fig. 21. Comparison of efficiency in the step-down mode.

mode and step-down mode, and the voltage gain of the proposed topology is also the highest.

V. Conclusion

A novel bidirectional isolated dc–dc converter with higher voltage gain and wide voltage range on the low side is proposed in this article. It has the following advantages: (1) higher voltage gain and galvanic isolation; it can be widely used in the battery of electric scooter; (2) it is not necessary to develop a specific converter for different voltage of battery specially; (3) it also increases the safety for use, which greatly reduces development and design costs; (4) the current ripple on the low voltage side of the topology in this article is continuous; it can reduce the burden of the battery during energy transmission in the application of electric vehicle batteries; and (5) high conversion efficiency, which can reduce the loss of power conversion.

The proposed topology in this article, which can be, confirmed the feasibility and correctness through theoretical analysis, and experimental results. When the low-side voltage is 24, 48, and 55 V, the maximum efficiency in step-up mode are 94.2%, 95.6%, and 96.9%, and the maximum efficiency are 92.6%, 94.2%, and 94.5% in the step-down mode, respectively.

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