A Dual Active Bridge Derived Hybrid Switched Capacitor Converter Based Two-Stage 48 V VRM

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***Abstract*—This article proposes a two-stage 48-V voltage regulator module using a hybrid switched-capacitor converter in the first stage. Apart from being compact in nature, this first-stage converter has several other advantages such as efficient regulation ability and hence scalability, inherent full/partial soft switching for most of the switches, reduced switch voltage and current stresses, and the possibility of wide range variable switching frequency operation. These combined features together help to obtain a flat high-efficiency curve for the first stage. The second-stage multiphase buck converter also exhibits flat high-efficiency characteristics through phase shedding. Steady-state circuit operation and analysis of the first-stage converter is presented in this article. An accurate discrete-time model of the first-stage converter is also developed. Thereafter, a design guideline for the two-stage converter is discussed. Finally, experimental results from an 80-W laboratory prototype show that the proposed converter possesses a relatively flat high-efficiency profile and exhibits a faster load transient response compared to that of the state-of-the-art solutions.**

***Index Terms*—48-V VRM, discrete-time model, hybrid switched-capacitor converter, switched-capacitor voltage divider.**

I. Introduction

EVOLUTION in different networking applications like cloud computing, Internet of Things (IoTs), video streaming activities, mobile Internet, etc. have imposed an ever increasing demand on the power consumption of the data centers [1]. The primary reason for this drastic rise in the electricity consumption is the use of power-hungry, high-performance multicore processor and memory loads to meet the required computational capability. This growing electricity demand with more stringent requirement on the efficiency and power density has entailed the transition from the 12- to 48-V server architecture (Fig. 1) in order to alleviate the excessive bus distribution losses, multiple conversion losses, cost, and size [2], [3]. However, this 48-V server architecture presents a significant challenge

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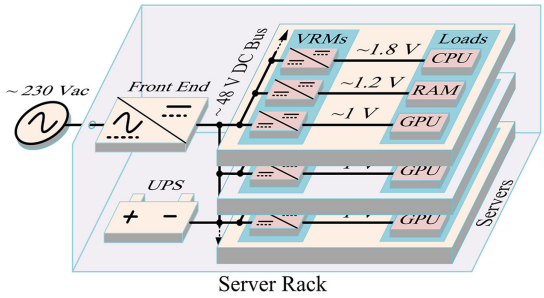

Fig. 1. Typical rack level power delivery system in a 48-V server architecture.

in the development of the 48-V input voltage regulator modules (VRMs) to supply those low voltage (0.5–1.85 V), high current (>200 A), and extremely dynamic CPU, GPU, and memory loads [4]. Therefore, the 48-V VRMs must have a large conversion ratio, must produce fast transient response, and should be compact and efficient. Since the servers frequently switch between light and heavy load conditions, the VRMs are desired to have a high flat efficiency profile over the entire load range, in order to maximize the overall energy efficiency of the data centers.

Several high conversion ratio converters have been developed recently for the 48-V VRM [5]–[24]. Among them, the transformer-based single-stage topologies [5]–[9] suffer from low power density because of the large size of the transformer core. The light-load efficiency is also compromised due to the significant amount of core losses. The coupled-inductor-based single-stage topologies [10], [11] also use large magnetics and require additional clamping circuits which limit their power density. The multiphase-buck-derived hybrid switched-capacitor converters [12]–[16] improve the power density by replacing the bulky magnetic elements with a more compact switched-capacitor voltage divider. However, the impracticality of phase shedding and inefficient discontinuous conduction mode (DCM) operation due to the interdependency of the phases degrade their light-load efficiency. Even though efficient, the 48/1 V sigma converter [17], [18] is unfavorable for handling a wide range variation in the input voltage. Moreover, the upper stage LLC resonant converter requires a large transformer.

The cascaded two-stage architecture has been a popular choice in many applications, due to its higher flexibility in the optimization of performance and volume [25], [26]. The first-stage converter, generally known as the bus converter, strives to maximize the power density and efficiency, whereas the second-stage is designed to meet the stringent transient performance requirement by the loads. The multiphase synchronous buck converter

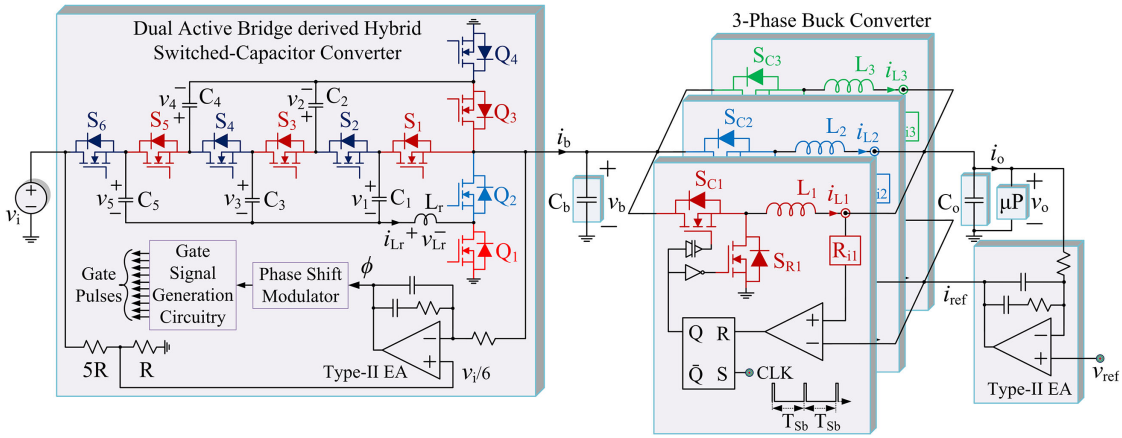

Fig. 2. Proposed two-stage 48-V VRM having a dual active bridge-derived hybrid switched-capacitor converter in cascade with a three-phase buck converter.

has been an attractive candidate for the second stage, due to its superior transient performance, flat high-efficiency profile, small filter capacitance requirement, and even heat distribution. However, a multiphase buck converter in the first-stage [19] incurs significant switching losses and also requires bigger inductors because of the high input and output voltages. The LLC resonant converter [20] in the first stage improves the efficiency through soft-switching, but still requires a bulky transformer even though the isolation is not required in this application [3], [27]. The hybrid switched-capacitor-based resonant converters called the switched tank converters [21], [22] reduce the volume up to certain extent. However, they exhibit high sensitivity toward component nonidealities, since their multiple L-C branches are expected to have equal resonant frequency for reliable operation. Being unregulated in nature, the LLC resonant, switched-tank, and the cascaded resonant switched-capacitor [23] converters are not easily scalable as they will not have any active control over the current distribution in different phases when used in multiphase configuration. The first market-available 48-V VRM made using a two-stage architecture by VICOR [24] also lacks scalability due to the unregulated second stage.

The main objective of this article is to propose a two-stage 48-V VRM (Fig. 2) using a regulated and compact first-stage converter. This is achieved by employing a dual active bridge (DAB)-derived hybrid switched-capacitor converter [28] in the first stage. This hybrid switched-capacitor converter requires only a small inductor and possesses very efficient load regulation ability unlike the LLC resonant [20], switched tank [21], [22], or the cascaded resonant converters [23]. This improves the power density and enables scalability. The quasi-trapezoidal inductor current waveforms of this converter reduce the root mean square (rms) and peak current stresses of the devices. Moreover, it can efficiently operate over a wide range variable switching frequency, which allows the reduction of the frequency to improve the light-load efficiency. Most of the switches here operate with full/partial zero voltage switching (ZVS). The device voltage ratings are also low, which allows the use of high-performance low-cost 30-V silicon devices. These features together help to obtain a flat high-efficiency profile even for the first stage. The second stage of this topology uses a multiphase buck converter in order to exploit its aforementioned favorable characteristics.

The rest of the article is organized as follows. Section II introduces the first-stage hybrid switched-capacitor converter along with its steady-state operation and analysis. The ZVS analysis of the first-stage converter is carried out in Section III. Section IV derives a discrete-time model of the first-stage converter along with SIMPLIS simulation verification. A light-load efficiency improvement technique of the first-stage converter is proposed in Section V. A design guideline of the proposed two-stage topology is given in Section VI. Section VII presents the experimental results. Finally, Section VIII concludes the article.

II. Overview of the Dual Active Bridge-Derived Hybrid Switched-Capacitor Converter

The conventional DAB converters employ a high-frequency transformer to provide the desired voltage matching between the bridge circuits, which is necessary for achieving higher efficiency. However, due to the large size of the transformer core, isolated DAB converters have not found practical use in VRM applications, where the isolation provided by the transformer is usually not necessary [3], [27]. In order to use this type of converters in VRM applications, a family of DAB-derived high power density hybrid switched-capacitor converters has been introduced in [28]. These converters eliminate the transformer, but retain its voltage-matching functionality using a switched-capacitor-based bridge circuit in the input side.

The DAB-derived hybrid switched-capacitor converter in the first-stage of this proposed two-stage 48-V VRM topology (Fig. 2) employs a 6:1 step-down ratio switched-capacitor bridge circuit in the input side, which produces a high-frequency ac voltage of $\pm v_{\rm i}/6$ volt peak. The switches $S_1 - S_6$ and the charge transfer (CT) capacitors $C_1 - C_5$ constitute this bridge. A standard full-bridge circuit is used in the output side of this converter. The full-bridge circuit is implemented using the switches $Q_1 - Q_4$. $L_{\rm r}$ is the ac link power transfer inductor placed strategically between the two bridge circuits. The power

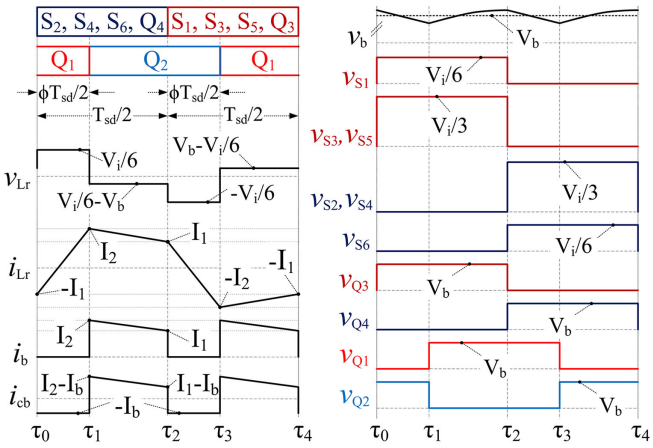

Fig. 3. Idealized switching waveforms of the converter.

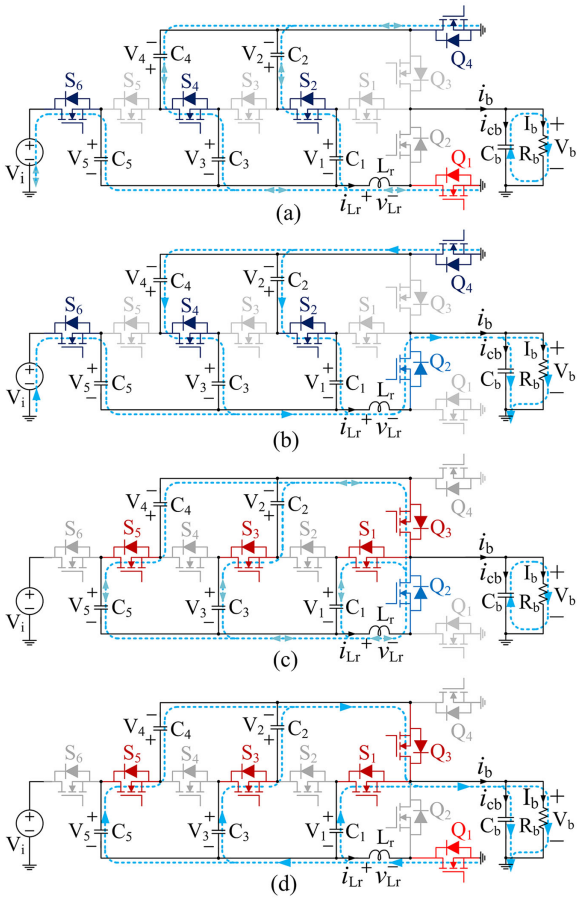

Fig. 4. Equivalent circuits for (a) mode 1 ($\tau_0 - \tau_1$), (b) mode 2 ($\tau_1 - \tau_2$), (c) mode 3 ($\tau_2 - \tau_3$), and (d) mode 4 ($\tau_3 - \tau_4$) of operation.

circuit of this first-stage converter resembles that of a Dickson switched-capacitor converter [29] except for the ac link inductor. But the operation and control of this converter is similar to a DAB converter. This converter can also operate as a series-resonant converter, when it is operated near the resonance frequency (f_r) of the resonant tank, formed by L_r and the CT capacitors ($C_1 - C_5$). For the DAB mode of operation, the switching frequency (f_sd) is kept much higher than f_r. In this mode of operation, a controllable phase shift between the two bridge circuits offers efficient voltage regulation ability. The operation of this hybrid switched-capacitor converter is analyzed below with the assumption that $f_\mathrm{sd} >> f_\mathrm{r}$. It is further assumed that all the switches are ideal and the CT capacitor voltage ripples are negligible compared to their average values.

A. *Steady-State Operating Principle*

Different idealized switching waveforms of the converter are shown in Fig. 3. The switched-capacitor bridge circuit consists of two sets of simultaneously operating switches, each set being complementary to the other. One leg (Q_3 and Q_4) of the output-side full-bridge circuit operates simultaneously with the switched-capacitor bridge circuit. The other leg (Q_1 and Q_2) of the full-bridge circuit is phase-shifted by $\phi T_\mathrm{sd}/2$ s (or $\phi\pi$ radian), where ϕ is the phase shift ratio. All the switches here operate with 0.5 duty ratio. As shown in [28], the average CT capacitor voltages V_1, V_2, V_3, V_4, and V_5 of C_1, C_2, C_3, C_4, and C_5 then attain the values $V_\mathrm{i}/6$, $2V_\mathrm{i}/6$, $3V_\mathrm{i}/6$, $4V_\mathrm{i}/6$, and $5V_\mathrm{i}/6$, respectively. Neglecting the dead times, the complete operation of this converter can be divided into four modes. Fig. 4 shows the equivalent circuits for different operational modes. For the sake of simplicity, the second-stage converter along with its load is replaced here by an effective load resistance (R_b).

1) Mode 1 ($\tau_0 - \tau_1$): The operating cycle starts at τ_0 with the turning OFF of S_1, S_3, S_5, and Q_3 followed by the turning ON of S_2, S_4, S_6, and Q_4 while Q_1 and Q_2 remain turned ON and OFF, respectively. The voltage across the inductor (v_Lr) becomes equal to $V_\mathrm{i}/6$, which starts to increase the inductor current (i_Lr) from its initial value of $-I_1$. In this mode, the output filter capacitor (C_b) alone supplies the load. A fraction of i_Lr here flows through the input source. This mode continues till τ_1, where Q_1 is turned OFF and Q_2 is turned ON. The final value of i_Lr at the end of this mode is assumed to be I_2.

2) Mode 2 ($\tau_1 - \tau_2$): Immediately after the turning ON of Q_2, v_Lr becomes equal to $(V_\mathrm{i}/6 - V_\mathrm{b})$, which starts to change i_Lr from I_2. Depending upon the values of V_i and V_b, i_Lr here may increase or decrease. In this mode, i_Lr directly flows to the parallel combination of C_b and R_b at the output, which charges C_b. Some current is drawn here from the input source. This mode ends at τ_2, when the switches S_2, S_4, S_6, and Q_4 are turned OFF and S_1, S_3, S_5, and Q_3 are turned ON. The first half-cycle of operation is completed here. From the half-cycle symmetry of operation and from the pure ac nature of i_Lr (due to the charge balance requirement of C_1, C_2, and C_3), it can be shown that at the end of this mode, i_Lr reaches I_1.

3) Mode 3 ($\tau_2 - \tau_3$): With the turning ON of S_1, S_3, S_5, and Q_3, the circuit enters into the mode 3 operation. This mode is similar to mode 1. A voltage of $-V_\mathrm{i}/6$ appears across L_r, which starts to decrease i_Lr from I_1. Here again C_b alone discharges to supply the load. The mode ends at τ_3, when Q_2 and Q_1 are turned OFF and ON, respectively. Here, i_Lr reaches $-I_2$.

4) Mode 4 ($\tau_3 - \tau_4$): This mode is similar to mode 2. Here, $(V_\mathrm{b} - V_\mathrm{i}/6)$ appears across L_r, which changes i_Lr from $-I_2$. C_b is charged here again as i_Lr flows directly to the output. This mode ends at τ_4, where the switches S_1, S_3, S_5, and Q_3 are

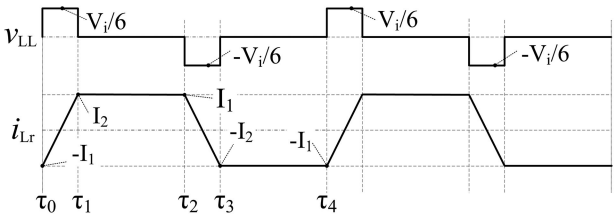

Fig. 5. Switching waveforms under nominal conversion ratio operation.

turned OFF and S_2, S_4, S_6, and Q_4 are turned ON again. The final value of i_{Lr} at the end of this mode becomes $-I_1$. After this, the circuit enters into the next switching cycle.

B. Average Output Current and Voltage Expressions

During mode 1 operation, $V_i/6$ volt appears across L_r which changes i_{Lr} from $-I_1$ to I_2 in $\phi T_{sd}/2$ s, as shown in Fig. 3. Therefore, $(I_1 + I_2) = V_i \phi T_{sd}/(12L_r)$. The average output current of the converter (I_b), which is actually the average of i_b, can then be calculated as

$$I_b = (I_1 + I_2)\frac{(1-\phi)}{2} = \frac{V_i \phi (1-\phi) T_{sd}}{24 L_r}. \quad (1)$$

Since I_b is directly related to the ϕ, providing the same ϕ during multiphase operation can ensure equal current sharing without requiring any current sensing arrangement. Multiplication of V_b to both the sides of (1) produces the expression for the average output power (P_b). This is given as follows:

$$P_b = V_b I_b = \frac{V_i V_b \phi (1-\phi) T_{sd}}{24 L_r}. \quad (2)$$

The power flow equation above is identical to a conventional DAB converter operating with phase shift control and using a 6:1 turns ratio transformer. This confirms that the basic power flow mechanism in this converter follows the DAB principle. Similarly, multiplication of R_b to both the sides of (1) produces the expression for V_b, which is given below

$$V_b = I_b R_b = \frac{V_i \phi (1-\phi) T_{sd} R_b}{24 L_r}. \quad (3)$$

Therefore, the voltage gain, $V_b/V_i = \phi(1-\phi)T_{sd}R_b/(24L_r)$. This converter can operate over a wide range of conversion ratios, depending upon the phase shift, load condition, and switching frequency. However, like the conventional DAB converters, this DAB-derived hybrid switched-capacitor converter operates most efficiently at its nominal conversion ratio of 6-to-1. When V_b is regulated to $V_i/6$, the inductor voltage during modes 2 and 4 becomes zero as shown in Fig. 5. This produces a flat top inductor current waveform, which results in minimum rms and peak current stresses for different active and passive devices. This also helps in achieving ZVS for most of the switches. In order to get the previously mentioned advantages of operating at the nominal conversion ratio, this hybrid switched-capacitor converter in the first stage of the proposed 48-V VRM topology is used to regulate the intermediate bus voltage (V_b) to $V_i/6$ only against the load variations. Therefore, the rest of the analysis considers this hybrid switched-capacitor converter to operate only at the nominal conversion ratio.

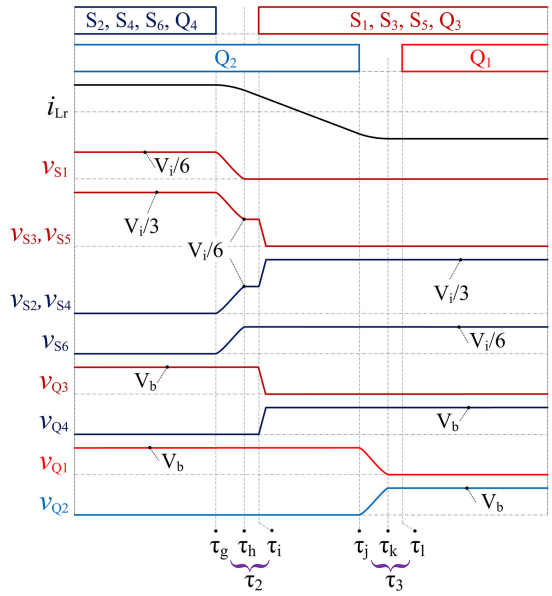

Fig. 6. Detailed switching waveforms of the converter under the nominal conversion ratio operation considering switching transitions during dead times.

C. Device Voltage and Current Stresses

The device voltage waveforms in Fig. 3 show that all the switches of the switched-capacitor bridge circuit (i.e. $S_1 - S_6$) have reduced voltage stresses. $S_2 - S_5$ have a peak voltage stress of $V_i/3$, and $V_i/6$ for S_1 and S_6. $Q_1 - Q_4$ withstand a peak voltage of V_b. The current stresses of $S_1 - S_6$ are also low as three of them always conduct in parallel (Fig. 4). The charge balance of the CT capacitors ensures equal average current sharing among them. If the CT capacitors are designed such that, $C_2 = C_4 >> C_1 = C_3 = C_5$, the equivalent capacitances of the three parallel paths through the switched-capacitor bridge circuit in each operational mode become nearly equal. As a result, i_{Lr} divides equally through each of these three parallel paths. Then, the instantaneous and rms current sharing by $S_1 - S_6$ become almost equal. This also reduces the current stresses of Q_3 and Q_4 as only 2/3rd of i_{Lr} flows through them (Fig. 4).

III. ZVS Analysis of the First-Stage Converter

Due to the inductive nature of the resonant tank, most of the switches of the first-stage hybrid switched-capacitor converter operate with full/partial ZVS. The switches S_1, S_6, Q_1, and Q_2 operate with full ZVS, whereas $S_2 - S_5$ operate with partial ZVS with half of their blocking voltage appearing during switching transition. Q_3 and Q_4 are hard switched. The converter undergoes a total of four switching/mode transitions in a cycle. Assuming the converter to be operating at the nominal conversion ratio detailed switching waveforms of the converter during dead times between the transitions from mode 2 to 3 and mode 3 to 4 are shown in Fig. 6 and discussed below.

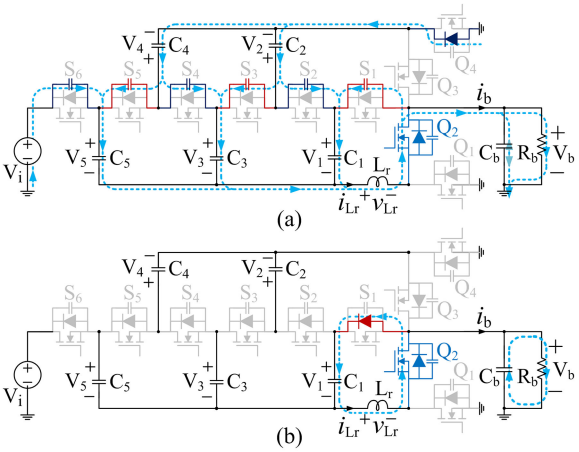

Fig. 7. Equivalent circuits of the converter during mode 2 to 3 transition in the time intervals (a) $\tau_g - \tau_h$ and (b) $\tau_h - \tau_i$.

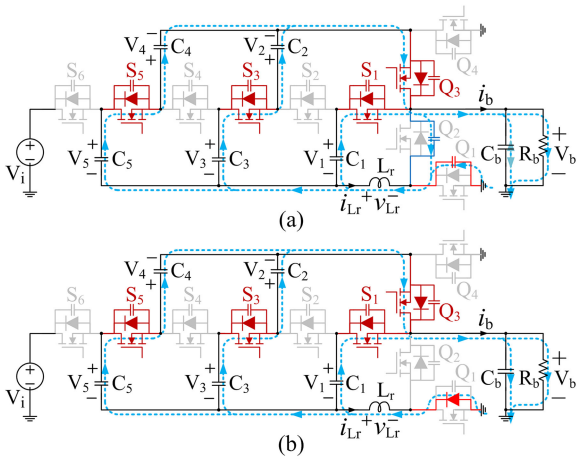

Fig. 8. Equivalent circuits of the converter during mode 3 to 4 transition in the time intervals (a) $\tau_j - \tau_k$ and (b) $\tau_k - \tau_l$.

A. ZVS Processes

1) Mode 2 to 3 Transition ($\tau_g - \tau_i$): At the end of mode 2, i.e., at τ_g, as soon as S_2, S_4, S_6, and Q_4 are turned OFF with positive i_{Lr} (Fig. 6), the body diode of Q_4 is turned ON and a resonance starts among L_r and the output capacitors of the switches $S_1 - S_6$. The corresponding equivalent circuit is shown in Fig. 7(a). The currents in different paths are divided such a way that the KVL in different loops is satisfied. During this process, v_{S1}, v_{S3}, and v_{S5} start to decrease and v_{S2}, v_{S4}, and v_{S6} start to rise from zero. v_{Q3} and v_{Q4} stay at V_b and zero, respectively. i_{Lr} starts to decrease as v_{Lr} starts to become negative. These continue until at τ_h the voltage across S_1 reaches zero and its body diode gets forward biased to clamp the voltage. The resonance stops here and the voltages across $S_2 - S_6$ reach $V_i/6$. The corresponding equivalent circuit is shown in Fig. 7(b). As soon as the body diode of S_1 starts to conduct, v_{Lr} is clamped to $V_i/6$. This continues to decrease i_{Lr} at a constant slope. In order to maintain KVL in different loops, no current flows through the output capacitors of the switches. Therefore, i_{Lr} here flows only through the body diode of S_1. The voltage across $S_2 - S_6$ stays at $V_i/6$. These continue until at τ_i, switches S_1, S_3, S_5, and Q_3 are turned ON. Then v_{S3}, v_{S5}, and v_{Q3} become zero. v_{S2} and v_{S4} rise to $V_i/3$ and v_{Q4} increases to V_b. The circuit enters into mode 3 operation [Fig. 4(c)]. The mode 4 to mode 1 transition is similar but opposite to this transition.

2) Mode 3 to 4 Transition ($\tau_j - \tau_l$): Immediately after Q_2 is turned OFF at the end of mode 3, i.e. at τ_j with negative i_{Lr} (Fig. 5), a resonance starts among L_r and the output capacitors of Q_1 and Q_2. The corresponding equivalent circuit is shown in Fig. 8(a). This starts to increase v_{Q2} and decrease v_{Q1}. The magnitude of v_{Lr} starts to decrease and hence the falling slope of i_{Lr} starts to reduce. These continue until at τ_k, v_{Q1} reaches zero and the body diode of Q_1 is turned ON. The corresponding equivalent circuit is shown in Fig. 8(b). v_{Q2} here reaches V_b. i_{Lr} starts flowing through the body diode of Q_1. Under the nominal conversion ratio operation, v_{Lr} here becomes zero and hence i_{Lr} stays constant. Finally, at τ_l, Q_1 can be turned ON to start mode 4 operation [Fig. 4(d)]. In this switching transition, the switches Q_1 and Q_2 are turned ON and OFF, respectively, with full ZVS. The mode 1 to mode 2 transition is similar to this, where Q_2 and Q_1 are turned ON and OFF, respectively, with full ZVS.

B. ZVS Conditions

1) ZVS Conditions for $S_1 - S_6$: Switches $S_1 - S_6$ are switched during mode 2 to 3 and mode 4 to 1 transitions only. During the mode 2 to 3 transition, as the resonance starts (among L_r and the output capacitors of $S_1 - S_6$) at τ_g, the switch voltages and the inductor current under the nominal conversion ratio operation take, approximately, the following form (for $t \geq \tau_g$):

$$v_{S6}(t) = v_{S4}(t) = v_{S2}(t) = i_{Lr}(\tau_g) Z_{Se} \sin\{\omega_{Se}(t - \tau_g)\} \tag{4}$$

$$v_{S5}(t) = v_{S3}(t) = V_i/3 - i_{Lr}(\tau_g) Z_{Se} \sin\{\omega_{Se}(t - \tau_g)\} \tag{5}$$

$$v_{S1}(t) = V_i/6 - i_{Lr}(\tau_g) Z_{Se} \sin\{\omega_{Se}(t - \tau_g)\} \tag{6}$$

$$i_{Lr}(t) = i_{Lr}(\tau_g) \cos\{\omega_{Se}(t - \tau_g)\} \tag{7}$$

where $Z_{Se} = \sqrt{L_r/C_{oss,Se}}$; $\omega_{Se} = 1/\sqrt{L_r C_{oss,Se}}$; $C_{oss,Se}$ is the summation of the output capacitances of $S_1 - S_6$; and $i_{Lr}(\tau_g)$ is the value of i_{Lr} at $t = \tau_g$. Therefore, in order to achieve the full ZVS for S_1 and S_6 and partial ZVS of $S_2 - S_5$ at $V_i/6$, the following condition must be satisfied:

$$i_{Lr}(\tau_g) \geq \begin{cases} V_i/\{6Z_{Se}\sin(\omega_{Se}\tau_{dS})\} & : \tau_{dS} < \pi/(2\omega_{Se}) \\ V_i/(6Z_{Se}) & : \tau_{dS} \geq \pi/(2\omega_{Se}). \end{cases} \tag{8}$$

Here τ_{dS} $(= \tau_i - \tau_g)$ is the dead time between the switching of the complementary sets of switches $S_1 - S_6$. Assuming $\tau_{dS} << (1 - \phi)T_{sd}/2$, the average output current of the first-stage converter (i.e., I_b) under the nominal conversion ratio operation can be approximated as follows:

$$I_b \approx (1 - \phi) i_{Lr}(\tau_g). \tag{9}$$

Hence, from (8) and (9), the necessary and sufficient condition for the desired ZVS operation of $S_1 - S_6$ can be obtained in

terms of $I_{\rm b}$, $V_{\rm i}$, and ϕ. This is given below:

$$I_{\rm b} \geq \begin{cases} (1-\phi)V_{\rm i}/\{6Z_{\rm Se}\sin(\omega_{\rm Se}\tau_{\rm dS})\} & : \tau_{\rm dS} < \pi/(2\omega_{\rm Se}) \\ (1-\phi)V_{\rm i}/(6Z_{\rm Se}) & : \tau_{\rm dS} \geq \pi/(2\omega_{\rm Se}). \end{cases} \tag{10}$$

Now, using (1), (2), and (10), the necessary and sufficient condition for the desired ZVS operation of $S_1 - S_6$ can be expressed in terms of $P_{\rm b}$ and $V_{\rm i}$ only. This is given below,

$$P_{\rm b} \geq \begin{cases} K_1 V_{\rm i}^2 & : \tau_{\rm dS} < \pi/(2\omega_{\rm Se}) \\ K_2 V_{\rm i}^2 & : \tau_{\rm dS} \geq \pi/(2\omega_{\rm Se}). \end{cases} \tag{11}$$

where $K_1 = 0.0278[T_{\rm sd}Z_{\rm Se}\sin(\omega_{\rm Se}\tau_{\rm dS}) - 4L_{\rm r}]/[T_{\rm sd}Z_{\rm Se}^2\sin^2(\omega_{\rm Se}\tau_{\rm dS})]$ and $K_2 = 0.0278(T_{\rm sd}Z_{\rm Se} - 4L_{\rm r})/(T_{\rm sd}Z_{\rm Se}^2)$. Due to the similarity, it can be shown that (10) and (11) are also the necessary and sufficient conditions for the desired ZVS operation of $S_1 - S_6$ during mode 4 to 1 transition.

2) ZVS Conditions for Q_1 and Q_2: Switches Q_1 and Q_2 are switched only during mode 1 to 2 and mode 3 to 4 transitions. Immediately after the start of the resonance (among $L_{\rm r}$ and the output capacitors of Q_1 and Q_2) at $\tau_{\rm j}$ during mode 3 to 4 transition, the switch voltages and the inductor current under the nominal conversion ratio operation take, approximately, the following form (for $t \geq \tau_{\rm j}$):

$$\begin{aligned} v_{\rm Q2}(t) &= V_{\rm i}/6 - v_{\rm Q1}(t) = V_{\rm i}/6[1-\cos\{\omega_{\rm Qe}(t-\tau_{\rm j})\}] \\ &\quad - i_{\rm Lr}(\tau_{\rm j})Z_{\rm Qe}\sin\{\omega_{\rm Qe}(t-\tau_{\rm j})\} \end{aligned} \tag{12}$$

$$\begin{aligned} i_{\rm Lr}(t) &= i_{\rm Lr}(\tau_{\rm j})\cos\{\omega_{\rm Qe}(t-\tau_{\rm j})\} \\ &\quad - V_{\rm i}\sin\{\omega_{\rm Qe}(t-\tau_{\rm j})\}/(6Z_{\rm Qe}) \end{aligned} \tag{13}$$

where $Z_{\rm Qe} = \sqrt{L_{\rm r}/C_{\rm oss,Qe}}$; $\omega_{\rm Qe} = 1/\sqrt{L_{\rm r}C_{\rm oss,Qe}}$; $C_{\rm oss,Qe}$ is the summation of the output capacitances of Q_1 and Q_2; and $i_{\rm Lr}(\tau_{\rm j})$ is the value of $i_{\rm Lr}$ at $t = \tau_{\rm j}$. Therefore, in order to achieve the full ZVS for Q_1 and Q_2, the following conditions must be satisfied:

$$-i_{\rm Lr}(\tau_{\rm j}) \geq \begin{cases} V_{\rm i}/\{6Z_{\rm Qe}\tan(\omega_{\rm Qe}\tau_{\rm dQ})\} & : \tau_{\rm dQ} < \pi/(2\omega_{\rm Qe}) \\ 0 & : \tau_{\rm dQ} \geq \pi/(2\omega_{\rm Qe}) \end{cases} \tag{14}$$

where $\tau_{\rm dQ}$ $(= \tau_{\rm l} - \tau_{\rm j})$ is the dead time between the switching of Q_1 and Q_2. Assuming $\tau_{\rm dQ} << (1-\phi)T_{\rm sd}/2$, the average output current of the first-stage converter (i.e., $I_{\rm b}$) under the nominal conversion ratio operation can also be approximated as follows:

$$I_{\rm b} \approx -(1-\phi)i_{\rm Lr}(\tau_{\rm k}). \tag{15}$$

$i_{\rm Lr}(\tau_{\rm k})$ is the value of $i_{\rm Lr}$ at $t = \tau_{\rm k}$, where $v_{\rm Q1}(t)$ reaches zero and the slope of $i_{\rm Lr}(t)$ becomes zero. Hence, from (12)–(15), the necessary and sufficient condition for the full ZVS of Q_1 and Q_2 during mode 3 to 4 transition can be obtained in terms of $I_{\rm b}$ as written below:

$$I_{\rm b} \geq \begin{cases} (1-\phi)V_{\rm i}/\{6Z_{\rm Qe}\sin(\omega_{\rm Qe}\tau_{\rm dQ})\} & : \tau_{\rm dQ} < \pi/(2\omega_{\rm Qe}) \\ (1-\phi)V_{\rm i}/(6Z_{\rm Qe}) & : \tau_{\rm dQ} \geq \pi/(2\omega_{\rm Qe}). \end{cases} \tag{16}$$

Now, using (1), (2), and (16), the necessary and sufficient condition for the full ZVS operation of Q_1 and Q_2 can be expressed in terms of $P_{\rm b}$ and $V_{\rm i}$ only. This is given as follows:

$$P_{\rm b} \geq \begin{cases} K_3 V_{\rm i}^2 & : \tau_{\rm dQ} < \pi/(2\omega_{\rm Qe}) \\ K_4 V_{\rm i}^2 & : \tau_{\rm dQ} \geq \pi/(2\omega_{\rm Qe}) \end{cases} \tag{17}$$

where $K_3 = 0.0278[T_{\rm sd}Z_{\rm Qe}\sin(\omega_{\rm Qe}\tau_{\rm dQ}) - 4L_{\rm r}]/[T_{\rm sd}Z_{\rm Qe}^2\sin^2(\omega_{\rm Qe}\tau_{\rm dQ})]$ and $K_4 = 0.0278(T_{\rm sd}Z_{\rm Qe} - 4L_{\rm r})/(T_{\rm sd}Z_{\rm Qe}^2)$. Due to similarity, (16) and (17) are also the necessary and sufficient conditions for the full ZVS for Q_1 and Q_2 during mode 1 to 2 transition. The shaded area in Fig. 9 shows the ZVS regions of $S_1 - S_6$, Q_1, and Q_2 in the $P_{\rm b}$ v/s $V_{\rm i}$ plane. Here, it is assumed that $L_{\rm r} = 72$ nH, the output capacitance of each of $S_1 - S_6 = 330$ pF, the output capacitance of each of Q_1 and $Q_2 = 750$ pF, $\tau_{\rm dS} = \tau_{\rm dQ} = 20$ ns, and $T_{\rm sd} = 2.86$ μs. The $P_{\rm b}$ is per unitized with respect to the rated power of the converter. It is seen that the ZVS is achieved in most of the load range. The ZVS is lost in the lower load conditions.

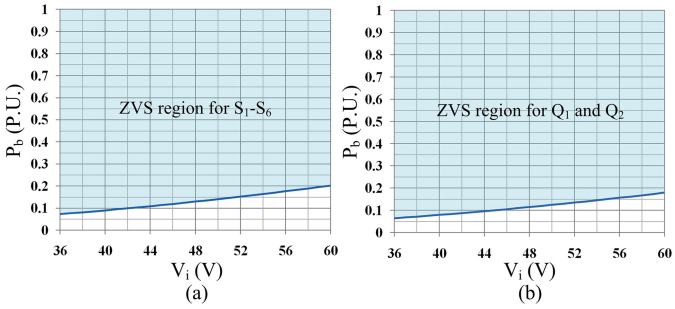

Fig. 9. ZVS regions for (a) $S_1 - S_6$ and (b) Q_1 and Q_2.

IV. Modeling of the First-Stage Converter

A. Large Signal Model

In Section II-A, it is shown that the first-stage hybrid-switched converter takes four different switch configurations in four modes. Fig. 10 shows the equivalent circuits for all the operational modes, including different parasitic resistances, where $r_{\rm C1}$, $r_{\rm C2}$, $r_{\rm C3}$, $r_{\rm C4}$, $r_{\rm C5}$, and $r_{\rm Cb}$ are the effective series resistances (ESRs) of the capacitors; $r_{\rm Lr}$ is the dc resistance (DCR) of $L_{\rm r}$; and $r_{\rm S1}$, $r_{\rm S2}$, $r_{\rm S3}$, $r_{\rm S4}$, $r_{\rm S5}$, $r_{\rm S6}$, $r_{\rm Q1}$, $r_{\rm Q2}$, $r_{\rm Q3}$, and $r_{\rm Q4}$ are the ON state resistances of the switches. In each operational mode, the converter circuit is linear and time invariant with the state-space representation

$$\left.\begin{aligned} \dot{X} &= A_{\rm j}X + B_{\rm j}v_{\rm i} \\ v_{\rm b} &= E_{\rm j}X \end{aligned}\right\} : {\rm j} \in \{1,2,3,4\} \tag{18}$$

where $X = [v_1\ v_2\ v_3\ v_4\ v_5\ i_{\rm Lr}\ v_{\rm Cb}]^{\rm T}$ is the state vector. j represents any particular mode. $A_{\rm j}$, $B_{\rm j}$, and $E_{\rm j}$ are the system, input, and output matrices, respectively, for different modes, the elements of which can be obtained by solving the circuits corresponding to each mode shown in Fig. 10. Since the input source stays disconnected from the circuit during modes 3 and 4, B_3 and B_4 are null vectors. A mode transition diagram of the converter is shown in Fig. 11, where $\phi_{\rm k}$ is the phase shift in the kth switching cycle. $X_{\rm k}$ and $X_{\rm k+1}$, respectively, are the values of the state vector at the beginning and end of that switching

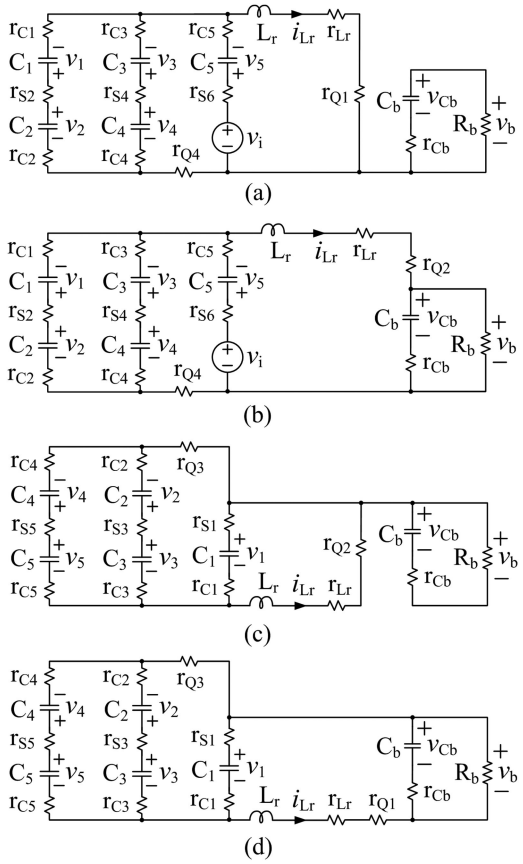

Fig. 10. Equivalent circuits for (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4 of operation including different parasitic resistances.

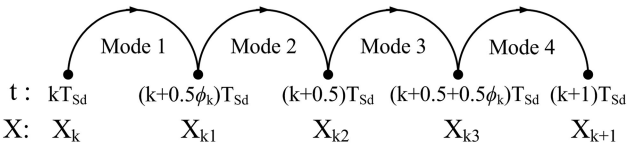

Fig. 11. Mode transition diagram showing different initial and final values of time (t) and the state vector (X).

cycle. Assuming $v_{\rm i}$ to be constant at $V_{\rm i}$, the final values of the state vector at the end of all four modes (i.e., $X_{\rm k1}$, $X_{\rm k2}$, $X_{\rm k3}$, and $X_{\rm k+1}$) can be calculated in terms of their respective initial values (i.e., $X_{\rm k}$, $X_{\rm k1}$, $X_{\rm k2}$, and $X_{\rm k3}$) using the following relations:

$$X_{\rm k1} = e^{A_1 t_1} X_{\rm k} + \int_0^{t_1} e^{A_1(t_1-\tau)} B_1 V_{\rm i} d\tau \tag{19}$$

$$X_{\rm k2} = e^{A_2 t_2} X_{\rm k1} + \int_0^{t_2} e^{A_2(t_2-\tau)} B_2 V_{\rm i} d\tau \tag{20}$$

$$X_{\rm k3} = e^{A_3 t_3} X_{\rm k2} \tag{21}$$

$$X_{\rm k+1} = e^{A_4 t_4} X_{\rm k3} \tag{22}$$

where $t_1 = t_3 = \phi_{\rm k} T_{\rm sd}/2$; $t_2 = t_4 = (1-\phi_{\rm k})T_{\rm sd}/2$. In order to get the closed form expressions of $X_{\rm k1}$ and $X_{\rm k2}$, the system matrices, A_1 and A_2, should be nonsingular. However, due to the presence of the linearly dependent states, both A_1 and A_2 are singular. During both mode 1 and 2 operations, C_1 stays in series with C_2, and C_3 with C_4 (Fig. 4). Therefore, during

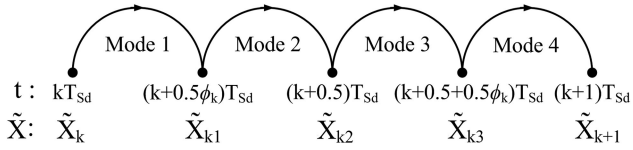

Fig. 12. Mode transition diagram showing different initial and final values of time (t) and the augmented state vector ($\tilde{X}$).

these modes, the states v_1 and v_2, and v_3 and v_4 become linearly related by the following equations:

$$C_1 \frac{dv_1}{\rm dt} = C_2 \frac{dv_2}{\rm dt} \tag{23}$$

$$C_3 \frac{dv_3}{\rm dt} = C_4 \frac{dv_4}{\rm dt}. \tag{24}$$

As a result, A_1 and A_2 become singular. Therefore, in order to derive the closed-form expressions of $X_{\rm k1}$ and $X_{\rm k2}$, a reduced-order approximation of the matrix exponentials needs to be made. This leads to a significant error in the model. This issue can be mitigated by using the augmented state-space method [30]. In this technique, the state vector, the system matrices, and the output vectors are augmented by inserting dummy elements as shown below:

$$\tilde{X} = \begin{bmatrix} X \\ 1 \end{bmatrix} \tag{25}$$

$$\tilde{A}_{\rm j} = \begin{bmatrix} A_{\rm j} & B_{\rm j} V_{\rm i} \\ \Theta & 0 \end{bmatrix} \tag{26}$$

$$\tilde{E}_{\rm j} = \begin{bmatrix} E_{\rm j} & 0 \end{bmatrix} \tag{27}$$

where $\tilde{X}$, $\tilde{A}_{\rm j}$, and $\tilde{E}_{\rm j}$ are the augmented state vector, system matrix, and output vector, respectively; and Θ is a zero row-vector of length equal to the order of the system matrix. The augmented state-space equations can then be written as follows:

$$\left.\begin{aligned} \dot{\tilde{X}} &= \tilde{A}_{\rm j}\tilde{X} \\ v_{\rm b} &= \tilde{E}_{\rm j}\tilde{X} \end{aligned}\right\} : {\rm j} \in \{1,2,3,4\}. \tag{28}$$

Another mode transition diagram in terms of the augmented state vector is shown in Fig. 12. Now, from the solution of (28), the closed-form expressions of the final values of the augmented state vectors at the end of all four modes (i.e. $\tilde{X}_{\rm k1}$, $\tilde{X}_{\rm k2}$, $\tilde{X}_{\rm k3}$, and $\tilde{X}_{\rm k+1}$) can be obtained in terms of their initial values (i.e., $\tilde{X}_{\rm k}$, $\tilde{X}_{\rm k1}$, $\tilde{X}_{\rm k2}$, and $\tilde{X}_{\rm k3}$). These are given as follows:

$$\tilde{X}_{\rm k1} = e^{\tilde{A}_1 t_1} \tilde{X}_{\rm k} \tag{29}$$

$$\tilde{X}_{\rm k2} = e^{\tilde{A}_2 t_2} \tilde{X}_{\rm k1} \tag{30}$$

$$\tilde{X}_{\rm k3} = e^{\tilde{A}_3 t_3} \tilde{X}_{\rm k2} \tag{31}$$

$$\tilde{X}_{\rm k+1} = e^{\tilde{A}_4 t_4} \tilde{X}_{\rm k3}. \tag{32}$$

Finally, from the solution of (29)–(32), the large signal model is obtained in terms the augmented state-vector as follows:

$$\tilde{X}_{\rm k+1} = e^{\tilde{A}_4 t_4} e^{\tilde{A}_3 t_3} e^{\tilde{A}_2 t_2} e^{\tilde{A}_1 t_1} \tilde{X}_{\rm k} = \tilde{\Psi} \tilde{X}_{\rm k} = \tilde{F}(\tilde{X}_{\rm k}, \phi_{\rm k}). \tag{33}$$

Now, from (28), the discrete-time output voltage equation of the converter can be derived as follows:

$$v_{\rm bk} = \tilde{E}_1 \tilde{X}_{\rm k} \tag{34}$$

where $v_{\rm bk}$ is the value of $v_{\rm b}$ at the beginning of the kth switching cycle of the converter.

B. Small Signal Model

Equation (33) implies that the derived discrete-time model is nonlinear. Therefore, the steady-state operating point can be obtained by solving $\tilde{X}_{\rm k+1} = \tilde{X}_{\rm k} = \tilde{X}^*$. This gives

$$\tilde{X}^* = \tilde{\Psi}^* \tilde{X}^* \tag{35}$$

where $\tilde{\Psi}^*$ is the steady-state value of $\tilde{\Psi}$. Interestingly, $\tilde{\Psi}^*$ always takes the following form [30]:

$$\tilde{\Psi}^* = \begin{bmatrix} \Psi^* & \Gamma^* \\ \Theta & 1 \end{bmatrix}. \tag{36}$$

Hence, Ψ^* and Γ^* can be calculated as follows:

$$\Psi^* = M \tilde{\Psi}^* M^{\rm T} \tag{37}$$

$$\Gamma^* = M \tilde{\Psi}^* N \tag{38}$$

where $M = [I_7 \; \Theta^{\rm T}]^{\rm T}$ and $N = [0\,0\,0\,0\,0\,0\,0\,1]^{\rm T}$ are the transformation matrices, and I_7 is a seventh-order identity matrix. Now, using (25) and (36), (35) can be rewritten as follows:

$$\tilde{X}^* = \begin{bmatrix} X^* \\ 1 \end{bmatrix} = \begin{bmatrix} \Psi^* & \Gamma^* \\ \Theta & 1 \end{bmatrix} \begin{bmatrix} X^* \\ 1 \end{bmatrix}. \tag{39}$$

Hence, from (39), the steady-state operating point (i.e., X^*) can be obtained as follows:

$$X^* = (I_7 - \Psi^*)^{-1} \Gamma^*. \tag{40}$$

Now, applying small-signal perturbations to (33) around the operating point obtained using (40) followed by Jacobian linearization, the small-signal model of the converter can be derived. This is written as follows:

$$\hat{\tilde{X}}_{\rm k+1} = \underbrace{\left.\frac{\partial \tilde{F}}{\partial \tilde{X}_{\rm k}}\right|_*}_{\tilde{\Psi}^*} \hat{\tilde{X}}_{\rm k} + \underbrace{\left.\frac{\partial \tilde{F}}{\partial \phi_{\rm k}}\right|_*}_{\tilde{\Upsilon}^*} \hat{\phi}_{\rm k}. \tag{41}$$

Application of small-signal perturbations to the output voltage equation of (34) gives

$$\hat{v}_{\rm bk} = \tilde{E}_1 \hat{\tilde{X}}_{\rm k}. \tag{42}$$

Applying z-transformation to (41) and (42), the discrete-time small-signal control-to-output transfer function of the converter [i.e., $G_{{\rm v}\phi}(z)$] can be obtained. This is given as follows:

$$G_{{\rm v}\phi}(z) = \frac{\hat{v}_{\rm b}(z)}{\hat{\phi}(z)} = \tilde{E}_1 [z I_8 - \tilde{\Psi}^*]^{-1} \tilde{\Upsilon}^* \tag{43}$$

where I_8 is an eighth-order identity matrix.

TABLE I
SET OF PARAMETERS USED FOR MODELING

Parameter	Value	Parameter	Value
$V_{\rm i}$	48 V	C_1, C_3, and C_5	7.5 μF
$V_{\rm b}$	8 V	C_2 and C_4	22 μF
ϕ	0.046	$r_{\rm Cb}$	2 mΩ
$C_{\rm b}$	240 μF	$r_{\rm Lr}$	0.32 mΩ
$R_{\rm b}$	2 Ω	$r_{\rm S1} - r_{\rm S6}$	5 mΩ
$T_{\rm sd}$	2.86 μs	$r_{\rm Q1} - r_{\rm Q4}$	1.7 mΩ
$L_{\rm r}$	72 nH	$r_{\rm C1} - r_{\rm C5}$	2 mΩ

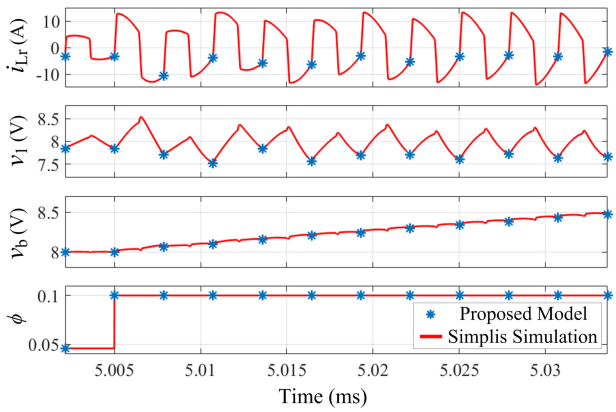

Fig. 13. Large signal model verification of the switching waveforms with the SIMPLIS simulation results with a step change in ϕ.

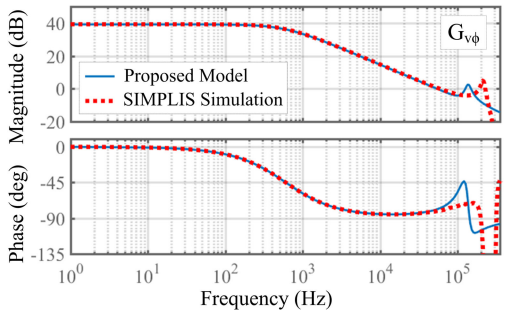

Fig. 14. Frequency domain model verification of $G_{{\rm v}\phi}$.

C. Model Verification

The proposed discrete-time model of the first-stage hybrid switched-capacitor converter is verified against the SIMPLIS simulation results using the set of parameters given in Table I. Fig. 13 presents time domain large signal model verification under a dynamic condition. Here, a step change in ϕ from 0.046 to 0.1 is applied at 5.005 ms, before which the converter is assumed to be in steady-state condition (as in Table I). Under this condition, the values of $i_{\rm Lr}$, v_1, and $v_{\rm b}$ are computed at the beginning and end of each switching cycle and then plotted over the simulated waveforms. The proposed model shows a good matching here. Finally, the small signal model verification of the frequency response of $G_{{\rm v}\phi}$ is shown in Fig. 14. The proposed model is observed to capture the frequency response of the converter with a great accuracy up to 1/5th of the switching frequency. It is further observed from Fig. 14 that the frequency

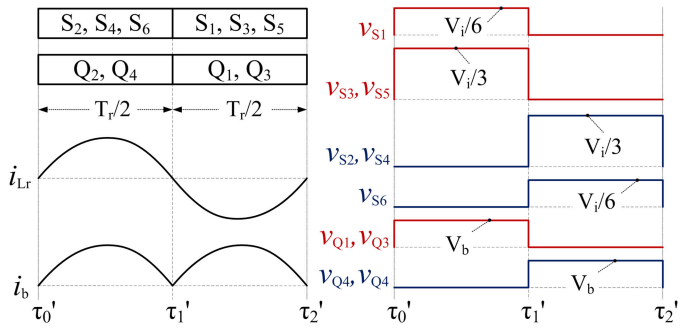

Fig. 15. Idealized switching waveforms under the resonant mode operation of the first-stage converter.

response of $G_{v\phi}$ is dominated by a stable pole due to the presence of the output RC filter.

V. Resonant Operation of the First-Stage Converter for Light-Load Efficiency Improvement

The first-stage hybrid-switched capacitor converter in DAB mode of operation starts to lose ZVS operation for most of its switches when the load power goes below certain limit, as shown in Fig. 9. Under this condition, the switch output capacitance-related switching losses become high which drastically reduce the efficiency. Under the light load condition, the gate driving losses also become dominant, which further degrades the efficiency. Fortunately, this converter allows the reduction of switching frequency down to the resonance frequency of the resonant tank. This reduces all switching-related losses, which significantly improves the efficiency under the light load conditions. Fig. 15 shows the switching waveforms under the resonant operation of the converter. In this resonant operation, each switching cycle can be divided into two modes. The equivalent circuits corresponding to mode 1 ($\tau_0' - \tau_1'$) and mode 2 ($\tau_1' - \tau_2'$) are the same as those shown in Fig. 4(b) and (d), respectively. As can be seen from Fig 4(b), during mode 1 of this resonant operation, the series combinations of C_1 and C_2, C_3 and C_4, and C_5 and the input source come in parallel. This series parallel combination of the CT capacitors along with L_r constitutes a series-resonant tank. The effective capacitance of this resonant tank during mode 1 (i.e. $C_{\mathrm{r}1}$) is found to be

$$C_{\mathrm{r}1} = \frac{C_1 C_2}{C_1 + C_2} + \frac{C_3 C_4}{C_3 + C_4} + C_5. \tag{44}$$

Similarly, as shown in Fig 4(d) during mode 2 of the resonant operation, another resonant tank is formed whose effective series capacitance (i.e., $C_{\mathrm{r}2}$) is given below

$$C_{\mathrm{r}2} = C_1 + \frac{C_2 C_3}{C_2 + C_3} + \frac{C_4 C_5}{C_4 + C_5}. \tag{45}$$

If the CT capacitors are designed such that $C_1 \approx C_3 \approx C_5$ and $C_2 \approx C_4$, $C_{\mathrm{r}1}$ and $C_{\mathrm{r}2}$ become nearly equal. The effective resonant capacitance in that case (C_r) is evaluated as follows:

$$C_{\mathrm{r}1} \approx C_{\mathrm{r}2} \approx C_\mathrm{r} = C_1 + 2\frac{C_1 C_2}{C_1 + C_2}. \tag{46}$$

The corresponding resonance frequency (f_r) is given as

$$f_\mathrm{r} = \frac{1}{T_\mathrm{r}} = \frac{1}{2\pi\sqrt{L_\mathrm{r} C_r}}. \tag{47}$$

In the resonant operation, the switching frequency is reduced near to the resonance frequency, i.e., $f_\mathrm{sd} \approx f_\mathrm{r}$. As a result, the resonant tank offers nearly zero impedance. The converter becomes naturally unregulated with its output voltage (V_b) staying around $V_\mathrm{i}/6$. The loss of regulation under light load condition is acceptable since parallel operation is not necessary then. It can be shown that under this resonant operation, the average CT capacitor voltages remain the same as that under the DAB mode operation. As shown in Fig. 15, the peak voltage stresses of the switches also remain the same.

Some major drawbacks of this mode of operation are the increased peak and rms current stresses of the active and passive devices due to the sinusoidal nature of the inductor current. As a result, the conduction losses become high, which becomes dominant in the heavy load condition. Furthermore, the reduction in switching frequency increases the steady-state output voltage ripple and may become excessive at high load current. Therefore, under medium and heavy load conditions, the converter is operated with $f_\mathrm{sd} >> f_\mathrm{r}$. As a consequence, the resonant tank offers inductive impedance. The converter then can operate like a DAB converter as discussed in Sections II–IV. As will be shown later in Section VII, the resonant-mode operation exhibits better experimental efficiency compared to that under the DAB-mode operation for up to 18% of the rated load.

VI. Design of the Two-Stage Converter

The proposed two-stage 48-V VRM (Fig. 2) is designed for 80 W with the specifications: 36 V $\leq V_\mathrm{i} \leq$ 60 V, 1 V $\leq V_\mathrm{o} \leq$ 1.2 V, and 0 A $\leq I_\mathrm{o} \leq$ 55 A. The nominal conversion ratio of the first-stage converter is selected to be 6-to-1 in order to maintain the duty ratio of the second-stage multiphase buck converter in the range of sufficiently high values, $0.1 \leq D_\mathrm{b} \leq 0.2$. Moreover, this choice results in near-perfect utilization of the high-performance 25/30 V silicon devices. A 4-to-1 converter in the first stage will require higher voltage devices and will also affect the regulation capability at the highest input voltage. A 8-to-1 converter, on the other hand, will require more number of switches and capacitors. The details on the power circuit and the closed-loop controller design for each converter stages are presented below.

A. Power Circuit Design of the First-Stage Converter

The inductor of the first-stage converter is designed such that it can deliver the maximum current demand ($I_{\mathrm{b,max}}$) with the minimum input voltage ($V_{\mathrm{i,min}}$). Assuming the maximum allowable value of ϕ to be ϕ_max, L_r can be designed using the following relation obtained from (1):

$$L_\mathrm{r} \leq \frac{V_{\mathrm{i,min}} \phi_\mathrm{max}(1 - \phi_\mathrm{max})}{24 f_\mathrm{sd} I_{\mathrm{b,max}}}. \tag{48}$$

For a good power density and control bandwidth, the f_sd is selected to be 350 kHz. With $V_{\mathrm{i,min}} = 36$ V, $I_{\mathrm{b,max}} = 13.33$ A

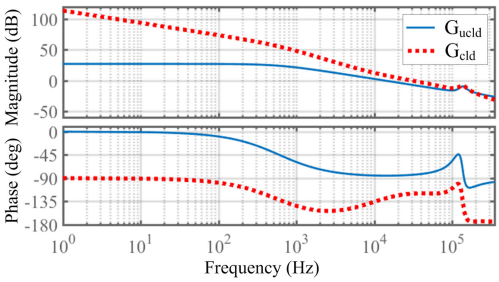

Fig. 16. Frequency responses of the uncompensated and compensated loop transfer functions (i.e., $G_{\rm ucld}$ and $G_{\rm cld}$, respectively) of the first-stage hybrid switched-capacitor converter under voltage mode control.

@ $V_{\rm b} = 6$ V, a 72 nH inductor is selected for $L_{\rm r}$, which keeps ϕ at a value lower than 0.34. The $f_{\rm r}$ is chosen to be 140 kHz, which keeps the ratio "$f_{\rm sd}/f_{\rm r}$" much above unity. From (47), the required value for $C_{\rm r}$ is then found to be 18.5 μF. This can be achieved by selecting $C_1 = C_3 = C_5 = 7.5$ μF and $C_2 = C_4 = 22$ μF. In order to keep the deviation in $V_{\rm b}$ within a sufficiently low value under load transients, 240 μF of ceramic capacitor is used for $C_{\rm b}$.

B. Controller Design for the First-Stage Converter

The first-stage hybrid switched-capacitor converter is operated with analog voltage mode control, the block diagram of which is shown in Fig. 2. The frequency response of the uncompensated loop transfer function [$G_{\rm ucld}(s) = \kappa_{{\rm m}\phi} G_{{\rm v}\phi}(s)$] is shown in Fig. 16, where the z-domain $G_{{\rm v}\phi}$ is converted to s-domain using pole-zero mapping method [31]. $\kappa_{{\rm m}\phi}$ is the gain of the phase shift modulator. A type-II compensator can be used to place the closed-loop bandwidth of this converter at around 1/10th of the switching frequency. Therefore, the compensator [$G_{\rm cd}(s)$] is designed using a type II error amplifier (EA) with a 30-kHz closed-loop bandwidth and 60° phase margin. The corresponding frequency response of the compensated loop transfer function [$G_{\rm cld}(s) = G_{\rm ucld}(s) G_{\rm cd}(s)$] is also shown in Fig. 16.

C. Power Circuit Design of the Second-Stage Converter

A three-hase buck converter is selected for the second stage to deliver 55 A load current with 18.33 A/phase. In order to get a sufficiently high control bandwidth, the switching frequency of the second-stage converter ($f_{\rm sb}$) is selected to be 700 kHz/phase. The filter inductors (L_1, L_2, and L_3) are designed to be 220 nH, each with a worst-case current ripple of 37.4%. The output filter capacitor ($C_{\rm o}$) is designed to maintain the deviations in $V_{\rm o}$ below 10% of its nominal value for a 50-A load transient. A parallel combination of ceramic capacitors having an equivalent value of 1330 μF is selected for $C_{\rm o}$.

D. Controller Design for the Second-Stage Converter

The three-phase buck converter operates with peak current mode control to ensure equal current sharing among the phases. The control block diagram of the converter without adaptive voltage positioning (AVP) function is shown in Fig. 2. The corresponding small-signal model can be obtained from [32]. Fig. 17(a) shows the frequency response of the uncompensated loop transfer function [$G_{\rm uclb}(s) = \hat{v}_{\rm o}(s)/\hat{i}_{\rm ref}(s)$]. A type-II compensator is sufficient for the outer voltage controller [$G_{\rm cb}(s)$], which can keep the closed-loop bandwidth at around 1/10th of the switching frequency for a good transient performance. The frequency response of the compensated loop transfer function [$G_{\rm clb}(s) = G_{\rm uclb}(s) G_{\rm cb}(s)$] is also shown in Fig. 17(a), where the closed-loop bandwidth and the phase margin are designed to be 70 kHz and 60°, respectively. In order to incorporate the AVP function, the AVP+ scheme of [33] can be used. In this control method, all the inductor information is subtracted from the reference voltage and fed to the noninverting terminal of the type-II EA. Here, the compensator is designed to achieve a flat closed-loop output impedance ($Z_{\rm ocb}$), which is decided by the load line slope ($R_{\rm LL}$) requirement of the load. The closed-loop output impedance vs. frequency plot under AVP control with $R_{\rm LL}$ =1.6 mΩ is shown in Fig. 17(b).

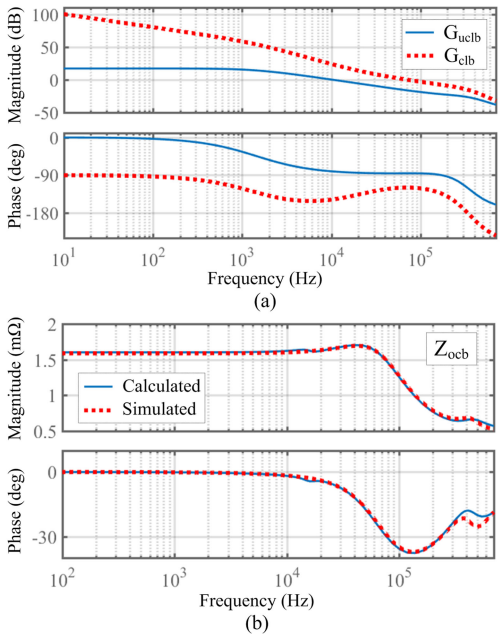

Fig. 17. Frequency responses of the (a) uncompensated and compensated loop transfer functions (i.e., $G_{\rm uclb}$ and $G_{\rm clb}$, respectively) of the three-phase buck converter under peak current mode control with out AVP function and (b) closed-loop output impedance ($Z_{\rm ocb}$) with AVP function.

VII. Experimental Results

A laboratory prototype of the proposed two-stage 48-V VRM, as shown in Fig. 18, is built in order to experimentally validate its performance. The converter parameters are selected to be the same as that designed in Section VI. The peak voltage stresses of all the switches in both first and second stages are well below 30 V. Therefore, the low-cost and high-performance 30- and 25-V silicon devices are used for them; 30-V MOSFET half-bridge modules (BSC0925ND) are used for the complementary pairs $S_1 - S_2$, $S_3 - S_4$, and $S_5 - S_6$; and 25-V discrete MOSFETs (BSC015NE2LS5I) are used for $Q_1 - Q_4$. The three-phase buck

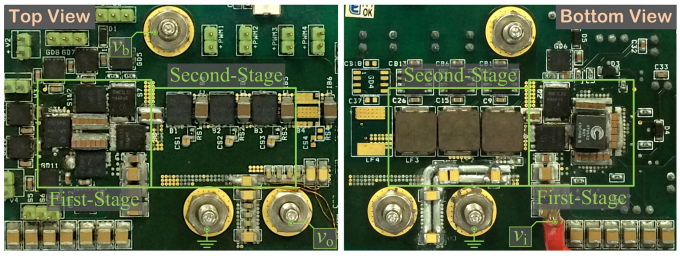

Fig. 18. Photograph of the experimental prototype.

TABLE II
SPECIFICATIONS OF THE POWER CIRCUIT COMPONENTS

Component	Specification
$S_1 - S_6$	BSC0925ND (Dual, 30 V, 5.6 mΩ)
$Q_1 - Q_4$	BSC015NE2LS5I (25 V, 1.7 mΩ)
$S_{C1} - S_{C3}$	BSC0910NDI (High Side, 25 V, 4.7 mΩ)
$S_{R1} - S_{R3}$	BSC0910NDI (Low Side, 25 V, 1.25 mΩ)
L_r	FP0705R2-R07-R (72 nH, 0.32 mΩ)
$L_1 - L_3$	IHLP3232CZERR22M01 (220 nH, 1.71 mΩ)
C_b	12103D476MAT2A (25 V, 47 μF × 4) C2012X5R1E106K085AC (25 V, 10 μF × 5)
C_o	12066D107MAT2A (6.3 V, 100 μF × 10) 06036D476MAT2A (6.3 V, 47 μF × 7)
C_1	GRM188R61H225KE11D (50 V, 2.2 μF × 10)
C_3	GRT21BR61H475KE13L (50 V, 4.7 μF × 5)
C_2 and C_4	GRT21BR61H475KE13L (50 V, 4.7 μF × 10)
C_5	08051C105K4T2A (100 V, 1 μF × 10)

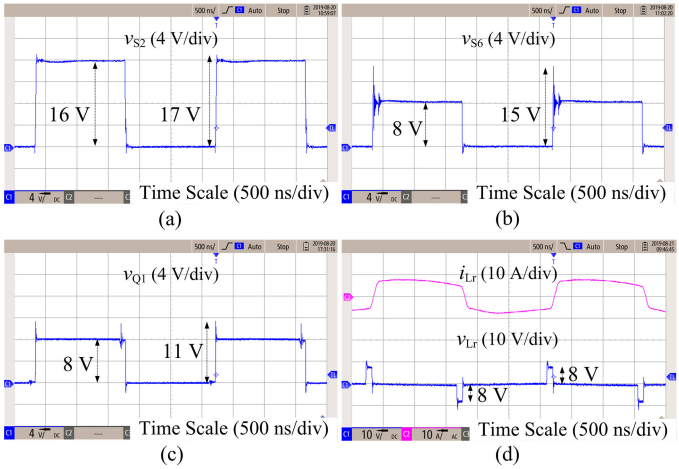

Fig. 19. Experimental waveforms of the drain-to-source voltages of (a) S_2 (b) S_6, and (c) Q_1, and (d) the inductor current (i_{Lr}) and voltage (v_{Lr}).

converter is implemented using 25-V MOSFET half-bridge modules (BSC0910NDI). The power circuit component specifications are summarized in Table II. The three-phase buck converter inductor currents are sensed using the lossless DCR current sensing method. The whole control circuit is realized in analog domain. The compensators (type-II EAs) are implemented using op-amps (THS4011).

Fig. 19 shows the experimental switching waveforms of the first-stage converter operating in DAB mode at $V_i = 48$ V, $V_o = 8$ V, and $I_o = 6$ A. Clearly, the experimental results show

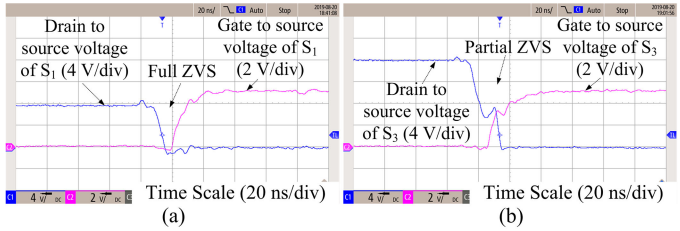

Fig. 20. ZVS operation showing the drain-to-source and gate-to-source voltages of (a) S_1 and (b) S_3.

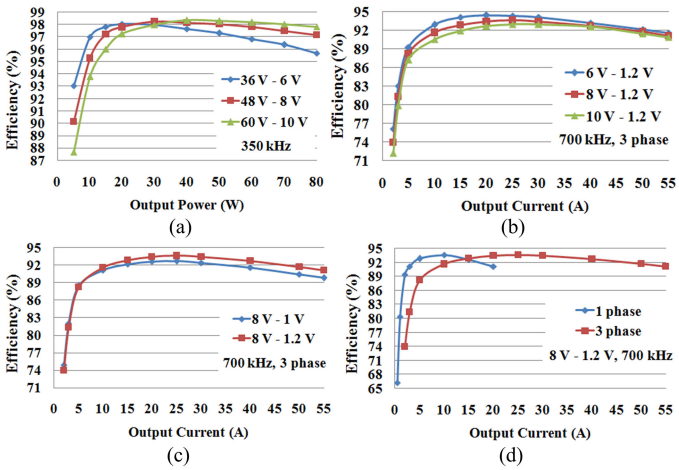

Fig. 21. Experimental efficiency plots of the (a) first-stage converter in DAB mode and of the second-stage converter with varying (b) intermediate voltage (V_b), (c) output voltage (V_o), and (d) number of phases.

good agreement with the theoretical analysis. It is further observed that the peak voltage stresses of the switches are well below their voltage ratings. The ZVS waveforms of S_1 and S_3 are shown in Fig. 20. It is seen that S_1 achieves full ZVS, whereas S_3 operates with partial ZVS. Similarly, S_6, Q_1, and Q_2 are observed to undergo full ZVS and S_2, S_3, S_4, and S_5 are observed to operate with partial ZVS. The experimental efficiency characteristics of the individual stages including the gate driving losses are presented in Fig. 21. The figures show that the first-stage converter in DAB mode attains peak efficiencies of 98.1%, 98.3%, and 98.4% at 36, 48, and 60 V input voltages, respectively. The converter maintains full load (80 W) efficiencies of 95.7%, 97.1%, and 97.8% at those input voltages, respectively. The second-stage three-phase buck converter attains peak efficiencies of 94.4%, 93.6%, and 93.0% at 6, 8, and 10 V of V_b, respectively, at $V_o = 1.2$ V and maintains over 91% full load ($I_o = 55$ A) efficiency at the same V_o. The peak and full load efficiencies drop to 92.7% and 89.8% at $V_o = 1$ V and $V_b = 8$ V. As depicted in Fig. 21(d), the efficiency of the second-stage converter is maintained above 89% over a wide load range (2–55 A) through phase shedding. The light-load efficiency of the first-stage converter is improved through the resonant mode operation. The corresponding experimental switching waveforms and efficiency plot are shown in Fig. 22. The inductor current is observed to have near-sinusoidal waveform. Q_1 and all other switches are observed to have the same voltage stresses as compared to that under the DAB mode of operation. As shown

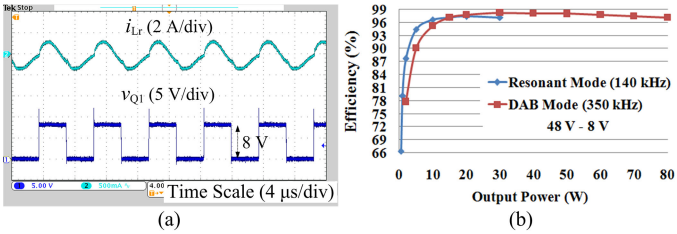

Fig. 22. (a) Experimental waveforms of the inductor current and drain-to-source voltage of Q_1 under the resonant mode operation of the first-stage converter at 48–8 V and $I_b = 0.5$ A, and (b) the efficiency comparison between the resonant and DAB mode of operation.

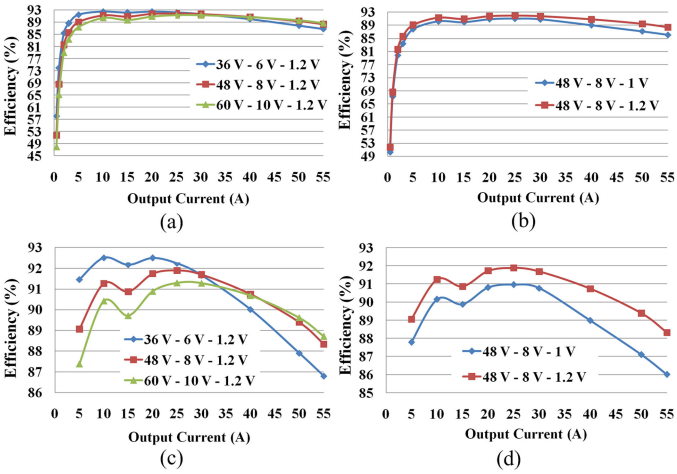

Fig. 23. Experimentally measured efficiency plots of the combined two-stage converter with varying (a) V_i and (b) V_o and the zoomed plots with varying (c) V_i and (d) V_o for the load range of 5–55 A.

in Fig. 22(b), the first-stage converter operating under resonant mode exhibits better efficiency at light load conditions. As much as around 10% of efficiency improvement is achieved at 48–8 V and 2 W through this mode change. The combined two-stage efficiency plots are presented in Fig. 23. The light-load efficiency improvement techniques of both the stages (i.e., resonant mode of operation of the first stage and single-phase operation of the second stage) are used up to 15 A of load current, beyond which both the stages are operated at their normal modes (i.e., DAB-mode operation of the first stage and three-phase operation of the second stage). This two-stage converter achieves peak efficiencies of 92.5%, 91.9%, and 91.3% at the input voltage of 36, 48, and 60 V, respectively, at $V_o = 1.2$ V and maintains above 89% efficiency over a wide load range of 5–50 A for the same output voltage. The peak efficiency reduces to 91% at 48–1 V.

The load transient performance of this two-stage converter is tested using a load board which has a fixed resistor to draw a fixed current and a stack of paralleled resistors in series with paralleled MOSFETs. The load transitions are performed by turning the paralleled MOSFETs ON and OFF. Fig. 24 shows the experimental results for load transitions from 5 to 55 A and vice versa at $V_i = 48$ V. The ac-coupled output voltage (V_o), sensed inductor current of phase 1 of second stage (i_{L1}), ac-coupled intermediate bus voltage (V_b), and the first-stage inductor current (i_{Lr}) are shown. The first-stage inductor current is measured using a positional current probe (Iprober 520). With $V_o = 1.2$ V,

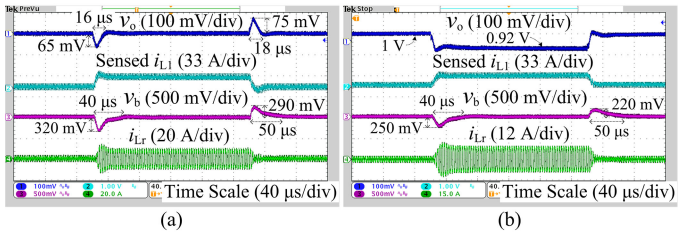

Fig. 24. Transient performance of the combined two stage with first stage in DAB mode and second stage in three phase at (a) $V_o = 1.2$ V with out AVP function and (b) $V_o = 1$ V with AVP function.

the undershoot and overshoot in V_o due to the load transitions are observed to be 65 mV with 16 μs settling time and 75 mV with 18 μs settling time, respectively. The intermediate bus voltage under this condition exhibits a maximum of 4% deviation and a worst-case settling time of 50 μs. As shown in Fig. 24(b), the converter produces a first and well-damped response with AVP function at $V_o = 1$ V. Here, the deviations in the intermediate bus voltage are reduced since the first stage experiences a lower power transient.

A performance comparison of the proposed two-stage 48-V VRM with the state-of-the-art solutions is given in Table III . It is seen that the proposed solution possesses relatively flat high efficiency profile and exhibits much faster dynamic response with a competitive power density. The converters in [7], [17], [18] show better peak and full load efficiency but suffer from poor light-load efficiency and slower transient performance. The quasi-resonant converter [7] is operated at a lower switching frequency, which reduces its control bandwidth and also degrades the power density. The sigma converter [17], [18] exhibits sluggish transient performance due to the use of an unregulated LLC resonant converter in the upper stage. Because of the same reason, the sigma converter also does not allow the 48-V bus voltage to vary over a wide range.

VIII. Conclusion

A new two-stage 48-V VRM topology based on a first-stage hybrid switched-capacitor converter has been proposed in this article. The first-stage converter uses only a small inductor and possesses very efficient regulation and ZVS ability. The ZVS analysis of the converter has been included in the article. An exact order discrete time model of the converter has also been developed in order to design a suitable controller with good dynamic performance. The resonant-mode operation to improve the light-load efficiency of the first-stage converter has also been discussed in the article. Thereafter, detailed design procedure of the two-stage converter has been presented. Finally, the experimental results are provided, which show that the converter maintains over 89% efficiency for most of the load range and hence possesses relatively flat high-efficiency profile compared to the state-of-the-art solutions. The converter also exhibits faster dynamic response against load step variations. The cost of the proposed solution is also low due to the use of silicon devices and fewer number of magnetic elements. Even though the first-stage

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED VRM TOPOLOGY WITH THE STATE-OF-THE-ART SOLUTIONS

Solutions	Operating Condition			I_{omax} (A)	Efficiency (%)			Power Density (W/in^3)	Transient Performance		
	V_{o}(V)	V_{i}(V)	f_{s}(MHz)		Peak	@ I_{omax}	@ $0.1 \times I_{\mathrm{omax}}$		ΔV_{o}(mV)	ΔI_{o}(A)	$t_{\mathrm{st1}}(\mu\mathrm{s})$
[7]	1.2	54	0.25	105	93.2	92.0	87.5	nr	45	50	40
[8]	1.2	48	1	45	90.6	86.6	84.3	310	63	42	18
[9]	1.1	48	0.325	60	90.0	88.5	70.0	231	nr	-	-
[10]	1.2	54	0.1	10	91.5	88.0	68.5	nr	nr	-	-
[13]	1.2	48	0.5	30	92.0	86.0	86.0	nr	200	5	30
[16]	1.0	48	0.333	100	90.9	87.0	82.0	440	nr	-	-
[17], [18]	1.0	48	1/0.6	80	93.4	91.6	85.0	420	50	20	120
[20]	1.8	48	1.6/1	120	91.0	89.0	88.5	nr	nr	-	-
Vicor [34], [35]	1.5	48	1.03/1.4	130	90.2	87.8	78.3	nr	nr	-	-
This Work	1.2	48	0.35/0.7	55	91.9	88.7	89.1	470	75	50	18

nr = not reported t_{st1} = settling time

converter uses more number of switches compared to the traditional inductor-based converters, its operation is simple as most of the switches (highly robust 25/30 V silicon devices) are simultaneously operating. Furthermore, the first-stage converter uses similar or less number of switches compared to other existing first-stage topologies. Therefore, the reliability of this converter is also comparable with the state-of-the-art solutions. The power density of this two-stage converter can be further improved by integrating all the switches of the first-stage converter into a single chip.

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