A Double-Modulation-Wave PWM With Reduced Dependency on Current Polarities for Dead-Time-Effect Elimination in Three-Level T-Type Converters

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***Abstract*—No dead-time is contained in the existing dead-time elimination pulsewidth modulation (PWM) for three-phase three-level T-type converters, where complementary drive pulses are allocated alternatively according to polarities of output currents. Consequently, the dead-time effect can be inherently avoided. However, the dependency on current polarities seriously limits its widespread application. Wrong current polarities, e.g., in a dynamic process, will lead to the output-voltage disappearance, thus aggravating the possible "algebraic loop" issue and impairing the stability of the system. In this article, in order to reduce the dependency on current polarities while retaining the characteristic of dead-time-effect elimination, a double-modulation-wave PWM is proposed by modifying the dead-time elimination PWM. Two modulation waves with a magnitude difference are adopted for generating underlap periods between complementary drive pulses, which can avoid the shoot-through failure and no dead-time effect will be generated. And to further simplify the implementation process, the two modulation waves are decomposed by introducing a magnitude-adjustment factor related to the current polarity. Whereas it is also due to the employment of two modulation waves, extra issues of overmodulation, single drive pulses, and a shorter underlap period may occur, which are analyzed in detail and the negative effect can be avoided. Finally, the proposed PWM is experimentally verified, showing the effectiveness on harmonic suppression and the reduced dependency on current polarities.**

***Index Terms*—Current polarities, dead-time effect, double-modulation-wave, pulse width modulation (PWM), three-level T-type converters.**

I. Introduction

THE dead-time for avoiding the shoot-through failure is usually inevitable in the well-known carrier-based [1], [2] or the space-vector [3]–[5] pulsewidth modulation (PWM) for three-phase three-level T-type converters. Correspondingly, the dead-time effect will bring extra voltage losses, low-frequency current harmonics, and reduced dc-link voltage utilizations [5], [6]. And, the dead-time effect will be more serious as the switching frequency goes higher.

The solutions to the dead-time effect of converters can be grouped into two categories. In the first solution, the converter employs a PWM with the dead-time, and the output current is "polluted" by the dead-time effect. Then, the dead-time effect is suppressed by dead-time compensation schemes. As indicated by previous publications [7]–[9], the generating mechanism of the dead-time effect in three-level converters is quite similar to that of two-level converters. Therefore, most of the dead-time compensation schemes for two-level converters can also be extended to three-level converters. For example, the scheme adjusting the magnitude of modulation waves according to current polarities can be adopted for compensating the dead-time effect of both two-level [10] and three-level [11] converters. However, the dead-time compensation is a "treatment after pollution" solution, which will lead to inevitable compensation errors.

In the second solution, rather than adopting compensation schemes after output currents are "polluted" by the dead-time, it would be better to directly adopt the dead-time elimination PWM [12] which can inherently avoid the dead-time effect. In the dead-time elimination PWM, complementary drive pulses are allocated alternatively according to polarities of output currents, thus the conventional dead-time for avoiding the shoot-through failure can be abandoned. Compared with PWM schemes containing dead-time, the dead-time elimination PWM has characteristics of low-voltage losses and output harmonics, high dc-link voltage utilization, and linear modulation region [13]–[15].

Most of the researches on the dead-time elimination PWM focus on implementation/control strategies and optimizations of current zero-crossings. The dead-time elimination PWM in [12] and [16] is implemented based on current polarities detected by auxiliary circuits in the power circuit of converters. The hysteresis control is investigated in [17] and [18] for supporting the operation of converters with the dead-time elimination PWM. In [19], the dead-time elimination PWM is combined with the

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discontinuous space-vector PWM, and implemented according to polarities of reference currents in a closed-loop control system. The current zero-crossing distortion is mitigated in [20] by applying the dead-time elimination PWM in a cascaded dual-buck inverter, where the amplitude of current ripples is reduced. In [21], to smooth the current zero-crossing distortion, an underlap period is added in the dead-elimination PWM when alternating the upper and lower drive pulses. In [22] and [23], the dead-time elimination PWM is applied in nonzero-crossing zones, while current distortions are mitigated by switching back to the conventional PWM with dead-time in zero-crossing zones.

Even though the above improvements have been put forward for implementation/control strategies and current zero-crossing optimizations, the dependency on current polarities is still the main limitation to the wide-spread application of the dead-time elimination PWM. Therefore, this article proposes a new double-modulation-wave PWM, aiming to reduce the dependency on current polarities while retaining the characteristic of dead-time-effect elimination.

In this article, the high dependency on current polarities is analyzed in the dead-time elimination PWM. Wrong current polarities will lead to the output-voltage disappearance, thus aggravating the possible "algebraic loop" issue and impairing the stability of the system. To reduce the dependency on current polarities, a double-modulation-wave PWM is proposed by modifying the dead-time elimination PWM. To further simplify the implementation process of the directly modified double-modulation-wave PWM, the two modulation waves are decomposed by introducing a magnitude-adjustment factor related to the current polarity. As a result of simplification, drive pules can be generated by specific modulation waves regardless of current polarities. Note that the double-modulation-wave PWM proposed in this article is different from the fast-processing modulation strategy [24] or the virtual-space-vector modulation [25] for eliminating neutral-point voltage oscillations, which also adopt two modulation waves. The two modulation waves with magnitude difference are adopted in this article for generating underlap periods to replace the dead-time for avoiding the shoot-through failure. However, it is also due to the employment of two modulation waves, extra issues of overmodulation, single drive pulses, and a shorter underlap period may occur, which will be analyzed in detail.

The contribution of this article lies in the new proposed double-modulation-wave PWM for three-level T-type converters, which have two main advantages. On the one hand, compared with existing dead-time compensation schemes [7]–[11], i.e., the "treatment after pollution" solutions, the proposed PWM can inherently avoid the dead-time effect without compensation errors. On the other hand, compared with the existing dead-time elimination PWM [12], the dependency on current polarities is effectively reduced in the proposed PWM. Even with wrong current polarities, a stable operation of the converter can still be achieved with only slightly increased output harmonics. In addition, simplifications are further made in this article by introducing a magnitude-adjustment factor varying with the current polarity, and issues brought by the employment of two modulation waves are addressed.

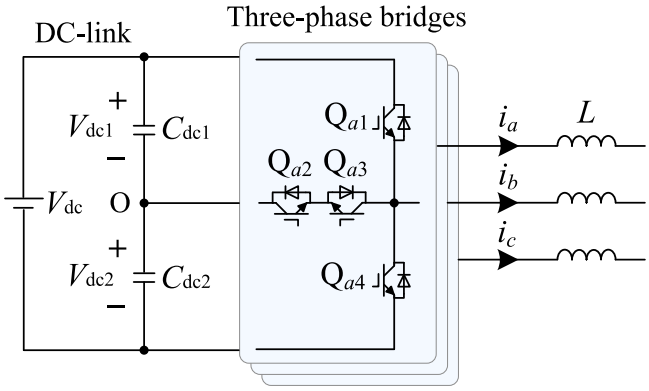

Fig. 1. Topology of three-phase three-level T-type converters.

The remaining parts of this article are structured as follows. Section II presents the modulation mechanism of the three-level dead-time elimination PWM. And the disappeared output-voltage with wrong current polarities and the "algebraic loop" issue are analyzed in Section III-A proposed double-modulation-wave PWM and its simplification is presented in Section IV. Section V shows the features of improved output voltage with wrong current polarities. Then, the overmodulation and zero-crossing drive pulses in the double-modulation-wave PWM are presented in Section VI. Section VII presents an application of the proposed double-modulation-wave PWM in the grid-connected converter. The experimental verifications are presented in Section VIII. Finally, Section IX concludes the article.

II. Modulation Mechanism of the Three-Level Dead-Time Elimination PWM

The topology of the three-phase three-level T-type converter with IGBTs is shown in Fig. 1. $V_{\rm dc}$ is the dc-link voltage; $C_{\rm dc1}$ and $C_{\rm dc2}$ are the upper and lower dc-link capacitances with voltages of $V_{\rm dc1}$ and $V_{\rm dc2}$; i_a, i_b, and i_c are the three-phase output currents. In the three-phase bridges, only the topology of Phase A with four IGBTs Q_{a1}~Q_{a4} is presented to make the figure clear. And the converter can be connected to various loads through the L filter or other filters.

The current boosting and freewheeling stages in Phase A of the T-type converter are shown in Fig. 2, where four cases are divided according to different polarities of the modulation wave $u_a{}^*$ and the output current i_a. The current boosting stage can actively increase the output current, while in the current freewheeling stage the output current is reactively freewheeled. In Fig. 2, S_{a1}~S_{a4} are the corresponding drive pulses of IGBTs Q_{a1}~Q_{a4}, and the low and high states of drive pulses are marked as "0" and "1," respectively.

In order to avoid the shoot-through failure of the converter, S_{a1} and S_{a3}, as well as S_{a2} and S_{a4}, should not be simultaneously set as "1." It should be noted that the drive pulses marked as "0 or 1" in Fig. 2 are "redundant states," which will neither cause the shoot-through failure nor affect the output voltage. Taking Fig. 2(a) when $u_a{}^* \geq 0$ and $i_a < 0$ as an example, in the current

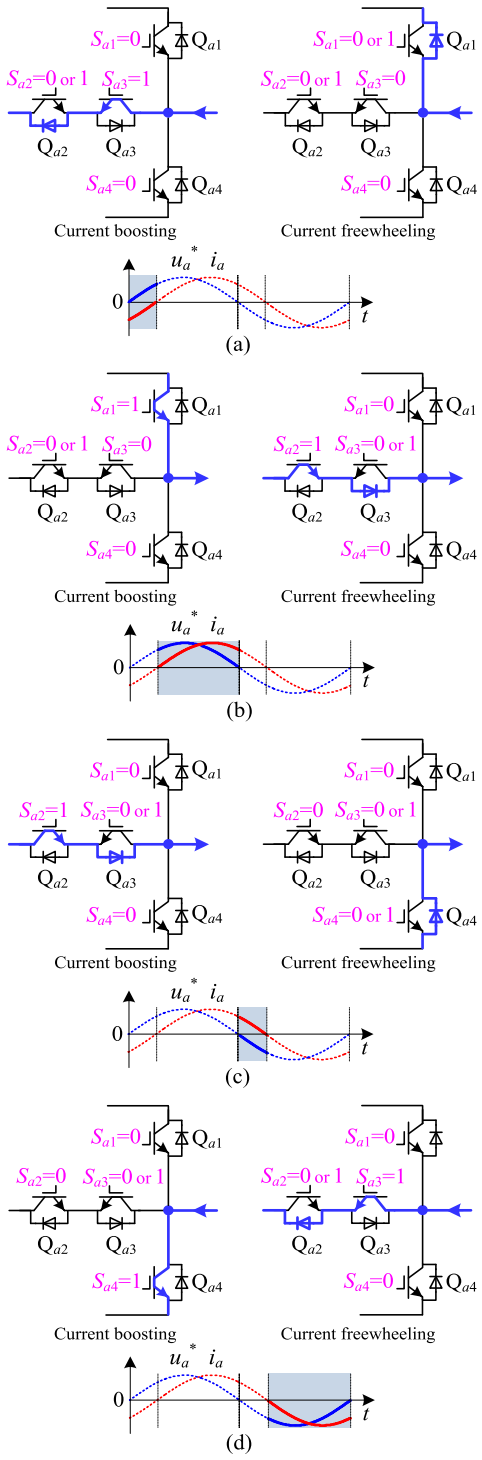

Fig. 2. Current boosting and freewheeling stages with different polarities of modulation wave and output current. (a) $u_a^* \geq 0$ and $i_a < 0$. (b) $u_a^* \geq 0$ and $i_a \geq 0$. (c) $u_a^* < 0$ and $i_a \geq 0$. (d) $u_a^* < 0$ and $i_a < 0$.

boosting stage, in order to output the right current and voltage, S_{a1} and S_{a4} should stay at "0" to block the current, and S_{a3} should be set as "1" to boost the output current. Redundant states exist in S_{a2}, i.e., neither shoot-through failure nor output-voltage variation will be caused by the S_{a2} state of "0" or "1." Meanwhile, in the current freewheeling stage, S_{a3} and S_{a4} should stay

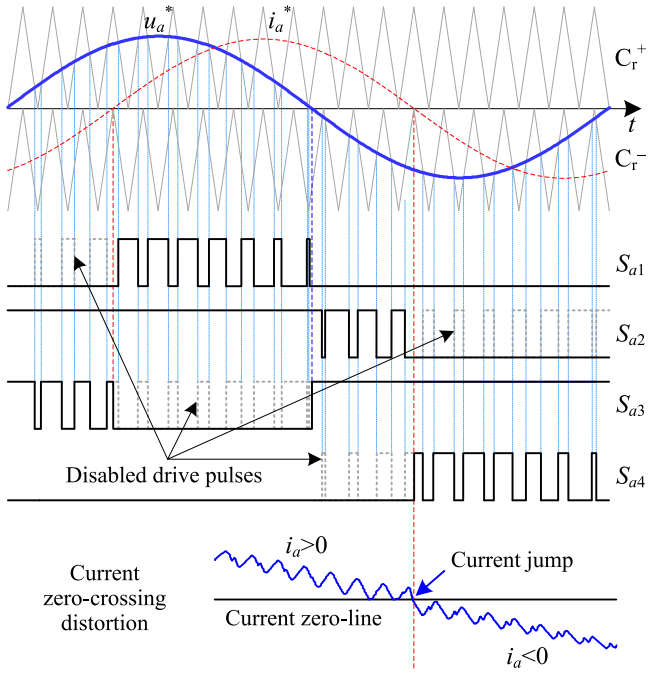

Fig. 3. Modulation mechanism and the current zero-crossing distortion of the dead-time elimination PWM in Phase A.

at "0" to block the current. Redundant states exist in S_{a1} and S_{a2} which will not affect the current freewheeling path.

To reduce the switching number of drive pulses while keeping the output voltage unchanged, redundant states in drive pulses can be eliminated. Through the elimination of redundant states, a carrier-based PWM with an auxiliary reference current i_a^* can be obtained as shown in Fig. 3. The basic mechanism of generating drive pulses is the same with the conventional carrier-based PWM [26]. Drive pulses are generated by comparing the modulation wave u_a^* with two cascaded carriers C_r^+ and C_r^-. Particularly, the generated drive pulses are alternately disabled according to the polarity of the reference current i_a^*, i.e., when $i_a^* < 0$, S_{a1} and S_{a2} are disabled, and when $i_a^* \geq 0$, S_{a3} and S_{a4} are disabled.

Note that the output current i_a with high-frequency ripples cannot be directly adopted for judging the polarity. In order to avoid the influence of high-frequency ripples and provide accuracy polarities for the drive-pulse allocation, the fundamental current extracted from the output current is adopted as the reference current i_a^* in the modulation.

The elimination of redundant states brings prominent advantages in the modulation shown in Fig. 3. As seen, S_{a1} and S_{a3}, as well as S_{a2} and S_{a4}, will never simultaneously equal to "1," which means the shoot-through failure can be inherently avoided. Therefore, the conventional dead-time [5] between complementary drive pulses (S_{a1} and S_{a3}, S_{a2} and S_{a4}) can be abandoned. And, no dead-time effect is generated thus decreasing the low-frequency output current/voltage distortions. With the characteristic of no dead-time, the PWM shown in Fig. 3 is thus designated as the "dead-time elimination PWM" [12]. In addition, as seen in Fig. 3, each moment only one of the four

drive pulses switches, so that the driver loss can be effectively reduced.

One issue in the dead-time elimination PWM is the zero-crossing distortion in the output current [20], [21], which is presented at the bottom of Fig. 3. The current zero-crossing, where i_a crosses the zero-line from positive to negative, is analyzed as an example. As seen in Fig. 3, when $i_a>0$ near the zero-crossing, since S_{a4} is disabled, i_a cannot actively decrease and cross the zero-line, therefore it can only fluctuate on the zero-line making current ripples always positive. Similarly, when $i_a < 0$ near the zero-crossing, the current ripples are always negative with the disabled S_{a2}. Due to the drive-pulse alternation, there is not a gradual transition for current ripples to across the zero-line, thus a current jump is generated at the zero-crossing.

Besides the zero-crossing distortion, the high dependency on current polarities seriously limits the widespread application of the dead-time elimination PWM, which will be analyzed in detail in the next section.

III. Disappeared Output-Voltage With Wrong Current Polarities and the "Algebraic Loop" in Dead-Time Elimination PWM

A. Output-Voltage Disappearance Caused by Wrong Current Polarities

Ideally, in the steady state of a converter control system, the output current should track the reference current within an acceptable error, and they should have the same polarities. However, when the converter system is started or in other dynamic processes with varying currents, a large dynamic-state error will inevitably exist between the reference current and the output current, thus causing a large polarity error between them. And the polarity error will cause the output voltage disappearance in the dead-time elimination PWM, which will be analyzed in this section.

In this article, in order to simplify the analysis with wrong current polarities, a sinusoidal reference current $i_a{}^*$ with a wrong polarity is adopted, which is used for allocating drive pulses. Two wrong-polarity areas are formed in Fig. 4, where the polarity of the reference current $i_a{}^*$ is different from the real current polarity of i_a'. In practice, arbitrary wrong current polarities will occur, which is inevitable in dynamic processes with varying currents. However, even with arbitrary wrong current polarities, the analysis on the output voltage in the two wrong-polarity areas of Fig. 4 is still tenable.

Compared with Fig. 3, in the wrong-polarity area I of Fig. 4, extra drive pulses are disabled in S_{a1}, while extra drive pulses are enabled in S_{a3}. Nevertheless, when $u_a{}^* \geq 0$ and $i_a \geq 0$, S_{a1} is the active drive pulse for generating output voltage rather than S_{a3}. Therefore, no output voltage is generated in the wrong polarity area I. Similarly in the wrong-polarity area II of Fig. 4, no output voltage is generated either, since the active drive pulses for generating output voltage is S_{a4} ($u_a{}^* < 0$ and $i_a < 0$) which however is disabled due to the wrong current polarity of $i_a{}^*$.

Since the polarity error between the reference current and the output current is inevitable, e.g., in a dynamic process, the disappeared output voltage in the wrong-polarity area will cause serious harmonics in output currents and impairing the stability of the system. And, the "algebraic loop" issue analyzed in the next section will also be aggravated.

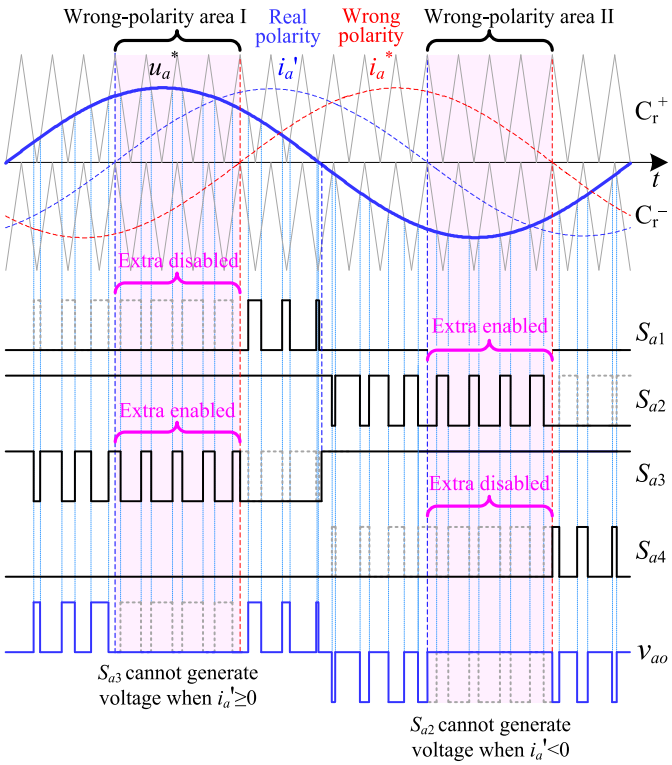

Fig. 4. Disappeared output voltage with a wrong current polarity in the dead-time elimination PWM.

B. "Algebraic Loop" for Implementing the Dead-Time Elimination PWM

Due to the requirement of current polarity, the dead-time elimination PWM can cause a possible "algebraic loop," which can even destabilize the operation of the converter.

Fig. 5 shows a control diagram with a direct feedback loop of output currents for implementing the dead-time elimination PWM. As seen in Fig. 5(a), the three-phase output currents i_a, i_b, and i_c are measured by current sensors, and directly feeding back to the modulation block. The modulation block has two groups of inputs: *Input 1* represents the three-phase modulation waves $u_a{}^*$, $u_b{}^*$, and $u_c{}^*$, and *Input 2* represents the measured three-phase output currents i_a, i_b, and i_c. Fig. 5(b) shows an equivalent model of the control diagram with the direct feedback loop of output currents, where the power circuit and the modulation block are together taken as the "plant" of the closed loop. As seen in Fig. 5(b), the output currents are both input and output of the "plant." In one control period, the "plant" needs the value of inputs (three-phase currents and modulation waves) to compute its outputs (three-phase currents), thus forming the "algebraic loop" [27], [28].

Such a converter system with the "algebraic loop" cannot reach a steady operation state or even cannot normally start. Taking the start process with zero currents for example, in the

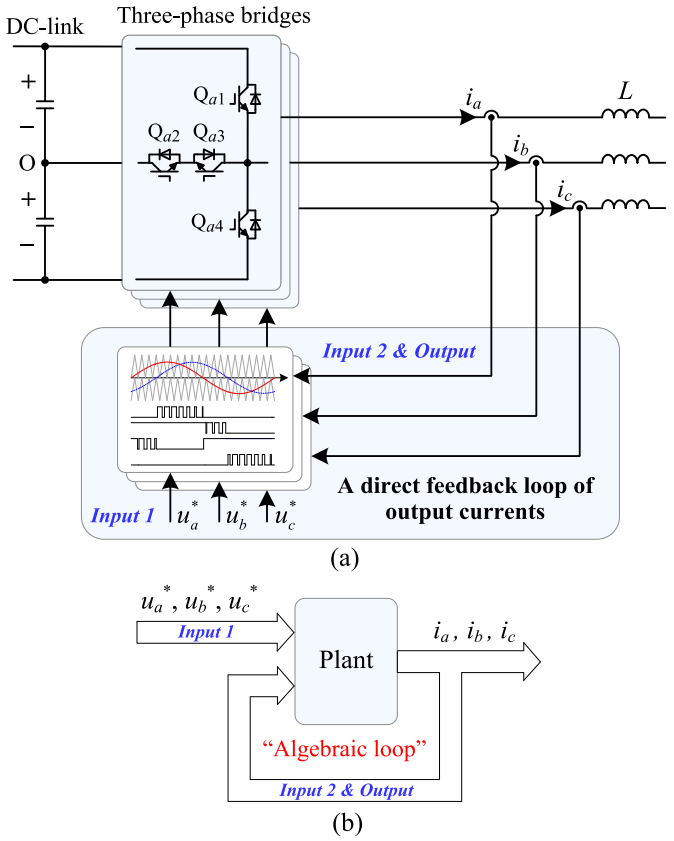

Fig. 5. "Algebraic loop" for implementing the dead-time elimination PWM. (a) Control diagram with a direct feedback loop of output currents. (b) "Algebraic loop" equivalent model.

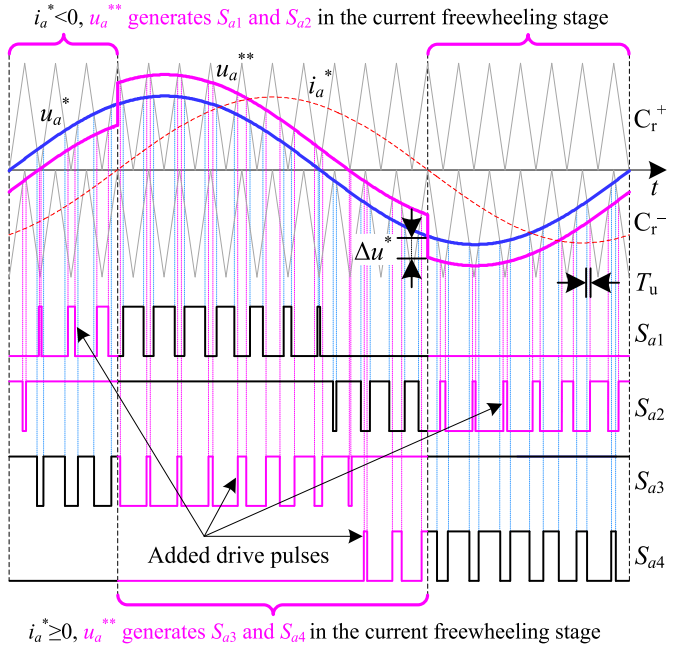

Fig. 6. Proposed double-modulation-wave PWM with reduced dependency on current polarities for dead-time-effect elimination.

"algebraic loop" system of Fig. 5(a), detecting zero currents by current sensors can inevitably cause wrong current polarities. And as analyzed in previous Section III-A, with wrong current polarities no output voltage will be generated by the dead-time elimination PWM. Consequently, the output currents will retain at zero, leading to the start-failure of the converter. Therefore, rather than using a direct feedback of output currents, indirect-feedback control schemes should be adopted to implement the dead-time elimination PWM [17]–[21].

IV. Proposed Double-Modulation-Wave PWM and its Simplification

A. Proposed Double-Modulation-Wave PWM With Reduced Dependency on Current Polarities for Dead-Time-Effect Elimination

In this section, in order to reduce the dependency on current polarities while retaining the characteristic of dead-time-effect elimination, a new double-modulation-wave PWM will be proposed.

Rather than abandoning all the redundant states, the redundant states in the current freewheeling stage are retained in drive pulses. However, a conflict exists between the shoot-through failure and the dead-time effect. On the one hand, simply adding the redundant states in the current freewheeling stage can cause the shoot-through failure if no dead-time is inserted; on the other hand, if the conventional dead-time is inserted, the dead-time effect will be inevitable. To address the conflict, an extra modulation wave is introduced, whose magnitude is adjusted according to the current polarity. Two modulation waves are together adopted to generate underlap periods between the added drive pulses in the current freewheeling stage and the original drive pulses of the dead-time elimination PWM. The underlap period can avoid the shoot-through failure and no dead-time effect will be generated.

The proposed double-modulation-wave PWM is shown in Fig. 6. As seen, besides the original modulation wave $u_a{}^*$, an extra modulation wave $u_a{}^{**}$ is added for generating redundant drive pulses in the current freewheeling stage. On the one hand when $i_a{}^* \geq 0, u_a{}^*$ still generates S_{a1} and S_{a2} like in the dead-time elimination PWM, while $u_a{}^{**}$ generates S_{a3} and S_{a4} in the current freewheeling stage; on the other hand when $i_a{}^* < 0, u_a{}^*$ still generates S_{a3} and S_{a4}, while $u_a{}^{**}$ generates S_{a1} and S_{a2} in the current freewheeling stage. The extra modulation wave $u_a{}^{**}$ is generated based on the original modulation wave $u_a{}^*$. When $i_a{}^* \geq 0$, the magnitude of $u_a{}^{**}$ is increased by Δu^* based on $u_a{}^*$; and when $i_a{}^* < 0$, the magnitude of $u_a{}^{**}$ is decreased by Δu^* based on $u_a{}^*$. Due to the magnitude difference of Δu^* between $u_a{}^{**}$ and $u_a{}^*$, underlap periods T_u are generated between S_{a1} and S_{a3}, as well as between S_{a2} and S_{a4}, so that the shoot-through failure can be avoided.

Note that the proposed double-modulation wave PWM in Fig. 6 is developed based on the dead-time elimination PWM in Fig. 3, which inherently has no dead-time effect. In Fig. 6, the width of the added drive pulses are $2T_u$ narrower than those of the disabled drive pulses in Fig. 3, so that the shoot-through failure can be avoided. Moreover, the added drive pulses in

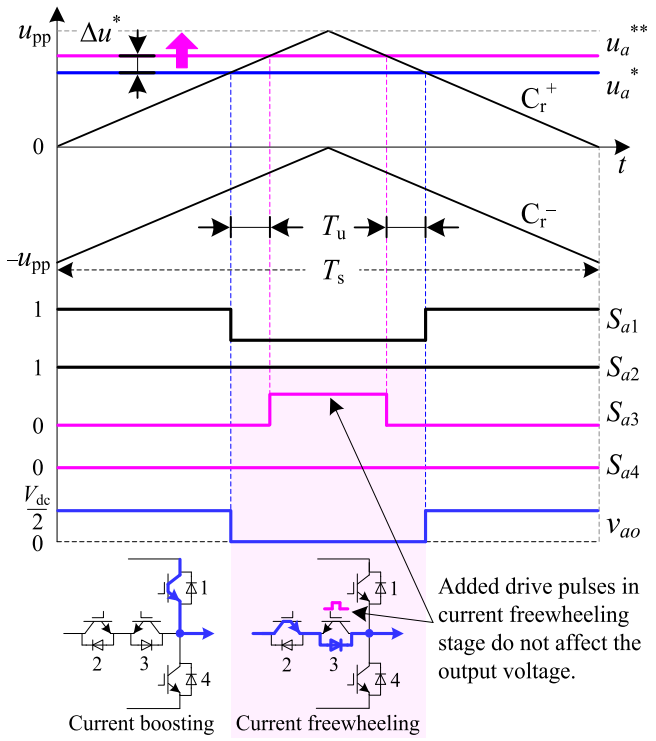

Fig. 7. Illustration of the double-modulation-wave PWM in one switching period when $u_a^* \geq 0$ and $i_a^* \geq 0$.

Fig. 6 are in the current freewheeling stage, which will not affect the original output voltage of the dead-time elimination PWM. Therefore, the characteristic of no dead-time effect is reserved in the proposed double-modulation-wave PWM.

In order to further illustrate the double-modulation-wave PWM, one switching period of Fig. 6 when $u_a^* \geq 0$ and $i_a^* \geq 0$ is zoomed-in as shown in Fig. 7. As seen, besides S_{a1} and S_{a2} originally generated from u_a^*, one extra pulse in S_{a3} is generated by comparing u_a^{**} with C_r^+, and S_{a4} remains at "0" by comparing u_a^{**} with C_r^-. With the magnitude difference of Δu^* between u_a^{**} and u_a^*, underlap periods T_u are generated between the high states of S_{a1} and S_{a3}, so that the shoot-through failure can be avoided.

To help with analyzing the effect of drive pulses on the output voltage, two power circuits in current boosting and freewheeling stages are attached at the bottom of Fig. 7. It can be noted that the added drive pulse in S_{a3} is in the current freewheeling stage, thus the current flowing path and the output voltage will not be affected. The shape of the output voltage v_a is still the same with that of the active drive pulse S_{a1} generated by comparing u_a^* with C_r^+, i.e., the output voltage of the converter is the same with that of the dead-time elimination PWM.

According to the characteristics of similar triangles in Fig. 7, the increased magnitude Δu^* of modulation wave can be derived as

$$\Delta u^* = \frac{2T\mathrm{u} \cdot u\mathrm{pp}}{T\mathrm{s}} \tag{1}$$

where u_{pp} is the peak-to-peak amplitude of the carrier, and T_s is the switching period. As seen in (1), the increased magnitude Δu^* is proportional to the underlap period T_u and inversely proportional to the switching period T_s. Therefore, in the proposed double-modulation-wave PWM, a large underlap period T_u or a high switching frequency (with a short T_s) can increase the possibility of the overmodulation. Nevertheless, the overmodulation can only happen in the extra modulation wave u_a^{**}, causing the disappearance of the added redundant drive pulses in the current freewheeling stage, and output voltage will not be affected. The overmodualtion issue will be analyzed later in Section VI-A.

Note that, different from the conventional dead-time which can cause the dead-time effect, the underlap period T_u does not affect the output voltage. Therefore, the added underlap period can be set equal to or larger than the normal dead-time. Considering a larger underlap period will increase the possibility of the overmodulation, an underlap period equal to the normal dead-time is therefore recommended in this article.

In the double-modulation-wave PWM, the added drive pulses in the current freewheeling stage do not affect the output voltage and no dead-time-effect is generated. In addition, new features of improved output voltage with wrong current polarities and mitigated "algebraic loop" issue can also be brought, which will be analyzed later in Section V.

B. Simplification of the Proposed Double-Modulation-Wave PWM

The proposed double-modulation-wave PWM presented in Fig. 6 is a direct modification of the dead-time elimination PWM. In this section, the two modulation waves will be further decomposed to simplify the directly modified PWM.

The correspondence between modulation waves and drive pules in the directly modified double-modulation-wave PWM is illustrated in Fig. 8(a). As seen, according to different current polarities, the extra added modulation wave u_a^{**} is adjusted by $\pm\Delta u^*$ based on the original modulation wave u_a^*. With different current polarities, S_{a1} and S_{a2}, as well as S_{a3} and S_{a4}, are generated by different modulation waves. Regarding the generation of S_{a1} and S_{a2}, when $i_a^* \geq 0$, u_a^* is employed for comparing with cascaded carriers; when $i_a^* < 0$, a different modulation wave of u_a^{**} is employed. Meanwhile, the generation of S_{a3} and S_{a4} employs u_a^{**} and u_a^*, respectively, when $i_a^* \geq 0$ and $i_a^* < 0$.

To simplify the implementation process of the double-modulation-wave PWM, the two modulation waves u_a^* and u_a^{**} in Fig. 8(a) are transformed as u_{a12}^* and u_{a34}^* in Fig. 8(b). Both the magnitudes of u_{a12}^* and u_{a34}^* are adjusted according to the polarity of the reference current i_a^*. In return, drive pules can be generated by specific modulation waves regardless of the polarity of i_a^*. As seen in Fig. 8(b), no matter $i_a^* \geq 0$ or $i_a^* < 0$, S_{a1} and S_{a2} are always generated by u_{a12}^*, and S_{a3} and S_{a4} are always generated by u_{a34}^*.

It should be noted that the above modification only simplifies the implementation process of the double-modulation-wave PWM. The overall shape of the two modulation waves in Fig. 8(a) is still the same with that in Fig. 8(b), and the same drive pulses will be generated. Therefore, equivalent output currents and voltages can be guaranteed through the simplification.

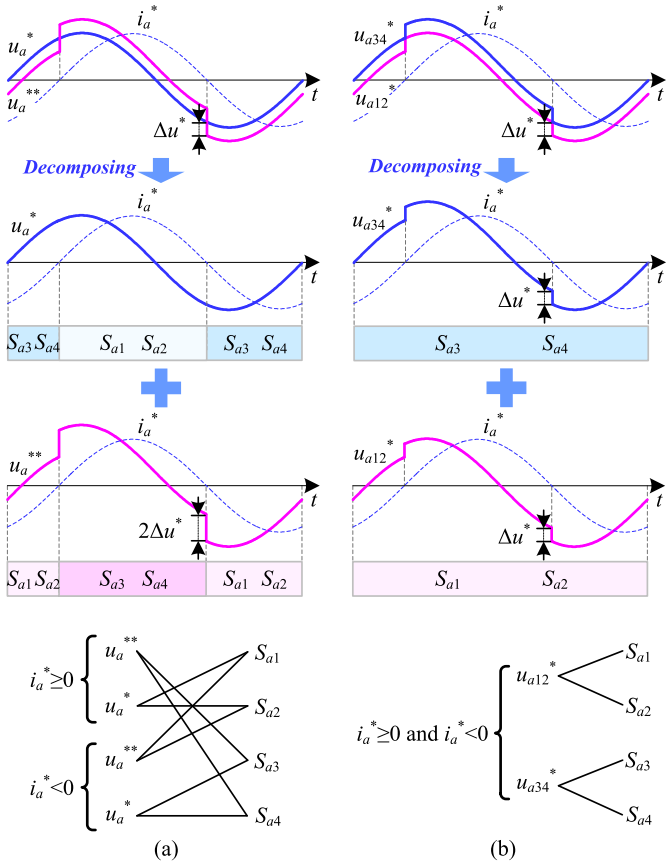

Fig. 8. Correspondence between modulation waves and drive pules (a) in the directly modified double-modulation-wave PWM and (b) in the simplified double-modulation-wave PWM.

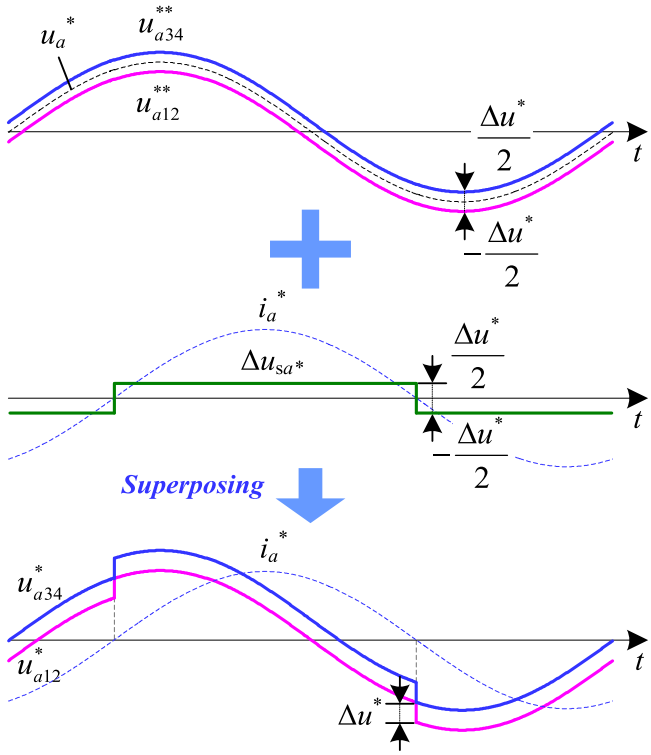

Fig. 9. Deriving process of the two modulation waves with the introduced magnitude-adjustment factor $\Delta u_{sa}{}^{*}$.

According to the simplification shown in Fig. 8(b), with different current polarities, the two modulation waves $u_{a12}{}^{*}$ and $u_{a34}{}^{*}$ can be expressed as

$$\begin{cases} u_{a12}^{*} = u_{a}^{*} \\ u_{a34}^{*} = u_{a}^{*} + \Delta u^{*} \end{cases} \quad (i_{a}^{*} \geq 0)$$

$$\begin{cases} u_{a12}^{*} = u_{a}^{*} - \Delta u^{*} \\ u_{a34}^{*} = u_{a}^{*} \end{cases} \quad (i_{a}^{*} < 0). \tag{2}$$

A magnitude-adjustment factor $\Delta u_{sa}{}^{*}$ varying with the current polarity is introduced and given by

$$\begin{cases} \Delta u_{sa}^{*} \frac{\Delta u}{2} & (i_{a}^{*} \geq 0) \\ \Delta u_{sa}^{*} \frac{\Delta u}{2} & (i_{a}^{*} \geq 0). \end{cases} \tag{3}$$

Subtracting $\Delta u_{sa}{}^{*}$ from $u_{a12}{}^{*}$ and $u_{a34}{}^{*}$ in (2), two modulation waves $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ independent of current polarities can be derived as

$$\begin{cases} u_{a12}^{**} = u_{a}^{*} - \frac{\Delta u^{*}}{2} \\ u_{a34}^{**} = u_{a}^{*} + \frac{\Delta u^{*}}{2} \end{cases} \quad (i_{a}^{*} \geq 0 \text{ and } i_{a}^{*} < 0). \tag{4}$$

The above derivation from (2) to (4) indicates that $u_{a12}{}^{*}$ and $u_{a34}{}^{*}$ can be formed by superposing $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ (independent of the current polarities) with a magnitude-adjustment factor $\Delta u_{sa}{}^{*}$ (varying with the current polarity). Fig. 9 shows the deriving process of the two modulation waves. First, $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ are produced based on $u_{a}{}^{*}$ by decreasing and increasing a magnitude of $\Delta u^{*}/2$, respectively. Then, the magnitude-adjustment factor $\Delta u_{sa}{}^{*}$ is generated according to the current polarity, i.e., $\Delta u_{sa}{}^{*} = \Delta u^{*}/2$ when $i_{a}{}^{*} \geq 0$, and $\Delta u_{sa}{}^{*} = -\Delta u^{*}/2$ when $i_{a}{}^{*} < 0$. Afterwards, $u_{a12}{}^{*}$ and $u_{a34}{}^{*}$ are formed by superposing $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ with $\Delta u_{sa}{}^{*}$, which are finally used for comparing with cascaded carriers to generate drive pulses.

V. Improved Output Voltage With Wrong Current Polarities in Double-Modulation-Wave PWM

Previously, the analysis on the dead-time elimination PWM in Section III-A indicates that wrong current polarities can result in the output-voltage disappearance and aggravate the "algebraic loop" issue. In this section, the output voltage of the proposed double-modulation-wave PWM will be analyzed in the same situation with wrong current polarities to verify the improvement.

As seen in the double-modulation-wave PWM of Fig. 10, two wrong-polarity areas are marked, where the real polarity of the output current contained in i_a' is different from that of the reference current $i_{a}{}^{*}$. In wrong-polarity area I, the real polarity of i_a' should be positive, but a wrong negative polarity is provided in $i_{a}{}^{*}$. According to the implementation process shown in Fig. 9, with a wrong negative current polarity, a magnitude-adjustment factor $\Delta u_{sa}{}^{*} = -\Delta u^{*}/2$ will be generated, other than $\Delta u_{sa}{}^{*} = \Delta u^{*}/2$ with the right positive polarity. Therefore, in Fig. 10, $u_{a12}{}^{*}$ and $u_{a34}{}^{*}$ are erroneously decreased by Δu^{*}. In each

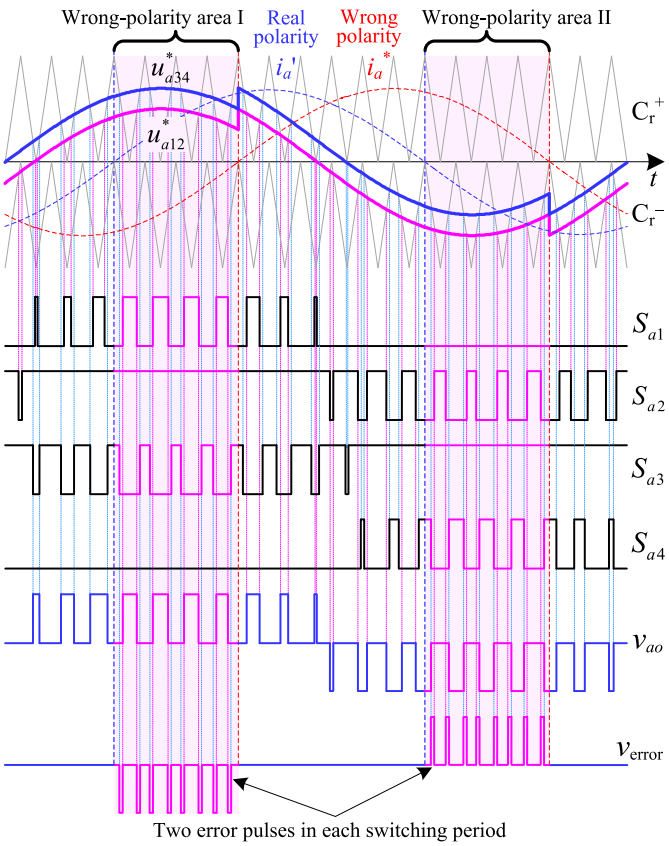

Fig. 10. Output voltage errors of the double-modulation-wave PWM with a wrong current polarity.

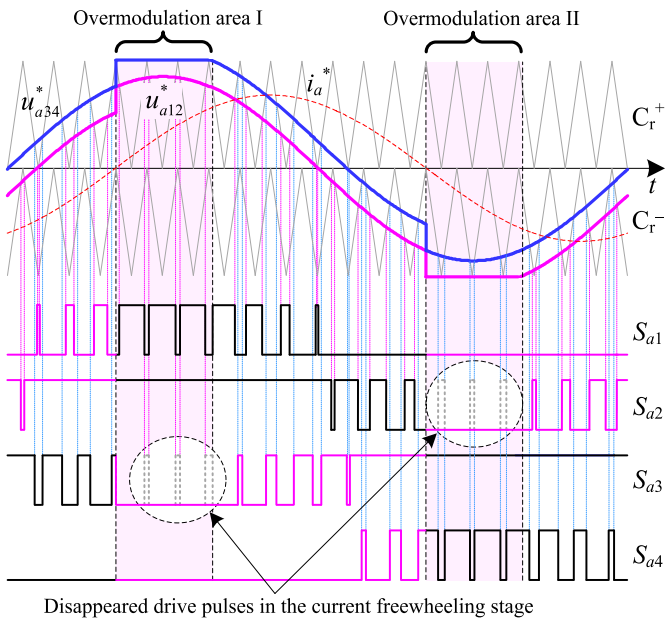

Fig. 11. Illustration of the overmodulation in Phase A of the double-modulation-wave PWM with a modulation index smaller than but close to 1.

switching period, two negative voltage-error pulses with the width of T_u and the amplitude of $-V_{dc}/2$ will be generated. Similarly, in wrong-polarity area II, two positive voltage-error pulses with the amplitude of $V_{dc}/2$ will be generated in each switching period.

In the situation with wrong current polarities, compared with the dead-time elimination PWM causing the output-voltage disappearance, the double-modulation-wave PWM only generates two voltage-error pulses in each switching period. The output voltage can be significantly improved in the dynamic process where current-polarity errors are inevitable. Only slight current distortions will be caused by the voltage-error pulses, and a much better dynamic performance will be provided for the operation of converters. Therefore, the dependency on current polarities is effectively reduced in the double-modulation-wave PWM. And the "algebraic loop" presented in Section III-B can also be well avoided, which is caused by the high dependency on current polarities.

VI. Overmodulation and Zero-Crossing Drive Pulses in Double-Modulation-Wave PWM

A. Analysis of Overmodulation in the Double-Modulation-Wave PWM

With a large modulation index, the magnitude adjustment in the two modulation waves can lead to a possible overmodulation, which will be analyzed in this section.

Fig. 11 presents the overmodulation phenomenon in Phase A with a modulation index smaller than but close to 1. Due to the magnitude difference of the two modulation waves $u_{a12}{}^*$ and $u_{a34}{}^*$ varying the current polarity, two overmodulation areas occur leading to the flat tops respectively in $u_{a12}{}^*$ and $u_{a34}{}^*$. In the overmodulation area I shown in Fig. 11, the magnitude of $u_{a34}{}^*$ is larger than $u_{a12}{}^*$, a flat top appears in $u_{a34}{}^*$ so that its magnitude can retain within the upper carrier $C_r{}^+$, while $u_{a12}{}^*$ retains unchanged. Consequently, the corresponding drive pulses in S_{a3} will disappear, which are caused by the flat top of $u_{a34}{}^*$. Meanwhile, the original drive pulses in S_{a1} generated by $u_{a12}{}^*$ are not affected by the overmodulation. It should be noted that the disappeared drive pulses in S_{a3} lie in the current freewheeling stage, therefore the overmodulation will not affect the output voltage. Similarly, in overmodulation area II, the absolute magnitude of $u_{a12}{}^*$ is larger than $u_{a34}{}^*$ (negative polarity). The flat top in $u_{a12}{}^*$ leads to the disappearance of drive pulses in S_{a2}, which are exactly in the current freewheeling stage. And the disappearance of S_{a2} will not affect the output voltage either.

As analyzed above, the overmodulation in the double-modulation-wave PWM can only cause drive pulses disappear in the current freewheeling stage, while the original drive pulses for generating the output voltage retain unchanged. The linearity in the output voltage is not affected by the overmodulation, and no additional loss is generated by the clamping in overmodulation areas. Therefore, it is also indicated that the proposed double-modulation-wave PWM can still achieve a maximum linear-modulation index of 1, which is calculated using the original modulation wave of $u_a{}^*$, i.e., dividing the amplitude of $u_a{}^*$ by the amplitude of the carrier $C_r{}^+$.

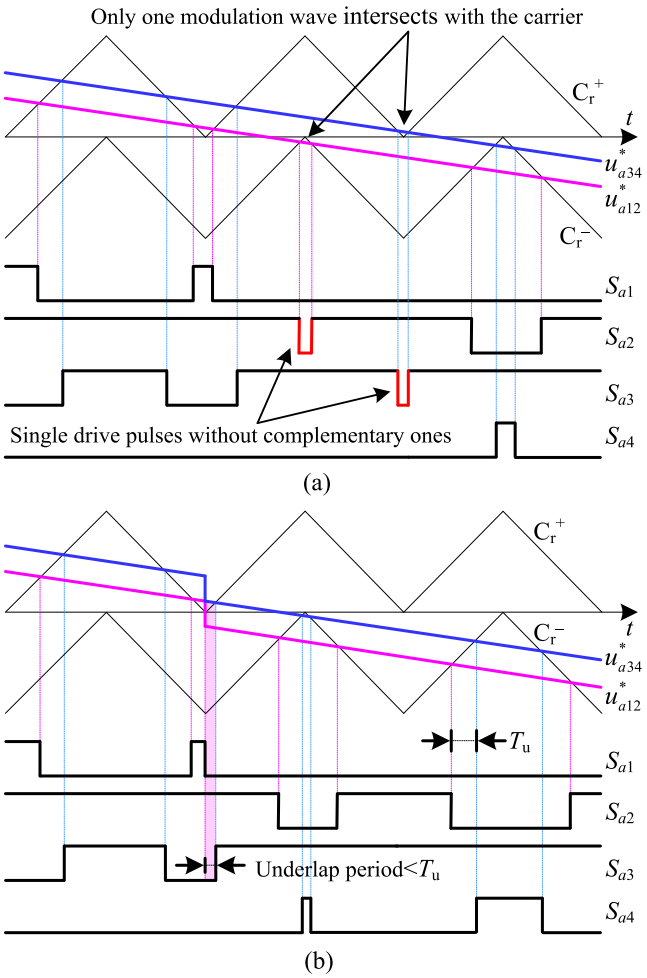

Fig. 12. Drive pulses around zero-crossings of modulation waves. (a) Single drive pulses without complementary ones. (b) Underlap period shorter than T_u.

B. Analysis of Zero-Crossing Drive Pulses in the Double-Modulation-Wave PWM

In the proposed double-modulation-wave PWM, due to the employment of two modulation waves, single drive pulses without complementary ones and an underlap period shorter than T_u may occur around zero-crossings of modulation waves, which are illustrated in Fig. 12(a) and (b), respectively.

Around the zero-crossings of the two modulation waves, three switching periods are shown in Fig. 12(a). In the middle switching period, $u_{a12}{}^*$ intersects with $C_r{}^-$ generating a single negative drive pulse in S_{a2}, but no complementary drive pule is generated in S_{a4}. The single drive pulse in S_{a2} may generate a narrow voltage-error pulse related to the output current polarity, but it cannot cause the shoot-through failure since S_{a4} remains in the low state. Similarly, on the right of the single pulse generated by $u_{a12}{}^*$, another single drive pulse is generated in S_{a3} by comparing $u_{a34}{}^*$ with $C_r{}^+$, while no complementary drive pule is generated in S_{a1}. Given the two single drive pules do not cause the shoot-through failure, their negative effect can be neglected.

Another case with a shorter underlap period is shown in Fig. 12(b), where the magnitudes of modulation waves are adjusted exactly at the bottom of one carrier. In this case, both the two modulation waves have intersections with carriers in each switching period. Therefore, the single drives pulse in Fig. 12(a) is not generated. However, an underlap period shorter than T_u is generated due to the magnitude decrement in the two modulation waves. The shorter underlap period may cause a possible shoot-through failure. Therefore, as a shoot-through protection of converters, the minimum length of the underlap period should be limited to T_u in the software program or in the designed drive circuit.

VII. Application of the Proposed Double-Modulation-Wave PWM in the Grid-Connected Converter

The proposed double-modulation-wave PWM can be inserted to existing closed-loop control systems conveniently. As an example of practical applications, the proposed PWM is applied to a grid-connected converter in this section. And to extract precise polarities from currents with high-frequency harmonics, the double second-order generalized integrator frequency-locked loop (DSOGI-FLL) [21], [29]–[30] is adopted, which has features of noise-attenuation and frequency-adaptability. The diagrams of the DSOGI-FLL-based double-modulation-wave PWM and the grid-connected converter are shown in Fig. 13(a) and (b), respectively.

As seen in Fig. 13(a), first, the three-phase currents i_a, i_b, and i_c with high-frequency harmonics are measured as i_{am}, i_{bm}, and i_{cm} by current sensors. Then, the measured three-phase currents are transformed into $i_{\alpha m}$ and $i_{\beta m}$, and a DSOGI-FLL is adopted to extract the fundamental components $i_\alpha{}^*$ and $i_\beta{}^*$. $i_\alpha{}^*$ and $i_\beta{}^*$ are further reversely transformed as the three-phase reference currents of $i_a{}^*$, $i_b{}^*$, and $i_c{}^*$, which provide the current-polarity information for the magnitude-adjustment factors of $\Delta u_{sa}{}^*$, $\Delta u_{sb}{}^*$, and $\Delta u_{sc}{}^*$. The magnitude-adjustment factors are used for generating three-phase modulation waves. Taking the modulation in Phase A for example, $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ are first generated from $u_a{}^*$ with $\pm\Delta u^*/2$ adjustments. Then, $u_{a12}{}^*$ and $u_{a34}{}^*$ are formed by superposing $u_{a12}{}^{**}$ and $u_{a34}{}^{**}$ with $\Delta u_{sa}{}^*$. Through the comparison with cascaded carriers, drive pulses $S_{a1}\sim S_{a4}$ are generated for switching devices.

The grid-connected converter in Fig. 13(b) is controlled by the commonly used feedforward decoupling scheme with PI controllers in the dq frame [31]. As seen, the DSOGI-FLL-based double-modulation-wave PWM of Fig. 13(a) is inserted to generate the drive pulses for three-phase bridges. The original modulation waves $u_a{}^*$, $u_b{}^*$, and $u_c{}^*$ are regulated by the current loop. In addition, the angle θ of the grid voltage is obtained by a phase-locked loop [32] to implement the grid-voltage oriented vector control. The scheme show in Fig. 13(b) will be finally validated by grid-connected experiments in the next section.

In addition, given the dead-time effect has a positive correlation with the switching frequency, it would be better to apply the proposed PWM in three-level converters with high-switching frequencies (e.g., >20 kHz), so that the advantage of its characteristic of dead-time-effect elimination can be taken.

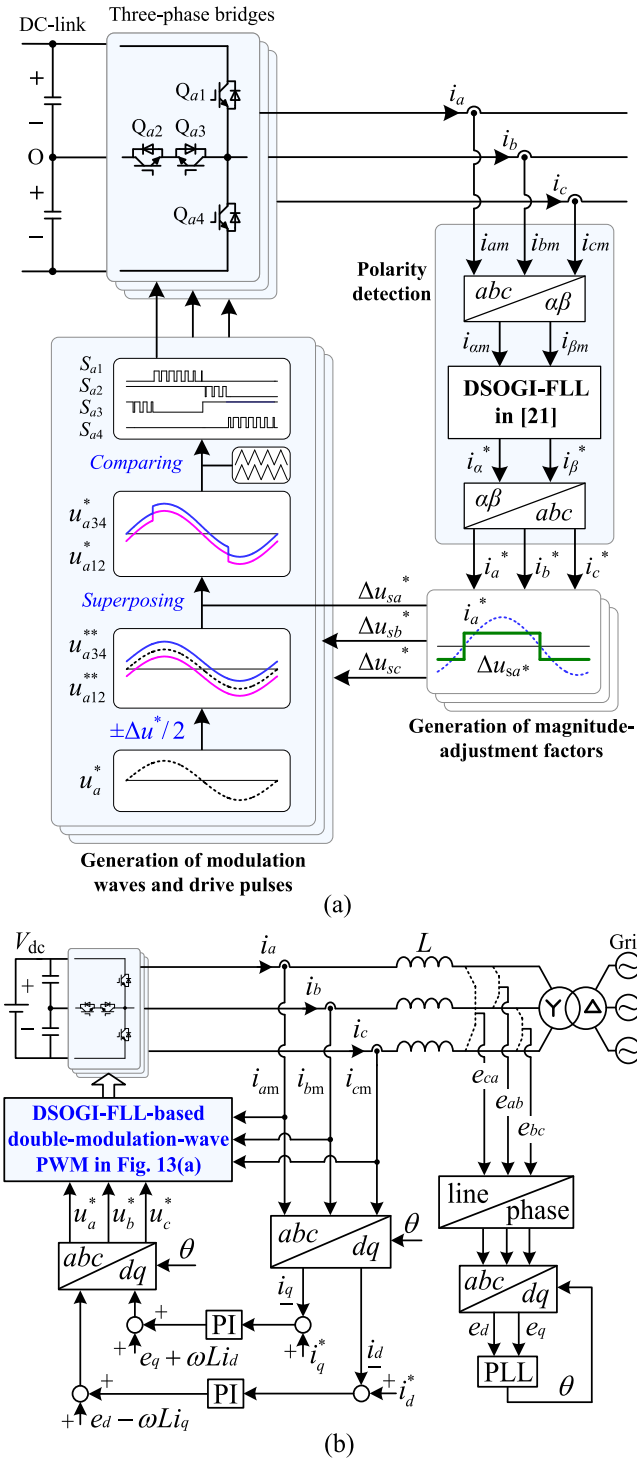

Fig. 13. Application in the grid-connected converter. (a) DSOGI-FLL-based double-modulation-wave PWM. (b) Diagram of the closed-loop control system.

VIII. Experimental Results

A. Experimental Setup

To experimentally verify the effectiveness of the proposed double-modulation-wave PWM, a 6-kVA three-phase three-level T-type converter is built as shown in Fig. 14. And the

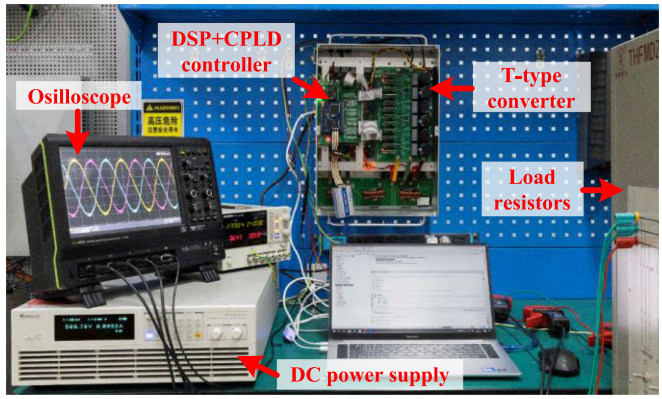

Fig. 14. Experimental setup of a 6-kVA three-phase three-level T-type converter.

TABLE I
Parameters of the Test System

Symbol	Parameter	Value
V_{dc}	DC-link voltage	600 V
R_L	Load resistance	36 Ω
L_{load}	Load inductance	1.5 mH
f_l	Line frequency	50 Hz
f_s	Switching frequency	40 kHz
T_d	Dead time	2 μs
T_u	Underlap period	2 μs
M	Modulation index	0.8
Δu^*	Adjusted magnitude	0.16

corresponding parameters of the test system are shown in Table I. The dc-link voltage is generated by the 62050H-600S programmable dc power supply from Chroma, and a three-phase *RL* load is connected to the ac side of the converter. The conventional SPWM with dead-time [26], the dead-time elimination PWM [12], and the proposed PWM are, respectively, employed as comparisons of the verification. Note that, to guarantee fair comparisons, current polarities extracted by the DSOGI-FLL are adopted both in the dead-time elimination PWM and the double-modulation-wave PWM.

The DSP TMS320F28335 from Texas Instruments is employed to implement different PWM schemes, and the minimum length of the underlap period is limited to T_u by the CPLD EPM240T100 from ALTERA. In the experiments, waveforms are captured by the HDO4024 200-MHz 2.5-GS/s oscilloscope from Teledyne LeCroy, simultaneously the data of waveforms are saved and loaded to Matlab. And the total harmonic distortion (THD) is calculated by the "Powergui FFT analysis Tool."

B. Harmonic Comparisons

First, as a comparison, Fig. 15 shows the three-phase currents with the conventional SPWM containing dead-time. Obvious distortions can be observed due to the dead-time effect. The THD of three-phase currents computed up to 100 kHz are 3.71%, 3.73%, and 3.80%, respectively.

Then, the dead-time elimination PWM is employed, and the three-phase currents and a zoomed-in zero-crossing are shown

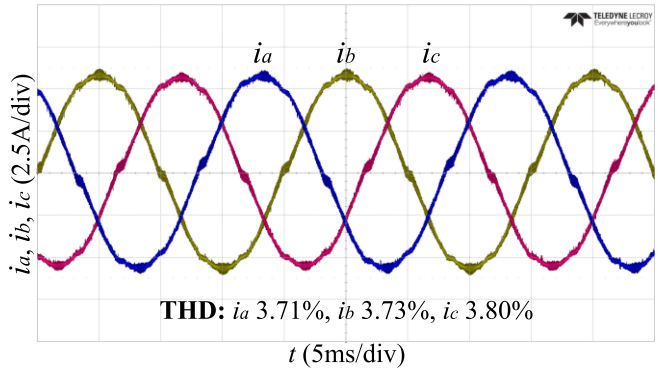

Fig. 15. Three-phase currents with the conventional SPWM Containing dead-time.

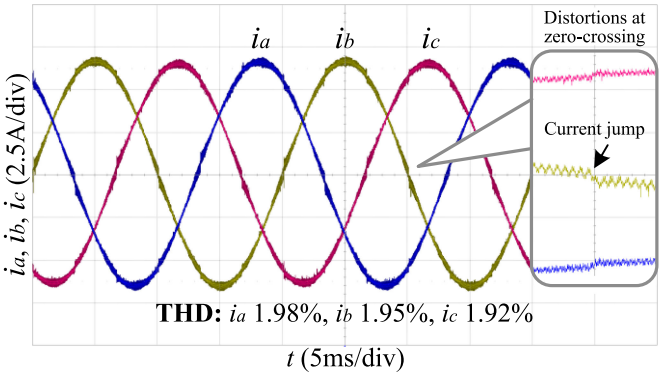

Fig. 16. Three-phase currents and a zoomed-in zero-crossing with the dead-time elimination PWM.

in Fig. 16. Due to no voltage losses in the dead-time elimination PWM, the amplitude of currents in Fig. 16 has been increased compared with that in Fig. 15. And the distortions in Fig. 16 are obviously mitigated compared with those in Fig. 15, and lower current THD are obtained as 1.98%, 1.95%, and 1.92%. In addition, the zoomed-in current zero-crossing shows the current-jump issue due to the elimination of redundant drive pulses [20], [21].

The double-modulation-wave PWM proposed in this article is further implemented. Given the double-modulation-wave PWM provides extra complementary drive pulses around the current zero-crossing, the current can cross the zero-line smoothly as seen from the zoomed-in current zero-crossing in Fig. 17. Consequently, the current THD in Fig. 17 are further reduced as 1.84%, 1.86%, and 1.78%.

C. Tests of Dependency on Current Polarities

To test the dependency on current polarities, experiments are carried out in wrong-polarity situations, where phase delays of $\pi/9$ and $\pi/6$ are artificially set in reference currents. The three-phase currents obtained with the dead-time elimination PWM and the double-modulation-wave PWM are shown in Figs. 18 and 19, respectively. As seen in Fig. 18(a) with the phase delay of $\pi/9$, in the three-phase currents obtained by

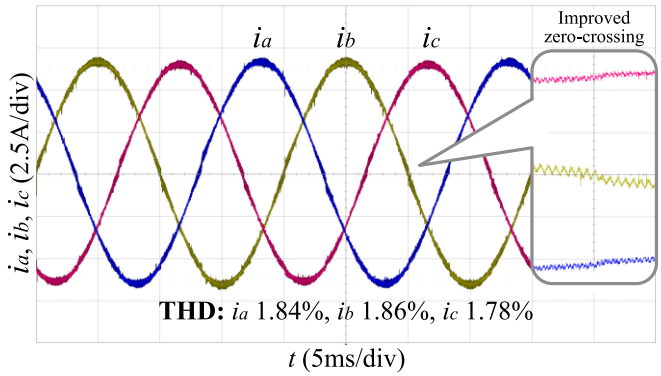

Fig. 17. Three-phase currents and a zoomed-in zero-crossing with the double-modulation-wave PWM.

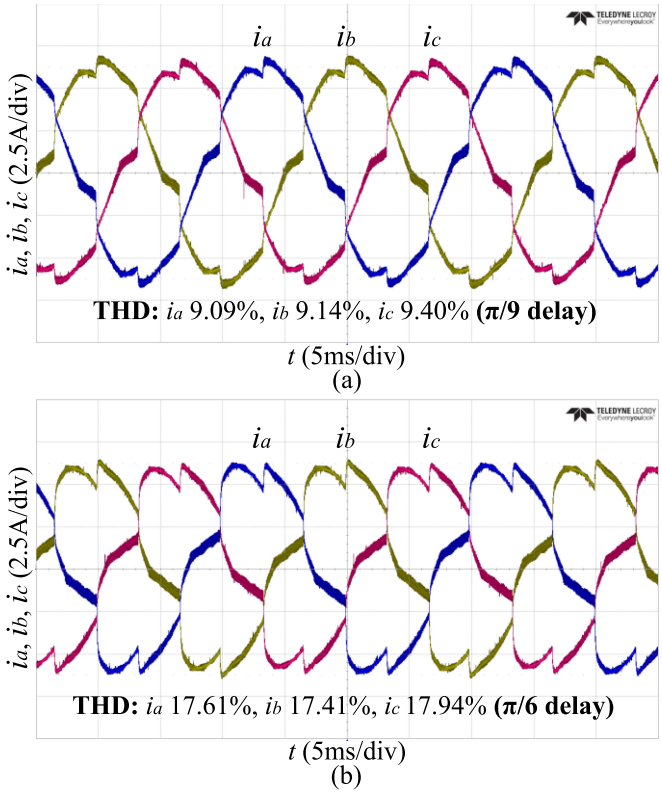

Fig. 18. Three-phase currents in wrong-polarity situations with phase delays of (a) $\pi/9$ and (b) $\pi/6$ using the dead-time elimination PWM.

the dead-time elimination PWM, obvious distortions appear at the top and the zero-crossing of currents. When the phase delay is increased as $\pi/6$ in Fig. 18(b), two peaks appear in the current of each phase. Such distortions in currents will seriously impair the stability of the converter in dynamic process. Meanwhile, as seen from Fig. 19(a) and (b) with the double-modulation-wave PWM, much lower distortions exist in the three-phase currents. Only the location of distortions varies in the currents with different phase delays.

The frequency-variation process, as a dynamic process in practical operations, is further tested. The frequency of

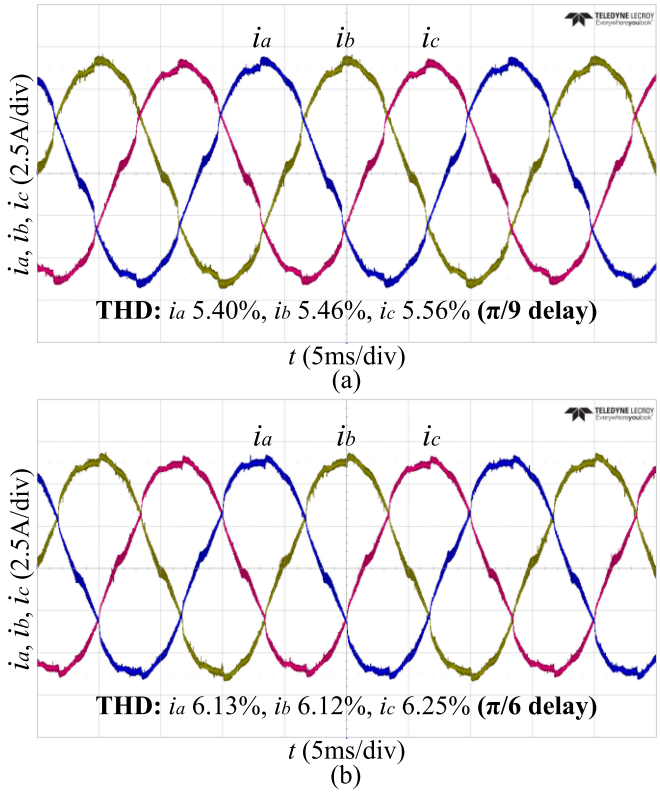

Fig. 19. Three-phase currents in wrong-polarity situations with phase delays of (a) $\pi/9$ and (b) $\pi/6$ using the double-modulation-wave PWM.

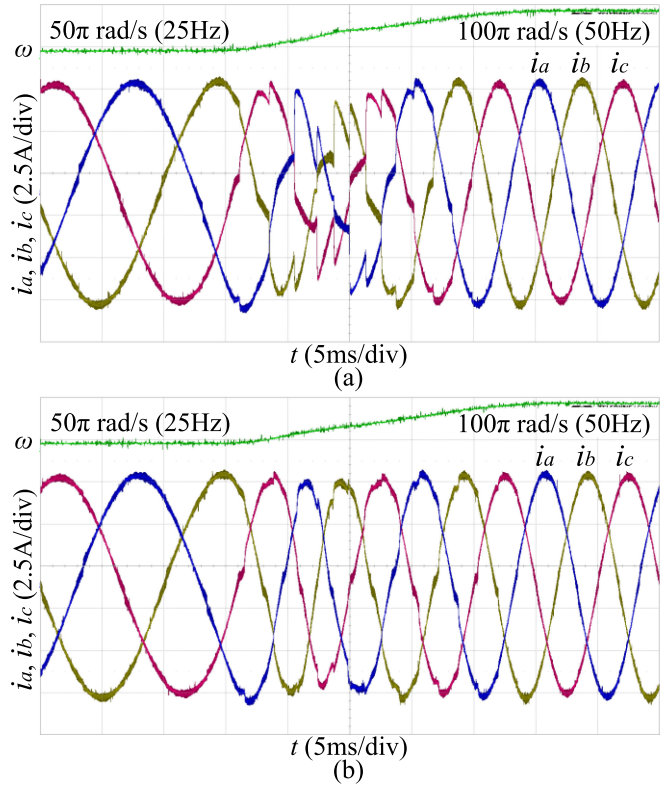

Fig. 20. Three-phase currents in the frequency-variation process (a) with the dead-time elimination PWM, and (b) with the double-modulation-wave PWM.

modulation waves is increased from 50π rad/s (25 Hz) to 100π rad/s (50 Hz). As seen in Fig. 20(a) with the dead-time elimination PWM, serious current distortions appear in the frequency-variation period, where errors inevitably exist in the current polarities extracted by the DSOGI-FLL. The distortions disappear until the frequency-variation ends. As a comparison, in Fig. 20(b), only slight current distortions appear in the frequency-variation period, since the double-modulation-wave PWM can work well with wrong-current polarities.

Based on the above comparisons from Figs. 18–20, it can be indicated that the limitation of current-polarity dependency to the widespread application of the dead-time elimination has been well solved. With the proposed double-modulation-wave PWM, sinusoidal output currents with acceptable harmonics are always presented even in wrong-polarity situations, so that a stable operation of the converter can be achieved in the dynamic process.

D. Overmodulation Test of the Double-Modulation-Wave PWM

A modulation index M of 1 is adopted to present the overmodulation issue analyzed in Section VI-A. The modulation waves $u_{a12}{}^*$ and $u_{a34}{}^*$ outputted by a digital-to-analog converter, as well as the complementary drive pulses S_{a1} and S_{a3}, are presented in Fig. 21(a). The corresponding output currents are presented in Fig. 21(b). As seen in Fig. 21(a), the magnitude-adjustment according to the current polarity leads to the flat tops in $u_{a12}{}^*$ and $u_{a34}{}^*$. And, the flat top of $u_{a34}{}^*$ causes the disappearance of the added drive pulses in S_{a3}. Since the disappeared drive pulses lie in the current freewheeling stage, neither overmodulation nor extra distortions appear in the three-phase currents of Fig. 21(b). It is verified that the proposed double-modulation-wave PWM can achieve a maximum linear-modulation index of 1.

E. Verification of the Proposed Double-Modulation-Wave PWM in the Grid-Connected Converter

To verify the feasibility in practical applications, the grid-connected converter with the proposed double-modulation-wave PWM shown in Fig. 13(b) is further implemented experimentally. The transformer voltage ratio is 380/304 V, and other parameters are the same with those in Table I. Fig. 22 shows the three-phase currents and the Phase A grid voltage with an operating power of 4.4 kW. The THDs of three-phase currents computed up to 100 kHz are 2.02%, 2.05%, and 1.96%, respectively, which can well meet the limit of 5% defined by IEEE Standard 1547-2003 [33].

Through the above experimental verifications in this section, it can be indicated that the dead-time elimination PWM and the proposed double-modulation-wave PWM can both effectively avoid the dead-time effect with low output harmonics, and achieve the maximum linear modulation index of 1. While the proposed double-modulation-wave PWM reduces the dependency on current polarities, and the stability of the converter

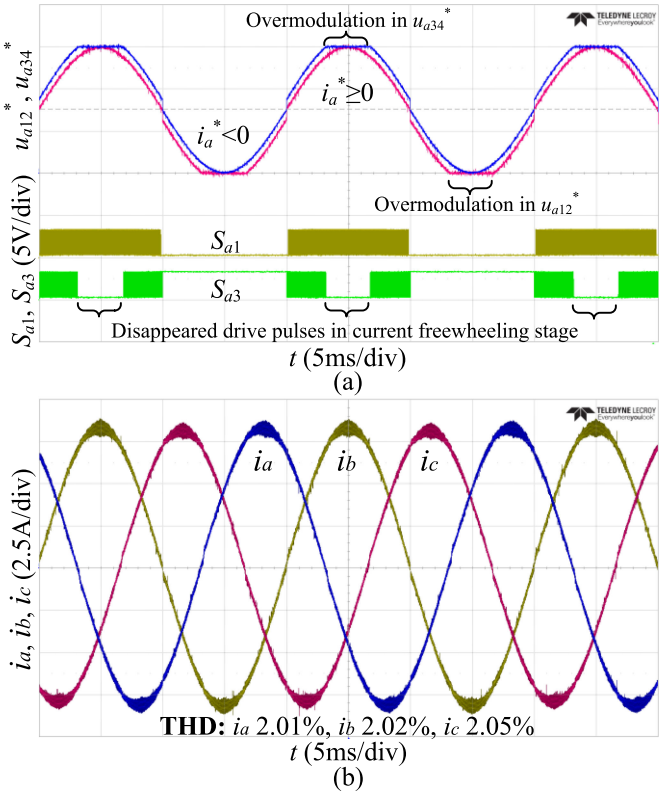

Fig. 21. Experimental results with the double-modulation-wave PWM when $M = 1$: (a) modulation waves and two complementary drive pulses; and (b) three-phase currents.

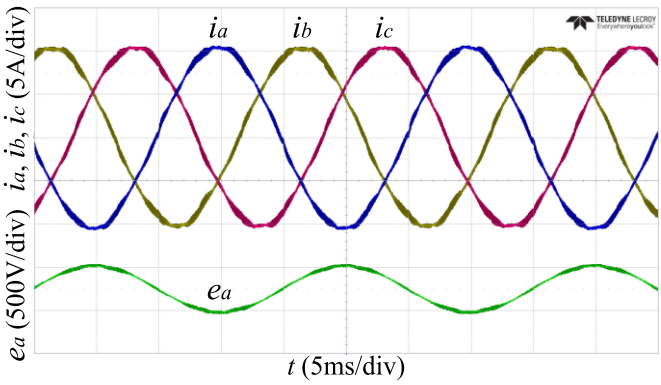

Fig. 22. Three-phase currents and the grid voltage in Phase A.

can be guaranteed in dynamic processes with inevitable current-polarity errors.

In addition, the current and voltage stresses are discussed as follows: regarding the conventional PWM with dead-time [26], the dead-time elimination PWM [12], and the proposed double-modulation-wave PWM. The three PWM schemes all belong to "hard-switching" modulations [34], which cannot affect the switching-transient waveforms. Even though their redundant drive pulses and output voltage errors are different, they still have the same current boosting and freewheeling paths as shown in Fig. 1 of this article. Therefore, with the mentioned three PWM schemes, the same current and voltage stresses are achieved in the T-type three-level converter adopted in this article.

The device losses with the three PWM schemes are further analyzed considering the switching loss and the conduction loss, respectively, as follows.

1) Regarding the switching loss, the mentioned three PWM schemes all belong to "hard-switching" modulations [34] and continuous PWM schemes [35], where the devices switch in the whole line-frequency period. Therefore, the switching losses with the three PWM schemes will be the same if they are employed in the same converter. Note that the disabled drive pulses of the dead-time elimination PWM are in the current freewheeling stage, where the current flows through body diodes. Therefore, the switching loss is not affected [13], and only the driver loss is reduced, which however can be negligible compared to the loss of the power devices.
2) Regarding the conduction loss, the power device of IGBT is adopted in the three-level converter of this article, where the current cannot flow reversely in the channel. No synchronous rectification [36] can be generated whether drive pulses exist in the current freewheeling stage or not. Therefore, the conduction loss will be the same with the three PWM schemes.

In summary, with the three mentioned PWM schemes, the switching and conduction losses, as well as the efficiencies, will be the same in three-level converters with IGBTs. In addition, if MOSFETs are adopted where the current can flow reversely in the channel, the synchronous rectification can be generated with a reduced conduction loss. The loss and efficiency analyses on three-level converters with MOSFETs can be a future work on the basis of this article.

IX. Conclusion

A double-modulation-wave PWM has been proposed based on the dead-time elimination PWM. To further simplify the implementation process, the two modulation waves have been decomposed by introducing a magnitude-adjustment factor varying with the currents polarity. The proposed double-modulation-wave PWM has successfully reduced the dependency on current polarities and mitigated the "algebraic loop" issue, while the characteristic of dead-time-effect elimination has been reserved. Even with wrong current polarities, a stable operation of the converter can still be achieved with only slightly increased output harmonics.

However, the employment of two modulation waves leads to new negative issues. The overmodulation can cause the drive-pulse disappearance in the current freewheeling stage. Nevertheless, the output voltage is not affected and a maximum linear-modulation index of 1 can still be guaranteed. Given the single drive pules around zero-crossing cannot cause the shoot-through failure, their negative effect can be neglected. To avoid the possible shoot-through failure caused by the shorter underlap period, the minimum length of the underlap period should be limited in the software program or in the designed drive circuit.

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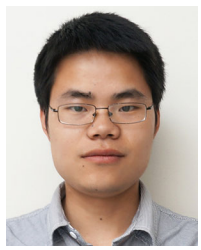

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