A Direct Carried-Based PWM Scheme With Reduced Switching Harmonics and Common-Mode Voltage for Current Source Converter

Lei Ming, *Student Member, IEEE*, Wenlong Ding, *Member, IEEE*, Changqing Yin, *Student Member, IEEE*, Zhen Xin, *Member, IEEE*, and Poh Chiang Loh

***Abstract*—The performance of a current source converter (CSC) is greatly affected by its adopted modulation schemes. Among various modulation schemes, the carrier-based pulsewidth modulation (CB-PWM) has gained increasing attention owing to its inherent autosequencing process. However, existing CB-PWM schemes suffer from either high switching harmonics in ac current or high low-order common-mode voltage (CMV), and sometimes, both, which restrains the application of this promising scheme. To address this issue, this article explores the modulation mechanism of CB-PWM for a CSC. Based on that, this article proposes a direct CB-PWM scheme. Its implementation, mechanism, and characteristics have been developed and presented in detail. It is shown that the proposed scheme enjoys inherent low switching frequency, easy implementation, as well as high dc current utilization. More importantly, compared with existing CB-PWMs, the proposed scheme can simultaneously reduce the switching harmonics of ac current and the low-order CMV for a CSC. These superior performances can bring potential benefits to scale down the ac filter and common-mode choke for practical CSC applications. Effectiveness of the proposed scheme is verified experimentally with a CSC operating as an inverter.**

***Index Terms*—Common-mode voltage (CMV), current source converter (CSC), direct carrier-based pulsewidth modulation (CB-PWM), switching harmonics.**

I. Introduction

CURRENT source converter (CSC) has always been treated as an attractive ac/dc converter due to its inherent current-limiting capability, four-quadrant operation, and direct current control [1]–[7]. It is adopted in both high-power applications, such as medium-voltage drives [1], wind-energy conversion system [2], and high-voltage direct current (HVdc) system [3], and low-power applications, such as photovoltaic (PV) system [4], fuel cell system [5], and integrated motor drive [6], [7].

Manuscript received July 25, 2020; revised October 22, 2020; accepted November 27, 2020. Date of publication December 3, 2020; date of current version March 5, 2021. This work was supported by the Shun Hing Institute of Advanced Engineering under Grant #RNE-p3-18. Recommended for publication by Associate Editor D. O. Neacsu. *(Corresponding author: Wenglong Ding.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2020.3042387.

Digital Object Identifier 10.1109/TPEL.2020.3042387

Modulation techniques play a key role in effectively driving a CSC, which can be categorized as OFF-line modulation, such as the selective harmonic elimination pulsewidth modulation (SHE-PWM) [8]–[10] and ON-line modulation, such as the space vector PWM (SVM) [11]–[23] and the carrier-based PWM (CB-PWM) [24]–[32]. SHE-PWM is popular in medium-voltage high-power drive systems due to its excellent harmonic performance with low switching frequency. However, it requires considerable computational effort and large store memory, and features poor dynamic response. ON-line techniques, on the other hand, are preferred in applications where a faster dynamic response is required. Generally, SVM is more flexible since its switching patterns can be adjusted easily. But, this is at the expense of higher computation burden, which will become unbearable when the level of CSC increases [24], [25]. As a contrast, the CB-PWM enjoys inherent scalability, modularity, and easy-implementation features owing to its autosequencing process.

There are mainly four CB-PWM schemes for a CSC, named as trapezoidal PWM (TPWM) [26], bi-tri logic SPWM [27]–[30], six-step direct PWM (SS-DPWM) [31], and direct duty-ratio PWM (DDPWM) [32]. Among these four methods, TPWM features the highest dc current utilization, but at the expense of poor output quality [8], [26]. The bi-tri logic SPWM derives from the voltage source converter (VSC) modulation through logic translation [27], [28]. However, the duality between line current of CSC and line voltage of VSC causes the line currents to lead the references by 30° and the maximum dc current utilization is 0.866. Therefore, the reference signals need to be preprocessed to compensate the leading 30° and to improve the dc current utilization [29], [30]. Unlike the above method, SS-DPWM directly generates gating signals by comparing two references (named as "master" and "slave," respectively) with the phase opposition disposition (POD) carriers [31]. Similarly, DDPWM can also generate gating signals directly, but with different current references and combination rules [32].

Essentially, the performance of a CSC is affected by its employed switching sequence, which is formed by available active current vectors (ACVs) and zero current vectors (ZCVs) [11]. Most existing CB-PWMs employ two adjacent ACVs and one ZCV to synthesize the reference current vector. But their ACV order and ZCV selection are different, resulting in different characteristics. Unfortunately, since their switching sequences

have not been optimized, they suffer from either high switching harmonics in ac current [32] or high low-order common mode voltage (CMV) [27], and sometimes, both [31].

Both the switching harmonics in ac current and the low-order harmonics in CMV have side effects on a CSC system. Specifically, the switching harmonics in ac current increase losses of the electric power system and cause high-frequency electromagnetic interference (EMI), disturbing the operation of surrounding electronic equipment [33], [34]. Therefore, the switching harmonics of ac current should be attenuated to meet grid standards, such as the IEEE 1547-2003. Nonnegligible low-order CMV from a CSC can similarly impact a system negatively. In a transformerless current source drive, resonance of the CM choke, parallel differential choke in the dc link, and two ac-side capacitors in a common-mode loop can be excited by the low-order CMV harmonics from an inverter [20]–[22]. The excited resonance then causes common-mode current, and hence, CM stresses experienced by the motor amplify significantly. A CM choke can effectively block the high-order CMV; however, it presents low impedance for the low-order components of CMV. A large inductive choke is thus essential to impede low-order CMV current and avoid saturation at a low frequency [35]. Else, undesired heating, mainly caused by third-order CM current flowing through a small CM filter, can occur, as reported in [36]. It should, however, be noted that both of them relate to the modulation scheme. Hence, it is meaningful for a CSC to simultaneously reduce the switching harmonics of ac current and the low-order harmonics in CMVs with a modulation scheme.

There are mainly two types of modulation schemes for reducing the CMV of a CSC. One of them relies on attenuating the peak value of the CMV [16]–[19], while the other depends on attenuating the low-order harmonics of the CMV [20]–[22]. For instance, in [16], the authors transfer the nonzero current vector modulation concept from a VSC to a CSC to reduce its peak CMV. Similarly, the reference-trajectory-optimized SVM in [17] is for reducing the peak CMV by abandoning the ZCVs. Alternatively, instead of removing the ZCVs, Shang *et al.* [18] proposed the reduction of peak CMV by selecting only ZCVs with the lowest amplitude. Recently, Ding *et al.* [19] also presented an optimized zero-state replacement method for the discontinuous bi-tri logic SPWM to reduce CMV of the CSC. To avoid exciting the *LC* resonance in CM circuit, all [20]–[22] presented modified SVMs to reduce the low-order harmonics, whose idea is to dynamically compensate CMVs caused by active vectors with proper ZCVs. In addition, CMV-reduced modulations have also been explored for four-leg [37], five-phase [38], paralleled [25], and back-to-back [39] CSCs. However, the mechanism of reducing the switching harmonics and CMV with a CB-PWM has not been comprehensively reported yet, which restrains the application of this promising modulation scheme.

To address this issue, this article explores the modulation mechanism of CB-PWM for a CSC. Based on that, a direct CB-PWM (DCB-PWM) scheme is proposed. The proposed scheme enjoys inherent low switching frequency, easy implementation, as well as high dc current utilization. More importantly, the proposed scheme can simultaneously reduce the switching harmonics in ac current and low-order CMV. These superior performances can bring potential benefits for increasing the power density of a practical CSC system by scaling down the ac filter and CM choke.

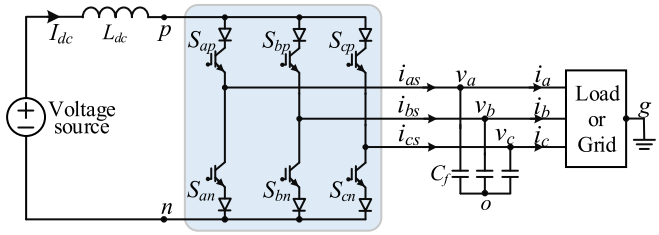

Fig. 1. Schematic diagram of a three-phase CSC.

The rest of this article is structured as follows. Section II analyzes the modulation mechanism of CB-PWM for a CSC. Then, the implementation, mechanism, and characteristics of the proposed DCB-PWM are detailed in Section III. Experimental results are then given in Section IV to verify the effectiveness of the proposed modulation method. Finally, the conclusion is drawn in Section V.

II. Analysis of Modulation Mechanism for CSC

This section analyzes the effects of the order of ACVs and selection of ZCVs in the switching sequence for a CSC. The mechanism of adjusting the ACV order and selecting the ZCV in a CB-PWM is discussed subsequently. Before that, the principle of modulation is first presented as follows.

A. Principle of Modulation for CSC

Fig. 1 shows the schematic diagram of a three-phase CSC operating as an inverter. The CSC is supplied by a constant current ($I_{\rm dc}$), which can be obtained by connecting a large inductor ($L_{\rm dc}$) in series with a voltage source. By properly driving its six switches (S_{xp} and S_{xn}, $x = a, b, c$), the dc-link current ($I_{\rm dc}$) is distributed to three ac phases, resulting in three pulsed ac currents (i_{as}, i_{bs}, and i_{cs}). Capacitors (C_f) are, therefore, required at the ac side to assist the devices commutation and to filter out the current harmonics.

Depending on its switching states, each of the three pulsed ac currents ($i_{xs}, x = a, b, c$) has three outputs

$$i_{xs} = \begin{cases} I_{dc} \text{ if } (S_{xp},\ S_{xn}) = (1,\ 0) \\ 0 \text{ if } (S_{xp},\ S_{xn}) = (1,\ 1)\ or\ (0,\ 0) \\ -I_{dc} \text{ if } (S_{xp},\ S_{xn}) = (0,\ 1) \end{cases} \tag{1}$$

where "1" and "0" stand for the turn-ON and turn-OFF states of a switch, respectively.

In a CSC, one upper switch {S_{ap}, S_{bp}, or S_{cp}} and one lower switch {S_{an}, S_{bn}, or S_{cn}} should always be turned ON at any instant to avoid interrupting inductor current. The upper and lower switches can be from the same or different phases, respectively, giving rise to three ZCVs ($\boldsymbol{I_7}$–$\boldsymbol{I_9}$) or six ACVs ($\boldsymbol{I_1}$–$\boldsymbol{I_6}$), as shown in Fig. 2. The reference vector $\boldsymbol{I_{\rm ref}}$ in Fig. 2 is formed by the three-phase reference currents ($i_{a\_\rm ref}$, $i_{b\_\rm ref}$,

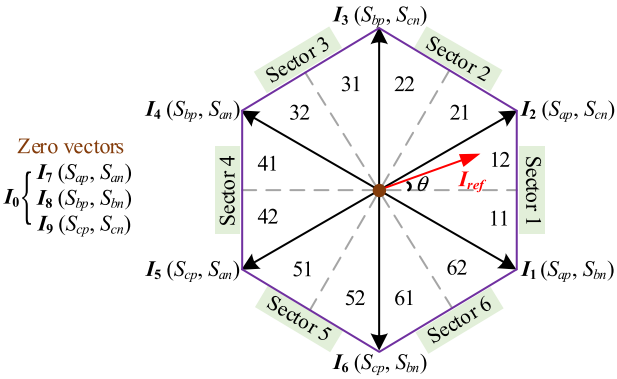

Fig. 2. Current space vector diagram of a CSC.

i_{c_ref}), which, under a balanced situation, can be expressed as

$$\begin{cases} i_{a\_ref} = m_{\mathrm{a}} \cos(\omega_i t) \\ i_{b\_ref} = m_a \cos(\omega_i t - 2\pi/3) \\ i_{c\_ref} = m_a \cos(\omega_i t + 2\pi/3) \end{cases} \tag{2}$$

where m_a is the modulation index and ω_i is the angular frequency. The reference currents can therefore be synthesized with three available currents (I_{dc}, 0, and $-I_{\mathrm{dc}}$) in average concept.

For a CB-PWM scheme, it requires at least two reference currents (one positive and one negative) to compare with the carrier. For lower switching frequencies, the positive and negative references should be synthesized with (I_{dc}, 0) and ($-I_{\mathrm{dc}}$, 0), respectively. According to (1), there is only one switching state for i_{xs} to output I_{dc} or $-I_{\mathrm{dc}}$. But, i_{xs} will output zero current no matter whether the two switches of the same phase are both turned ON or OFF. Taking the synthesis of the positive reference current with (I_{dc}, 0) as an example, the i_{xs} can output the desired "I_{dc}" by turning on its upper switch, i.e., (S_{xp}, S_{xn}) = (1, 0). But there are two options to output "0." More specifically, if the "0" is generated by turning ON S_{xp} and S_{xn}, i.e., (S_{xp}, S_{xn}) = (1, 1), S_{xp} will be always turned ON. On the contrary, S_{xn} will be always turned OFF if the "0" is generated by turning OFF S_{xp} and S_{xn}, i.e., (S_{xp}, S_{xn}) = (0, 0). Similarly, S_{xn} (S_{xp}) remains in ON (OFF) state if both the two switches are turned ON (OFF) to generate "0" when synthesizing a negative reference current.

The principle of modulation can also be interpreted from the space vector perspective, which is to synthesize the reference current vector with available ACVs and ZCVs [8], [13]–[17]. For example, the vector $\boldsymbol{I_{\mathrm{ref}}}$ in sector 1 can be synthesized by the nearest two ACVs and one ZCV

$$\begin{cases} T_1 = m_a \sin(\pi/6 - \theta)\, T_s \\ T_2 = m_a \sin(\pi/6 + \theta)\, T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{3}$$

where $-\pi/6 \le \theta \le \pi/6$ and T_S is the sampling period; and T_1, T_2, and T_0 are dwell times for vectors $\boldsymbol{I_1}$, $\boldsymbol{I_2}$, and $\boldsymbol{I_0}$, respectively.

The switching sequence, formed by ACVs and ZCVs, plays a key role in affecting the performance of a CSC. The following two subsections will focus on the effects and mechanisms of the order of ACVs and selection of ZCVs, respectively.

TABLE I
SWITCHING SEQUENCES OF THREE EXISTING CB-PWM SCHEMES IN SECTOR 1

Subsector	Bi-tri logic SPWM-Dis [27]	SS-DPWM [31]	DDPWM [32]
11	[I_1-I_2-I_7-I_2-I_1]	[I_7-I_1-I_2-I_1-I_7]	[I_9-I_2-I_1-I_2-I_9]
12	[I_7-I_1-I_2-I_1-I_7]		[I_8-I_1-I_2-I_1-I_8]

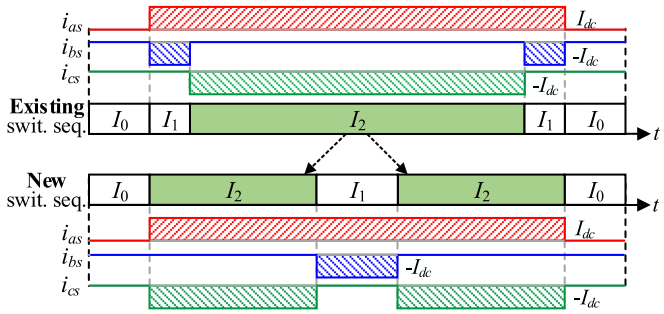

Fig. 3. Two switching sequences and their corresponding ac currents (i_{as}, i_{bs}, and i_{cs}) when I_{ref} is in sector 12 (top: Existing ACV order; bottom: New ACV order).

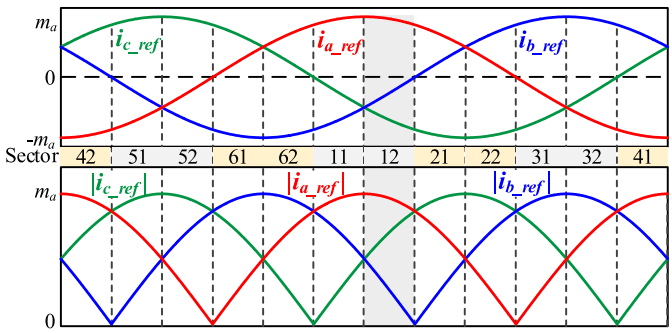

Fig. 4. Three-phase reference currents (top) and their absolute values (bottom) in one line cycle.

B. Analysis of the Order of ACVs

1) Effects of the Order of ACVs: The dwell times for vectors $\boldsymbol{I_1}$ and $\boldsymbol{I_2}$ vary with $\boldsymbol{I_{\mathrm{ref}}}$. According to (3), T_1 is larger than T_2 when $-\pi/6 \le \theta < 0$, while T_2 is greater when $0 < \theta \le \pi/6$. Accordingly, sector 1 can be further divided into subsector 11 and 12, as marked in Fig. 2. Table I summarizes the switching sequences of three existing CB-PWM schemes in sector 1. These three schemes share similar switching sequences as "$\boldsymbol{I_0}$–$\boldsymbol{I_1}$–$\boldsymbol{I_2}$–$\boldsymbol{I_1}$–$\boldsymbol{I_0}$" in subsector 12, where T_2 is greater than T_1. With this switching sequence, the long-acting vector $\boldsymbol{I_2}$ remains intact, but the short-acting vector $\boldsymbol{I_1}$ is divided into two narrow segments. Consequently, the three-phase pulsed currents are not distributed evenly within a switching period (as shown at the top of Fig. 3), resulting in larger switching harmonics. Alternatively, if the order of $\boldsymbol{I_1}$ and $\boldsymbol{I_2}$ is swapped, the long-acting $\boldsymbol{I_2}$ rather than the short-acting $\boldsymbol{I_1}$ will be divided to form a more "evenly" pulsed ac current, as shown at the bottom of Fig. 3.

2) Mechanism of Adjusting the Order of ACVs in a CB-PWM: Fig. 4 shows the three-phase reference currents that have been divided into 12 sectors in one line cycle. In each sector, there are always one positive (negative) reference current and two negative (positive) ones. Taking sector 12 as an example, where

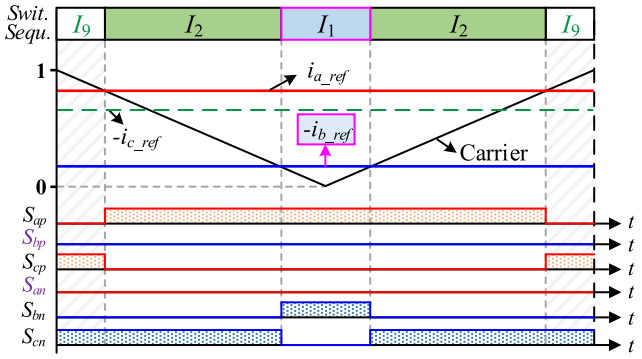

Fig. 5. Gating signals and resulted switching sequence when i_{a_ref} and $-i_{b\_\mathrm{ref}}$ are chosen as the reference currents in sector 12.

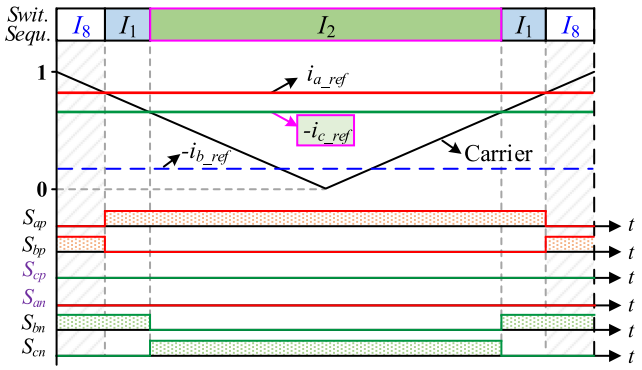

Fig. 6. Gating signals and resultant switching sequence when i_{a_ref} and $-i_{c\_\mathrm{ref}}$ are chosen as the reference signals in sector 12.

$i_{a\_\mathrm{ref}} > -i_{c\_\mathrm{ref}} > -i_{b\_\mathrm{ref}} > 0$, the positive reference is i_{a_ref}, while the negative one can be selected from i_{b_ref} and i_{c_ref}. Influences of the two negative references on the modulation of a CSC are explored as follows.

For simplicity, absolute values of two chosen references (one positive and one negative) are used to compare with only one triangular carrier. In addition, assuming that the required "0" state is generated by turning OFF the two switches of the same phase (i.e., $(S_{xp}, S_{xn}) = (0, 0)$) in the following two cases.

Case 1: i_{b_ref} is chosen as the negative reference.

Fig. 5 shows the gating signals and resultant switching sequence when i_{a_ref} and i_{b_ref} are chosen as the positive and negative references, respectively. According to the above assumption, both S_{bp} and S_{an} remain in OFF state. Therefore, S_{ap} and S_{cp} are complementary, which can be effected by comparing i_{a_ref} with the triangular carrier. To be specific, S_{ap} will turn ON when i_{a_ref} is greater than carrier, otherwise, S_{cp} will turn ON. The switching states of S_{bn} and S_{cn} are determined by comparing $-i_{b\_\mathrm{ref}}$ with the carrier in the same way. As shown at the top, the long-acting vector I_2 is divided into two segments in this case, which will cause a more "evenly" pulsed ac current.

Case 2: i_{c_ref} is chosen as the negative reference.

Fig. 6 shows the gating signals and resultant switching sequence when i_{a_ref} and i_{c_ref} are chosen as the positive and negative references, respectively. According to the above assumption, both S_{cp} and S_{an} are turned OFF in this sector. The gating signals for S_{ap} and S_{bp} are generated by comparing i_{a_ref} with the carrier, while the gating signals for S_{cn} and S_{bn} are generated by comparing $-i_{c\_\mathrm{ref}}$ with the carrier. However, the long-acting vector I_2 remains intact and placed at the center of the switching sequence in this case, which will cause narrow pulsed ac currents, as illustrated at the top of Fig. 3.

It can therefore be summarized that the sequence of ACVs is affected by the chosen references. By choosing the two references with the maximum and minimum absolute values, the long-acting ACV can be divided, which will result in a more "evenly" distributed dc-link current at the ac side.

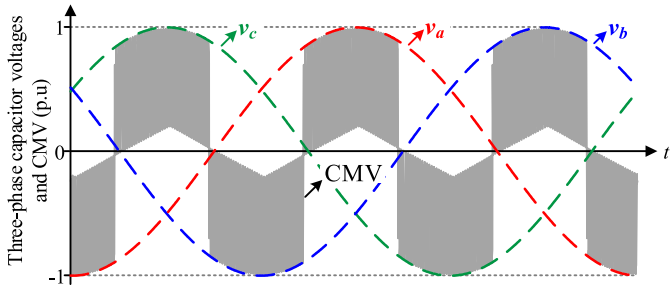

Fig. 7. Three-phase capacitor voltages and CMV of a CSC with the SS-DPWM scheme where ZCVs are selected by the nearest three vectors rule ($m_a = 0.8$ and displacement angle $\varphi = \pi/50$).

C. Analysis of the Selection of ZCVs

1) Effects of the Selection of ZCVs: In addition to the order of ACVs, selection of ZCV affects characteristics of a CSC as well. All three ZCVs ($\boldsymbol{I_7}$, $\boldsymbol{I_8}$, and $\boldsymbol{I_9}$) are equal in terms of providing a freewheeling path for dc-link current. But the selection of ZCVs has effects on the CMV of a CSC, which is defined as [17]

$$v_{cm} = (v_{pg} + v_{ng})/2 \tag{4}$$

where v_{pg} and v_{ng} are voltages at points p and n, respectively, with respect to ground g.

According to (4), the CMVs of three ZCVs are equal to one of the instantaneous values of three-phase capacitor voltages (v_a, v_b, v_c). Therefore, the maximum CMV peak value produced by ZCVs can be as high as the amplitude of capacitor voltage (V_m), while the maximum CMV peak value produced by ACVs is only $0.5V_m$. Fig. 7 shows the CMV of a CSC with the SS-DPWM scheme where ZCVs are selected according to the nearest three vector rule. It can be seen that the maximum CMV value is affected by the chosen ZCV, which equals V_m.

To reduce the CMV of a CSC, the selected ZCV should have lower CMV value. For instance, by always selecting the ZCV with the lowest magnitude of CMV and adjusting the switching sequence for minimal commutation times in each of the 12 divided sectors, the modified SVM features a reduced CMV [17], as shown in Fig. 8.

2) Mechanism of Selecting the ZCVs in a CB-PWM: A CB-PWM scheme requires at least one positive and one negative references, which can be specified as i_{a_ref} and i_{b_ref} in sector 12, respectively. When synthesizing them, the required "0" state

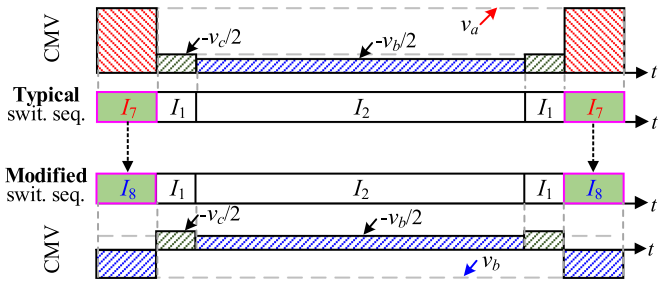

Fig. 8. Two switching sequences and their corresponding CMVs when $I_{\rm ref}$ is in sector 12 (typical: SS-DPWM).

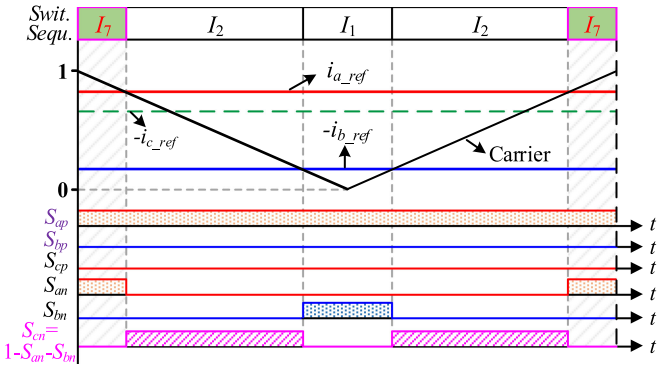

Fig. 9. Gating signals and resultant switching sequence when $(S_{ap}, S_{an}) = (1, 1)$ and $(S_{bp}, S_{bn}) = (0, 0)$ for zero state in sector 12.

can be generated by turning ON or OFF the two switches of the same phase. Therefore, there are four combinations to synthesize the two references. Influences of the four combinations on the modulation are explored as follows.

Case 1: $(S_{ap}, S_{an}) = (0, 0)$ and $(S_{bp}, S_{bn}) = (0, 0)$ for "0" state.

In this case, both S_{an} and S_{bp} are never turned ON within a switching period. Therefore, the gating signals for S_{ap} and S_{cp} can be directly obtained by comparing $i_{a\_\rm ref}$ with the carrier since they are complementary. Similarly, S_{bn} and S_{cn} are also complementary. So, their gating signals can also be directly obtained by comparing $-i_{b\_\rm ref}$ with the carrier. The resulted switching sequence is shown in Fig. 5, where $\boldsymbol{I_9}$ is automatically selected as the ZCV.

Case 2: $(S_{ap}, S_{an}) = (0, 0)$ and $(S_{bp}, S_{bn}) = (1, 1)$ for "0" state.

In this case, S_{an} remains in OFF state while S_{bn} is always turned ON. According to Fig. 2, the available ACVs are $\boldsymbol{I_1}$ and $\boldsymbol{I_6}$ rather than the nearest two ACVs ($\boldsymbol{I_1}$ and $\boldsymbol{I_2}$). In order not to break the ampere-second equilibrium principle, this combination should be abandoned.

Case 3: $(S_{ap}, S_{an}) = (1, 1)$ and $(S_{bp}, S_{bn}) = (0, 0)$ for "0" state.

Fig. 9 shows the gating signals and resultant switching sequence of this combination. In this case, S_{ap} is always turned ON and S_{bp} is always turned OFF. To satisfy the restriction imposed on three upper switches, S_{cp} should also be turned OFF. S_{an} is turned ON when $i_{a\_\rm ref}$ is less than carrier and S_{bn} is turned ON when $-i_{b\_\rm ref}$ is greater than carrier. Finally, the gating signal for S_{cn} can be obtained by using logical operations or the restriction relationship on the three lower switches. In this case, $\boldsymbol{I_7}$ is automatically selected as the ZCV.

TABLE II
SELECTED ZCVS AND THEIR CORRESPONDING CMVS OF THE FOUR COMBINATIONS IN SECTOR 12

Combinations	$(S_{bp}, S_{bn}) = (0, 0)$	$(S_{bp}, S_{bn}) = (1, 1)$
$(S_{ap}, S_{an}) = (0, 0)$	I_9 (v_b)	Abandoned
$(S_{ap}, S_{an}) = (1, 1)$	I_7 (v_a)	Abandoned

Case 4: $(S_{ap}, S_{an}) = (1, 1)$ and $(S_{bp}, S_{bn}) = (1, 1)$ for "0" state.

In this case, both S_{ap} and S_{bn} are always turned ON within a switching period. To satisfy the restrictions on the three upper and lower switches, the remaining four switches are always turned OFF. Therefore, there is only ACV $\boldsymbol{I_1}$ in this case, which reflects that this combination should also be abandoned.

Table II summarizes the above four combinations and their resultant ZCVs in sector 12. Based on this discussion, it can be concluded that the mechanism of selecting ZCVs is to properly choose the combination rules for generating the desired "0" state during the synthesization of two reference signals.

The above analyses reveal that the switching harmonics of ac current in a CSC can be reduced by adjusting the order of ACVs, while CMV relates to the selection of ZCVs. Motivated by simultaneously reducing the switching harmonics and CMV in a CSC, this article proposes a direct CB- PWM scheme as follows.

III. PROPOSED DIRECT CB-PWM SCHEME

This section begins by presenting implementation of the proposed DCB-PWM scheme. Its mechanism has then been analyzed and presented next. This is followed by detailed analyses of its characteristics in terms of dc current utilization, switching harmonics of ac current, common-mode voltage, switching frequency, and implementation effort.

A. Implementation of the Proposed DCB-PWM Scheme

According to the above analyses, the order of ACVs can be adjusted by choosing different reference signals, while the CMV can be regulated by using proper combination rules. These two processes are decoupled from each other. Based on that, this subsection presents a new modulation scheme to simultaneously reduce the switching harmonics and the low-order CMV. The proposed scheme follows two rules.

1) The chosen two references (one positive and one negative) should have the maximum and minimum absolute values in each of the 12 divided sectors.
2) The required "0" state during the synthesization of the two references (i.e., $(I_{\rm dc}, 0)$ for the positive reference, and $(-I_{\rm dc}, 0)$ for the negative one) should be generated by turning OFF the two switches of the same phase.

Fig. 10 shows the block diagram of the proposed DCB-PWM scheme. First, one line cycle of three current references $(i_{x\_\rm ref}, x = a, b, c)$ is divided into 12 sectors according to the relationship described in Fig. 4. In each sector, two references

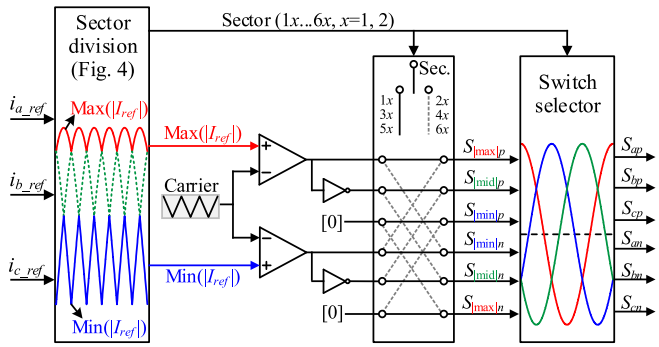

Fig. 10. Block diagram of the proposed DCB-PWM scheme.

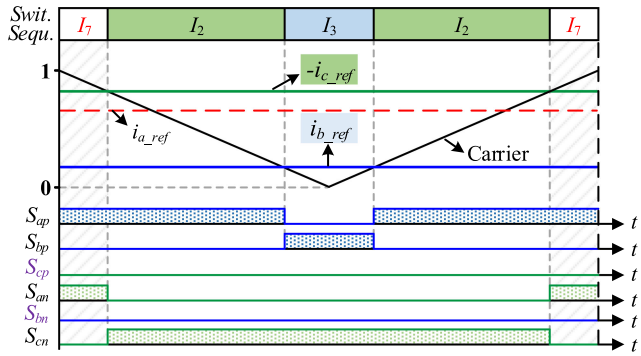

Fig. 11. Gating signals and resultant switching sequence when i_{b_ref} and $-i_{c\_\mathrm{ref}}$ are chosen as the reference signals in sector 21.

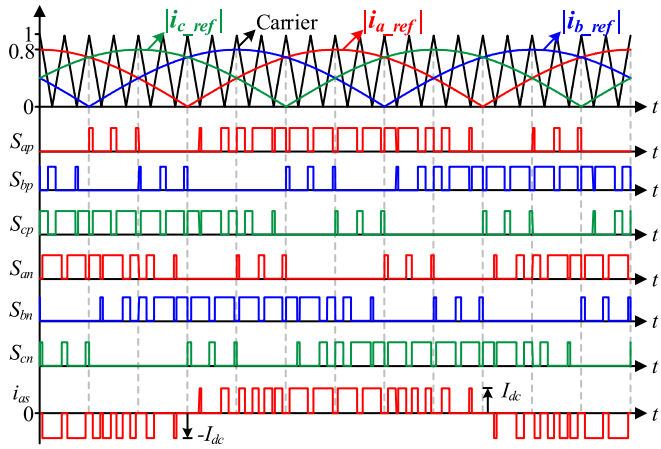

Fig. 12. Generation of gating signals for a CSC in one line cycle.

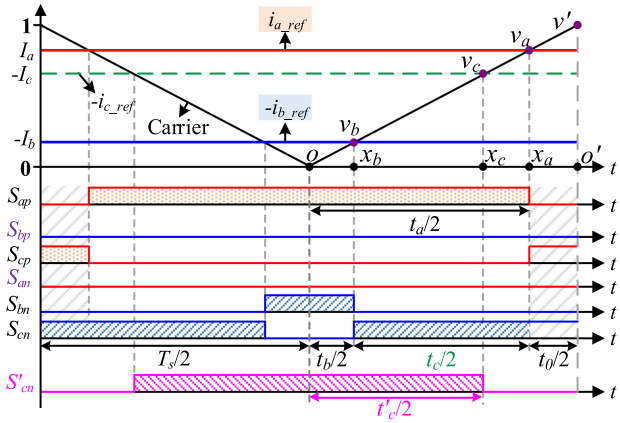

Fig. 13. Mechanism of the proposed DCB-PWM scheme.

are chosen and compared with one carrier according to the above two rules. The generated gating signals can then be used to drive the six switches of a CSC. In this scheme, only one upper and one lower switches are turned ON simultaneously.

The modulation process in sector 12, where the reference current that has the maximum absolute value is positive, has been illustrated in Fig. 5. For completeness, Fig. 11 shows the modulation process in sector 21, where $-i_{c\_\mathrm{ref}} > i_{a\_\mathrm{ref}} > i_{b\_\mathrm{ref}} > 0$.

According to the above two rules, i_{b_ref} and i_{c_ref} are chosen as the positive and negative references, respectively. In addition, both S_{bn} and S_{cp} are always turned OFF in sector 21. Given the restriction on the three upper switches, S_{bp} and S_{ap} are complementary. Therefore, their gating signals can be directly obtained by comparing i_{b_ref} with the carrier. Specifically, S_{bp} will turn ON when i_{b_ref} is greater than the carrier, otherwise, S_{ap} will turn ON. Similarly, gating signals for S_{cn} and S_{an} can be directly obtained by comparing $-i_{c\_\mathrm{ref}}$ with the carrier in the same way.

The modulation process in one line cycle (assumed 50 Hz) is illustrated in Fig. 12, where the modulation index is 0.8 and the carrier frequency is 1200 Hz. It can be seen from the bottom that the resultant a-phase current (i_{as}) has unipolar modulation during each half-period. Mechanism of the proposed DCB-PWM will be presented next.

B. Mechanism of the Proposed DCB-PWM Scheme

To illustrate the mechanism, Fig. 13 is taken from Fig. 5, where i_{a_ref} and i_{b_ref} are chosen as the positive and negative references, respectively. Assuming a symmetrical regular sampled method is used, I_x ($x = a, b, c$) is the instantaneous value of i_{x_ref} sampled at time $t = 0$. The amplitude of the carrier is normalized as 1 and its period is T_s.

In Fig. 13, the right-angled triangles labeled as ov_ax_a, ov_bx_b and ovo' are similar triangles. Hence, the following two expressions can be obtained:

$$\begin{cases} \frac{|I_a|}{1} = \frac{t_a/2}{T_s/2} \\ \frac{|I_b|}{1} = \frac{t_b/2}{T_s/2} \end{cases} \tag{5}$$

where t_a and t_b are the turn-ON durations in a carrier period for S_{ap} and S_{bn}, respectively. Accordingly, the pulsewidths for S_{cp} and S_{cn} can be calculated as $T_s - t_a$ and $T_s - t_b$, respectively. It is noted that both the top and bottom switches in phase C are turned ON during the duration $T_s - t_a$ (notated as t_0); thus, the effective operating durations for phase C in a carrier period is equal to $t_a - t_b$ (notated as t_c). In addition, according to Kirchhoff's current law (KCL), the summation of three-phase references should always be zero, i.e., $I_a + I_b + I_c = 0$. Therefore, the relationship between the references and the effective turn-ON

durations can be derived as

$$\frac{|I_a|}{t_a} = \frac{|I_b|}{t_b} = \frac{|I_c|}{t_a - t_b} \tag{6}$$

which shows that the references are directly proportional to the effective turn-ON durations for the corresponding switches.

Furthermore, the t_c' in Fig. 13 can be calculated as

$$t_c^{'} = t_a - t_b = t_c \tag{7}$$

where the duration t_c' is the pulsewidth of S_{cn}' generated by comparing $-I_c$ with the carrier. It is shown from (7) that, with the proposed direct CB-PWM scheme, the effective turn-ON duration of S_{cn} is proportional to $|I_c|$, though it is not determined by comparing $-I_c$ with the carrier, but by the comparison of I_a and $-I_b$ with the carrier.

C. Characteristics of the Proposed DCB-PWM Scheme

1) DC Current Utilization: According to (1), the pulsed ac current $i_{xs}(t)$, where $x = a, b, c$, can also be defined as

$$i_{xs}(t) = S_x(t)\, I_{dc} \tag{8}$$

where $I_{\rm dc}$ is the dc-link current, $S_x(t)$ is the switched function of phase x, and $S_x(t) = S_{xp} - S_{xn}$. Theoretically, $S_x(t)$ in (8) can be explored in the general form as a double-summation Fourier series [40]

$$\begin{aligned} S_x(t) = {} & \frac{A_{00}}{2} + \sum_{n=1}^{+\infty} \\ & \times [A_{0n}\cos(n\omega_0 t + n\varphi_x) + B_{0n}\sin(n\omega_0 t + n\varphi_x)] \\ & + \sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty} \{A_{mn}\cos[(mk_c+n)\omega_0 t + m\varphi_c + n\varphi_x] \\ & + B_{mn}\sin[(mk_c+n)\omega_0 t + m\varphi_c + n\varphi_x]\} \end{aligned} \tag{9}$$

where k_c is the ratio of the carrier frequency ω_c (in radians per second) to the reference frequency ω_0 (in radians per second), i.e., $k_c = \omega_c / \omega_0$; φ_x and φ_c are the initial phases of the reference $i_{x\_\rm ref}$ and the carrier, respectively. The coefficients of (9) can be obtained by evaluating the double Fourier integral of

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} S_x(\alpha,\beta)e^{j(m\alpha+n\beta)}d\alpha d\beta \tag{10}$$

where $\alpha = \omega_c\, t$ and $\beta = \omega_0\, t$. However, the evaluation of (10) requires significant algebraic transformation due to the use of "noncontinuous" modulation waveforms. According to [31] and [41], $S_x(t)$ can be approximately expanded as the following double Fourier formulation:

$$\begin{aligned} S_x(t) = {} & m_a\sin(\omega_0 t + \varphi_x) + \frac{2}{\pi}\sum_{m=1}^{+\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty}\frac{1}{m}\sin\left(\frac{n\pi}{2}\right) \\ & \times J_n(m_a m\pi)\sin[(mk_c+n)\omega_0 t + m\varphi_c + n\varphi_x] \end{aligned} \tag{11}$$

where $J_n(z)$ is the Bessel function of the first kind with the argument z and the order n; and m_a is the modulation index $0 < m_a \leq 1$. Substituting (11) in (8), we will obtain

$$\begin{aligned} i_{xs}(t) = {} & m_a I_{dc}\sin(\omega_0 t + \varphi_x) + \frac{2}{\pi}I_{dc}\sum_{m=1}^{+\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty}\frac{1}{m}\sin\left(\frac{n\pi}{2}\right) \\ & \times J_n(m_a m\pi)\sin[(mk_c+n)\omega_0 t + m\varphi_c + n\varphi_x]. \end{aligned} \tag{12}$$

Therefore, the dc current utilization ratio ρ, which is defined as the ratio of the amplitude I_{m1} of the fundamental component in the pulsed ac current to the dc-link current $I_{\rm dc}$, can be derived from (12) as

$$\rho = \frac{I_{m1}}{I_{dc}} = \frac{m_a I_{dc}}{I_{dc}} = m_a\,,\ (0 < m_a \leq 1)\,. \tag{13}$$

Equation (13) indicates that the maximum dc current utilization of the proposed direct CB-PWM scheme is 1.

2) Switching Harmonics of AC Current: In the proposed scheme, the two ACVs share same the effective times as that in traditional methods [27], [31], [32], but their order in the switching sequence has been swapped by choosing the references with the largest and smallest absolute values. Hence, the ACV that has longer effective time is divided into two segments, resulting in a more "evenly" pulsed ac current.

In theory, the harmonic performance of a CSC is affected by the order of ACVs [11]. For illustration, harmonic spectrums of pulsed ac current i_{as} with the three direct CB-PWM schemes are shown in Fig. 14, which are obtained in simulation with $m_a = 0.8$ and $k_c = 240$.

Fig. 14 shows that the resulting three harmonic spectrums have similar shapes over a wide frequency range up to $2f_s$, where f_s is the switching frequency. In these three cases, the amplitude of low-order harmonics (e.g., $5f_0$–$19f_0$) is relatively small (less than 0.05 A @ $I_{\rm dc} = 10$ A), while harmonics near the switching frequency account for a large proportion. Specifically, with the traditional ACV order (the one in SS-DPWM and DDPWM), the harmonic current is around 2.6 A at $f_s \pm f_0$. But it is reduced to 2.05 A with the new ACV order in the proposed DCB-PWM scheme. The same applies to the harmonic currents at $f_s \pm 5f_0$ and $f_s \pm 7f_0$. It is also noted that high-frequency harmonics are organized in sidebands and are symmetrical about integer multiples of the reference frequency, so only three harmonic currents with the highest amplitude on the left of f_s (i.e., $f_s - f_0$, $f_s - 5f_0$, and $f_s - 7f_0$) are considered.

As revealed in (12), the harmonic currents relate to the modulation index m_a. To complete the analysis, Fig. 15 compares the three modulation schemes in terms of their harmonics within input current i_{as} around switching frequencies (i.e., $f_s - f_0$, $f_s - 5f_0$, and $f_s - 7f_0$) when their modulation indexes change from 0.1 to 1. The figure shows that with the proposed DCB-PWM scheme, the switching harmonics of a CSC can be reduced over the full modulation index range.

3) Common-Mode Voltage: The CMV peak value of a CSC is affected by the chosen ZCVs. Specifically, CMVs produced by three ZCVs are equal to one of the instantaneous values of three-phase capacitor voltages (v_a, v_b, and v_c). Table III summarizes the selected ZCVs and their corresponding CMVs

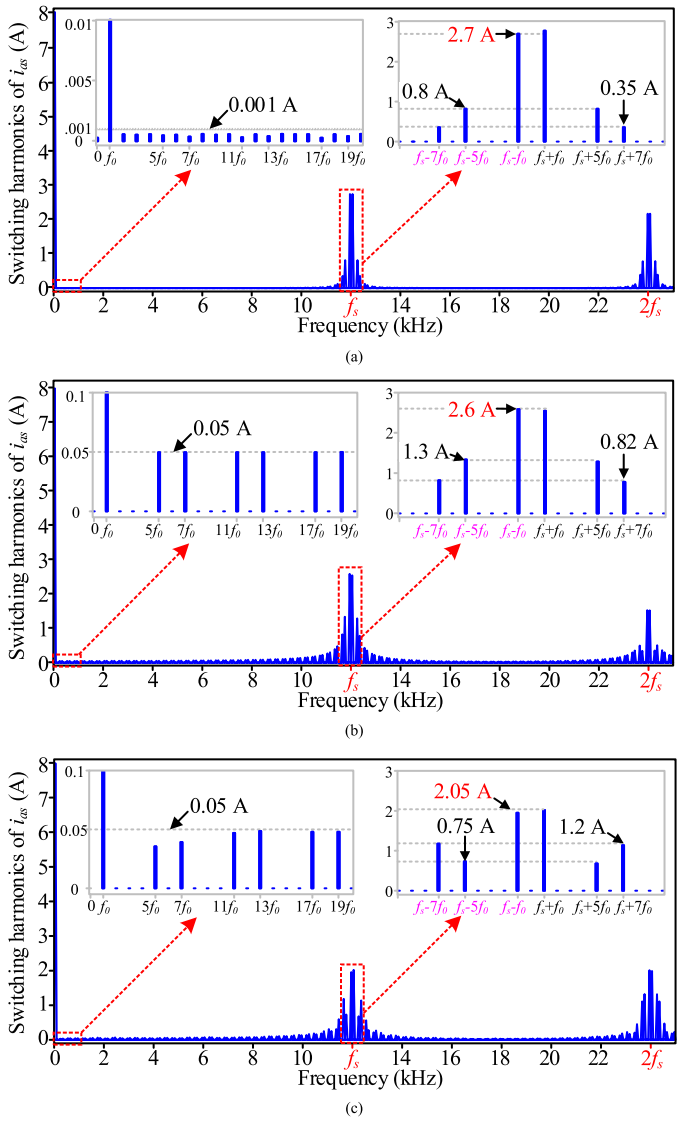

Fig. 14. Harmonic spectrum of pulsed ac current i_{as} when $m_a = 0.8$, $f_0 = 50$ Hz, $f_s = 12$ kHz, and $I_{\rm dc} = 10$ A (a) with SS-DPWM, (b) with DDPWM, and (c) with the proposed DCB-PWM scheme.

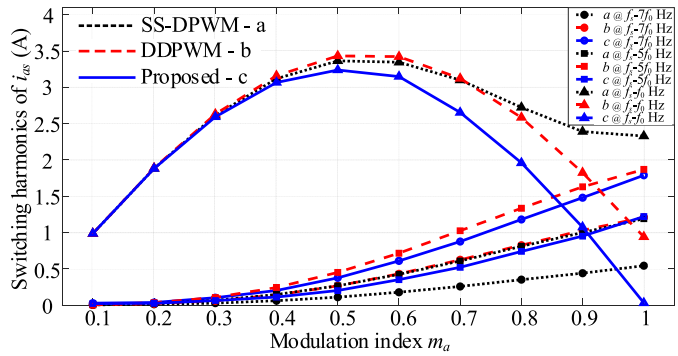

Fig. 15. Comparison of switching harmonics of pulsed ac current i_{as} with the three direct CB-PWM schemes when the modulation index m_a changes from 0.1 to 1, $f_0 = 50$ Hz, $f_s = 12$ kHz, and $I_{\rm dc} = 10$ A.

TABLE III
SELECTED ZCVS AND CORRESPONDING CMVS OF THE PROPOSED SCHEME

Sector	11	12	21	22	31	32	41	42	51	52	61	62
ZCV	I_8	I_9	I_7	I_8	I_9	I_7	I_8	I_9	I_7	I_8	I_9	I_7
CMV	v_b	v_c	v_a	v_b	v_c	v_a	v_b	v_c	v_a	v_b	v_c	v_a

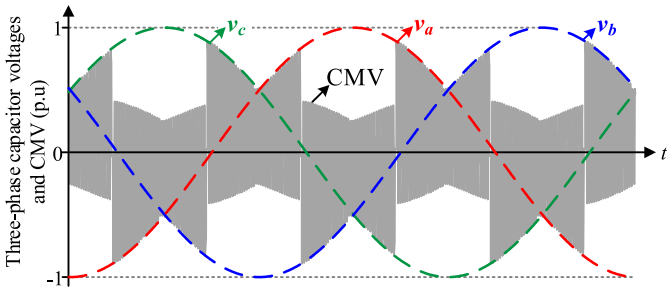

Fig. 16. Three-phase capacitor voltages and the CMV of a CSC with the proposed DCB-PWM scheme when $m_a = 0.8$, $f_0 = 50$ Hz, $f_s = 12$ kHz, and displacement angle $\varphi = \pi/50$.

with the proposed DCB-PWM scheme, and Fig. 16 shows the resultant CMV. Compared with that in the SS-DPWM scheme (see Fig. 7), the resulted CMV has smaller peak value in this case.

Fig. 17 further compares the spectrums of CMV over a wide frequency range up to $2f_s$. As shown in Fig. 17(a), the dominant harmonic of CMV in the SS-DPWM is the third-order component, which is 0.475 p.u. (with respect to the capacitor voltage). For the DDPWM, its third-order CMV is smaller (0.12 p.u.). As a contrast, the value is reduced to 0.045 p.u. with the proposed scheme, as shown in Fig. 17(c). It is also noted that the high-order CMV (i.e., f_s) of the proposed scheme is slightly higher than that of the other two schemes. Both the high-order and low-order components of the CMV can be attenuated by a CM choke. Since the CM choke presents low impedance for the low-order CMV, the proposed DCB-PWM scheme tends to require smaller CM choke than the traditional scheme due to its reduced low-order CMV [35].

Fig. 18 shows the magnitude of third-order CMV from a CSC modulated by one of the three direct CB-PWM schemes, while changing its modulation index from 0.1 to 1 and displacement angle from 0° to 90°. Clearly, as compared to SS-DPWM and DDPWM, the proposed scheme can better reduce third-order CMV over wide ranges of modulation index and displacement angle. Particularly, the CMV excited by the proposed scheme is significantly smaller than that in the SS-DPWM when $m_a > 0.5$ and $\varphi < 45°$. It is also noted that the proposed scheme features larger CMV than the SS-DPWM under high displacement angle ($> 45°$) and low modulation index (< 0.45); however, the actual value is relative small due to the low base value under low modulation index range.

4) Switching Frequency: The switching states of six switches within a carrier period are shown in Fig. 5, where two switches (S_{bp} and S_{an}) are always turned OFF and the remaining four switches switch only once. It is also noted that the transition from one switching state to the next involves only two switches

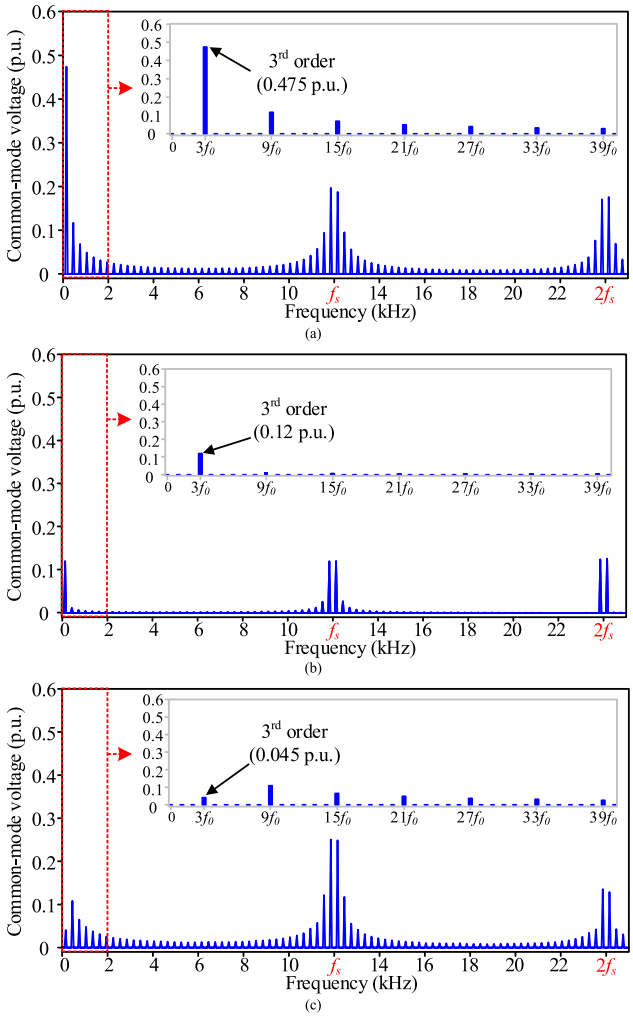

Fig. 17. Harmonic spectrum of CMV (per unit value with respect to capacitor voltage) of a CSC when $m_a = 0.8, f_0 = 50$ Hz, $f_s = 12$ kHz, and displacement angle $\varphi = \pi/50$ (a) with SS-DPWM, (b) with DDPWM, and (c) with the proposed DCB-PWM scheme.

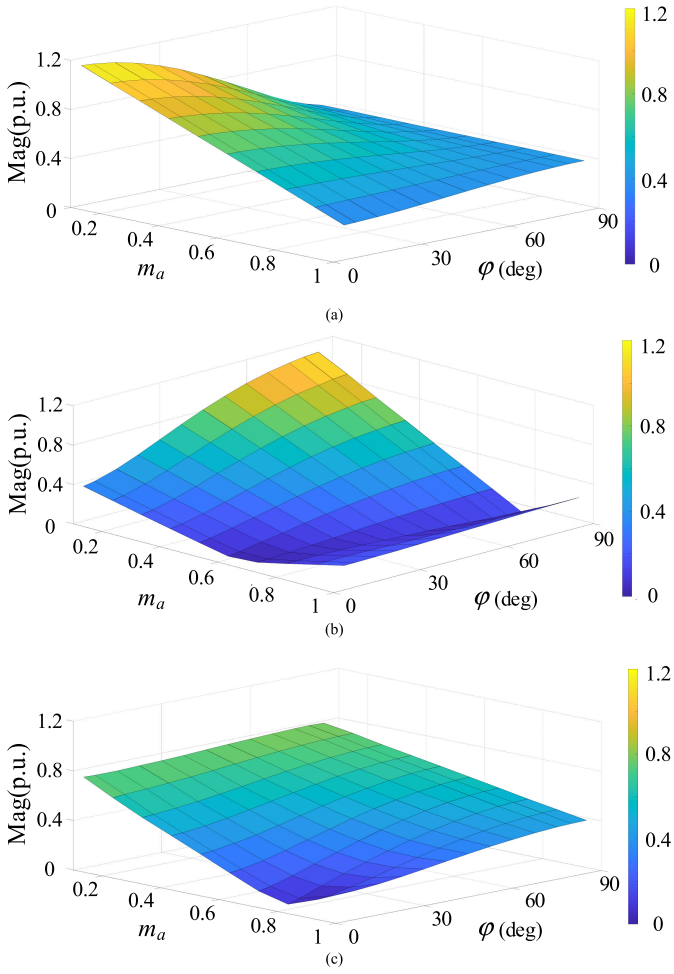

Fig. 18. Magnitude of CMV third-order component (per unit value with respect to capacitor voltage) of a CSC with varying modulation index (m_a) and displacement angle (φ) (a) with SS-DPWM, (b) with DDPWM, and (c) with the proposed DCB-PWM scheme.

within one sector. For one switch, its switching states in a line cycle are shown in Fig. 12, where every switch remains OFF in four sectors and switches once for each carrier period in eight sectors. Therefore, the average switching frequency $f_{s,av}$ can be calculated by

$$f_{s,av} = \frac{2}{3} f_c \tag{14}$$

where f_c is the carrier frequency and $f_c = \omega_c / (2\pi)$.

5) Implementation Effort: The proposed DCB-PWM scheme requires three reference currents, although only two of them are employed to compare with one carrier. The required sector information can therefore be easily obtained from the three reference currents by using Fig. 4. As seen in (11), the fundamental component of the ac current is in phase with its reference. Hence, the preprocessing, which is required by the traditional bi-tri logic PWM to improve the dc current utilization or to compensate the angle mismatch, has been removed. In addition, all the gating signals are generated directly by comparing the references with a carrier. In other words, there is no logical operation, such as "AND" and "XOR" in SS-DPWM, during the modulation process. For comparison, implementation efforts of existing CB-PWM schemes are summarized in Table IV.

TABLE IV
IMPLEMENTATION EFFORT COMPARISON OF CB-PWM SCHEMES

Items	Bi-tri logic PWM	SS-DPWM	DDPWM	**Proposed Scheme**
Reference currents	3	3	3	3
Carrier numbers	1	2	2	1
Sector information	No	Yes	Yes	Yes
Pre-processing	Yes	No	No	No
Logical operation	Yes	Yes	No	No

IV. EXPERIMENTAL RESULTS

For verification, a three-phase current source inverter has been built and tested in the lab, whose physical layout and the experimental parameters are given in Fig. 19 and Table V, respectively.

The dc-link current, supported by a dc source (TC.GSS Bidirectional DC PSU), is transferred to three-phase *R* load via a

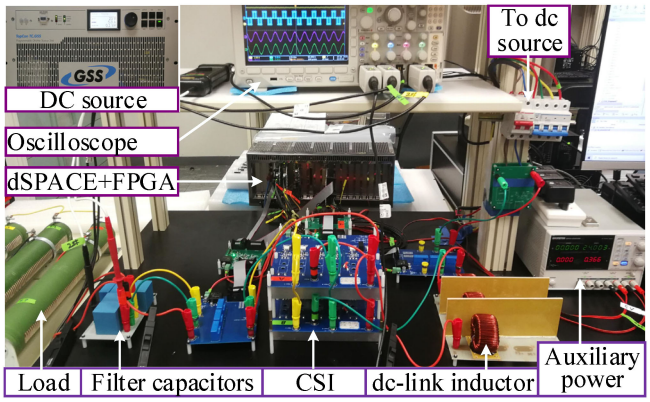

Fig. 19. Experimental system of a three-phase current source inverter.

TABLE V
EXPERIMENTAL PARAMETERS

Symbol	Parameter	Value
I_{dc}	dc-link current	5 A
m_a	Modulation index	0.8
f_o	Output frequency	50 Hz
f_s	Switching frequency	12 kHz
L_{dc}	DC-link inductor	4.5 mH
R_L	Load resistor	4 Ω
C_f	Filter capacitor	50 μF
T_{ol}	Overlap time	1 μs
S_{IGBT}	IGBT	IGW25N120H3
S_{diode}	Diode	ASTRI-12-55A

CSC operated at the switching frequency of 12 kHz, which is an integral multiple of $6f_0$ to eliminate the even and triplen harmonics [11]. An overlap time (1 μs, in this case) is inserted between two commutating switches to avoid the overvoltage spikes caused by the inductor current interruption [15]. Both the SS-DPWM and the DDPWM have been chosen for comparison, since they also belong to direct CB-PWM schemes, as summarized in Table I. These two schemes, together with the proposed DCB-PWM scheme, are implemented in a dSPACE (DS1007) plus FPGA (DS5203_7K325) digital control system. Open-loop control with specific output frequency and modulation index is adopted to compare these modulation methods under different conditions. Their characteristics are presented in four different aspects as follows.

A. AC Current

Fig. 20 shows the pulsed ac current i_{as} and its fast Fourier transform (FFT) result for the three direct CB-PWM schemes. It can be seen that all three schemes have the same fundamental component (2.7 A @ f_0) under the same modulation index ($m_a = 0.8$). In addition, both SS-DPWM and DDPWM have similar switching harmonics (around 0.8 A @ f_s−f_0), which is 25% higher than that of the proposed DCB-PWM (0.6 A @ f_s−f_0). That is because in the proposed scheme, the long-acting vector rather than the short-acting one has been divided into two segments in each switching sequence, resulting in a more "evenly" pulsed ac current. Fig. 21 shows the total harmonic distortion (THD) of the filtered ac current i_a and its first ten

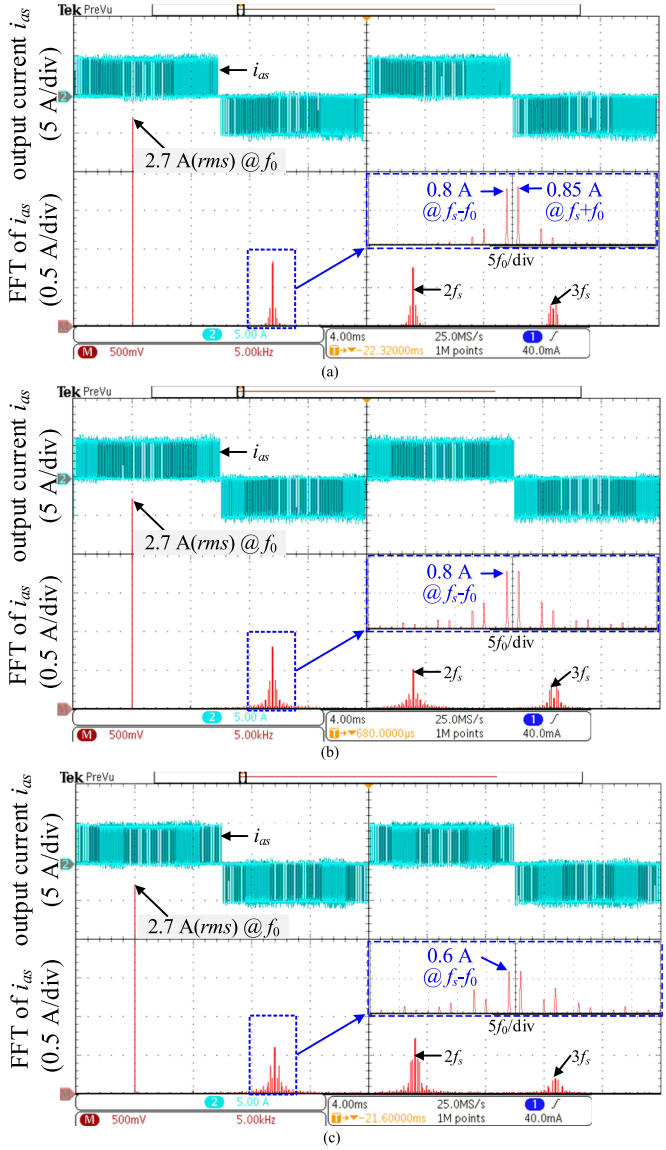

Fig. 20. Waveforms of pulsed ac current i_{as} and its FFT result when $m_a = 0.8$, $f_0 = 50$ Hz, and $f_s = 12$ kHz. (a) SS-DPWM. (b) DDPWM. (c) Proposed DCB-PWM.

harmonics for the three schemes. The THD is measured through the MDO3PWR (power analysis application module) of the oscilloscope (MDO3104 from TEKTRONIX), which records the first 100 harmonics (i.e., up to 5 kHz) for calculation. It can be seen that the THD of the proposed scheme is lower than that of the DDPWM scheme, but slightly higher than that of the SS-DPWM scheme, which is consistent with the low-frequency spectrum of pulsed ac current presented in Fig. 14.

B. Common-Mode Voltage

Fig. 22 shows the CMV and its FFT result for the three direct CB-PWM schemes. As shown in Fig. 22(a), the dominated CMV for the SS-DPWM scheme is the third-order harmonic, which is 4.5 V with load resistor R_L equaling 4 Ω. For the DDPWM scheme [see Fig. 22(b)], its third-order harmonic component is reduced to 1.1 V. As a contrast, the proposed

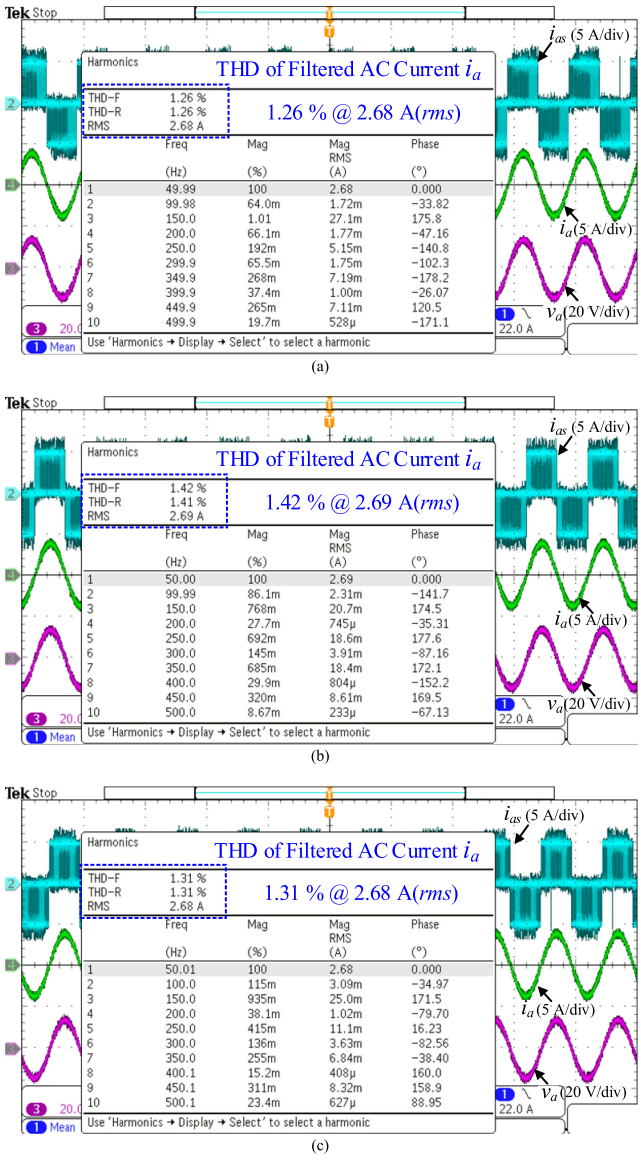

Fig. 21. THD of filtered ac current i_a and its first ten harmonics when $m_a = 0.8$, $f_0 = 50$ Hz, and $f_s = 12$ kHz. (a) SS-DPWM. (b) DDPWM. (c) Proposed DCB-PWM.

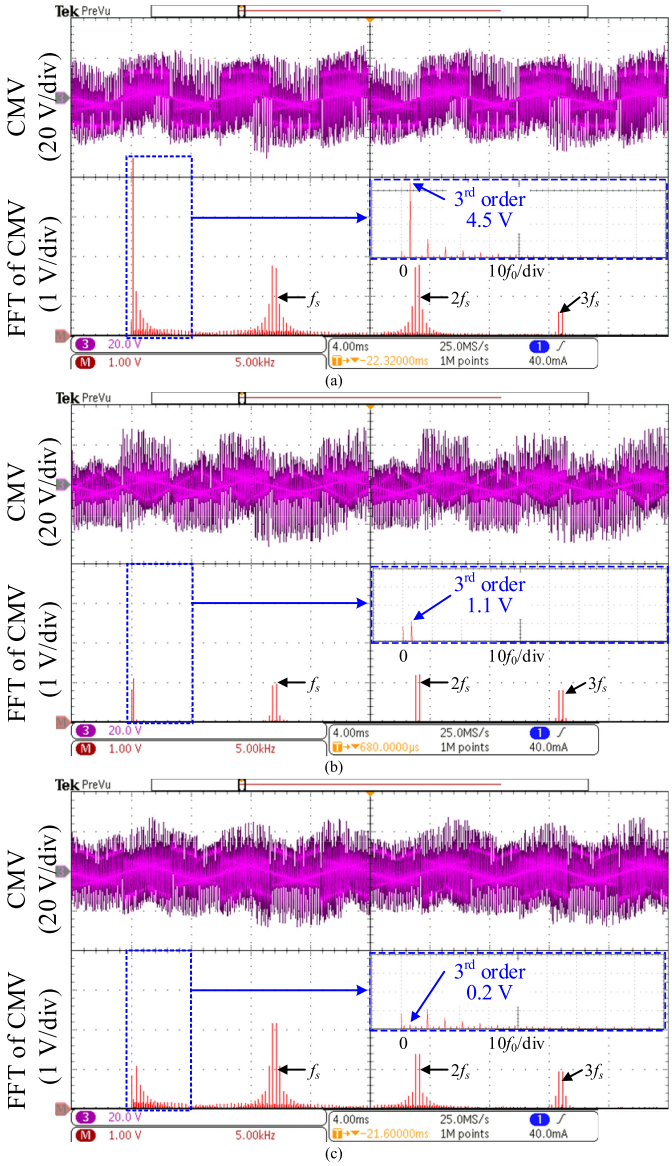

Fig. 22. Waveforms of CMV and its FFT result when $m_a = 0.8$, $f_0 = 50$ Hz, $f_s = 12$ kHz, and displacement angle $\varphi = \pi/50$. (a) SS-DPWM. (b) DDPWM. (c) Proposed DCB-PWM.

scheme has the lowest third-order harmonic of CMV under this situation, which is only 0.2 V, as shown in Fig. 22(c). It is also noted that the DDPWM features the lowest CMV at switching frequency, while the proposed scheme has higher switching-frequency CMV. The difference of the CMV between the three CB-PWM schemes is caused by the different selection of ZCVs, as analyzed in Section II. The CMV relates to the modulation index and displacement angle as well, whose effects have been summarized in Fig. 18.

C. DC Current Utilization

Fig. 23 shows waveforms of dc-link current $i_{\rm dc}$, pulsed ac current i_{as}, and its corresponding FFT result with the proposed modulation scheme when m_a is 1. As shown on the top right corner of Fig. 23, the dc current utilization ratio ρ of the proposed

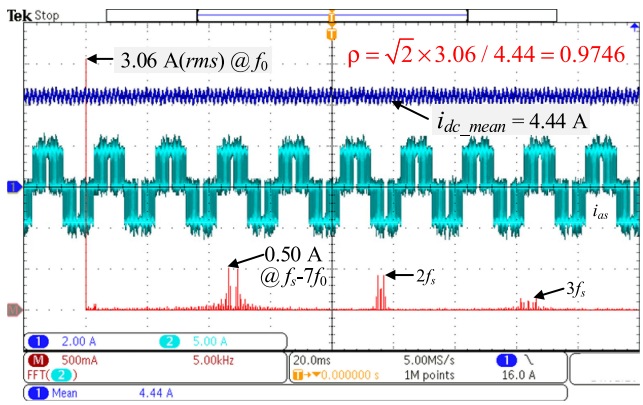

Fig. 23. Waveforms of dc-link current $i_{\rm dc}$, pulsed ac current i_{as}, and its corresponding FFT result with the proposed modulation scheme when $m_a = 1$, $f_0 = 50$ Hz, and $f_s = 12$ kHz.

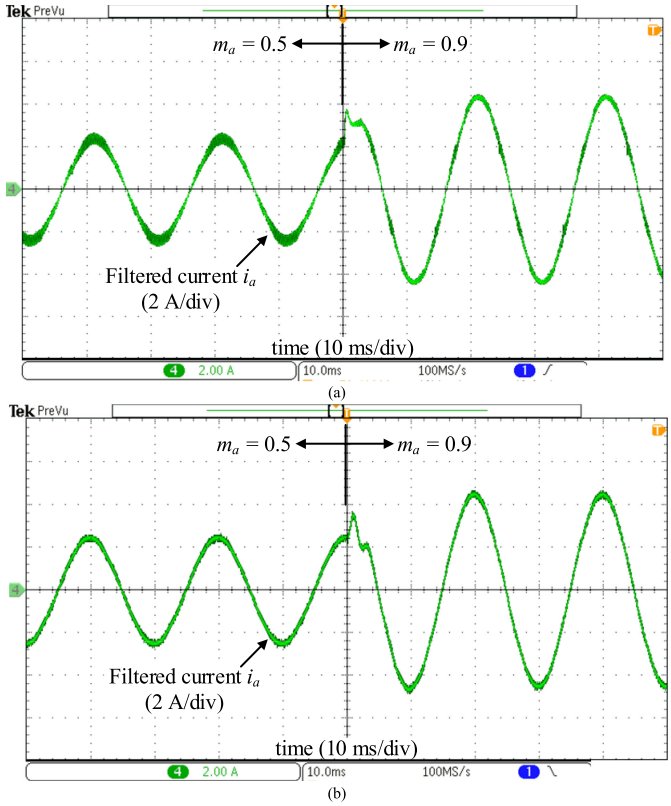

Fig. 24. Waveform of filtered ac current i_a with the proposed modulation scheme when the modulation index m_a changes from 0.5 to 0.9 and $I_{\rm dc} = 5$ A (a) with R load ($R_L = 4\ \Omega$) and (b) with RL load ($R_L = 4\ \Omega$, $L = 4.5$ mH).

scheme is slightly lower than 1. This is caused by the overlap time ($T_{ol} = 1\ \mu$s , in this case) used to ensure the safety of current commutation. Both SS-DPWM and DDPWM share similar dc current utilization ratio since they also require the overlap time to ensure the safe operation of a CSC.

D. Dynamic Waveform

Fig. 24 shows the waveform of filtered ac current i_a with the proposed scheme when the modulation index changes from 0.5 to 0.9 under both R and RL loads. In both cases, the amplitude of i_a changes immediately from 2.5 to 4.5 A with the dc-link current $I_{\rm dc} = 5$ A. It is also noted that i_a in Fig. 24(b) shows less harmonics than that in Fig. 24(a), which is due to the enhanced harmonic attenuation introduced by the LC filter.

In addition, Fig. 25 shows the waveforms of ac currents i_{as} and i_a when the frequency of current reference changes from 25 to 50 Hz. It can be seen that the CSI can operate smoothly in these two frequencies with the proposed modulation scheme.

To summarize, the proposed DCB-PWM scheme can help to simultaneously reduce the switching harmonics of ac current and low-order CMV, especially the third-order component, for a CSC, which is consistent with the theoretical analyses in Section III. Effectiveness of the proposed scheme has therefore been verified.

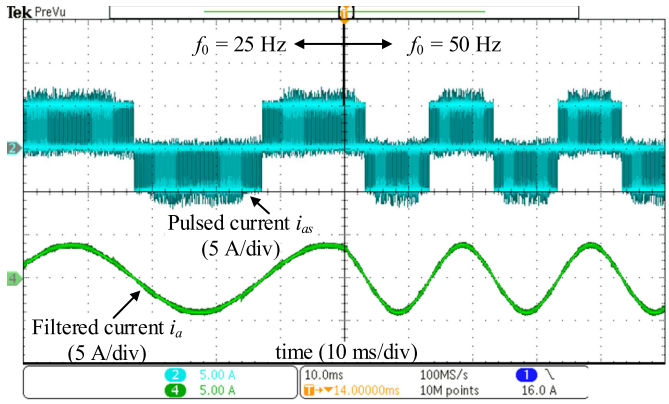

Fig. 25. Waveforms of pulsed ac current i_{as} and filtered ac current i_a with the proposed modulation scheme when the frequency of reference changes from 25 to 50 Hz at $m_a = 0.8$ and $I_{\rm dc} = 5$ A.

V. Conclusion

This article investigates the modulation mechanism of CB-PWM for a three-phase CSC and reveals that the order of ACVs can be adjusted by choosing the reference signals, while the selection of ZCV relates to the adopted combination rules. Based on that, this article proposes a DCB-PWM scheme for a CSC. In the proposed scheme, two references with the maximum and minimum absolute values are chosen to compare with only one carrier, and switching patterns are directly generated to drive a CSC. Its implementation, mechanism, and characteristics have been developed and discussed in detail. It is shown that, the proposed scheme features high dc current utilization ($\rho_{\max} = 1$), reduced switching frequency ($f_{s,av} = 2/3f_c$), and easy implementation (requires no logical operation). More importantly, compared with existing CB-PWM schemes, the proposed scheme can simultaneously reduce the switching harmonics of ac current (e.g., 25% lower than SS-DPWM and DDPWM @ $m_a = 0.8$) and the low-order CMV of a CSC (e.g., the third-order CMV reduces from 4.5 to 0.2 V @ $m_a = 0.8$ and $\varphi = \pi/50$). Effectiveness of the proposed scheme has been verified experimentally with a CSC operating as an inverter. Owing to its superior properties, the proposed DCB-PWM scheme has the potential benefits to scale down the ac filter and CM choke for practical CSC applications.

Acknowledgment

The authors would like to thank the Hong Kong Applied Science and Technology Research Institute (ASTRI) for providing the power devices for experiments and for the thoughtful suggestions. The author L. Ming would like to thank X. Xue for her encouragement and help.

References

[1] B. Wu, *High-Power Converters and AC Drives*. New York, NY, USA: Wiley, 2006.

[2] Q. Wei, B. Wu, D. Xu, and N. R. Zargari, "Further study on a PWM current-source-converter-based wind energy conversion system considering the DC-link voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5378–5387, Jun. 2019.

[3] K. Gnanasambandam, A. K. Rathore, A. Edpuganti, D. Srinivasan, and J. Rodriguez, "Current-fed multilevel converters: An overview of circuit topologies, modulation techniques, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3382–3401, May 2017.
[4] X. Guo, N. Wang, J. Zhang, B. Wang, and M. Nguyen, "A novel transformerless current source inverter for leakage current reduction," *IEEE Access*, vol. 7, pp. 50681–50690, 2019.
[5] P. Cossutta, M. P. Aguirre, A. Cao, S. Raffo, and M. I. Valla, "Single-stage fuel cell to grid interface with multilevel current-source inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5256–5264, Aug. 2015.
[6] R. A. Torres, H. Dai, W. Lee, T. M. Jahns, and B. Sarlioglu, "Current-source inverters for integrated motor drives using wide-bandgap power switches," in *Proc. IEEE Trans. Elect. Conf. Expo.*, 2018, pp. 1002–1008.
[7] T. M. Jahns and H. Dai, "The past, present, and future of power electronics integration technology in motor drives," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 197–216, Sep. 2017.
[8] Q. Wei, L. Xing, D. Xu, B. Wu, and N. R. Zargari, "Modulation schemes for medium-voltage PWM current source converter-based drives: An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1152–1161, Jun. 2019.
[9] H. R. Karshenas, H. A. Kojori, and S. B. Dewan, "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 566–573, Sep. 1995.
[10] J. He, C. Zhang, M. Lei, J. Han, P. Guo, and Y. Li, "An active bypass pulse injection based low switching frequency PWM approach for harmonic compensation of current source converters," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1614–1625, Feb. 2021.
[11] Y. W. Li, B. Wu, D. Xu, and N. R. Zargari, "Space vector sequence investigation and synchronization methods for active front-end rectifiers in high-power current-source drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1022–1034, Mar. 2008.
[12] Q. Wei, B. Wu, D. Xu, and N. R. Zargari, "A natural-sampling-based SVM scheme for current source converter with superior low-order harmonics performance," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6144–6154, Sep. 2016.
[13] X. Guo, Y. Yang, and X. Wang, "Optimal space vector modulation of current-source converter for DC-link current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1671–1680, Mar. 2019.
[14] X. Guo, Y. Yang, B. Wang, and Z. Lu, "Generalized space vector modulation for current source converter in continuous and discontinuous current modes," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9348–9357, Nov. 2020.
[15] P. Liu, Z. Wang, Y. Xu, H. Xiao, and Y. Li, "Optimal overlap-time distribution of space vector modulation for current-source rectifier," *IEEE Trans. Ind. Electron.*, early access, Apr. 28, 2020, doi: 10.1109/TIE.2020.2989714.
[16] N. Zhu, D. Xu, B. Wu, N. R. Zargari, M. Kazerani, and F. Liu, "Common-mode voltage reduction methods for current-source converters in medium-voltage drives," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 995–1006, Feb. 2013.
[17] J. Shang and Y. W. Li, "A space-vector modulation method for common-mode voltage reduction in current-source converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 374–385, Jan. 2014.
[18] A. Hu, D. Xu, B. Wu, J. Wang, and J. Su, "Reference-trajectory-optimized SVM for high-power current-source converters to improve harmonic performance and reduce common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3488–3498, Jul. 2015.
[19] L. Ding, Y. W. Li, and K. Sun, "Discontinuous bi-tri logic SPWM for current source converter with optimized zero-state replacement," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 718–723.
[20] J. Shang, Y. W. Li, N. R. Zargari, and Z. Cheng, "PWM strategies for common-mode voltage reduction in current source drives," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5431–5445, Oct. 2014.
[21] Y. Lian, Y. Zhang, Y. W. Li, N. R. Zargari, and Z. Cheng, "Common-mode resonance suppression in transformerless PWM current-source drive," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5721–5731, Aug. 2016.
[22] Y. Lian, Y. W. Li, Z. Quan, N. R. Zargari, and Z. Cheng, "SVM strategies for common-mode current reduction in transformerless current-source drives at low modulation index," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1312–1323, Feb. 2017.
[23] K. Tian, J. Wang, B. Wu, Z. Cheng, and N. R. Zargari, "A virtual space vector modulation technique for the reduction of common-mode voltages in both magnitude and third-order component," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 839–848, Jan. 2016.
[24] L. K. Ries and M. L. Heldwein, "Current balancing control methods using advanced carrier-based modulation for five-level current source rectifiers," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10213–10226, Oct. 2020.
[25] L. Ding and Y. Li, "Simultaneous DC current balance and CMV reduction for parallel CSC system with interleaved carrier-based SPWM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8495–8505, Oct. 2020.
[26] B. Wu, S. B. Dewan, and G. R. Slemon, "PWM-CSI inverter for induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 28, no. 1, pp. 64–71, Jan./Feb. 1992.
[27] J. R. Espinoza and G. Joos, "Current-source converter on-line pattern generator switching frequency minimization," *IEEE Trans. Ind. Electron.*, vol. 44, no. 2, pp. 198–206, Apr. 1997.
[28] J. Isozaki, K. Suzuki, W. Kitagawa, and T. Takeshita, "PWM strategies with duality between current and voltage source AC/DC converters for suppressing AC harmonics or DC ripples," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.
[29] O. Ojo, "The generalized discontinuous PWM scheme for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 6, pp. 1280–1289, Dec. 2004.
[30] Y. Li, L. Ding, and Y. W. Li, "Isomorphic relationships between voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7131–7135, Aug. 2019.
[31] Z. Bai, X. Ruan, and Z. Zhang, "A generic six-step direct PWM (SS-DPWM) scheme for current source converter," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 659–666, Mar. 2010.
[32] N. Choi, K. Lee, and B. Han, "A novel carrier based PWM for current source converter," in *Proc. IEEE Inter. Power Electron. Motion Control Conf.*, 2012, pp. 1945–1950.
[33] A. Bhowmik, A. Maitra, S. M. Halpin, and J. E. Schatz, "Determination of allowable penetration levels of distributed generation resources based on harmonic limit considerations," *IEEE Trans. Power Del.*, vol. 18, no. 2, pp. 619–624, Apr. 2003.
[34] A. Charalambous, X. Yuan, and N. McNeill, "High-frequency EMI attenuation at source with the auxiliary commutated pole inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5660–5676, Jul. 2018.
[35] N. Zhu, J. Kang, D. Xu, B. Wu, and Y. Xiao, "An integrated AC choke design for common-mode current suppression in neutral-connected power converter systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1228–1236, Mar. 2012.
[36] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1152–1158, Mar. 2012.
[37] X. Guo, D. Xu, and B. Wu, "Four-leg current-source inverter with a new space vector modulation for common-mode voltage suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6003–6007, Oct. 2015.
[38] J. He, Y. Lyu, J. Han, and C. Wang, "An SVM approach for five-phase current source converters output current harmonics and common-mode voltage mitigation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5232–5245, Jul. 2020.
[39] X. Guo, D. Xu, and B. Wu, "Common-mode voltage mitigation for back-to-back current source converter with optimal space vector modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 688–697, Jan. 2016.
[40] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.
[41] Z. Bai, Z. Zhang, and X. Ruan, "A natural soft-commutation PWM scheme for current source converter and its logic implementation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2772–2779, Jul. 2011.

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