A Bidirectional DC–DC Converter With High Voltage Conversion Ratio and Zero Ripple Current for Battery Energy Storage System

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***Abstract*—In this article, a novel bidirectional dc–dc converter (BDC) consisting of an active switched-inductor (A-SL) cell, a zero current ripple cell and an auxiliary capacitor cell is proposed for the battery energy storage system. The proposed BDC integrates with the advantages of high voltage conversion ratio, low power switch voltage stresses, zero ripple current on the low voltage side (LVS), and constant potential difference between the grounds of LVS and high voltage side. Thanks to the use of synchronous rectification technology, the efficiency of the proposed BDC is increased. The operating principles, the characteristics analysis and the parameter design of the proposed BDC are given. In addition, to show the merits of the proposed BDC, a comparison study involves the proposed converter and other BDCs is demonstrated. Finally, some experimental results obtained using a 1000 W prototype are presented to valid the effectiveness of the proposed BDC. 96.43% and 96.67% maximum conversion efficiencies can be achieved in the step-up and step-down modes, respectively.**

***Index Terms*—Battery energy storage system (BESS), bidirectional dc–dc converter, high voltage conversion ratio, low voltage stress, zero ripple current.**

I. Introduction

BATTERY energy storage system (BESS) with characters of robustness and high energy density has been widely used in renewable power generation, microgrids, electric and hybrid vehicles, and uninterrupted power supplies [1], [2]. It serves as an energy buffer (storage energy or release energy) to transfer bidirectional power flow with the dc bus. In the BESS, the paralleled battery cell structures are mainly used to improve the system reliability and avoid charge imbalance phenomenon [3]. However, due to the paralleled connection of the battery cells, the low output voltage of the BESS (24–48 V) results in a voltage-level mismatch between the BESS and the dc bus (200–400 V). To overcome this issue, a bidirectional dc–dc converter (BDC) with high voltage conversion ratio is required to link the BESS with the dc bus [4].

BDCs are divided into isolated and nonisolated topologies. For isolated dc–dc converters, a high frequency (HF) transformer realizes the two stage dc–ac–dc power conversion, accompanied by galvanic isolation between low voltage side (LVS) and high voltage side (HVS). The nonisolated dc–dc converters are superior to isolated topologies in simple structure and control strategy when the galvanic isolation is not necessary [5].

Due to the simple structure and low cost, the conventional nonisolated buck/boost BDC has been widely applied. However, its highest achievable voltage conversion ratio is limited by existence of the circuit parasitic parameters and extreme duty-cycle. Besides, its high power switch voltage stresses also prevent it from high voltage applications. To fill this gap, many improved nonisolated BDCs have been proposed in the last decades [6]–[17].

The boost voltage conversion techniques adopted by these BDCs mainly include multilevel technique [6]–[8], cascaded technique [9], voltage multiplier [10], coupled-inductor [11]–[14], switched-inductor and switched-capacitor [15]–[17]. The multilevel technique is an effective solution to improve the voltage conversion ratio. Meanwhile, it also suppresses the voltage stresses on power switches [6]. Unfortunately, such technique introduces a large quantity of power switches and the voltage balance issue on these power switches significantly increase the difficulties of the controller design [7], [8]. Although the cascaded structure provides the BDC a high conversion ratio [9], the high voltage stresses on power switches still remain to be solved. In addition, the multistage energy conversion exists in the cascaded structure degrades the converter efficiency. A dc–dc converter with voltage multiplier cells, which possesses high voltage conversion ratio and low voltage stresses, has been proposed in [10]. However, the high voltage conversion ratio only can be achieved with a large amount of voltage multiplier cells, which results in the converter a low power density and high cost. The coupled-inductor techniques have been adopted in several topologies [11]–[14]. The high conversion ratio is achieved by adjusting the turn ratio of the magnetic coupling components. However, the unavoidable leakage inductance issue leads to voltage spikes on power switches [11]. Hence, additional

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snubber circuit is required to recycle the energy stored in leakage inductance [12]. Two kinds of basic switched-inductor structures have been presented in [15]. Owing to its unique energy transfer rule, a high voltage conversion ratio is obtained. In addition, a higher voltage conversion ratio and lower power switch voltage stresses can be achieved by inserting extra switched-capacitor cells. However, the HF pulsewidth modulation (HF PWM) potential difference between the grounds of their LVS and HVS may result in severe electromagnetic interference (EMI) problem [16], [17]. Besides the pros and cons of the aforementioned BDCs, one of their common drawbacks is the large ripple current on the LVS. Since the BESS is very sensitive to the LVS current ripple, where the large LVS current ripple reduces the service life of the BESS, the design of the BDCs using the ripple current limit techniques is required [18].

Interleaved structure is one of the effective methods to reduce the large LVS current ripple [19]. However, to achieve current ripple cancelation, the converter duty-cycle must strictly satisfy certain fixed proportion with the number of the interleaving phase. Another useful LVS current ripple suppresser is the ripple injection circuit. It can be categorized as active type and passive type. The former has been proposed in [20]. An additional ripple mirror circuit is used to counteract the original current ripple on the LVS. Whereas, in order to realize zero current ripple, the converter has to operate with fixed duty-cycle, which limits the achievable voltage conversion ratio. The latter perfectly removes the current ripple by constructing the injected passive ripple current in [21]. However, the zero current ripple is obtained at the expense of circuit complexity and cost. In [22] and [23], an LVS ripple cancellation network (RCN) has been integrated to eliminate the current ripple. The networks mainly consist of coupled inductors and *LC* circuits. Although the RCN can effectively eliminate the current ripple, the complicated parameter design process is not desired. Recently, current ripple suppressor using a simple *LC* filter structure has been proposed in [24], [25]. Its simple structure, which only includes an inductor and a capacitor, makes it attractive in industrial applications. In addition, once the parameters of the *LC* filter are selected, the performance on the current ripple eliminate is irrelevant to neither the converter duty-cycle nor other circuit parameters. Such feature provides the *LC* filter current ripple suppressor a wide range of operation conditions and makes it suitable for various BESS applications.

In this article, a novel nonisolated bidirectional dc–dc converter for the BESS is proposed. This BDC has following main characters:

1) high conversion ratio without extreme duty-cycle;
2) zero ripple current on the LVS;
3) low voltage stresses on power switches;
4) constant potential difference between the grounds of its LVS and HVS.

The rest of this article is organized as follows. Topology of the proposed converter is demonstrated in Section II. Section III presents the operating principles and analyses of the proposed converter. Characteristics of the proposed converter are given in Section IV. The experimental results and corresponding analysis are described in Section V. Finally, Section VI concludes this article.

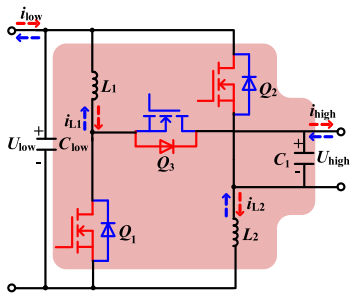

Fig. 1. Configuration of the basic bidirectional A-SL based converter.

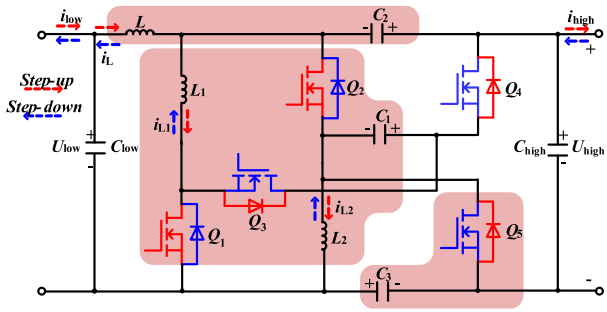

Fig. 2. Configuration of the proposed converter.

II. Topology of the Proposed Converter

A basic bidirectional active switched-inductor (A-SL) based converter [15], [26] is demonstrated in Fig. 1, where the $Q_{\rm i}$ ($i = 1, 2, 3$) represents the power switch. The $U_{\rm low}$ denotes the voltage of the LVS, which is connected to a BESS, while the $U_{\rm high}$ stands for the voltage at the HVS, which is connected to the dc bus of a microgrid. After Q_1 and Q_2 are simultaneously turned ON and Q_3 is turned OFF, the inductors L_1 and L_2 are charged/discharged in parallel. Then, both Q_1 and Q_2 are turned OFF and only Q_3 is conducting, L_1 and L_2 are discharged/charged in series. Owing to the parallel and series connections of the inductors, a higher voltage conversion ratio can be achieved compared with the conventional bidirectional two-level buck-boost converter [15]. However, the aforementioned A-SL based converter suffers from some drawbacks. Several key drawbacks are listed as follows.

1) The high LVS current ripple degrades the service life of the BESS.
2) The switch Q_3 endures a very high voltage stress which is greater than $U_{\rm high}$ (the voltage on HVS).
3) An inductor links the negative pole of the LVS and HVS, which introduces HF harmonics in both $U_{\rm low}$ and $U_{\rm high}$.

In order to overcome the above drawbacks, an improved bidirectional converter is proposed in this section. The schematic of the proposed converter is shown in Fig. 2. This topology is composed of three main parts, i.e., the A-SL cell (inductors L_1 and L_2, power switches Q_1, Q_2, and Q_3, and capacitor C_1), the zero current ripple cell (L and C_2) and the auxiliary capacitor cell (Q_5 and C_3). The power switch Q_4 is used to connect the A-SL cell and the zero current ripple cell. $C_{\rm low}$ and $C_{\rm high}$ denote the filter capacitors on the LVS and HVS, respectively. In addition,

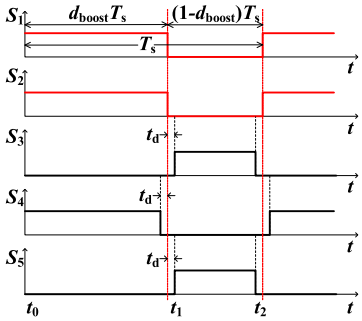

Fig. 3. Gate signals in the step-up mode.

$i_{\rm low}$ and $i_{\rm high}$ stand for the currents pass the terminals of LVS and HVS, respectively. $U_{\rm Qi}$ $(i = 1, 2, 3, 4, 5)$ represents the voltage stress of $Q_{\rm i}$. $U_{\rm Ci}$ is the voltage stress of $C_{\rm i}$ $(i = 1, 2, 3)$. The currents pass L, L_1, and L_2 are indicated by $i_{\rm L}$, $i_{\rm L1}$, and $i_{\rm L2}$, respectively. It is worth noting that $i_{\rm L} = i_{\rm low}$.

Thanks to the zero current ripple cell, the current ripple on the LVS can be effectively eliminated. The auxiliary capacitor cell connects the negative poles of the $U_{\rm high}$ and $U_{\rm low}$, which significantly reduces the voltage HF harmonics compared with the basic A-SL based converter. In addition, the combination of the three parts also provides the converter a higher voltage conversion ratio and lower voltage stresses on all power switches.

III. Operating Principles and Analyses of the Proposed Converter

The proposed converter is able to operate in two modes, namely step-up mode and step-down mode, to realize bidirectional power flow between the LVS and the HVS. The operating principles of the proposed converter in the continuous conduction mode (CCM) are analyzed in this section.

To simplify the analysis, the following reasonable assumptions have been made.

Assumption 1: All the components are considered ideal and the components parasitic parameters are ignored.

Assumption 2: All capacitors are large enough to avoid the voltage ripple.

A. Step-Up Mode

In the step-up operating mode, the power flow is transmitted from LVS to HVS. Q_1 and Q_2 work as main power switches, while Q_3, Q_4, and Q_5 are treated as the slave power switches. Here, the main power switch indicates the switch, where the current flows through the MOSFET part when it is turned ON; the slave power switch indicates the switch where the antiparallel diode part provides the current flow path. To further reduce the conduction loss and improve the efficiency, the synchronous rectification technology is applied to the slave power switches. As results, the current will flows the MOSFET part of the slave power switches instead of the antiparalleled diode.

The corresponding gate signals S_1–S_5 for Q_1–Q_5 are shown in Fig. 3, respectively. The $d_{\rm boost}$ represents the duty-cycle of S_1 and S_2, and $T_{\rm s}$ indicates one switching period. It can be found

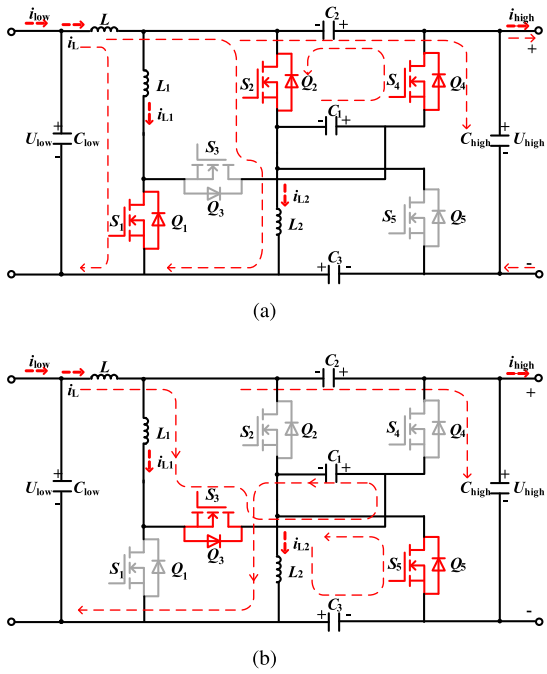

Fig. 4. Current flow paths of the proposed converter in the step-up mode. (a) State I. (b) State II.

that the dead-time $t_{\rm d}$ is adopted on Q_3, Q_4, and Q_5 to avoid the short circuit issues caused by power switches. In addition, thanks to the introduction of the dead-time, the antiparallel diodes of Q_3–Q_5 are conducted during the period of $t_{\rm d}$, which leads to zero-voltage-switching (ZVS) on the MOSFET of Q_3–Q_5 after the dead-zone, and, hence, significantly reduces the switching losses.

In addition, there are two switching states in step-up mode, whose current flow paths of the proposed converter are depicted in Fig. 4. The typical waveforms of the converter are presented in Fig. 5.

State I: As shown in Fig. 4(a), Q_1 and Q_2 are forward turned ON; Q_4 is reversely turned ON while Q_3 and Q_5 are turned OFF. Under such switch configuration, L_1 and L_2 are charged by BESS ($U_{\rm low}$). Meanwhile, due to the existence of slight voltage difference between C_1 and C_2, C_1 releases energy to C_2 through Q_2 and Q_4. In addition, $C_{\rm high}$ is charged by $U_{\rm low}$, L, C_2, and C_3. And it also feeds the load. It is worth mentioning that, in practice, the possible current spike caused by the energy transfer between C_1 and C_2 can be suppressed by the circuit equivalent series resistances (ESRs).

State II: The current flow paths in state II are demonstrated in Fig. 4(b). Q_3 and Q_5 are reversely turned ON, and all other switches are turned OFF. The $U_{\rm low}$, L, L_1, and L_2 are connected in series to feed energy to C_1. And L_2 also charges C_3. Besides, $C_{\rm high}$ is charged by $U_{\rm low}$, the zero current ripple cell, and C_3 together. Similarly, the load is fed by $C_{\rm high}$.

B. Step-Down Mode

In step-down mode, the proposed converter transfers energy from HVS to LVS. In this operating mode, Q_3, Q_4, and Q_5

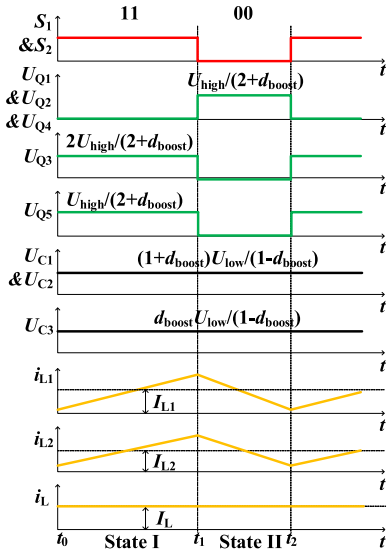

Fig. 5. Typical waveforms of the proposed converter in the step-up mode.

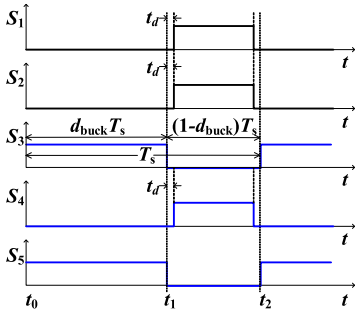

Fig. 6. Gate signals in the step-down mode.

serve as the main power switches. The gate signals of Q_3 and Q_5 share the same duty-cycle d_{buck}, and Q_4 is complementary to Q_3 and Q_5. Besides, synchronous rectification technology are adopted on the slave switches Q_1 and Q_2. Fig. 6 demonstrates the S_1–S_5, the corresponding converter current flow paths are shown in Fig. 7, and Fig. 8 presents the typical waveforms in step-down mode.

State I: The current flow paths in this state are illustrated in Fig. 7(a). Q_3 and Q_5 are forward turned ON and others are turned OFF. C_1 transfers energy to L_1, L_2, and C_{low}. Meanwhile, L_2 is magnetized by C_3. In addition, dc bus (U_{high}) deliveries energy to C_{low} through L, C_2, and C_3. And the load power is provided by C_{low}.

State II: It can be seen from Fig. 7(b), Q_4 is forward turned ON, and Q_1 and Q_2 are reversely turned ON. In contrast, Q_3 and Q_5 are turned OFF. In this mode, C_{low} is charged by L_1 and L_2 in parallel, and C_2 charges C_1. Besides, U_{high} transfers energy to C_2, C_3, and C_{low}. Similarly, the load is fed by C_{low}.

C. Averaged Reduced-Order Model

To design the controller for the proposed BDC, a corresponding averaged state-space converter model is necessary.

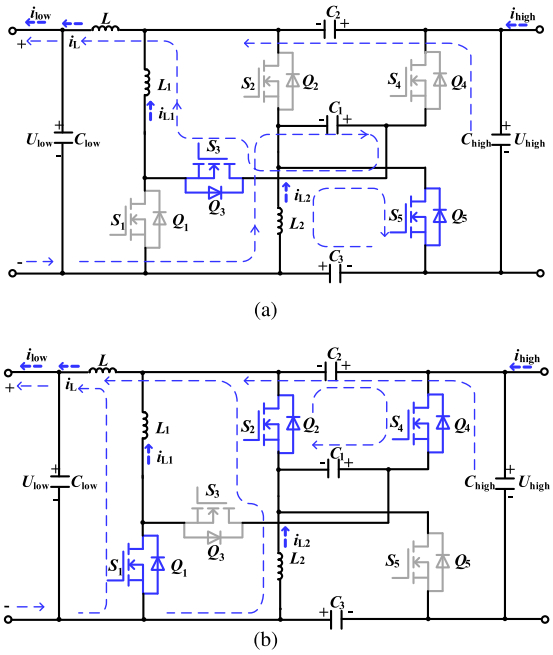

Fig. 7. Current flow paths of the proposed converter in the step-down mode. (a) State I. (b) State II.

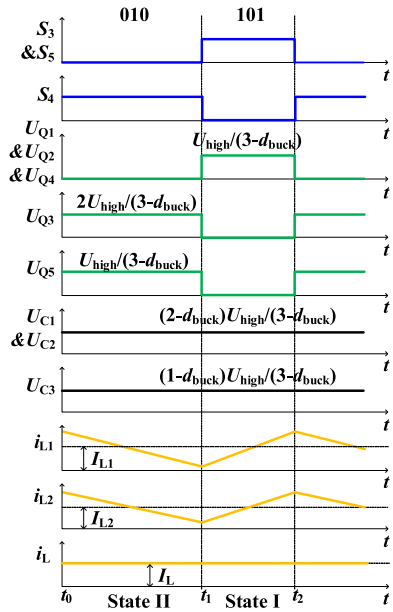

Fig. 8. Typical waveforms of the proposed converter in the step-down mode.

Considering the feature of zero current ripple on the inductor L and using the converter operational principle given above, the reduced-order models for the proposed BDC operating in the step-up model and the step-down mode are derived as (1) and (2), respectively. Note that, for the purpose of achieving an accurate model, the ESRs of the middel capacitors, i.e. C_1, C_2, and C_3, are taken into account in the modeling process.

It is worth noting that, in both (1) and (2), i_{L1} and i_{L2} represent the averaged currents pass inductors L_1 and L_2, respetively;

u_{C1}, u_{C2}, u_{C3}, u_{high}, and u_{low} denote the averaged voltages across the capacitors C_1, C_2, C_3, C_{high}, and C_{low}, respectively; $d_{boost}(d_{buck}) \in (0,1)$ are the duty cycle for the step-up mode (the step-down mode); $r_{ESR} = 0.05\ \Omega$ is the equivalent resistance of the capacitors C_1, C_2, and C_3. In addition, $i_{Ci\_SI/SII}$ ($i \in \{1,2,3\}$) indicates the averaged current passes capacitor at State I or State II in step-up mode or step-down mode, respectively.

Remark: Since u_{low} and u_{high} are the input voltage of the converter operating in the step-up mode and the step-down mode, respectively, it is reasonable to assume $u_{low} = U_{low}$ in (1) and $u_{high} = U_{high}$ in (2), where U_{low} and U_{high} are constant.

IV. Characteristics of the Proposed Converter

A. Zero Ripple Current on LVS

By using Fig. 2 and the Kirchhoff's Voltage Law (KVL), the following relationship can be obtained:

$$u_L = U_{low} + u_{C2} + u_{C3} - U_{high} \tag{3}$$

where u_L, u_{C2}, and u_{C3} represent the dynamic voltages of L, C_2, and C_3, respectively.

Averaging (3) over one switching period yields

$$U_L = U_{low} + U_{C2} + U_{C3} - U_{high} \tag{4}$$

where U_L, U_{C2}, and U_{C3} are the averaging voltages of L, C_2, and C_3 over one switching period, respectively.

According to the voltage–second balance principle, it can be obtained that

$$U_L = 0. \tag{5}$$

Substituting (5) into (4) results in

$$U_{high} = U_{low} + U_{C2} + U_{C3}. \tag{6}$$

Based on the Assumption 2, the voltage ripples on C_2 and C_3 can be ignored. Hence, $u_{C2} \approx U_{C2}$ and $u_{C3} \approx U_{C3}$ are achieved. Substituting $u_{C2} \approx U_{C2}$, $u_{C3} \approx U_{C3}$ and (6) into (3) yields

$$u_L \approx 0. \tag{7}$$

Therefore, the current ripple of i_L can be derived as follows:

$$\frac{di_L}{dt} = \frac{u_L}{L} \approx 0. \tag{8}$$

Since $i_{low} = i_L$, the zero current ripple on the LVS can be realized and the value of L is not related to the current ripple

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = dU_{low} + (1-d_{boost})(u_{high} - u_{C1} - u_{C2} - i_{L1}r_{ESR} - i_{C2\_SII}r_{ESR}) \\ L_2 \frac{di_{L2}}{dt} = dU_{low} + (1-d_{boost})(-u_{C3} - i_{C3\_SII}r_{ESR}) \\ C_1 \frac{du_{C1}}{dt} = di_{C1\_SI} + (1-d_{boost})\, i_{L1} \\ C_2 \frac{du_{C2}}{dt} = di_{C2\_SI} + (1-d_{boost})\, i_{C2\_SII} \\ C_3 \frac{du_{C3}}{dt} = d(i_{C1\_SI} + i_{C2\_SI}) + (1-d)(-i_{L1} + i_{L2} + i_{C2\_SII}) \\ C_{high} \frac{du_{high}}{dt} = -\frac{u_{high}}{R} - d_{boost}(i_{C1\_S1} + i_{C2S1}) + (1-d_{boost})\, i_{C2\_SII} \end{cases}$$

$$\text{where} \begin{cases} i_{C1\_SI} = (u_{high} + u_{C2} - 2u_{C1} - u_{C3} - U_{low})/3r_{ESR} \\ i_{C2\_SI} = (u_{high} + u_{C1} - 2u_{C2} - u_{C3} - U_{low})/3r_{ESR} \\ i_{C2\_SII} = [(i_{L1} - i_{L2})\, r_{ESR} + u_{high} - u_{C2} - u_{C3} - U_{low}]/2r_{ESR} \\ i_{C3\_SII} = [(i_{L2} - i_{L1})\, r_{ESR} + u_{high} - u_{C2} - u_{C3} - U_{low}]/2r_{ESR} \end{cases} \tag{1}$$

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = d_{buck}(u_{C1} + u_{C2} - U_{high} - i_{L1}r_{ESR} + i_{C2\_SI}r_{ESR}) - (1-d_{buck})\, u_{low} \\ L_2 \frac{di_{L2}}{dt} = d_{buck}(u_{C3} + i_{C3\_SI}r_{ESR}) - (1-d_{buck})\, u_{low} \\ C_1 \frac{du_{C1}}{dt} = -d_{buck} i_{L1} + (1-d)\, i_{C1\_SII} \\ C_2 \frac{du_{C2}}{dt} = d_{buck} i_{C2\_SI} + (1-d)\, i_{C2\_SII} \\ C_3 \frac{du_{C3}}{dt} = d_{buck}(i_{L1} - i_{L2} + i_{C2\_SI}) + (1-d_{buck})(i_{C1\_SII} + i_{C2\_SII}) \\ C_{high} \frac{du_{high}}{dt} = -\frac{u_{high}}{R} + i_{L1} + di_{C2\_SI} + (1-d_{buck})(i_{L2} + i_{C1\_SII} + i_{C2\_SII}) \end{cases}$$

$$\text{where} \begin{cases} i_{C2\_SI} = [(i_{L2} - i_{L1})\, r_{ESR} + U_{high} - u_{C2} - u_{C3} - u_{low}]/2r_{ESR} \\ i_{C3\_SI} = [(i_{L1} - i_{L2})\, r_{ESR} + U_{high} - u_{C2} - u_{C3} - u_{low}]/2r_{ESR} \\ i_{C1\_SII} = (U_{high} + u_{C2} - 2u_{C1} - u_{C3} - u_{low})/3r_{ESR} \\ i_{C2\_SII} = (U_{high} + u_{C1} - 2u_{C2} - u_{C3} - u_{low})/3r_{ESR} \end{cases} \tag{2}$$

of $i_{\rm low}$. Consequently, a small L can be selected to achieve high power density and low cost. It is also worth mentioning that, the merit of zero current ripple on LVS will not be deteriorated by neither the converter duty-cycle changing nor circuit parameter uncertainties.

B. Analysis of Voltage Conversion Ratio

1) Step-Up Mode: According to Fig. 4 and (6), following equations can be obtained from the voltage-second balance principle on L_1 and L_2 as:

$$\begin{cases} U_{\rm low} \times d_{\rm boost} + (U_{\rm low} - U_{\rm C1} + U_{\rm C3}) \times (1 - d_{\rm boost}) = 0 \\ U_{\rm low} \times d_{\rm boost} - U_{\rm C3} \times (1 - d_{\rm boost}) = 0. \end{cases} \tag{9}$$

As shown in Fig. 4(a), the turn-ON of Q_2 and Q_4 results in the paralleled C_1 and C_2, and, hence

$$U_{\rm C1} = U_{\rm C2}. \tag{10}$$

Considering (6), (9), and (10), following relationships can be obtained:

$$\begin{cases} U_{\rm C1} = U_{\rm C2} = \frac{1+d_{\rm boost}}{1-d_{\rm boost}} U_{\rm low} \\ U_{\rm C3} = \frac{d_{\rm boost}}{1-d_{\rm boost}} U_{\rm low} \\ U_{\rm high} = \frac{2+d_{\rm boost}}{1-d_{\rm boost}} U_{\rm low}. \end{cases} \tag{11}$$

Based on (11), the step-up mode voltage conversion ratio $M_{\rm boost}$ can be derived as

$$M_{\rm boost} = \frac{U_{\rm high}}{U_{\rm low}} = \frac{2 + d_{\rm boost}}{1 - d_{\rm boost}}. \tag{12}$$

2) Step-Down Mode: Similarly, using Fig. 7 and the voltage–second balance principle yields

$$\begin{cases} (U_{\rm low} - U_{\rm C1} + U_{\rm C3}) \times d_{\rm buck} + U_{\rm low} \times (1 - d_{\rm buck}) = 0 \\ -U_{\rm C3} \times d_{\rm buck} + U_{\rm low} \times (1 - d_{\rm buck}) = 0 \\ U_{\rm C1} = U_{\rm C2} \\ U_{\rm low} = U_{\rm high} - U_{\rm C2} - U_{\rm C3}. \end{cases} \tag{13}$$

Therefore, the voltage across each capacitor can be calculated as

$$\begin{cases} U_{\rm C1} = U_{\rm C2} = \frac{2-d_{\rm buck}}{3-d_{\rm buck}} U_{\rm high} \\ U_{\rm C3} = \frac{1-d_{\rm buck}}{3-d_{\rm buck}} U_{\rm high} \\ U_{\rm low} = \frac{d_{\rm buck}}{3-d_{\rm buck}} U_{\rm high}. \end{cases} \tag{14}$$

According to (14), the step-down mode voltage conversion ratio $M_{\rm buck}$ can be easily obtained as

$$M_{\rm buck} = \frac{U_{\rm low}}{U_{\rm high}} = \frac{d_{\rm buck}}{3 - d_{\rm buck}}. \tag{15}$$

Equations (12) and (15) imply that the available voltage conversion ratio of the proposed converter is much wider than the traditional bidirectional two-level buck-boost converter. Specifically, in the step-up mode, it is within the range of 2.75∼14 for $0.2 < d_{\rm boost} < 0.8$, and, in the step-down mode, it is in the range of 0.07∼0.36 for $0.2 < d_{\rm buck} < 0.8$.

C. Analysis of Voltage Stresses on Power Switches

1) Step-Up Mode: By applying the KVL on the circuit given in Fig. 4, the voltage stresses of all power switches in step-up mode can be derived as follows:

$$\begin{cases} U_{\rm Q1} = U_{\rm Q4} = \frac{U_{\rm C2}+U_{\rm low}}{2} = \frac{1}{2+d_{\rm boost}} U_{\rm high} \\ U_{\rm Q2} = U_{\rm Q5} = U_{\rm C3} + U_{\rm low} = \frac{1}{2+d_{\rm boost}} U_{\rm high} \\ U_{\rm Q3} = U_{\rm C1} + U_{\rm low} = \frac{2}{2+d_{\rm boost}} U_{\rm high}. \end{cases} \tag{16}$$

2) Step-Down Mode: Similarly, according to Fig. 7, the voltage stresses of all power switches in step-down mode can be obtained as follows:

$$\begin{cases} U_{\rm Q1} = U_{\rm Q4} = \frac{U_{\rm C2}+U_{\rm low}}{2} = \frac{1}{3-d_{\rm buck}} U_{\rm high} \\ U_{\rm Q2} = U_{\rm Q5} = U_{\rm C3} + U_{\rm low} = \frac{1}{3-d_{\rm buck}} U_{\rm high} \\ U_{\rm Q3} = U_{\rm C1} + U_{\rm low} = \frac{2}{3-d_{\rm buck}} U_{\rm high}. \end{cases} \tag{17}$$

It can be seen from (16) and (17) that the voltage stresses of all power switches are lower than $U_{\rm high}$. In detail, the voltage stresses of most power switches, i.e., Q_1, Q_2, Q_4, and Q_5, are less than $U_{\rm high}$/2. Hence, the power switches with low voltage rating and small ON-state resistance can be selected to achieve a higher conversion efficiency.

D. Analysis of Current Stresses on Power Switches

1) Step-Up Mode: According to Fig. 4, the currents pass C_1, C_2, C_3, and $C_{\rm high}$ in each operation state are derived as

$$\begin{cases} i_{\rm C1} = \begin{cases} I_{\rm C1\_SI} \\ I_{\rm C1\_SII} = I_{\rm L1} \end{cases} \\ i_{\rm C2} = \begin{cases} I_{\rm C2\_SI} = I_{\rm L2} - I_{\rm C1\_SI} - I_{\rm L} + I_{\rm L1} \\ I_{\rm C2\_SII} = I_{\rm L1} - I_{\rm L} \end{cases} \\ i_{\rm C3} = \begin{cases} I_{\rm C3\_SI} = I_{\rm L2} + I_{\rm L1} - I_{\rm L} \\ I_{\rm C3\_SII} = I_{\rm L2} - I_{\rm L} \end{cases} \\ i_{\rm Chigh} = \begin{cases} I_{\rm Chigh\_SI} = I_{\rm L} - I_{\rm L2} - I_{\rm L1} - I_{\rm high} \\ I_{\rm Chigh\_SII} = I_{\rm L} - I_{\rm L1} - I_{\rm high}. \end{cases} \end{cases} \tag{18}$$

where $I_{\rm L1}$ and $I_{\rm L2}$ are the averaged value of $i_{\rm L1}$ and $i_{\rm L2}$, respectively; $I_{\rm Ci\_SI}(i = 1, 2, 3,$ and high) indicates the averaged value of $i_{\rm Ci}$ on state I, while $I_{\rm Ci\_SII}(i = 1, 2, 3,$ and high) implies the averaged value of $i_{\rm Ci}$ on state II.

By using the ampere-second balance principle on the capacitors C_1, C_2, C_3, and $C_{\rm high}$, i.e.

$$\langle i_{\rm Ci} \rangle_{\rm ave} = [I_{\rm Ci\_SI} d_{\rm boost} T_{\rm s} + I_{\rm Ci\_SII}(1 - d_{\rm boost}) T_{\rm s}]/T_{\rm s} = 0$$

the averaged current of the inductors can be derived as

$$\begin{cases} I_{\rm L} = I_{\rm low} = \frac{2+d_{\rm boost}}{1-d_{\rm boost}} I_{\rm high} \\ I_{\rm L1} = \frac{1}{2+d_{\rm boost}} I_{\rm L} = \frac{1}{1-d_{\rm boost}} I_{\rm high} \\ I_{\rm L2} = 2I_{\rm L1} = \frac{2}{1-d_{\rm boost}} I_{\rm high} \end{cases} \tag{19}$$

Substituting (19) into (18) yields

$$\begin{cases} i_{\mathrm{C1}} = \begin{cases} I_{\mathrm{C1\_SI}} = \frac{-1}{d_{\mathrm{boost}}} I_{\mathrm{high}} \\ i_{\mathrm{C1\_SII}} = \frac{1}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \end{cases} \\ i_{\mathrm{C2}} = \begin{cases} i_{\mathrm{C2\_SI}} = \frac{1+d_{\mathrm{boost}}}{d_{\mathrm{boost}}} I_{\mathrm{high}} \\ i_{\mathrm{C2\_SII}} = \frac{-1-d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \end{cases} \\ i_{\mathrm{C3}} = \begin{cases} i_{\mathrm{C3\_SI}} = I_{\mathrm{high}} \\ i_{\mathrm{C3\_SII}} = \frac{-d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \end{cases} \\ i_{\mathrm{Chigh}} = \begin{cases} i_{\mathrm{Chigh\_SI}} = -2I_{\mathrm{high}} \\ i_{\mathrm{Chigh\_SII}} = \frac{2d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \end{cases} \end{cases} \tag{20}$$

Next, the current stresses of the power switches in the step-up mode will be derived. It is worth noting that, since each power switch is only turned ON in one operation state, in this article, the current stress of a power switch is defined as the averaged current passes the power switch when it is turned ON. Similar definition of the current stress of the power switch has also been used in several previous work [16], [27] and [28]. Using the Kirchhoff's current law (KCL) to analyze the topology given in Fig. 4, the current stresses of the power switches can be obtained as

$$\begin{cases} I_{\mathrm{Q1}} = I_{\mathrm{L1}} = \frac{1}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \\ I_{\mathrm{Q2}} = I_{\mathrm{L2}} - I_{\mathrm{C1\_SI}} = \frac{1+d_{\mathrm{boost}}}{(1-d_{\mathrm{boost}})d_{\mathrm{boost}}} I_{\mathrm{high}} \\ I_{\mathrm{Q3}} = I_{\mathrm{L1}} = \frac{1}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \\ I_{\mathrm{Q4}} = -I_{\mathrm{C1\_SI}} = \frac{1}{d_{\mathrm{boost}}} I_{\mathrm{high}} \\ I_{\mathrm{Q5}} = I_{\mathrm{L2}} - I_{\mathrm{L1}} = \frac{1}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} \end{cases} \tag{21}$$

2) Step-Down Mode: Similarly, using the same procedure to derive the current stress of the power switches based on Fig. 7, the averaged inductor currents and the corresponding current stresses of power switches in the step-down mode can, respectively, be given as follows:

$$\begin{cases} I_{\mathrm{L}} = I_{\mathrm{low}} \\ I_{\mathrm{L1}} = \frac{1}{3-d_{\mathrm{buck}}} I_{\mathrm{low}} \\ I_{\mathrm{L2}} = \frac{2}{3-d_{\mathrm{buck}}} I_{\mathrm{low}} \end{cases} \tag{22}$$

$$\begin{cases} I_{\mathrm{Q1}} = I_{\mathrm{L1}} = \frac{1}{d_{\mathrm{buck}}} I_{\mathrm{high}} \\ I_{\mathrm{Q2}} = I_{\mathrm{L2}} + I_{\mathrm{C1\_SII}} = \frac{(2-d_{\mathrm{buck}})}{(1-d_{\mathrm{buck}})d_{\mathrm{buck}}} I_{\mathrm{high}} \\ I_{\mathrm{Q3}} = I_{\mathrm{L1}} = \frac{1}{d_{\mathrm{buck}}} I_{\mathrm{high}} \\ I_{\mathrm{Q4}} = I_{\mathrm{C1\_SII}} = \frac{1}{(1-d_{\mathrm{buck}})} I_{\mathrm{high}} \\ I_{\mathrm{Q5}} = I_{\mathrm{L2}} - I_{\mathrm{L1}} = \frac{1}{d_{\mathrm{buck}}} I_{\mathrm{high}} \end{cases} \tag{23}$$

E. Comparisons Study

In order to show the merits of the proposed converter, a comparison study involves the proposed BDC and other existing BDCs is carried out in this section. As shown in Table I, although the basic bidirectional A-SL based converter employs fewest components to achieve high voltage conversion ratio, one of the power switch withstands high voltage stress (greater than U_{high}). In addition, the existence of HF PWM potential difference between the grounds of converter's LVS and HVS may cause EMI issue, and the large LVS current ripple is another drawback. To further improve the voltage conversion ratio, the converter based on A-SL and switched-capacitor structure have been presented in [16]. However, similar with the aforementioned A-SL based converter, this converter also suffers from the issues of large LVS current ripple and HF PWM potential difference. Besides, the low components voltage stress merit is only available within limited converter operation conditions. Specifically, once $d_{\mathrm{boost}} < 1/3$ ($d_{\mathrm{buck}} > 2/3$), the voltage stresses of two power switches are higher than U_{high}. Although the converter reported in [17] exhibits the merits of higher conversion ratio and reduced voltage stresses, large current ripple on LVS and the existence of HF PWM potential difference between converter grounds significantly limit its practical application. For the sake of achieving high voltage conversion ratio, low voltage stresses and constant potential difference between the grounds of the BDC's LVS and HVS simultaneously, a hybrid switched-capacitor/switched-quasi-Z-source BDC has been proposed in [27]. However, the small LVS current ripple only can be obtained with a quite large inductor, which sacrifices the power density and converter efficiency. The converter has been presented in [28] adopts an interleaved technique to smooth the current ripple on its LVS. However, the low LVS current ripple is sensitive to the number of interleave phases and the duty-cycle of the converter. In addition, its achievable voltage conversion ratio is narrower than that of the converters reported in [16], [17], and [27]. A hybrid BDC with the quadratic gain has been proposed in [29]. Although the reported BDC possesses a high conversion ratio and a common ground, high voltage stresses on the power switches and the large current ripple on the LVS make it unattractive in terms of the BESS application. In [30], a three-level BDC has been proposed. The features of low LVS current ripple and the common ground make it attractive. However, the voltage gain of the three-level BDC is not desired. In addition, the unbalance charging/discharging issue on the fly capacitor complicates the controller design.

According to the analysis in previous sections, compared with the aforementioned BDCs, the proposed converter possesses the lowest LVS current ripple (almost zero) with relatively low power switch stresses. In addition, it also avoids the HF PWM potential difference issue existing in the bidirectional A-SL based converter and the converters reported [16], [17].

Next, to clearly show the voltage conversion ratios of each converter, the phase diagram of voltage conversion ratio versus duty-cycle is shown in Fig. 9. It can be seen that, although the proposed BDC achieves aforementioned merits, its voltage conversion ratio is not compromised. Specifically, it shows the same voltage conversion ratio as the state-of-the-art converter reported in [27].

The total energy stored in capacitors (E_{C}) and that stored in inductors (E_{L}) are commonly used as a measure of weight and cost on passive components [31], and the total active switch stress (S_{Q}) is widely used to define the economic costs/losses of power switches [16]. Hence, to fairly compare the cost/size of different solutions, comparison studies involve the energy on the capacitors/inductors and the active switch stress on the power switches of the BDC topologies given in Table I are carried out.

TABLE I
COMPARISON WITH OTHER BIDIRECTIONAL CONVERTERS

Converter	Components count	Voltage conversion ratio		V_{Grounds}	Voltage stress on power switches ($M = U_{\mathrm{high}}/U_{\mathrm{low}}$)	Current ripple on LVS
		Step-up mode	Step-down mode			
Bidirectional A-SL based converter	2 inductors 2 capacitors 3 power switches	$\frac{1+d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{2-d_{\mathrm{buck}}}$	HF PWM voltage	$\frac{(1+M)U_{\mathrm{high}}}{2M}$ & $\frac{(1+M)U_{\mathrm{high}}}{M}$	Large
Converter in [16]	3 inductors 4 capacitors 4 power switches	$\frac{1+3d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{4-3d_{\mathrm{buck}}}$	HF PWM voltage	$\frac{(3+M)U_{\mathrm{high}}}{4M}$ & $\frac{(3+M)U_{\mathrm{high}}}{2M}$	Large
Converter in [17]	2 inductors 4 capacitors 5 power switches	$\frac{3+d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{4-d_{\mathrm{buck}}}$	HF PWM voltage	$\frac{(1+M)U_{\mathrm{high}}}{4M}$ & $\frac{(1+M)U_{\mathrm{high}}}{2M}$	Large
Converter in [27]	2 inductors 6 capacitors 5 power switches	$\frac{2+d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{3-d_{\mathrm{buck}}}$	Constant voltage	$\frac{(1+M)U_{\mathrm{high}}}{3M}$	Medium
Converter in [28]	2 inductors 4 capacitors 5 power switches	$\frac{2}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{2}$	Constant voltage	$\frac{U_{\mathrm{high}}}{2}$	Low
Converter in [29]	2 inductors 3 capacitors 4 power switches	$\frac{1}{(1-d_{\mathrm{boost}})^2}$	d_{buck}^2	$0V$	U_{high} & $\frac{U_{\mathrm{high}}}{\sqrt{M}}$ & $\frac{(\sqrt{M}+1)U_{\mathrm{high}}}{\sqrt{M}}$	Large
Converter in [30]	1 inductors 3 capacitors 4 power switches	$\frac{1}{1-d_{\mathrm{boost}}}$	d_{buck}	$0V$	$\frac{U_{\mathrm{high}}}{2}$	Low
Proposed converter	3 inductors 5 capacitors 5 power switches	$\frac{2+d_{\mathrm{boost}}}{1-d_{\mathrm{boost}}}$	$\frac{d_{\mathrm{buck}}}{3-d_{\mathrm{buck}}}$	Constant voltage	$\frac{(1+M)U_{\mathrm{high}}}{3M}$ & $\frac{2(1+M)U_{\mathrm{high}}}{3M}$	Zero

Based on [32], the expression of E_{C} for a converter can be obtained as

$$E_{\mathrm{C}} = \sum \frac{C_{\mathrm{i}} U_{\mathrm{Ci}}^2}{2} = \sum \frac{U_{\mathrm{Ci}}}{2} \left(\frac{dT_{\mathrm{s}} I_{\mathrm{Ci}}}{r_{\mathrm{uCi}}} \right) \tag{24}$$

where d is the duty-cycle of the converter; T_{s} indicates the switching period; I_{Ci} is the current passes the capacitor C_{i} during dT_s, and U_{Ci} represent the voltage across capacitor C_{i}; and r_{uCi} denotes the voltage ripple rates of U_{Ci}.

Similarly, the inductor energy E_{L} can be expressed as

$$E_{\mathrm{L}} = \sum \frac{L_{\mathrm{i}} I_{\mathrm{Li}}^2}{2} = \sum \frac{I_{\mathrm{Li}}}{2} \left(\frac{dT_{\mathrm{s}} U_{\mathrm{Li}}}{r_{\mathrm{iLi}}} \right) \tag{25}$$

where U_{Li} stands for the voltage across the L_{i} during dT_s, I_{Li} implies the inductor current of L_{i}, and the r_{iLi} is the current ripple rate of I_{Li}.

In addition, the total active switch stress of the power switches S_{Q} can be expressed as follows:

$$S_{\mathrm{Q}} = \sum U_{\mathrm{Qi}} I_{\mathrm{Qi}} \tag{26}$$

where U_{Qi} and I_{Qi} represent, respectively, the voltage stress and current stress of the power switch Q_{i}.

To fairly obtain the comparison results, the calculations of E_{C}, E_{L}, and S_{Q} for different topologies are carried out using the same system operation condition. Specifically, all the converters operate with the same power level ($P_{\mathrm{n}} = 1$ kW), the same switching frequency ($f_{\mathrm{s}} = 50$ kHz), the same voltage conversion ratio ($M = U_{\mathrm{high}}/U_{\mathrm{low}}$), the same permit voltage ripple rates r_{uCi} (10% for capacitor on LVS or HVS, and 20% for the middle capacitors), and the same permit current ripple rate r_{iLi} (25% for the inductor on LVS or HVS, and 100% for the middle inductors).

Using (24)–(26) and the above assumption, the corresponding E_{C}, E_{L}, and S_{Q} of different converter topologies listed in Table I are calculated. To clearly show the comparison results, E_{C} and E_{L} of each converter are normalized by dividing those of the proposed converter, i.e., $E_{\mathrm{C}}^* = E_{\mathrm{C}}/E_{\mathrm{C\_proposed}}$ and $E_{\mathrm{L}}^* = E_{\mathrm{L}}/E_{\mathrm{L\_proposed}}$. The plots of E_{C}^* and E_{L}^* of each converter against the conversion rate M are shown in Figs. 10 and 11, respectively. In addition, the phase-portrait of S_{Q} against M is shown in Fig. 12.

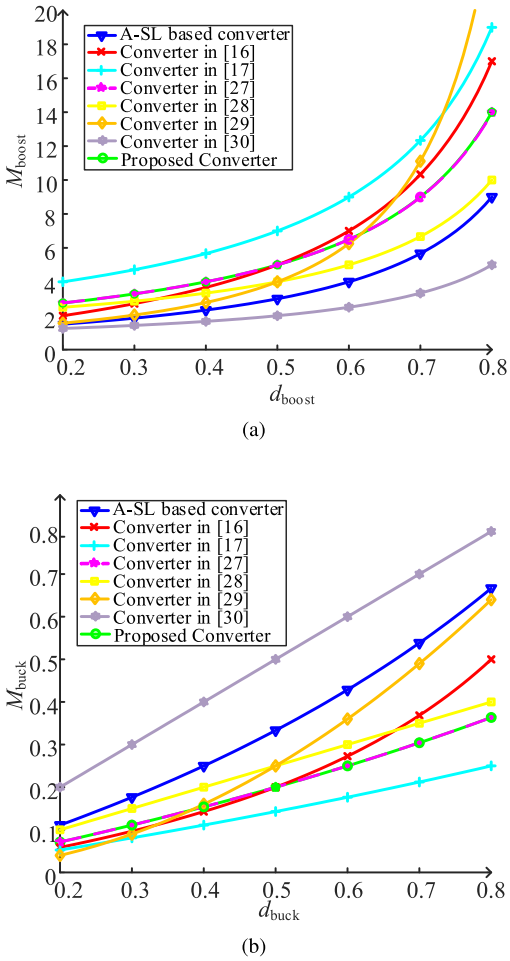

Fig. 9. Comparisons of the voltage conversion ratio against duty-cycle. (a) Step-up mode. (b) Step-down mode.

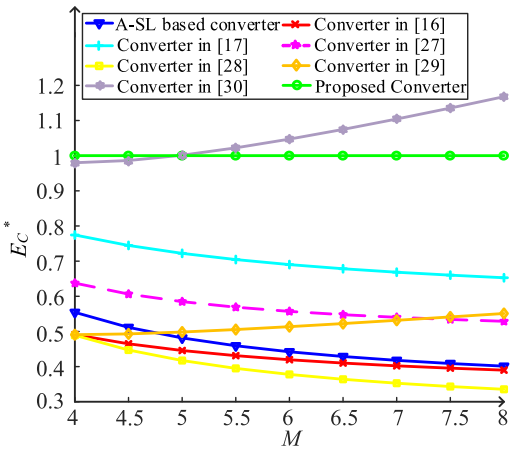

Fig. 10. Normalized total energy stored in capacitors against different M.

Considering all above analyzed, regarding to the proposed BDC, the feature of small inductor size compensates the drawback of large capacitor size, which let the proposed BDC hold a good performance/size compared to the other BDCs listed in Table I. In addition, the proposed BDC also show low total active

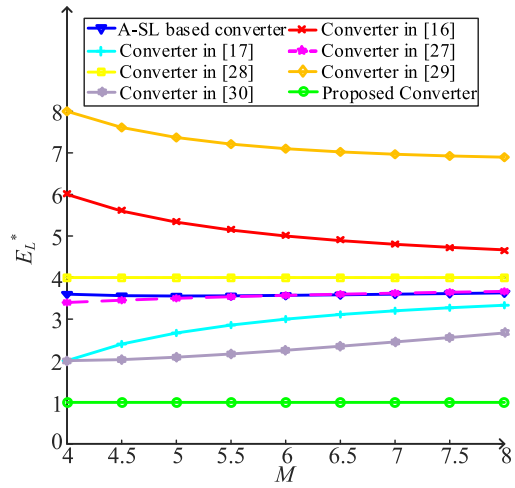

Fig. 11. Normalized total energy stored in inductors against M.

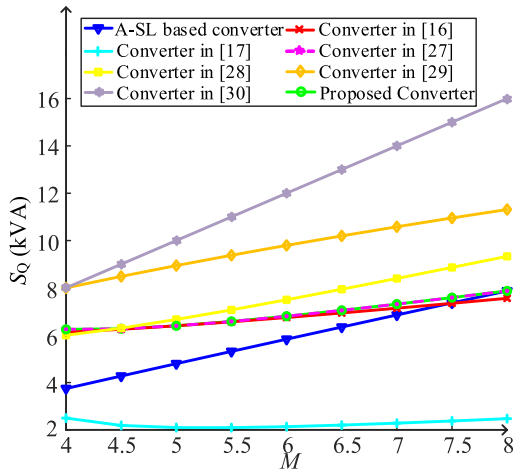

Fig. 12. Total active switch stress of power switches (S_Q) against M.

power stress among the BDCs listed in Table I, which makes it more attractive.

Therefore, the features of zero LVS current ripple, low power switch voltage stresses, constant potential difference between the grounds of LVS and HVS and good voltage conversion ratio make the proposed BDC become a promising solution to interface the BESS and dc bus.

F. Efficiency Analysis

The total power loss P_{loss} of the proposed converter can be expressed as

$$P_{\text{loss}} = P_{\text{QC}} + P_{\text{QS}} + P_{\text{Cu}} + P_{\text{Fe}} + P_{\text{C}} \tag{27}$$

where P_{QC} strands for the conduction losses of power switches; P_{QS} represents the switching losses of power switches; P_{Cu} and P_{Fe} imply the copper losses and core losses of inductors, respectively; the capacitor losses are represented by P_{C}.

The conduction loss P_{QC} and the switching loss P_{QS} are caused by the operation of power switches. The expressions of

them are listed in (28) and (29), respectively.

$$P_{\mathrm{QC}} = \sum_{i=1}^{5} I^2{}_{\mathrm{QiRMS}} R_{\mathrm{Qi}} \tag{28}$$

$$P_{\mathrm{QS}} = \begin{cases} \frac{1}{2}\sum_{i=1}^{2}\left[V_{\mathrm{Qi}} I_{\mathrm{Qi}} f_{\mathrm{s}}\left(t_{\mathrm{rise}} + t_{\mathrm{fall}}\right)\right], \text{step-up mode} \\ \frac{1}{2}\sum_{i=3}^{5}\left[V_{\mathrm{Qi}} I_{\mathrm{Qi}} f_{\mathrm{s}}\left(t_{\mathrm{rise}} + t_{\mathrm{fall}}\right)\right], \text{step-down mode} \end{cases} \tag{29}$$

where I_{QiRMS} represents the rms current of the power switch Q_{i}; V_{Qi} denotes the reversed voltage on Q_{i} when it is fully turned OFF; I_{Qi} is the current flows through Q_{i} when the power switch is fully turned ON; t_{rise} and t_{fall}, respectively, indicate the rise time and fall time of Q_{i}, and f_{s} implies the switching frequency.

It is worth mentioning that, due to the employment of synchronous rectification on slave power switches, Q_3–Q_5 are soft switching in the step-up mode while Q_1–Q_2 are soft switching in the step-down mode. Considering the switching losses of the soft switched power switches are negligible, only the switching losses of their hard switching counterparts are calculated.

Next, the inductors (L, L_1, and L_2) related power losses are discussed. The copper losses P_{Cu} are mainly generated by the ESRs R_{Li} of the inductors, and the core losses P_{Fe} are the magnetic losses caused by the inductor cores. The expressions of both losses are given as

$$\begin{aligned} P_{\mathrm{Cu}} &= I^2_{\mathrm{LRMS}} \times R_{\mathrm{L}} \\ &\quad + I^2_{\mathrm{L1RMS}} \times R_{\mathrm{L1}} + I^2_{\mathrm{L2RMS}} \times R_{\mathrm{L2}} \end{aligned} \tag{30}$$

$$\begin{aligned} P_{\mathrm{Fe}} &= l_{\mathrm{L}} A_{\mathrm{L}} (a B^b_{\mathrm{acL}} f^{\mathrm{c}}_{\mathrm{s}}) \\ &\quad + l_{\mathrm{L1}} A_{\mathrm{L1}} (a B^b_{\mathrm{acL1}} f^{\mathrm{c}}_{\mathrm{s}}) + l_{\mathrm{L2}} A_{\mathrm{L2}} (a B^b_{\mathrm{acL2}} f^{\mathrm{c}}_{\mathrm{s}}) \end{aligned} \tag{31}$$

where $R_{\mathrm{i}} (i = L, L_1 \text{ and } L_2)$ represents the ESR of the inductor L_{i}; $I_{\mathrm{iRMS}} = \sqrt{I_{\mathrm{i}}^2 + \frac{\Delta I_{\mathrm{i}}^2}{12}}$ is the rms current of the inductor L_{i}; $B_{\mathrm{aci}} = \frac{L \times \Delta I_{\mathrm{i}}}{2 N_{\mathrm{i}} A_{\mathrm{i}}}$ denotes the ac magnetic flux density of the inductor iron core, and ΔI_{i} represents the current ripple. N_{i} indicates the number of the turns; l_{i} and A_{i} stand for the lengths of the magnetic flux path and the cross sectional areas of the inductor iron core, respectively. In addition, a, b, and c are the coefficients determined by the core material.

The capacitor losses P_{C} are caused by ESRs of capacitors. It can be calculated by

$$P_{\mathrm{C}} = \sum I^2_{\mathrm{CiRMS}} \times R_{\mathrm{Ci}} \tag{32}$$

where R_{Ci} indicates the ESR of the capacitor C_{i} and I_{CiRMS} is the rms value of the current passes the capacitor.

G. Parameters Design of the Converter

1) Design of Inductors: The parameter design of inductors is determined by the rated inductor currents I_{L1} and I_{L2}, the rated HVS voltage U_{high}, the duty-cycle d_{boost} or d_{buck}, the switching frequency f_{s}, and allowable inductor current ripple rates r_{iL1} and r_{iL2}.

Using the ampere–second balance principle on capacitors yields

$$\begin{cases} I_{\mathrm{L1}} = \frac{1}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} = \frac{1}{3-d_{\mathrm{buck}}} I_{\mathrm{low}} \\ I_{\mathrm{L2}} = \frac{2}{1-d_{\mathrm{boost}}} I_{\mathrm{high}} = \frac{2}{3-d_{\mathrm{buck}}} I_{\mathrm{low}}. \end{cases} \tag{33}$$

Therefore, the minimum allowable inductances for L_1 and L_2 in both step-up and step-down modes can be derived as

$$\begin{cases} L_1 \geq \frac{(1-d_{\mathrm{boost}})^2 d_{\mathrm{boost}} U_{\mathrm{high}}}{(2+d_{\mathrm{boost}}) I_{\mathrm{high}} r_{\mathrm{L1}} f_{\mathrm{s}}} = \frac{d_{\mathrm{buck}}{}^2 (1-d_{\mathrm{buck}}) U_{\mathrm{high}}}{(3-d_{\mathrm{buck}}) I_{\mathrm{high}} r_{\mathrm{L1}} f_{\mathrm{s}}} \\ L_2 \geq \frac{(1-d_{\mathrm{boost}})^2 d_{\mathrm{boost}} U_{\mathrm{high}}}{2(2+d_{\mathrm{boost}}) I_{\mathrm{high}} r_{\mathrm{L2}} f_{\mathrm{s}}} = \frac{d_{\mathrm{buck}}{}^2 (1-d_{\mathrm{buck}}) U_{\mathrm{high}}}{2(3-d_{\mathrm{buck}}) I_{\mathrm{high}} r_{\mathrm{L1}} f_{\mathrm{s}}} \end{cases} \tag{34}$$

It is worth noting that the maximums of r_{iL1} and r_{iL2} are 200%, which ensure the BDC operates in CCM.

According to the assumption proposed in the Section III and (6)–(7), ideally, the value of u_{L} equals zero. Thus, exact zero current ripple on L can be achieved, which implies that the inductance of L can be negligible small. However, in practice, the voltage ripples across the capacitors cannot be fully neglected. Consequently, the current ripple on L, i.e., Δi_{L}, is tightly related to the inductance of L. To achieve a desired Δi_{L}, the design criterion of L is given as follows.

According to [24], the flux linage of L can be expressed as

$$\lambda = \frac{\Delta u_{\mathrm{L}}}{2} \times \frac{T_{\mathrm{s}}}{2} = 2L\Delta i_{\mathrm{L}} \tag{35}$$

where Δu_{L} represents the ripples of u_{L}.

Rearranging (35), the inductance of L can be expressed as

$$L = \frac{\Delta u_{\mathrm{L}} T_{\mathrm{s}}}{8 \Delta i_{\mathrm{L}}}. \tag{36}$$

Then, considering the current ripple rate of L as r_{iL} ($r_{\mathrm{iL}} < 2\%$ to achieve zero current ripple) and the averaged state–state current of L as I_{L}, (36) can be rewritten as

$$L = \frac{\Delta u_{\mathrm{L}} T_{\mathrm{s}}}{8 r_{\mathrm{iL}} I_{\mathrm{L}}}. \tag{37}$$

2) Design of Capacitors: The key specifications determine the capacitors parameter design are the rated HVS current I_{high}, the capacitor rated voltages, the duty-cycle d_{boost} or d_{buck}, switching frequency f_{s}, and the permitted capacitor voltage ripple rates r_{uC1}, r_{uC2}, r_{uC3}, r_{uChigh}, and r_{uClow}.

By using (11) and (14), the minimum available capacitances for C_1, C_2, C_3, C_{high}, and C_{low} in CCM can be easily derived as

$$\begin{cases} C_1 \geq \frac{(2+d_{\mathrm{boost}}) I_{\mathrm{high}}}{(1+d_{\mathrm{boost}}) f_{\mathrm{s}} r_{\mathrm{uC1}} U_{\mathrm{high}}} = \frac{(3-d_{\mathrm{buck}}) I_{\mathrm{high}}}{(2-d_{\mathrm{buck}}) f_{\mathrm{s}} r_{\mathrm{uC1}} U_{\mathrm{high}}} \\ C_2 \geq \frac{(2+d_{\mathrm{boost}}) I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uC2}} U_{\mathrm{high}}} = \frac{(3-d_{\mathrm{buck}}) I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uC2}} U_{\mathrm{high}}} \\ C_3 \geq \frac{(2+d_{\mathrm{boost}}) I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uC3}} U_{\mathrm{high}}} = \frac{(3-d_{\mathrm{buck}}) I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uC3}} U_{\mathrm{high}}} \\ C_{\mathrm{high}} \geq \frac{2 d_{\mathrm{boost}} I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uChigh}} U_{\mathrm{high}}} = \frac{2(1-d_{\mathrm{buck}}) I_{\mathrm{high}}}{f_{\mathrm{s}} r_{\mathrm{uChigh}} U_{\mathrm{high}}} \\ C_{\mathrm{low}} \geq \frac{r_{\mathrm{iL}} I_L}{8 r_{\mathrm{uClow}} U_{\mathrm{low}} f_{\mathrm{s}}} = \frac{r_{\mathrm{iL}} P_{\mathrm{n}}}{8 r_{\mathrm{uClow}} U_{\mathrm{low}}{}^2 f_{\mathrm{s}}}. \end{cases} \tag{38}$$

According to the engineering rule of thumb, the voltage ripple rates r_{uC1}, r_{uC2}, r_{uC3}, r_{uChigh}, and r_{uClow} should be within $\pm 0.5\%$ of their rated voltages.

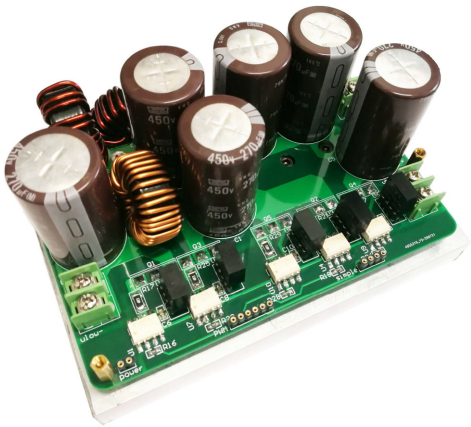

Fig. 13. Experimental prototype of the proposed BDC.

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	Values
Rated power P_n	1000W
Filtering capacitor $C_{\rm low}$	220μF
Filtering capacitor $C_{\rm high}$	440μF
Switched capacitors C_1-C_3	220μF
Inductor L	10μH
Inductor L_1	110μH
Inductor L_2	55μH
High side voltage $U_{\rm high}$	400V
Low side voltage $U_{\rm low}$	40-120V
Switching frequency $f_{\rm s}$	50kHz
Power switches Q_1/Q_2/Q_4/Q_5	IXTH88N30P
Power switch Q_3	IXFX98N50P3

3) Design of Power Switches: The voltage stresses and current stresses are the key specifications to select the power switches. The voltage stresses on power switches are given in (16) and (17), and the corresponding current stresses of are listed in (21) and (23).

To ensure the safe operation of the power switches, the peak current of Q_1–Q_5 should also be taken into consideration. The peak values of $i_{\rm Q1}$–$i_{\rm Q5}$ are listed in (39) shown at the bottom of this page. The $i_{\rm C1\_SIpeak\_up}$ indicates the peak value of $i_{\rm C1}$ at state I in the step-up mode, and $i_{\rm C1\_SIIpeak\_down}$ represents the peak value of $i_{\rm C1}$ at state II in the step-down mode.

Based on (16), (17), (21), (23), and (39), the proper power switches (MOSFETs) can be selected.

V. EXPERIMENTAL RESULTS AND ANALYSES

To verify the previous theoretical analyses and the effectiveness of the proposed BDC, some experiments have been carried out. The 1-kW prototype of the proposed converter adopted in the experiments is shown in Fig. 13, and the used experimental circuit parameters are listed in Table II. All the circuit parameters selected follow the circuit parameter design guidelines are given in Section IV.

A. Experimental Results in the Step-Up Mode

Fig. 14 shows the key experimental waveforms of the proposed BDC in step-up mode, where the LVS voltage $U_{\rm low} = 40$ V and $d_{\rm boost} = 0.727$. In Fig. 14(a), the steady-state voltages across the capacitors are illustrated. It can be easily obtained that $U_{\rm C1} = U_{\rm C2} = 254$ V, $U_{\rm C3} = 106$ V, and $U_{\rm high} = 400$ V, which are in aligned with (11) and (12). It is also worth noting that the constant $U_{\rm C3}$ implies the potential between the negative poles of LVS and HVS is with negligible HF ripples, which alleviates the EMI problem. The currents pass the inductors are shown in Fig. 14(b). The average values of $i_{\rm L1}$, $i_{\rm L2}$, and $i_{\rm low}$ are $I_{\rm L1} = 9$ A, $I_{\rm L2} = 18$ A, and $I_{\rm low} = 25$ A, respectively, which verify the correctness of (33). It is also worth mentioning that the zero ripple of $i_{\rm low}$ verifies the zero LVS current ripple feature of the proposed BDC. The voltage stresses of Q_1–Q_5 are demonstrated in Fig. 14(c) and (d). It can be seen that the voltage stresses of all the power switches ($U_{\rm Q1} = U_{\rm Q2} = U_{\rm Q4} = U_{\rm Q5} = 146$ V and $U_{Q3} = 292$ V) are lower than $U_{\rm high} = 400$ V, and $U_{\rm Qi}$ ($i \in \{1, 2, 4, 5\}$) are even lower than $U_{\rm high}/2$. In addition, the black circles indicate that both turn-ON ZVS and turn-OFF ZVS are realized on the slave power switches Q_3, Q_4, and Q_5.

B. Experimental Results in the Step-Down Mode

The key waveforms of the proposed BDC operating in step-down mode are shown in Fig. 15. The used HVS voltage and the buck duty-cycle are $U_{\rm high} = 400$ V and $d_{\rm buck} = 0.283$, respectively. As seen from Fig. 15(a), the $U_{\rm low} = 40$ V is achieved, which verifies (15) ($M_{\rm buck} = 0.283/(3 - 0.283) = 0.1$). Again, $U_{\rm C1} = U_{\rm C2} = 254$ V and $U_{\rm C3} = 106$ V valid the correctness of (14) and show the merit of constant LVS and HVS potential difference. The current waveforms of $i_{\rm L1}$, $i_{\rm L2}$, and $i_{\rm low}$ are illustrated in Fig. 15(b), which agree with (8) and (33). Fig. 15(c) and (d) shows the voltages across the power switches. It can be found that the voltage stresses of Q_1, Q_2,

$$
\begin{cases}
I_{\rm Q1peak} = I_{\rm L1} + \frac{i_{\rm L1}}{2} = \frac{1}{1-d_{\rm boost}} I_{\rm high} + \frac{U_{\rm high} d_{\rm boost}(1-d_{\rm boost})}{2(2+d_{\rm boost}) L_1 f_{\rm s}} = \frac{1}{d_{\rm buck}} I_{\rm high} + \frac{U_{\rm high}(1-d_{\rm buck}) d_{\rm buck}}{2(3-d_{\rm buck}) L_1 f_{\rm s}} \\
I_{\rm Q2peak} = I_{\rm L2} + \frac{i_{\rm L2}}{2} = \frac{2}{1-d_{\rm boost}} I_{\rm high} + \frac{U_{\rm high} d_{\rm boost}(1-d_{\rm boost})}{2(2+d_{\rm boost}) L_2 f_{\rm s}} = \frac{2}{d_{\rm buck}} I_{\rm high} + \frac{U_{\rm high}(1-d_{\rm buck}) d_{\rm buck}}{2(3-d_{\rm buck}) L_2 f_{\rm s}} \\
I_{\rm Q3peak} = I_{\rm L1} + \frac{i_{\rm L1}}{2} = \frac{1}{1-d_{\rm boost}} I_{\rm high} + \frac{U_{\rm high} d_{\rm boost}(1-d_{\rm boost})}{2(2+d_{\rm boost}) L_1 f_{\rm s}} = \frac{1}{d_{\rm buck}} I_{\rm high} + \frac{U_{\rm high}(1-d_{\rm buck}) d_{\rm buck}}{2(3-d_{\rm buck}) L_1 f_{\rm s}} \\
I_{\rm Q4peak} = i_{\rm C1\_SIpeak\_up} = i_{\rm C1\_SIIpeak\_down} \approx \frac{2}{d_{\rm boost}} I_{\rm high} = \frac{2}{(1-d_{\rm buck})} I_{\rm high} \\
I_{\rm Q5peak} = I_{\rm L2} + \frac{i_{\rm L2}}{2} - (I_{\rm L1} + \frac{i_{\rm L1}}{2}) = \frac{1}{1-d_{\rm boost}} I_{\rm high} + \frac{U_{\rm high} d_{\rm boost}(1-d_{\rm boost})}{2(2+d_{\rm boost}) L_2 f_{\rm s}} - \frac{U_{\rm high} d_{\rm boost}(1-d_{\rm boost})}{2(2+d_{\rm boost}) L_1 f_{\rm s}} \\
\qquad = \frac{1}{d_{\rm buck}} I_{\rm high} + \frac{U_{\rm high}(1-d_{\rm buck}) d_{\rm buck}}{2(3-d_{\rm buck}) L_2 f_{\rm s}} - \frac{U_{\rm high}(1-d_{\rm buck}) d_{\rm buck}}{2(3-d_{\rm buck}) L_1 f_{\rm s}}
\end{cases}
\tag{39}
$$

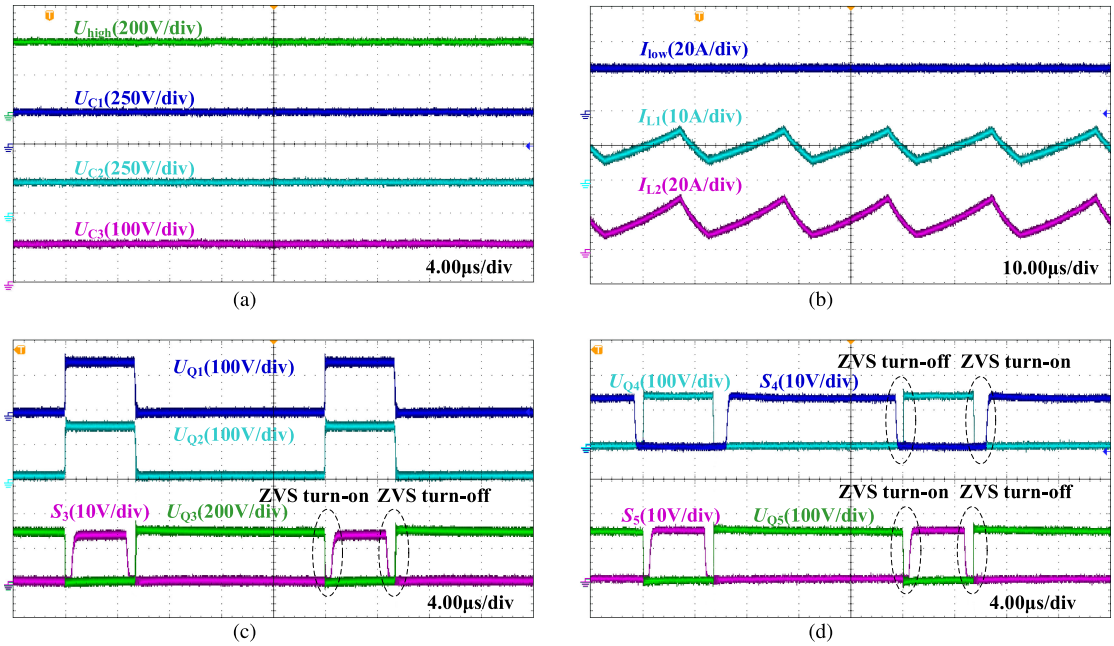

Fig. 14. Experimental waveforms in step-up mode. (a) $U_{\rm high}$, $U_{\rm C1}$, $U_{\rm C2}$, and $U_{\rm C3}$. (b) $i_{\rm low}$, $i_{\rm L1}$, and $i_{\rm L2}$. (c) $U_{\rm Q1}$, $U_{\rm Q2}$, S_3, and $U_{\rm Q3}$. (d) S_4, $U_{\rm Q4}$, S_5, and $U_{\rm Q5}$.

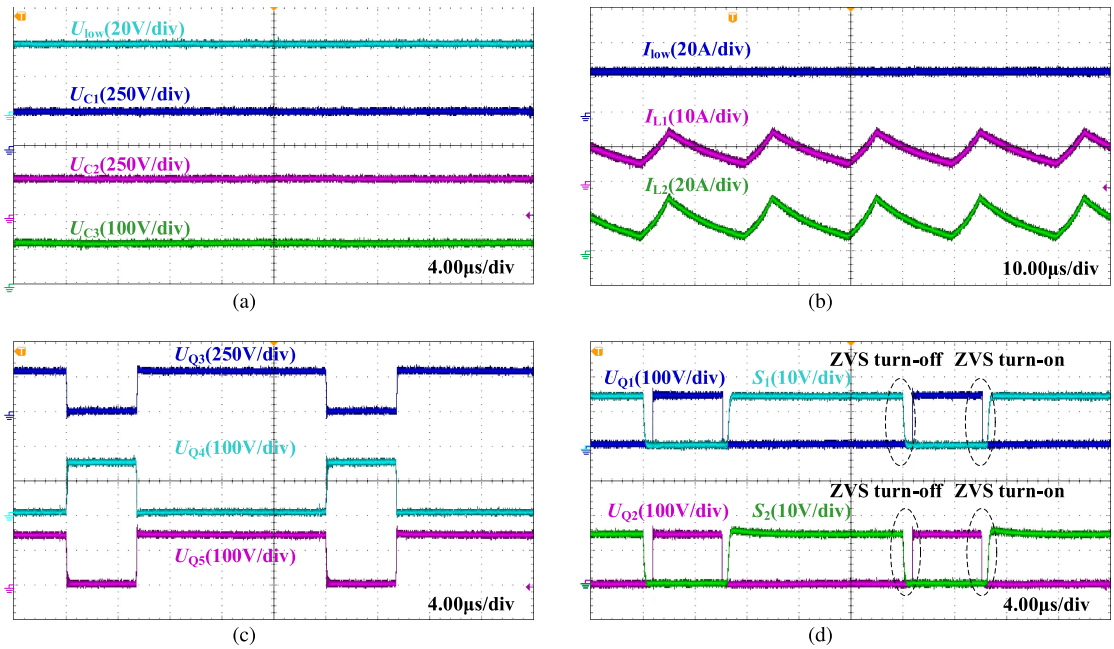

Fig. 15. Experimental waveforms in step-down mode. (a) $U_{\rm high}$,$U_{\rm C1}$, $U_{\rm C2}$, and $U_{\rm C3}$. (b) $i_{\rm low}$, $i_{\rm L1}$, and $i_{\rm L2}$. (c) $U_{\rm Q3}$, $U_{\rm Q4}$, and $U_{\rm Q5}$. (d) S_1, $U_{\rm Q1}$, S_2, and $U_{\rm Q2}$.

Q_3, Q_4, and Q_5 are $U_{\rm Q1} = 146$ V, $U_{\rm Q2} = 146$ V, $U_{\rm Q3} = 292$ V, $U_{\rm Q4} = 146$ V, and $U_{\rm Q5} = 146$ V, respectively, which satisfy (17). In addition, in Fig. 15(d), the black circles highlight the ZVS switching features of Q_1 and Q_2.

C. Dynamic Performance

To show the dynamic performance of the proposed BDC, two sets of experiments are carried out. In the experiments, the classic Type-II controller is adopted to regulate the voltage at the HVS and that at LVS in step-up mode and step-down mode, respectively.

First, the design procedure of the controller for the proposed BDC operating in the step-up mode is briefly given out. Linearizing the reduced-order averaged model given in (1) around its equilibrium point and using the circuit parameters given in Table II, the Bode-plot of the transfer function between the output voltage $u_{\rm high}$ and the duty-cycle $d_{\rm boost}$, i.e., $G_{\rm dvhigh} =$

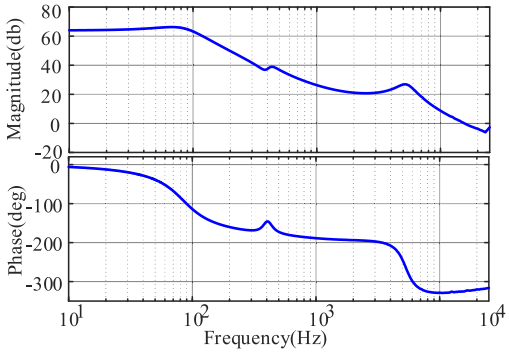

Fig. 16. Bode-plot of $G_{\rm dvhigh} = \hat{u}_{\rm high}/\hat{d}_{\rm boost}$.

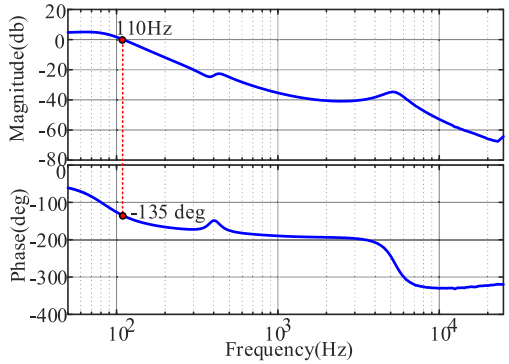

Fig. 17. Bode-plot of $T_{\rm OLV\_boost}(s)$.

$\hat{u}_{\rm high}/\hat{d}_{\rm boost}$, can be obtained as Fig. 16. The variable with "hat" indicates the small-signal value of it. Based on Fig. 16 and using the well-known k factor method, the type-II controller $G_{\rm PIV\_boost}$ is developed as

$$G_{\rm PIV\_boost}(s) = \frac{6.379\,(s+62.62)}{s\,(s+7647)}. \tag{40}$$

The corresponding Bode-plot of the open loop gain $T_{\rm OLV\_boost}(s) = G_{\rm PIV\_boost}G_{\rm dvhigh}$ can be obtained are illustrated in Fig. 17. It can be found the 110 Hz crossover frequency and 45° phase margin of the open loop gain $T_{\rm OLV\_boost}$ are obtained.

Similarly, using the averaged model given in (2) and following the controller design procedure shown above, a type-II voltage controller for the proposed BDC operating in the step-down mode is developed as

$$G_{\rm PIV\_buck}(s) = \frac{51.893\,(s+1537)}{s(s+4.014\times10^4)}. \tag{41}$$

The corresponding Bode-plot of the open loop gain $T_{\rm OLV\_buck}(s) = G_{\rm PIV\_buck}G_{\rm dvlow}$ is shown in Fig. 18. It can be seen that the magnitude curve of $T_{\rm OLV\_buck}$ cross zero at 1250 Hz and the phase margin of 45° is obtained.

Fig. 19 illustrates the HVS voltage of the BDC with linear changes of the LVS voltage. Specifically, in Fig. 19(a), the BDC operates in step-up mode. The LVS voltage (input voltage) gradually increases from 40 to 120 V and the HVS voltage

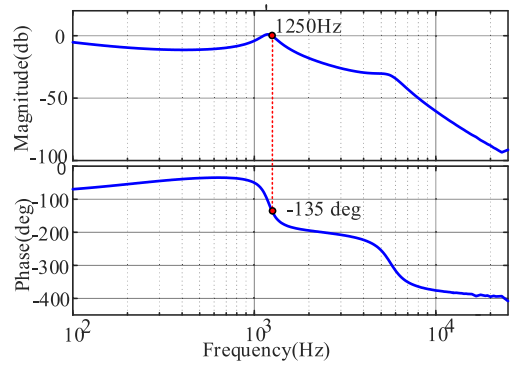

Fig. 18. Bode-plot of $T_{\rm OLV\_buck}(s)$.

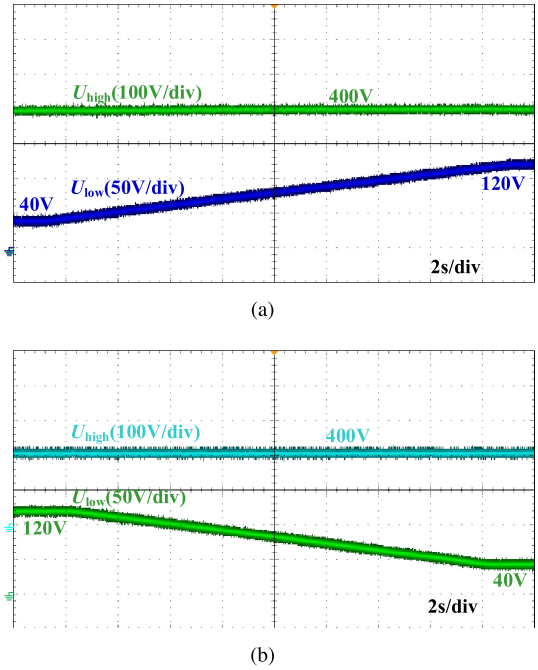

Fig. 19. Dynamic performance of the BDC with wide voltage gain range. (a) Step-up mode. (b) Step-down mode.

(output voltage) is held at 400 V. In contrast, in Fig. 19(b), the BDC operates in step-down mode. The control reference smoothly reduces from 120 to 40 V with a fixed converter input voltage $U_{\rm high} = 400$ V, and the output voltage $U_{\rm low}$ tightly tracks its reference. The results not only show the good voltage tracking ability of the regulated BDC system, but also imply that the proposed BDC possesses a wide voltage gain range. Fig. 20 shows the BDC output voltage in the presence of 500 to 1000 W output power change. In both the sub figures, the output voltages are barely affected by the output power jumps, which indicate that the regulated BDC system has good dynamic performance in the presence of load power sudden changes.

D. Converter Efficiency Analysis

Expect for the voltage gain range, voltage stress and dynamic performance, the conversion efficiency is another important

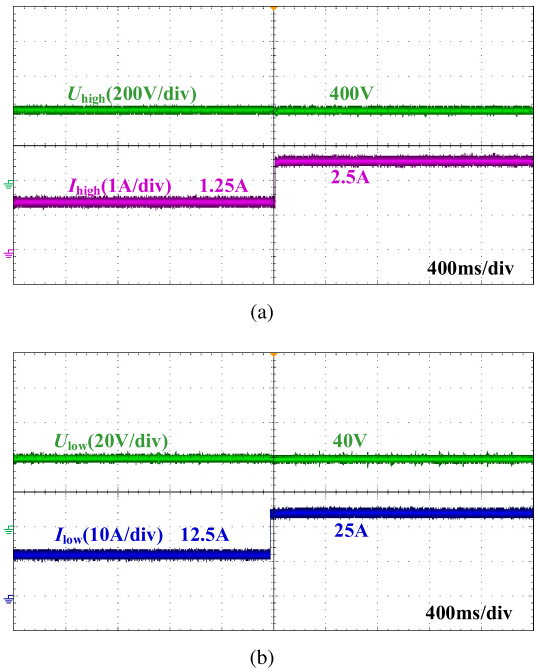

Fig. 20. Dynamic performance of the BDC in the presence of step load change. (a) Step-up mode. (b) Step-down mode.

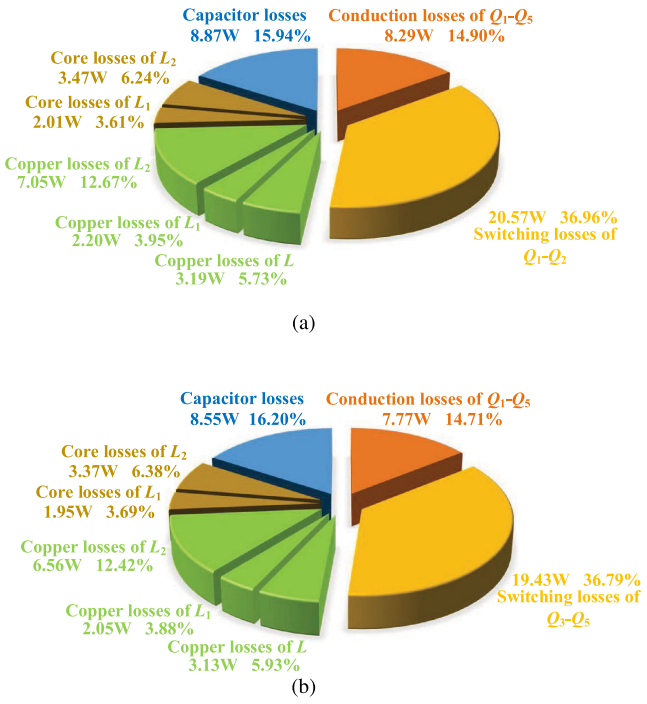

Fig. 21. Theoretical power loss distributions. (a) In the step-up mode. (b) In the step-down mode.

factor to evaluate a converter. In this section, the power losses analysis and measured experimental efficiencies are given out.

Fig. 21 shows the theoretical loss distribution for the experimental prototype under the operation condition of $U_{\rm low}$ = 40 V, $U_{\rm high}$ = 400 V, and P_n = 1000 W. In the step-up mode

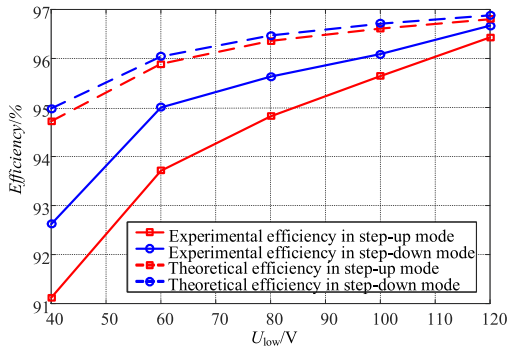

Fig. 22. Efficiencies with different $U_{\rm low}$ in 1000 W rated power.

[see Fig. 21(a)], the total converter power losses are 55.65 W. Specifically, the conduction losses of Q_1–Q_5 (8.29 W), switching losses of Q_1 and Q_2 (20.57 W), core losses of inductors (5.48 W), copper losses of inductors (12.44 W), and capacitor losses (8.87 W) account for 14.90%, 36.96%, 9.85%, 22.35%, and 15.94%, respectively. Among the losses caused by the inductors, the core losses caused by L_1 and L_2 are 3.47W and 2.01 W, respectively, and the copper losses caused by L, L_1, and L_2 are 3.19, 2.20, and 7.05 W, respectively. The theoretical loss distribution in the step-down mode is depicted in Fig. 21(b). The total losses are 52.81 W. In details, the conduction losses of Q_1–Q_5 (7.77 W), switching losses of Q_3, Q_4, and Q_5 (19.43 W), core losses of inductors (5.32 W), copper losses of inductors (11.74 W), and capacitor losses (8.55 W) account for 14.71%, 36.79%, 10.07%, 22.23%, and 16.20%, respectively. Looking into the inductor losses, it can be obtained that 3.37 and 1.95 W core losses are generated by L_1 and L_2, respectively, and 3.13, 2.05, and 6.56 W copper losses are, respectively, caused by L, L_1, and L_2. It is worth mentioning that, thanks to the zero current ripple technique, the ripple of the current flows through the inductor L can be negligible. Therefore, the core loss caused by L can be reasonably ignored.

The experimental efficiencies are measured using the YOKOGAWA WT3000 power analyzer. The corresponding efficiency curves for varying $U_{\rm low}$ (from 40 to 120 V), fixed $U_{\rm high}$ = 400 V and $P_{\rm n}$ = 1000 W are shown in Fig. 22. The efficiency curve for the step-up mode is in red while that for the step-down mode is plotted in blue. It can be seen that the experimental efficiency ranges from 91.12% (at $U_{\rm low}$ =40 V) to 96.43% (at $U_{\rm low}$ =120 V) in the step-up mode and 92.62% (at $U_{\rm low}$ = 40 V) to 96.67% (at $U_{\rm high}$ = 120 V) in the step-down mode. In addition, to show the difference between the calculated theoretical efficiency and the experimental efficiency, the converter theoretical efficiencies obtained using (27)–(32) are also given in Fig. 22. Noted that, as mentioned in the efficiency analysis part, the ideal rms currents are used to calculate the power losses of each component. However, in practice, to provide the same output power as the ideal case, higher input side currents are required. As results, the experimental efficiency is supposed to be lower than that obtained from the theoretical calculation as Fig. 22 shown. In addition, since a lower $U_{\rm low}$ results in a higher operation current level under the same output power, the

differences between the experimental and theoretical efficiency deceases with the increase of the U_{low}.

VI. Conclusion

This article proposed a nonisolated BDC for the BESS. The converter operating principles, specifications and corresponding circuit parameter design are comprehensively reported. Owing to its high voltage conversion ratio, low components voltage stresses, and constant potential difference between the grounds of input/output ports, the proposed BDC can be an excellent interface to link the BESS and the dc bus of grid without extreme duty-cycle. In addition, the merit of zero LVS current ripple effectively protects the BESS and extends its service life. The dynamic performance and conversion efficiency are also illustrated experimentally. Hence, all of these merits make the proposed BDC become a suitable solution for connecting BESS with the dc bus.

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