Simultaneous Wireless Power Transfer and Full-Duplex Communication With a Single Coupling Interface

Yuanshuang Fan, Yue Sun, *Member, IEEE*, Xin Dai, *Member, IEEE*, Zhiping Zuo, and Anhong You

***Abstract*—A method to achieve simultaneous wireless power transfer and full-duplex communication with a pair of coupling coils is proposed in this article. A double-side *LCC* compensation topology for power transfer is adopted, while the data transfer channel is constituted by a four resonance dual-rejection structure. In the process of power transfer and full-duplex communication, from the view of data transmitting and receiving, the data transmitting/receiving circuits on one side can not only transmit/receive the desired data carriers but also block the interference data carriers, and from the view of power transfer, the rated power transfer can be realized with little influence. Moreover, the parameter design method of the proposed system is given. Besides, the interference between the power wave and data carriers and the crosstalk between the data carriers are analyzed. Finally, an experimental prototype is built, which achieves an output power of 600 W and a data transmission rate of 80 kbps.**

***Index Terms*—Amplitude-shift keying (ASK), double data carriers, full-duplex communication, simultaneous power and data transfer, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) technology can realize electric power transfer over certain distances without physical contact [1]. It has attracted widespread attention in recent years and has been widely used in applications, such as electric vehicles, rotary mechanisms, biomedical implants, consumer electronics, and household appliances [2]–[7].

Generally, in some practical applications, real-time communication between the primary side and the secondary side is needed to improve system performance and stability. It is noted that the conventional technologies, such as Bluetooth, ZigBee, Wi-Fi, and radio frequency, can be used in WPT systems to realize the communication between the two sides, but these technologies need complicated pairing between the transmitting and receiving sides, and the transmission delay is relatively long [8]. Recently, many researchers have studied simultaneous wireless power and data transfer methods integrated into WPT systems. The advantages of these methods have been proved to be cost-effective and straightforward.

Among them, methods sharing the inherent power transfer channel of a WPT system to realize data transmission can not only eliminate the data transmission cables or wireless signal transmitters but also have the advantages of flexibility [9]. Especially for the rotating joints of robots and implantable medical devices with limited operating space, it has special significance and value. The main methods include transferring of data by modulating the power carrier [10]–[13] and transferring of data by modulating a single data carrier [8], [9], [14], [15]. These methods are of great significance to the application of WPT technology, especially for the development of simultaneous wireless power and data transmission technology. However, the power transfer of WPT systems adopting the first method will be affected by the data transmission and the data rate is limited by the relatively low-frequency power carrier. Besides, only half-duplex data transmission is realized by these methods. Qian *et al.* [16] achieve full-duplex communication by modulating double carriers using the quadrature phase-shift keying. The frequency-shift keying is used to realize full-duplex communication through partial coupling coils in [17]. However, the relatively complicated modulation and demodulation methods may limit their implementation in cost-sensitive applications.

This article proposes a new method to realize full-duplex communication. The signal channels are made up of serial networks and parallel networks constituted by low-cost passive components, inductors and capacitors, leading to a lower cost of the whole system. Besides, a simpler modulation method—amplitude-shift keying (ASK)—that can be realized by only an analog switch can be employed in the proposed method. Parallel *LC* networks and serial *LC* networks are modeled by equivalent inductors or capacitors under different frequencies to constitute a four resonance dual-rejection (FRDR) structure. In the data transfer channel, two data carriers are transferred via two equivalent *S*–*S* compensation topologies formed by the parallel *LC* networks and serial *LC* networks. The serial *LC* network is used to transfer two data carriers and the parallel *LC* networks are used to block one carrier while transmitting the other. With the proposed topology, two signal sources can be applied to the system at the same time, thus achieving full-duplex communication.

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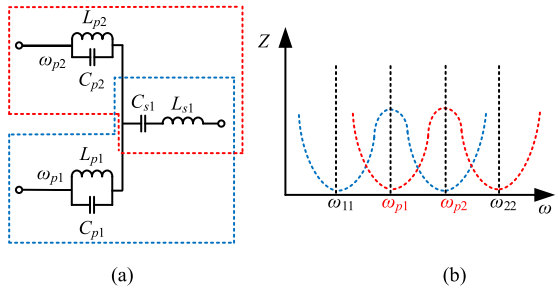

Fig. 1. (a) Proposed FRDR structure and (b) its frequency response.

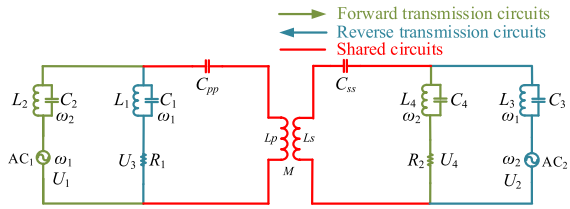

Fig. 2. Topology of the proposed full-duplex communication channel.

Full-duplex communication does not need direction switching, so there is no time delay caused by switching operations, which is very beneficial for interactive applications (such as remote monitoring and control systems) where the communication time delay should be strictly considered.

II. Full-Duplex Communication Channel and System Operation Principles

A. Full-Duplex Communication Channel

The proposed FRDR structure and its frequency response are shown in Fig. 1. It consists of two parallel *LC* networks (i.e., L_{p1} and C_{p1}, and L_{p2} and C_{p2}) and a serial *LC* network (i.e., L_{s1} and C_{s1}), where L_{p1}, C_{p1}, L_{p2}, and C_{p2} satisfy $1 = {\omega_{p1}}^2 L_{p1} C_{p1} = {\omega_{p2}}^2 L_{p2} C_{p2}$ and $\omega_{p2} > \omega_{p1}$. To transfer two data carriers simultaneously, two of the resonance points of the FRDR structure are tuned to be identical with its two rejection points, respectively. It means that one of the resonance points of one branch is exactly the rejection point of the other branch.

Fig. 2 shows the topology of the full-duplex communication channel proposed. It consists of four *LC* parallel networks (i.e., L_1 and C_1, L_2 and C_2, L_3 and C_3, and L_4 and C_4), two *LC* serial networks (i.e., L_p and C_{pp}, and L_s and C_{ss}), two sampling resistors (i.e., R_1 and R_2), and two ac signal sources (i.e., AC_1 and AC_2). The angular frequencies for AC_1 and AC_2 are ω_1 and ω_2, respectively.

The relationships between L_1 and C_1, and L_3 and C_3 satisfy $\omega_1 = 2\pi f_1 = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_3 C_3}$. The relationships between L_2 and C_2, and L_4 and C_4 satisfy $\omega_2 = 2\pi f_2 = 1/\sqrt{L_2 C_2} = 1/\sqrt{L_4 C_4}$. L_p and L_s are self-inductances of the primary and secondary coils, respectively. To simplify the analysis, it is assumed that $L_p = L_S$, $L_1 = L_3$, and $L_2 = L_4$. M is the mutual inductance between L_p and L_s. The green line and blue line indicate the separate forward transmission circuits and reverse transmission circuits, respectively, and the red line indicates the shared circuits of the two transmission channels. U_1 and U_2 represent the voltage of AC_1 and AC_2, respectively. U_3 and U_4 represent the receiving voltages for the reverse data transmission and forward data transmission, respectively. When data are forward transferred, the data carrier of the primary side is transferred via the forward transmission circuits and shared circuits (i.e., L_2, C_2, C_{pp}, L_p, L_s, C_{ss}, L_4, C_4, and R_2), and for the reverse data transmission, the data carrier of the secondary side is transferred via the reverse transmission circuits and shared circuits (i.e., L_1, C_1, C_{pp}, L_p, L_s, C_{ss}, L_3, C_3, and R_1).

B. Topology of the Proposed WPT System With Full-Duplex Communication

In this article, the double-side *LCC* compensation topology is adopted for WPT to illustrate the proposed simultaneous wireless power and data transfer method. The double-side *LCC* compensation topology is adopted in this article for the following reasons. First, the resonant frequency of the *LCC* topology is only related to inductances and capacitances, independent of the coupling and load condition. Different from the *S–S* compensation topology, the transferred power, input current, and output current are proportional to mutual inductance *M* [18]. It can realize a constant primary coil current and constant secondary output current and has a high design freedom. Second, what is more, the series inductors and parallel capacitors for both the primary side and secondary side can filter out a large portion of the high-order harmonics generated by the primary inverter and the secondary rectifier, which is very advantageous for the data transmission, reducing the harmonic interference and increasing the signal-to-noise ratio. The proposed method is also applicable to other WPT topologies. The circuit diagram of the whole system is shown in Fig. 3.

$E_{\rm dc}$ is the input dc voltage source. *S*1–*S*4 are the four MOSFETs used to constitute the full-bridge inverter. (L_p, C_p, L_{f1}, and C_{f1}) and (L_s, C_s, L_{f2}, and C_{f2}) constitute the primary *LCC* resonant tank and the secondary *LCC* resonant tank, respectively. (L_{r1} and C_{r1}), (L_{r2} and C_{r2}), (L_{r3} and C_{r3}), and (L_{r4} and C_{r4}) constitute the wave trappers of the primary side and the secondary side, respectively, and they satisfy $\omega_1 = 1/\sqrt{L_{r1} C_{r1}} = 1\sqrt{L_{r3} C_{r3}}$ and $\omega_2 = 1/\sqrt{L_{r2} C_{r2}} = 1\sqrt{L_{r4} C_{r4}}$. To simplify the analysis, it is assumed that $L_{r1} = L_{r3}$ and $L_{r2} = L_{r4}$. The trappers whose center frequencies are tuned to data carrier frequencies that are far from the power transfer frequency are used to block the data carriers from flowing through the full-bridge inverter, the rectifier, and the load, and from being weakened by them [14]. C_{pc} and C_{sc} are adopted in this article to compensate for the inductance to power wave resulting from the wave trappers added and to make the power transfer not be affected. With these two compensation capacitors, the value of the inductor of the trapper is no longer necessary to be very small and a higher impedance of trappers can be achieved. Actually, C_{pc} and C_{sc} can be eliminated by replacing the primary and secondary resonant capacitors C_p and C_s with $C_{\rm peq}$ and $C_{\rm seq}$, respectively, and they satisfy $C_{\rm peq} = C_p C_{pc}/(C_p + C_{pc})$ and

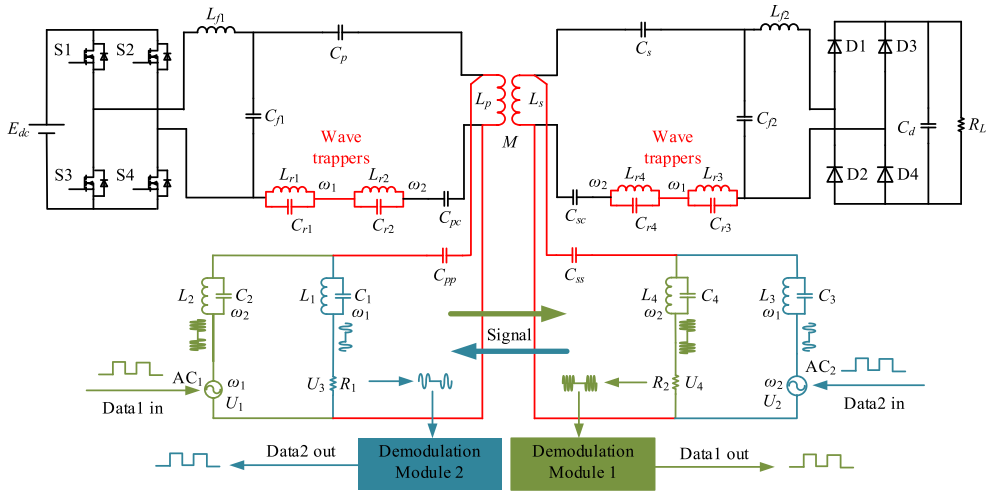

Fig. 3. Topology of WPT with full-duplex communication.

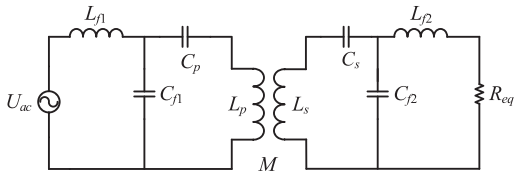

Fig. 4. Equivalent circuit of the power transfer channel.

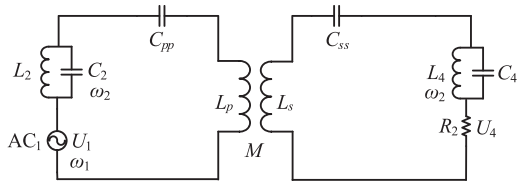

Fig. 5. Equivalent circuit of the forward transmission channel.

$C_{\text{seq}} = C_s C_{sc}/(C_s + C_{sc})$. *D*1–*D*4 and C_d constitute the rectifier, and R_L is the load resistor.

C. Operation Principles of Power and Data Transmission

1) Power Transfer: When the full-bridge inverter works, the data transfer channels show a high impedance, which can be treated as open circuits (analyzed further in Section IV), and the wave tappers act as inductors. Besides, the inductors are compensated by capacitors connected in series. Therefore, the power transfer channel is equivalent to the original double-side *LCC* structure WPT system. The equivalent circuit of the power transfer channel is shown in Fig. 4, where U_{ac} is the output voltage of the full-bridge inverter, and R_{eq} is the equivalent resistance of the rectifier and load R_L. Based on the article presented in [19], the resistance of the equivalent resistor can be expressed as $R_{\text{eq}} = \frac{8R_L}{\pi^2}$.

2) Forward Data Transmission: According to the superposition principle, when the primary signal source AC_1 works alone, the secondary signal source AC_2 acts as a short circuit and the parallel networks (L_1 and C_1), (L_3 and C_3), (L_{r1} and C_{r1}), and (L_{r3} and C_{r3}) act as the open circuits. The equivalent circuit of the forward transmission channel is shown in Fig. 5.

Assuming that $\omega_1 > \omega_2$, when data are forward transferred, the parallel network formed by (L_2 and C_2) and (L_4 and C_4) acts as capacitors, and the capacitance of the equivalent capacitors can be derived as

$$C_{\text{eq}\omega_1} = C_2 - \frac{1}{{\omega_1}^2 L_2} = C_4 - \frac{1}{{\omega_1}^2 L_4}. \quad (1)$$

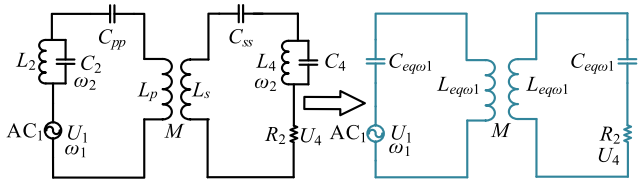

Fig. 6. Further simplified circuit of the forward transmission channel.

To make the primary and secondary circuits resonant at the angular frequency ω_1, the serial networks formed by (L_p and C_{pp}) and (L_s and C_{ss}) must act as inductors at the angular frequency ω_1. The equivalent inductance can be obtained as

$$L_{\text{eq}\omega_1} = L_p - \frac{1}{{\omega_1}^2 C_{pp}} = L_s - \frac{1}{{\omega_1}^2 C_{ss}} = \frac{1}{{\omega_1}^2 C_{\text{eq}\omega_1}}. \quad (2)$$

The equivalent circuit of the forward transmission channel can be further simplified, as shown in Fig. 6.

As shown in Fig. 6, when data are forward transferred, the sinusoidal signal generated by signal source AC_1 is transferred from the primary side to the secondary side by the equivalent *S*–*S* compensation resonant network and the signal is sampled by the sampling resistor R_2. Thus, the data have been transferred from the primary side to the secondary side successfully.

3) Reverse Data Transmission: Similar to the forward transmission, the parallel networks formed by (L_1 and C_1) and (L_3 and C_3) act as inductors, and the inductance of the equivalent

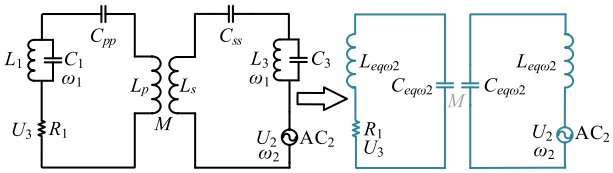

Fig. 7. Further simplified circuit of the reverse transmission channel.

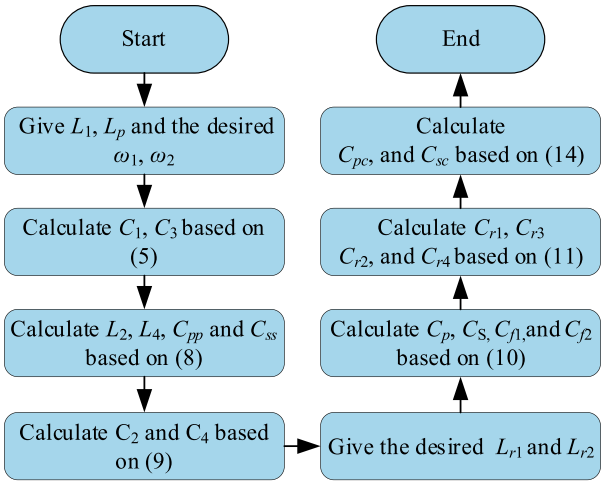

Fig. 8. Flowchart for the parameter design.

inductors can be derived as

$$L_{\mathrm{eq}\omega_2} = \frac{L_1}{1-\omega_2{}^2 L_1 C_1} = \frac{L_3}{1-\omega_2{}^2 L_3 C_3}. \tag{3}$$

The capacitance of the equivalent capacitors of the serial networks formed by (L_p and C_{pp}) and (L_s and C_{ss}) can be derived as

$$C_{\mathrm{eq}\omega_2} = \frac{C_{pp}}{1-\omega_2{}^2 L_p C_{pp}} = \frac{C_{ss}}{1-\omega_2{}^2 L_s C_{ss}} = \frac{1}{\omega_2{}^2 L_{\mathrm{eq}\omega_2}}. \tag{4}$$

The further simplified equivalent circuit of reverse transmission is shown in Fig. 7. As shown in Fig. 7, when data are transferred in reverse, the sinusoidal signal generated by signal source AC$_2$ is transferred from the secondary side to the primary side by the equivalent *S–S* compensation resonant network and the signal is sampled by the sampling resistor R_1. Thus, data have been transferred from the secondary side to the primary side successfully.

III. System Parameter Design

The parameters of the system proposed can be designed following the steps, as illustrated in Fig. 8.

In the process of parameter design, the frequencies of the two data carriers (i.e., ω_1 and ω_2), L_1 and L_p can be predetermined, and C_1 and C_3 can be derived as

$$C_1 = C_3 = \frac{1}{\omega_1{}^2 L_1} = \frac{1}{\omega_1{}^2 L_3}. \tag{5}$$

According to (1) and (2), it can be derived that

$$\begin{aligned} L_{\mathrm{eq}\omega_1} &= L_p - \frac{1}{\omega_1{}^2 C_{pp}} = L_s - \frac{1}{\omega_1{}^2 C_{ss}} \\ &= \frac{1}{\omega_1{}^2\left(C_2 - \frac{1}{\omega_1{}^2 L_2}\right)} = \frac{1}{\omega_1{}^2\left(C_4 - \frac{1}{\omega_1{}^2 L_4}\right)}. \end{aligned} \tag{6}$$

According to (3) and (4), it can be derived that

$$\begin{aligned} C_{\mathrm{eq}\omega_2} &= \frac{C_{pp}}{1-\omega_2{}^2 L_p C_{pp}} = \frac{C_{ss}}{1-\omega_2{}^2 L_s C_{ss}} \\ &= \frac{1}{\omega_2{}^2\left(\frac{L_1}{1-\omega_2{}^2 L_1 C_1}\right)} = \frac{1}{\omega_2{}^2\left(\frac{L_3}{1-\omega_2{}^2 L_3 C_3}\right)}. \end{aligned} \tag{7}$$

Combining (6) with (7), the following equations can be obtained:

$$\begin{cases} L_2 = L_4 = \frac{L_p\left(\omega_1{}^4+\omega_2{}^4\right)-\omega_1{}^2\omega_2{}^2(L_1+2L_p)}{\omega_1{}^2\omega_2{}^2} \\ C_{pp} = C_{ss} = \frac{\omega_1{}^2-\omega_2{}^2}{\omega_2{}^2((L_1+Lp)\omega_1{}^2-L_p\omega_2{}^2)} \end{cases} \tag{8}$$

and based on (8), it can be derived that

$$\begin{aligned} C_2 = C_4 &= \frac{1}{\omega_2{}^2 L_2} = \frac{1}{\omega_2{}^2 L_4} \\ &= \frac{\omega_1{}^2}{L_p\left(\omega_1{}^4+\omega_2{}^4\right)-\omega_1{}^2\omega_2{}^2\left(L_1+2L_p\right)}. \end{aligned} \tag{9}$$

Defining the operation angular frequency of the full-bridge inverter as $\omega_r = 2\pi f_r$, for a double-side *LCC*-type WPT system, C_p, C_s, C_{f1}, and C_{f2} satisfy

$$\begin{cases} C_p = \frac{1}{\omega_r{}^2(L_p-L_{f1})} \\ C_s = \frac{1}{\omega_r{}^2(L_s-L_{f2})} \\ C_{f1} = \frac{1}{\omega_r{}^2 L_{f1}} \\ C_{f2} = \frac{1}{\omega_r{}^2 L_{f2}}. \end{cases} \tag{10}$$

According to Sun *et al.* [14], the trappers are used to block the high-frequency data carriers out of the power inverter and rectifier, and the higher the impedance of the trappers, the better. However, in practical applications, restricted by the equivalent serial resistance of the inductor, system space, and cost, the inductance values of L_{r1} and L_{r2} should be selected reasonably. In the permissible range of technical conditions, an inductor with a higher inductance and higher Q value leading to a higher impedance of the trapper is preferred, and it can be derived that

$$\begin{cases} C_{r1} = C_{r3} = \frac{1}{\omega_1 L_{r1}} = \frac{1}{\omega_1 L_{r3}} \\ C_{r2} = C_{r4} = \frac{1}{\omega_2 L_{r2}} = \frac{1}{\omega_2 L_{r4}}. \end{cases} \tag{11}$$

To minimize the interference between power and data, in the proposed system, the angular frequencies should satisfy $\omega_1 > \omega_2 >> \omega_r$, where the corresponding frequencies f_2 and f_r of ω_2 and ω_r are at megahertz level and kilohertz level, respectively.

According to the previous analysis, the trappers can be represented by inductors for the power wave. The inductances of the equivalent inductors can be obtained as

$$\begin{cases} L_{r1\mathrm{eq}\omega_r} = \frac{L_{r1}}{1-\omega_r{}^2 L_{r1} C_{r1}} = \frac{L_{r3}}{1-\omega_r{}^2 L_{r3} C_{r3}} \\ L_{r2\mathrm{eq}\omega_r} = \frac{L_{r2}}{1-\omega_r{}^2 L_{r2} C_{r2}} = \frac{L_{r4}}{1-\omega_r{}^2 L_{r4} C_{r4}}. \end{cases} \tag{12}$$

Defining the ratio of ω_r to ω_1 and ω_r to ω_2 as α and β, respectively, $\frac{\omega_r}{\omega_1} = \alpha \approx 0$ and $\frac{\omega_r}{\omega_2} = \beta \approx 0$, and substituting them to (12), it can be derived that

$$\begin{cases} L_{r1\mathrm{eq}\omega_r} = \frac{L_{r1}}{1-\alpha^2} = \frac{L_{r3}}{1-\alpha^2} \approx L_{r1} = L_{r3} \\ L_{r2\mathrm{eq}\omega_r} = \frac{L_{r2}}{1-\beta^2} = \frac{L_{r4}}{1-\beta^2} \approx L_{r2} = L_{r4}. \end{cases} \tag{13}$$

From (13), it can be derived that

$$C_{pc} = \frac{1}{{\omega_r}^2 (L_{r1} + L_{r2})} = C_{sc} = \frac{1}{{\omega_r}^2 (L_{r3} + L_{r4})}. \tag{14}$$

R_1 and R_2 are used for sampling the signal currents in this article. The received signal voltage will increase with the increase of R_1 and R_2, and a larger signal voltage is conducive to increase the signal-to-noise ratio of the signal transmission. However, in practical applications, with the existence of the internal resistances of the inductors, the impedances of the parallel networks connected in series with R_1 and R_2 are not infinite at their center frequencies. The interference voltage of the ipsilateral transmitter signal will be divided by the parallel network and sampling resistors. A larger resistor will also lead to a larger interference of the same side transmitting signal.

Therefore, the value of the sampling resistor should be as small as possible, while the sampling voltage is greater than the minimum input voltage of the demodulation circuits.

IV. System Performance Analysis

A. Interference of the Data Transfer on Power Transfer

Two issues need to be considered when analyzing the influence on power transfer due to the data transfer channel added. One is the power transfer losses due to the adding of data transfer circuits; another is the influence of data transfer on the power transfer [8]. According to the characteristics of serial *LC* networks, the resonant angular frequency of the networks formed by (L_p and C_{pp}) and (L_s and C_{ss}) is much higher than the power channel resonant angular frequency, and C_{pp} and C_{ss} are very small. The impedances of these two capacitors are very high at the power carrier frequency. Therefore, the power current flowing through the data transfer channel is quite small and can be neglected compared with the primary coil current and the secondary coil current, and the power transfer losses due to the data transfer channel added can be neglected. In terms of the interference of data transfer on power transfer, the signal circuit energy is extremely small [10], [14], [15]; therefore, the interference of data transfer on the power channel can be ignored.

B. Interference of the Power Transfer on Data Transfer

To realize the high-quality data transfer, the output data carriers capacity should be enlarged and the interference of power transfer should be weakened as possible, in the process of system design. The interference of power transfer mainly comes from the interference voltage on the sampling resistor generated by the low-frequency power current flowing through the resistor. Taking the primary side as an example, the working circuit of the interference of the power channel on R_1 is shown in Fig. 9.

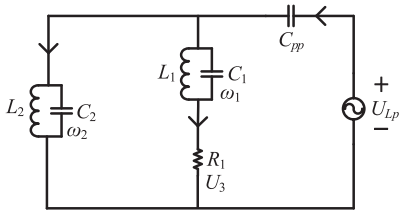

Fig. 9. Working circuit of the interference of the power channel.

In this article, only the interference of the fundamental component of the power wave was considered because the low-pass filters whose cutoff frequencies are equal to the power carrier frequency are formed by the serial compensation inductors (i.e., L_{f1} and L_{f2}) and parallel compensation capacitors (i.e., C_{f1} and C_{f2}), and the high-order harmonics generated by the inverter and rectifier are almost filtered by them. Besides, the frequencies of the data carriers are much higher than the power carrier frequency and the amplitude of harmonics at the data carrier frequency is very small. Therefore, the interference of high-order harmonics can be neglected.

$\dot{U}_{Lp}$ is the voltage of the primary coil. When calculating the voltage of the primary coil excited by the power current, the data transfer channel can be neglected because of the high impedance of the data transfer channel to the power wave. The voltage of the primary coil can be derived as

$$\dot{U}_{Lp} = \frac{\dot{U}_{\mathrm{ac}}}{j\omega_r L_{f1}} (Z_r + j\omega_r L_p) \tag{15}$$

where Z_r is the reflected impedance of the secondary side. Z_r can be expressed as

$$Z_r = \frac{{\omega_r}^2 M^2 C_{f2} R_{\mathrm{eq}}}{L_{f2}}. \tag{16}$$

The interference voltage of power on R_1 can be obtained as

$$\dot{U}_{\mathrm{int}\mathrm{R}_1} = \frac{\dot{U}_{L_p} j\omega_r L_2 R_1}{Z_{p_{sig}} (j\omega_r L_2 + j\omega_r L_1 + R_1)} \tag{17}$$

where Z_{psig} is the impedance of the data transfer channel to the power wave. Based on (13), Z_{psig} can be expressed as

$$Z_{p_{sig}} = \frac{j\omega_r L_2 (j\omega_r L_1 + R_1)}{j\omega_r L_2 + j\omega_r L_1 + R_1} + \frac{1}{j\omega_r C_{pp}}. \tag{18}$$

The interference voltage of power on R_2 can be obtained with the same method.

C. Crosstalk Between Two Data Carriers

In practice applications, there exists the internal resistance of the inductor and the impedance of the parallel network cannot achieve infinity at the resonant angular frequency. To analyze the data transfer crosstalk, the internal resistance of the inductor should be considered. The circuit diagram of the full-duplex communication channel can be shown in Fig. 10. R_{s1}, R_{s2}, R_{sp}, R_{ss}, R_{s4}, and R_{s3} are the internal resistances of L_2, L_1, L_P, L_s, L_4, and L_3, respectively.

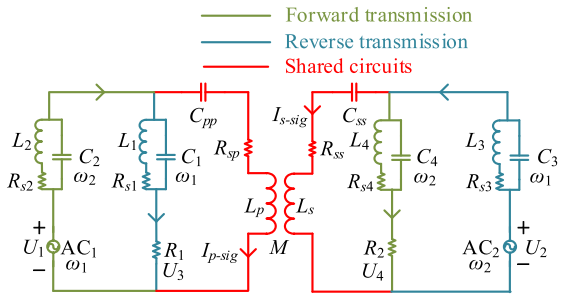

Fig. 10. Circuit diagram of the full-duplex communication channel.

When the internal resistance of the inductor is considered, the impedance of a parallel network can be expressed as

$$Z_{\text{para}} = \frac{R}{\left(1-\omega^2 LC\right)^2 + R^2\omega^2C^2} + j\frac{\left(1-\omega^2 LC\right)\omega L - R^2\omega C}{\left(1-\omega^2 LC\right)^2 + R^2\omega^2C^2} \tag{19}$$

where L, C, R, and ω are the inductance, capacitance, internal resistance of the inductor of the parallel network, and the angular frequency of the data carrier, respectively.

Defining $\gamma = \frac{R}{\omega L}$ and substituting it to (19), it can be obtained that

$$Z_{\text{para}} = \frac{\gamma\omega L}{1-2\omega^2 LC + \left(1+\gamma^2\right)\omega^4L^2C^2} - j\frac{\omega L\left(\omega^2 LC\left(1+\gamma^2\right)-1\right)}{1-2\omega^2 LC + \left(1+\gamma^2\right)\omega^4L^2C^2}. \tag{20}$$

When $\omega L >> R$, $\gamma \approx 0$, and $\omega^2 LC - 1 > 0$ ($\omega^2 LC - 1 < 0$), the imaginary part of Z_{para} can be rewritten as

$$\text{Im}\left(Z_{\text{para}}\right) \approx \frac{\omega L}{\omega^2 LC - 1}. \tag{21}$$

It can be inferred from (21) that the resonant tank can be barely influenced when the internal resistance of the inductor is far less than ωL.

When the data are forward transferred, the interference of the reverse data transfer is mainly the voltage generated by AC_2 on R_2. The impedance of (L_2 and C_2) parallel network is relatively large and can be treated as an open circuit for simplification. The reflection impedance of the primary data transfer channel can be expressed as

$$Z_{r-sigp} = \frac{{\omega_2}^2M^2}{R_1 + \frac{R_{s1}}{\left(1-{\omega_2}^2L_1C_1\right)^2 + {R_{s1}}^2{\omega_2}^2{C_1}^2} + R_{sp}}. \tag{22}$$

When calculating the data carrier current of the secondary side, the impedance of (L_4 and C_4) parallel network is relatively large and can be treated as an open circuit for simplification. The data carrier current of the secondary side can be derived as

$$\dot{I}_{s-sig} = \frac{\dot{U}_2}{\frac{R_{s3}}{\left(1-{\omega_2}^2L_3C_3\right)^2 + {R_{s3}}^2{\omega_2}^2{C_3}^2} + R_{ss} + Z_{r-sigp}}. \tag{23}$$

The voltage of the secondary-side serial network (L_s and C_{ss}) can be obtained as

$$\dot{U}_{\text{s-s}} = \dot{I}_{s-sig}\left(j\omega_2L_s + R_{ss} + \frac{1}{j\omega_2C_{ss}} + Z_{r-sigp}\right). \tag{24}$$

The interference voltage $\dot{U}_{\text{int-AC2}}$ of the reverse data carrier on R_2 can be obtained as

$$\begin{cases} \dot{U}_{\text{int-AC2}} = \dot{U}_{s-\text{s}}\frac{R_2}{R_2+Z_{\text{para-}R_2}} \\ Z_{\text{para-}R_2} = \frac{R_{s4}+j\left(\left(1-{\omega_2}^2L_4C_4\right)\omega_2L_4-{R_{s4}}^2\omega_2C_4\right)}{\left(1-{\omega_2}^2L_4C_4\right)^2+{R_{s4}}^2{\omega_2}^2{C_4}^2} \end{cases} \tag{25}$$

where $Z_{\text{para}-R_2}$ is the impedance of the parallel network connected with R_2.

When data are transferred in reverse, the same with the forward transmission, the interference voltage $\dot{U}_{\text{int-AC1}}$ of the forward data carrier on R_1 can be obtained as

$$\begin{cases} \dot{U}_{\text{int-AC1}} = \dot{U}_{s-p}\frac{R_1}{R_1+Z_{\text{para-}R1}} \\ \dot{U}_{s-p} = \dot{I}_{p-sig}\left(j\omega_1L_p + R_{sp} + \frac{1}{j\omega_1C_{pp}} + Z_{r-sigs}\right) \\ \dot{I}_{p-sig} = \frac{\dot{U}_1}{\frac{R_{s2}}{\left(1-{\omega_1}^2L_2C_2\right)^2+{R_{s2}}^2{\omega_1}^2{C_2}^2}+R_{sp}+Z_{r-sigs}} \\ Z_{r-sigs} = \frac{{\omega_1}^2M^2}{R_2+\frac{R_{s4}}{\left(1-{\omega_1}^2L_4C_4\right)^2+{R_{s4}}^2{\omega_1}^2{C_4}^2}+R_{ss}} \\ Z_{\text{para\_}R1} = \frac{R_{s1}+j\left(\left(1-{\omega_1}^2L_1C_1\right)\omega_1L_1-{R_{s1}}^2\omega_1C_1\right)}{\left(1-{\omega_1}^2L_1C_1\right)^2+{R_{s1}}^2{\omega_1}^2{C_1}^2} \end{cases} \tag{26}$$

where $\dot{U}_{s-p}$, $Z_{\text{para}-R_1}$, $\dot{I}_{p-sig}$, $Z_{r\text{-}sigs}$ are the voltage of the primary serial network, the impedance of parallel network connected with R_1, the data carrier current of the primary side, and the reflected impedance of the secondary data transfer channel, respectively.

D. Voltage Gains of Data Transmission and Power Transfer

When data are forward transferred, the transfer function from the primary signal source voltage $\dot{U}_1$ to the secondary sampling resistor R_2 voltage $\dot{U}_4$ can be expressed as

$$G_{\text{fwd}} = \frac{\dot{U}_4}{\dot{U}_1} = \frac{j\omega_1M\dot{I}_{p-sig}R_2}{\left(R_{ss}+R_2+\frac{R_{s4}}{\left(1-{\omega_1}^2L_4C_4\right)^2+{R_{s4}}^2{\omega_1}^2{C_4}^2}\right)\dot{U}_1}. \tag{27}$$

When data are transferred in reverse, the transfer function from the secondary signal source voltage $\dot{U}_2$ to the primary sampling resistor R_1 voltage $\dot{U}_3$ can be expressed as

$$G_{\text{rev}} = \frac{\dot{U}_3}{\dot{U}_2} = \frac{j\omega_2M\dot{I}_{s-sig}R_1}{\left(R_{sp}+R_1+\frac{R_{s1}}{\left(1-{\omega_2}^2L_1C_1\right)^2+{R_{s1}}^2{\omega_2}^2{C_1}^2}\right)\dot{U}_2}. \tag{28}$$

From the operation principles of the double-side *LCC* compensation topology [18], the transfer function from the output voltage of the full-bridge inverter to the voltage of load R_L can be derived as

$$G = \frac{\dot{U}_{R_L}}{\dot{U}_{\text{ac}}} = \frac{8MR_L}{j\omega_rL_{f1}L_{f2}\pi^2}. \tag{29}$$

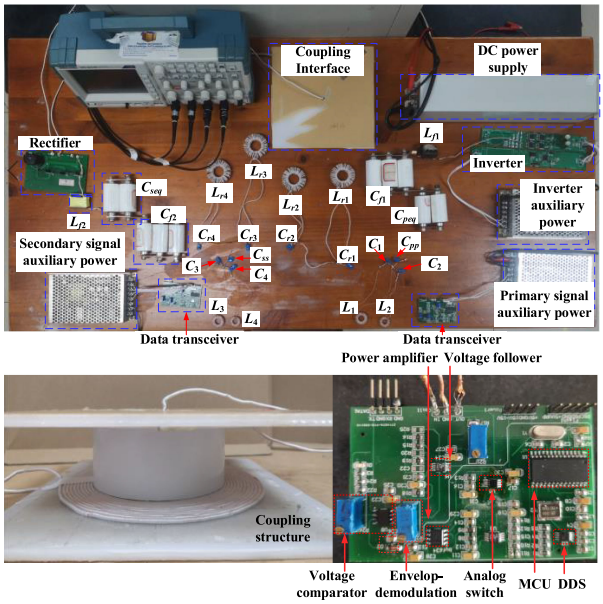

Fig. 11. Experimental prototype.

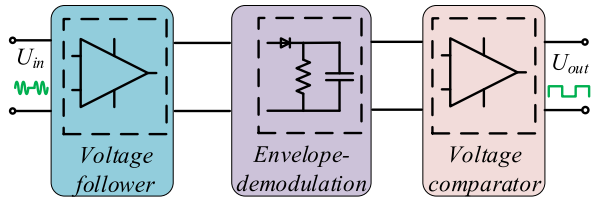

Fig. 12. Signal demodulation module.

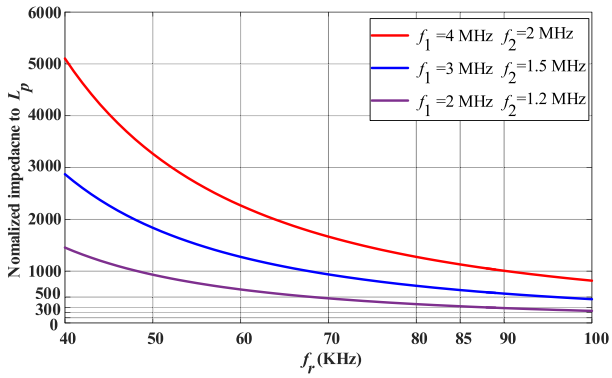

Fig. 13. Normalized impedance of data transfer channel to L_p.

V. Experimental Results and Verification

To verify the validity of the proposed method, an experimental prototype built based on Fig. 3 is shown in Fig. 11. In the data transceiver, an microcontroller unit (MCU) (PIC18F25K22) is used to program the direct digital synthesis (DDS) (AD9833) to generate sinusoidal data carriers and to control the analog switch (ADG5419) to modulate data carriers.

ASK and load-shift keying (LSK) are the most commonly adopted data modulation methods in data transfer [20]–[22]. ON–OFF keying (OOK) can be regarded as a special case of ASK, which is also widely used in signal modulation. The greatest advantage of ASK and LSK is simplicity. OOK is adopted in this article and it can be expressed as

$$f(t) = \begin{cases} A \sin \omega t & \text{bit} = 1 \\ 0 & \text{bit} = 0 \end{cases} \tag{30}$$

where A and ω are the amplitude and angular frequency of the data carrier, respectively. When the data to be transferred are "1," the sinusoidal wave will be transferred. When the data to be transferred are "0," there is no data carrier in the signal channel.

The signal demodulation circuit is mainly made up of a voltage-following module, an envelope-demodulation module, and a voltage comparator. First, the signal is followed by a voltage follower made up of an operational amplifier, then the envelope of the signal is extracted by the envelope-demodulation module, and finally, the signal envelope is shaped by a voltage comparator to restore the baseband signal. The signal demodulation module is shown in Fig. 12.

As mentioned in Section II, the data transfer channel shows a high impedance to power wave and can be treated as open circuits. With parameters $L_1 = 22\ \mu$H, $L_2 = 47\ \mu$H, $R_1 = 470\ \Omega$, and three groups of ω_1 and ω_2 (i.e., $\omega_1 = 2\pi{*}2{*}10^6$ and $\omega_2 = 2\pi{*}1.2{*}10^6$, $\omega_1 = 2\pi{*}3{*}10^6$ and $\omega_2 = 2\pi{*}1.5{*}10^6$, and $\omega_1 = 2\pi{*}4{*}10^6$ and $\omega_2 = 2\pi{*}2{*}10^6$), and other parameters, such as C_1, C_2, L_p, and C_{pp} can be derived. Substituting the parameters into (18) and when the switching frequency of the inverter f_r varies from 40 to 100 kHz, the normalized impedance curves to L_p can be acquired, as shown in Fig. 13, which indicates the following.

1) The impedance of the data transfer channel to the power wave is much higher than the impedances of L_p to the power wave.
2) The impedances of the data transfer channel are positively correlated with the ratio of the frequency of the signal wave to the power wave. The larger the ratio, the higher the impedance.

As mentioned in Section IV, the interference of data transfer on power transfer can be ignored. A group of system parameters, as listed in Table I, are selected to analyze the power transfer channel responses with the data transfer channel (wave trappers) added or not.

The bode plots of the power transfer channel are shown in Fig. 14. It can be inferred from the figure that the gains of the power channel are the same before and after the trappers are added at the switching frequency of the full-bridge inverter.

TABLE I
System Parameters

Parameter	Value	Parameter	Value
E_{dc}	100 V	f_r	85 kHz
L_p, L_s	60.6 μH	C_p	86.4 nF
L_{f1}	20 μH	C_s	70.7 nF
L_{f2}	11 μH	C_{f1}	175.3 nF
L_{r1}, L_{r3}	30 μH	C_{f2}	318.7 nF
L_{r2}, L_{r4}	30 μH	C_{r1}, C_{r3}	211 pF
C_{pc}, C_{sc}	58.4 nF	C_{r2}, C_{r4}	586 pF
L_1, L_3	22 μH	U_1, U_2	13 V(pk)
f_1	2 MHz	C_1, C_3	287.8 pF
L_2, L_4	47 μH	f_2	1.2 MHz
C_{pp}, C_{ss}	185 pF	C_2, C_4	374 pF
R_1	470 Ω	M	18 μH
R_L	4.85 Ω	R_2	470 Ω

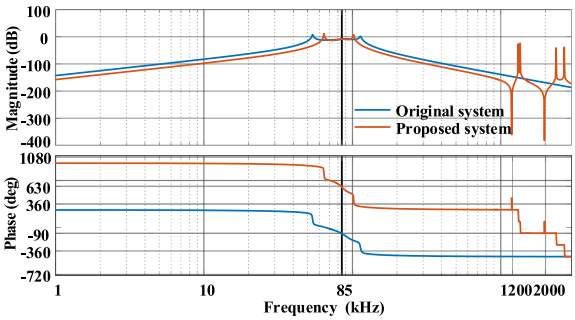

Fig. 14. Bode plots of the power transfer channel when $R_L = 4.85\ \Omega$.

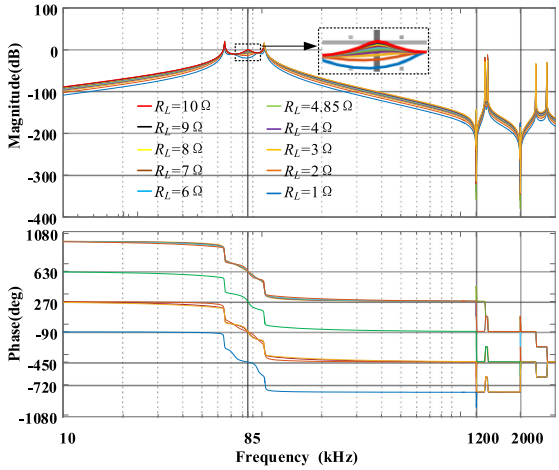

Fig. 15. Bode plots of the power transfer channel at different loads.

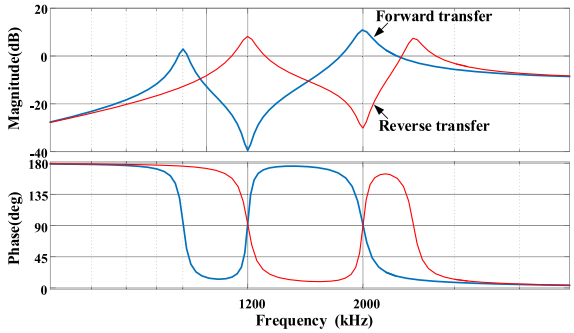

Fig. 16. Bode plots of data transfer channels.

The power transfer at the inverter switching frequency is almost unaffected by the data transfer channel added. Besides, the bode plots of the power transfer channel at different load R_L are also drawn, as shown in Fig. 15. It can be seen from Fig. 15 that the gain of the power transfer channel increases with the increase of R_L and the phase difference between the output voltage and the input voltage is constant. Therefore, the constant-current output characteristic of the system, which is indicated by that the output voltage increases with the increase of load, remains unchanged, and the resonant frequency of the system remains unchanged after the trappers are added to the power transfer channel.

To analyze the responses of data transfer channels, the bode plots of them are also drawn, as shown in Fig. 16. It can be seen from the figure that the forward transfer channel can block the data carrier of 1.2 MHz while conducting the data carrier

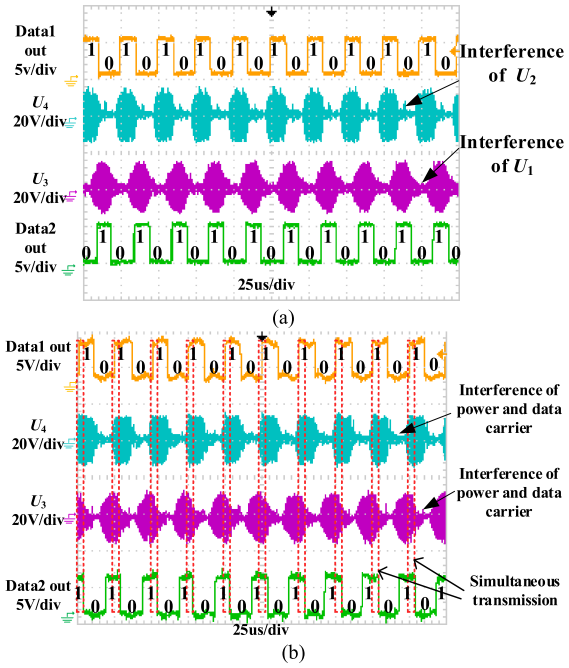

Fig. 17. Waveforms of data transfer channels. (a) Without the power transfer. (b) With the parallel power transfer.

of 2 MHz. As to the reverse transfer channel, it is just on the contrary. Thus, full-duplex communication can be achieved based on the responses of data transfer channels.

Fig. 17 shows the waveforms of the data transfer channels without and with simultaneous power transfer. The data carriers are modulated by the OOK with the analog switches controlled by MCUs and the received sampling signal is first followed by a voltage follower and demodulated by an envelope detector, and then shaped by a voltage comparator with an appropriate threshold to filter out the interference and to recover the original data. The waveforms in the red dashed box indicate that the two data carriers are transferred in data transfer channels simultaneously.

The fast Fourier transform (FFT) results of the sampling signals of the primary side and secondary side are shown in Fig. 18(a) and (b), respectively. In the primary sampling signal, the 2 MHz data carrier is suppressed, while in the secondary side, the 1.2 MHz is suppressed. It can be inferred from Fig. 18(a) and (b) that the suppression effect of the parallel network to 2 MHz is much better than 1.2 MHz because, with the existence of internal resistance of the inductors, in the experimental platform built, the impedance of the parallel network whose center frequency is 2 MHz is much higher than that of the parallel network with the center frequency of 1.2 MHz. Fig. 18(c) shows the voltage of the primary coil and its FFT results. It can be inferred that three waves are transferred on a pair of coils. It should be noted that Fig. 18(c) here shows the coil voltage when the input voltage is 30 V and it is used to demonstrate the components of the wave flowing through the primary coil.

When the output power is 600 W, the waveforms of the power transfer channel and data transfer channel are shown in Fig. 19. The mean value of the output voltage is 54.4 V and the load is 4.85 Ω. As expected, simultaneous full-duplex communication and power transfer are achieved.

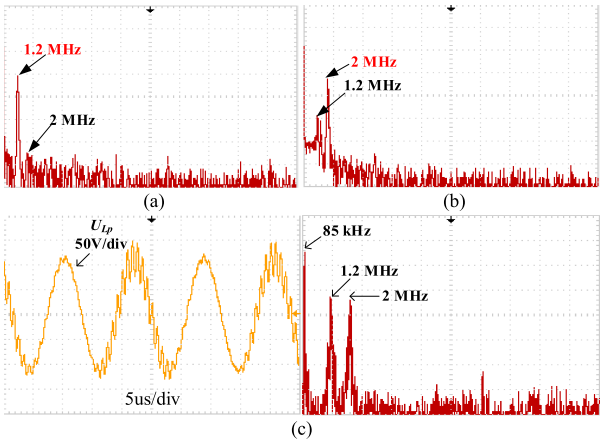

Fig. 18. Simultaneous transfer of the power carrier and data carriers. (a) FFT results of the primary sampling signal U_3. (b) FFT results of the secondary sampling signal U_4. (c) Waveform of the primary coil voltage and its FFT results.

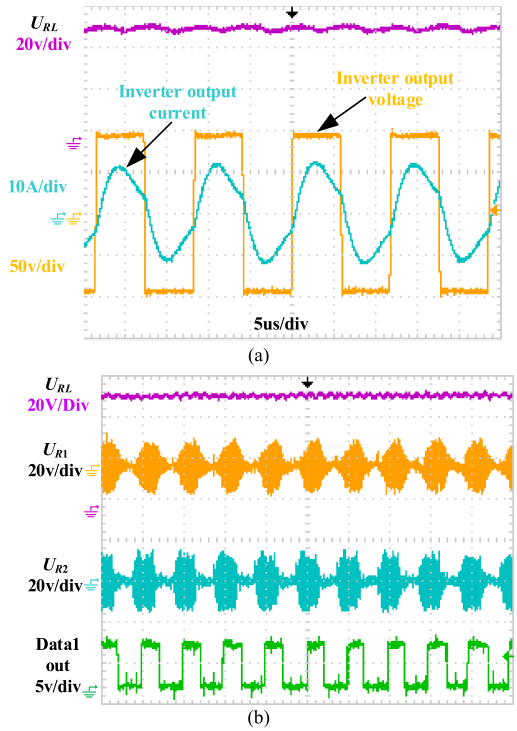

Fig. 19. (a) Waveforms of the power transfer channel and (b) signal waveforms and output voltage when the output power is 600 W and the load is 4.85 Ω.

Fig. 20 shows the dc–dc efficiency of the power transfer channel with/without trappers. When the trappers are added to the power transfer channel, the efficiency of the power transfer channel drops to some extent.

To evaluate the performance of the proposed system, the power losses, including inverter loss, inductor loss, coil loss, trapper loss, and rectifier loss, are measured and the power loss distribution is shown in Fig. 21. It can be known from the figure that the power loss caused by the trappers' accounts for a high proportion because the internal resistances of the inductors of the trappers are relatively high. In the experimental prototype, the internal resistance of each inductor measured at the power carrier frequency reaches 0.1 Ω.

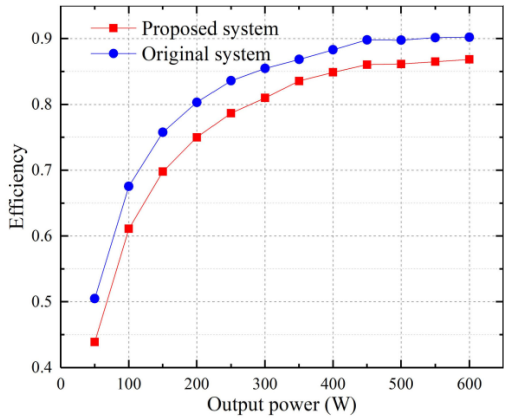

Fig. 20. Efficiency of the power transfer channel.

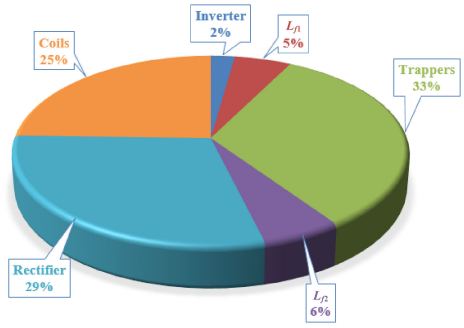

Fig. 21. Power losses distribution.

In the experimental prototype, the two separate trappers depicted in the proposed topology are used to illustrate the operation principles, and the relatively large value of the inductors of the trappers is chosen to realize high impedance to data carriers, which will also increase the internal resistances of the inductors at the power carrier frequency, thus leading to a relatively large reduction in the efficiency. Some measures can be taken to improve the performance of the proposed system, such as parameter optimization, adopting inductors with higher Q value, and parallel dual-rejection trappers. To eliminate the power losses caused by the trappers, the two trappers can also be integrated into coupling coils. However, there will be cross coupling between the coils, which needs to be further analyzed in future research.

VI. Conclusion

A simultaneous full-duplex communication and power transfer method for the WPT systems is proposed in this article and the feasibility of this method is verified by the experiment. The characteristics of serial network and parallel network are utilized to form three independent transfer channels. Two data carriers are modulated by ASK and transferred along with the power carrier via a single coupling interface. Besides, the system performance and crosstalk between the power transfer and data transfer are analyzed in this article. The experimental results indicate that the data can be transferred bidirectionally and simultaneously at a baud rate of 80 kbps. Despite the power loss caused by the trappers added, the method proposed provides a new solution to achieve full-duplex communication for WPT systems.

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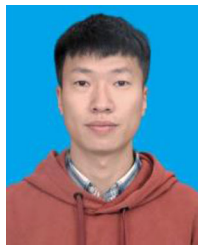

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