Series Synchronized Triple Bias-Flip Circuit: Maximizing the Usage of a Single Storage Capacitor for Piezoelectric Energy Harvesting Enhancement

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***Abstract*—The synchronized multiple bias-flip (SMBF) interface circuits enhance the piezoelectric energy harvesting (PEH) capability by maximizing the extracted energy from the piezoelectric source and simultaneously minimizing the dissipated energy in the power conditioning circuit. They provide the most energy-economic solution for the piezoelectric energy harvesting enhancement. However, the growing scale of the switches network and the increasing number of bias voltages have added much complexity to the circuit design and control. In this article, we reduce the number of passive components to the biggest extent by maximizing the usage of a single capacitor, which simultaneously acts as an energy storage and provides two nonzero bias voltages. Together with the free zero-volt bias, triple bias-flip actions (S3BF) are realized in the new design. Compared with other single-capacitor designs, it makes the best energy harvesting capability so far. Moreover, the proposed series S3BF circuit can automatically shift among single, double, and triple bias-flip operations under heavy-, medium-, and light-load conditions, respectively, which is unprecedented in the previous designs. Theoretical and experimental results show that the harvested power can always follow the maximum power envelope of the single, double, or triple bias-flip operations.**

***Index Terms*—AC–DC conversion, bias-flip, energy harvesting, piezoelectric, vibration.**

I. Introduction

THE number of Internet of Things (IoT) devices will experience an unprecedented growth in the coming decades. The limitations of conventional power supply technologies have attracted more attention. The grid power can run the devices uninterruptedly; yet, the power cable limits the deployment range of the IoT devices. Chemical batteries liberate the devices from cable constraint; yet, the storage capacity of a battery is limited after all. New power supply technologies are beckoned toward the realization of absolute independent, maintenance-free, and everlasting IoT. Energy harvesting technology provides one of the most promising solutions for autonomous everlasting IoT [2]. For example, the moving things can scavenge mechanical kinetic energy by themselves from the surrounding movements and convert it into useful electric power, such that to realize the energy self-sufficiency.

Piezoelectric materials can be made into compact and high-efficiency electromechanical transducers. They have attracted much attention in the research of kinetic energy harvesting. As constitutive parts of a piezoelectric energy harvesting (PEH) system, the power conditioning circuit [3], mechanical structure [4], [5], and transducer [6] play important roles toward a successful engineering design. In particular, in the electrical domain, power electronics provide many possibilities toward the enhancement of the energy harvesting capability [7], [8]. Advanced synchronized switch circuits increase the system-level coupling. As stated by Shu *et al.*, using the synchronized switch circuits, such as the synchronized switch harvesting on inductor (SSHI), could make a weakly coupled system into a strongly coupled one [9]. Improving the circuit capability maximizes the usage of the relatively expensive piezoelectric materials.

The study of the PEH circuit started from the basic full-wave bridge rectifier for the general ac–dc conversion [10], [11], which was later regarded as the benchmark standard energy harvesting (SEH) interface circuit [12]. The improvements started from the synchronized single-switch technology [13]–[18]. The most investigated synchronized switch circuit families include: parallel SSHI (P-SSHI), series SSHI (S-SSHI), and synchronous electric charge extraction (SECE). In the integrated circuit (IC) research community, the SSHI technology was called *bias-flip rectifier* since the early study in 2010 [19]. Some studies considered maximizing the power extraction by enlarging the piezoelectric voltage magnitude according to the Ericsson cycle [20], [21]. Recent IC solutions discussed how to minimize the power dissipation in voltage inversion by dividing it into multiple steps with switched-capacitor array [22]–[25]. On the other hand, it should be noted that the net harvested power is the difference between the extracted power and dissipated power [26], [27]. Some double bias-flip solutions are more rational to make both the two tasks [28]–[30]. The objective function of the harvested power

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was further mathematically formulated in a general synchronized multiple bias-flip (SMBF) model [31]. With the theoretical guidance, parallel synchronized triple (P-S3BF) and septuple (P-S7BF) bias-flip solutions were implemented recently [32], [33]. Compared with the hard-switching active PEH scheme using an ordinary H-bridge [21], the SMBF designs cut down the switching dissipation by enabling the zero-current switching (ZCS) on the inversion inductor.

The aforementioned multiple switch solutions can effectively enhance the PEH capability. However, no matter for the inductorless switched-capacitor IC solutions [22]–[25] or the SMBF solutions [31]–[33], the switch network, and its control logics have become more complex than the well-received SSHI circuits. More auxiliary capacitors are involved as well for offering scheduled dc bias voltages. Given that solid-state switches do not occupy much area in an IC solution, their control can also be integrated easily, the number of passive components is of the biggest concern.

In this article, rather than further complicating the switch network, we take the other way round to simplify the existing P-S3BF network via maximizing the usage of a single external capacitor. Although the harvesting performance is sacrificed a little bit, it is the first time to realize triple bias-flip actions and energy storage in a PEH interface circuit using only one single external capacitor. Section I introduces the technological background and design. Section II discusses the operational principle of the circuit by explaining its working phases and characteristic waveforms. Section III provides a detailed analysis of the energy flow and dynamics of the circuit. Section IV shows some experimental results for validating the new design. Finally, Section V concludes this article.

II. Principle

In the previous double bias-flip (S2BF) designs, the intermediate voltage between two bias-flip actions was preset to zero-volt without a strong reason [28]–[30]. Based on the generalized SMBF model, the optimal bias-flip strategy was mathematically derived [31]. It provides theoretical guidance for the future development of the SMBF circuit family. For example, from the theory, we knew that the optimal intermediate voltage in S2BF is $V_{\rm oc}$ the open-circuit voltage magnitude, rather than zero-volt. The switched-capacitor designs can also be regarded as special cases of the SMBF, in which the flipping factor $\gamma = 0$. No matter for bias-flip or switched-capacitor solutions, according to the optimal bias-flip strategy, the maximum harvested power is obtained when all the voltage steps are equal.

The P-S3BF and P-S7BF circuits were developed by strictly following the optimal bias-flip strategy. Based on two useful observations [32], [33], the implementation of the parallel bias-voltage network was significantly simplified; otherwise, it is impractical to realize many adaptive dc bias voltages in such an energy-constrained scenario. Theoretically speaking, the more complex switched bias-voltage network we use, with proper control, the higher energy harvesting capability we can catch. On the other hand, from a practical point of view, a more complex switched network is very likely to introduce additional overhead, such as switch control, etc. Therefore, a good compromise should be made to balance the number of bias-flip actions and the scale of the switched bias-voltage network. Such task can be realized by maximizing the usage of the existing passive components in the bias-flip interface circuit.

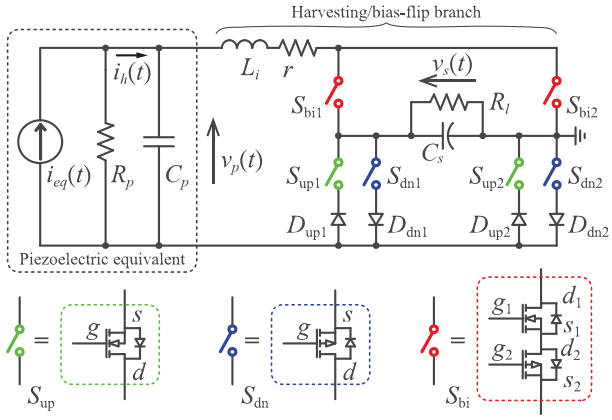

Fig. 1. S-S3BF circuit topology.

A. Circuit Topology

In P-S3BF, the interface circuit is divided into two branches. One for carrying out bias-flip actions, while the other for ac–dc conversion, i.e., energy harvesting. In the previous S2BF designs, the bias voltage was preset by an external dc voltage source [29]. Owning to the current steering network in the S3BF design, the bias voltage is self-adaptive, and therefore, can be realized by simply using a normal capacitor [32]. Given the self-adaptability, i.e., self-charging and self-discharging capability, of the bias voltage source in P-S3BF, it is possible to remove the harvesting branch in P-S3BF and merge both the bias-flip and energy harvesting functions into a single branch toward a new circuit topology. As there were already some multiple switches derivatives of P-SSHI [32], [33] and SECE [34], there should be a multiple switches version for another extensively studied PEH interface circuit family, i.e., S-SSHI. The new circuit proposed in this article fills this gap. It is the multiple switches version of S-SSHI and also the series version of S3BF (S-S3BF). Comparing P-S3BF, S-S3BF, and multishot SECE (MS-SECE) [34], although they are all multiple switches PEH interface circuits, their switching actions are different. P-S3BF and S-S3BF use bias-flip actions, which are the same as P-SSHI and S-SSHI did. On the other hand, MS-SECE uses charge extraction, which is the same as the conventional SECE did. Therefore, we should refer to S-SSHI, rather than SECE, as a closer corresponding technique of S-S3BF.

The circuit topology of S-S3BF is shown in Fig. 1. The equivalent current source $i_{\rm eq}$, the piezoelectric clamped capacitance C_p, and dielectric leakage resistance R_p form the piezoelectric equivalent. Inductor L_i, whose parasitic resistance is r, and C_p form an underdamped *RLC* circuit for carrying out voltage flipping actions. The current steering network is the key point for establishing the stable triple bias-flip actions. It is formed by two bidirectional switch $S_{{\rm bi}x}$ ($x = 1, 2$) in red in Fig. 1, and four current-directing branches (two $S_{{\rm up}x}$ in green for upward current only and two $S_{{\rm dn}x}$ in blue for downward current only).

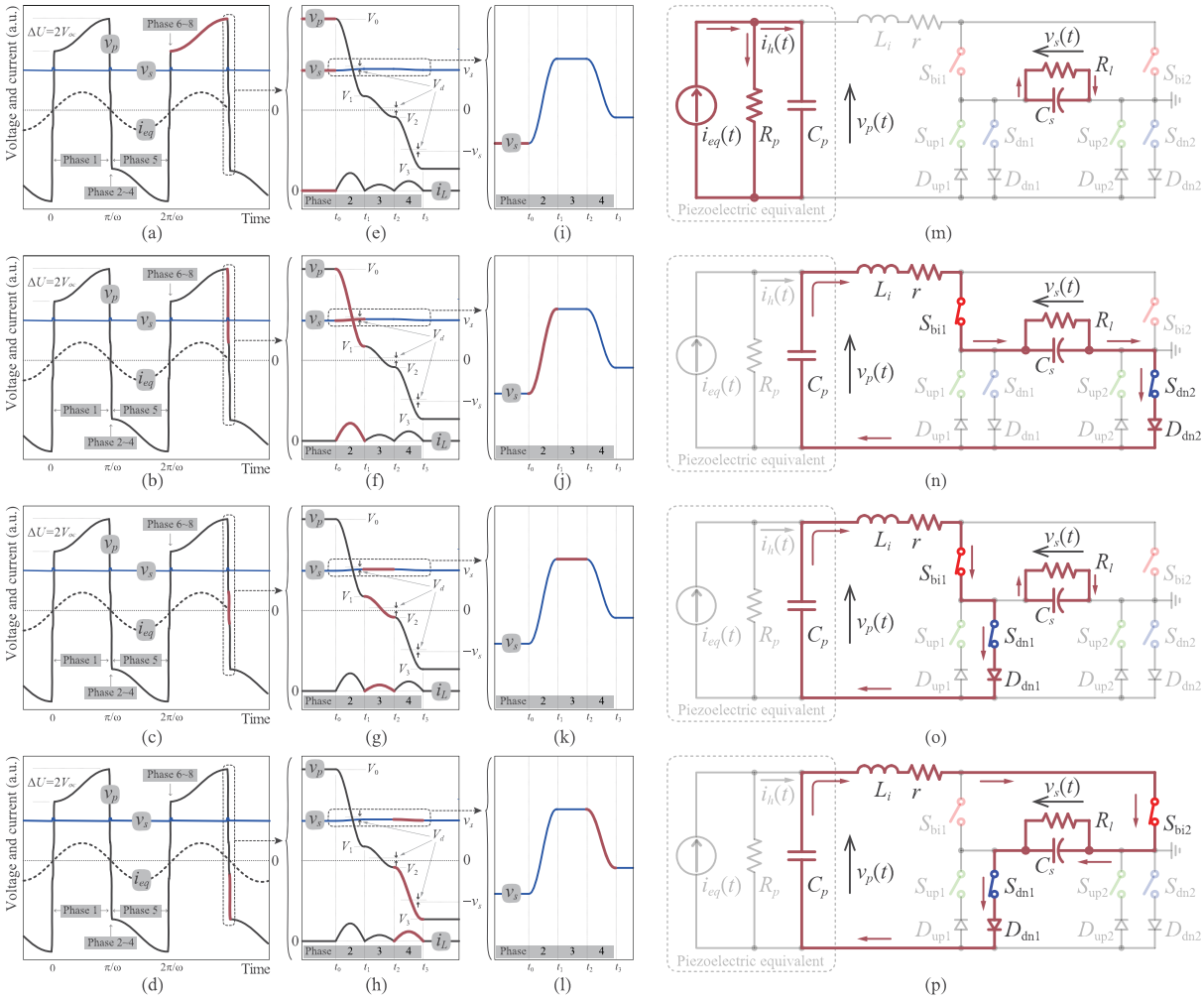

Fig. 2. Four working phases of S-S3BF in half of a vibration cycle including the downstairs bias-flip actions. (a)–(d) Operation waveforms. (e)–(h) Enlarged view at a synchronized switch instant. (i)–(l) Enlarged view of the change of the storage voltage v_s at a synchronized switch instant. (m)–(p) Active circuit branch. (a), (e), (i), and (m) Phase 1: Open circuit. (b), (f), (j), and (n) Phase 2: The first bias-flip action. (c), (g), (k), and (o) Phase 3: The second bias-flip action. (d), (h), (l), and (p) Phase 4: The third bias-flip action.

There is only one external capacitor C_s in the S-S3BF circuit. C_s not only acts as an energy storage, but also simultaneously provide two dc voltage references,[1] i.e., $\pm v_s$, for the first and third bias-flip actions.[2] R_l in parallel with C_s represents the dc load.

Compared with the previous H-bridge design for "active PEH" [21], the bias-flip design in SMBF realizes the zero-current switching (ZCS) for i_L current flowing through L_i at t_1, t_2, and t_3 instants, as shown in Fig. 2(f), (g), and (a)–(h), respectively. The switch dissipation for realizing the same instantaneous piezoelectric voltage change, therefore, is minimized. Compared with the previous version of S3BF implementation [32], the current steering network in this design is further refined. This design can be rationally extended to more bias-flip cases [33].

[1]The voltage bias-flip action was also called voltage inversion in some literature [13], [14]

[2]The value of the storage capacitor C_s is designed much larger than the piezoelectric capacitance C_p. Therefore, v_s across C_s can be regarded as a constant dc voltage.

B. Working Principle

When using S-S3BF, every vibration cycle can be divided into eight phases, two open-circuit phases (phases 1 and 5) and six bias-flip phases (phases 2–4 and 6–8), respectively. The detailed operation waveform and conducting branches of S-S3BF under different phases are illustrated in Fig. 2. As shown in Fig. 2(a)–(d), the outer profile of v_p in S-S3BF looks similar to that in S-SSHI with strong synchronized voltage inversions [35], except that there are three bias-flip actions instead of one in S-SSHI. By properly carrying out more bias-flip actions, the magnitude of v_p gets larger, such that the input power, as the product of the piezoelectric voltage v_p and equivalent voltage i_{eq}, becomes higher [32]. The voltage and current details during a synchronized voltage downstairs instant are magnified and shown in Fig. 2(e)–(h). The bias voltages of the three bias-flip actions in phases 2–4 are $V_s + V_d$, V_d, and $-V_s + V_d$, respectively, where V_s is the approximate constant of v_s, and V_d is the forward voltage drop of a diode. The intermediate voltages of v_p during the three bias-flip actions are denoted as V_0–V_3, respectively, as

TABLE I
OPERATION MODES AND EFFECTIVE FLIPPING FACTORS

Operation mode	Valid BF action	Effective flipping factor
S1BF	1^{st}	$\gamma_1 = \gamma$, $\gamma_2 = \gamma_3 = 1$
S2BF	1^{st}, 3^{rd}	$\gamma_1 = \gamma_3 = \gamma$, $\gamma_2 = 1$
S3BF	1^{st}, 2^{nd}, 3^{rd}	$\gamma_1 = \gamma_2 = \gamma_3 = \gamma$

γ is the actual flipping factor, which equals to $-e^{-\pi/(2Q)}$. $Q = \sqrt{L_i/r^2 C_p}$ is the quality factor of the $L_i C_p$ circuit loop. Unit flipping factor means that the corresponding bias-flip action is muted.

shown in Fig. 2(a)–(d). The actions in the synchronized voltage upstairs instant use the symmetric components in the circuit, where the bias voltage in phases 6–8 are $-V_s - V_d$, $-V_d$, and $V_s - V_d$, respectively.

In every synchronized instant of P-S3BF, there are three bias-flip actions, whose strokes, i.e., voltage changes in half of a $L_i C_p$ cycle, have the same length under steady state [32]. In S-S3BF, the number of three bias-flip actions remains the same; however, their strokes are in different length under a steady-state operation. The first bias-flip action extracts energy from C_p and pumps a part of the extracted energy into C_s (the rest is dissipated due to the underdamped bias-flip action). The second one only flips the voltage across C_p. C_s is energy neutral during this bias-flip action. The third one reversely extracts energy from C_s and injects part of the extracted energy back to C_p. The energy extraction and injection are controlled in a proper order by the current-directing diodes D_{upx} and D_{dnx}. The corresponding bias-flip action will be automatically muted if the current flow is not in the desired direction. The adaptability of the S3BF design was explained in detail in our previous paper [32]. For working at the S3BF mode, the system has to go through S1BF and S2BF modes transiently. The valid BF actions and effective flipping factors of the three operation modes are summarized in Table I. We denote the flipping factors of the three bias-flip actions as γ_1–γ_3. When any of them is assigned to γ, flipping factor of the r-L_i-C_p loop, it means the corresponding bias-flip action is valid; when assigned to one, it means the corresponding action is muted.

C. Steady-State Operations

In P-S3BF, C_s only acts as the bias voltage source, and it is energy neutral under steady-state operation, i.e., the energy income and expense of the first and third bias-flip actions are the same; therefore, the strokes of every bias-actions will be eventually equalized. In S-S3BF, because C_s simultaneously acts as an energy storage to power the dc load in every vibration cycle, an additional storage-to-load energy expense must be taken into consideration. Therefore, in S-S3BF, the energy income from the piezoelectric source must be larger than the reverse energy injection, such that to make ends meet.

Given the energy balance among energy extraction (from piezosource), reverse energy injection (to the piezo-source), and energy consumption by the dc load, after the charging transient, the storage voltage v_s is stabilized at S1BF, S2BF, or S3BF zones under heavy (small R_l), medium, or light (large R_l) load conditions, respectively. The charging profiles under the three load conditions are illustrated in Fig. 3. From the enlarged views

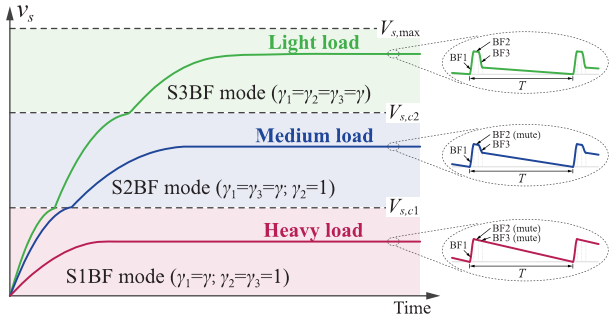

Fig. 3. Charging profiles of storage/bias voltage v_s under three different loading conditions.

of the steady-state v_s, we can get some ideas about the income and expense under different load conditions. Among the aforementioned three working zones, there are two critical storage voltages $V_{s,c1}$, and $V_{s,c2}$, as shown in Fig. 3. Their values are related to transient mode switches as well as steady-state critical load conditions. The formulas will be provided in Section III.

III. ANALYSIS

To formulate the dynamics of the S-S3BF circuit as well as to theoretically quantify the harvested power, we follow the established procedures of the equivalent impedance modeling. The analysis can be carried out by three steps: first, to clarify the energy flow relation by studying the energy cycle [27]; second, to figure out the equivalent impedance of the specific circuit according to the relation between current and voltage fundamental harmonics [12]; and finally, substitute the circuit equivalent impedance into the system impedance network and get the power result.

A. Energy Cycle

The partitioned hysteric charge $q(t)$ versus voltage $v_p(t)$ diagram under the steady-state operation gives an intuitive description of the energy flow in a vibration cycle. It was called *work cycle* or *energy cycle* in literature. The energy cycles of S1BF, S2BF, and S3BF operations are shown in Fig. 4. The q–v_p trajectory is composed of two segments, the dot lines with a slope of C_p^{-1} and the upright solid lines. The area enclosed by the q–v_p trajectory corresponds to the extracted energy from the equivalent current source i_{eq} in one cycle. The enclosed area is divided into three parts in different colors. The blue triangles represent the energy dissipated during the corresponding underdamped bias-flip actions due to a finite quality factor Q of the r–L_i–C_p loop. The red parallelograms represent the energy dissipated in the current steering diodes due to their forward voltage drops. The rest area in green represents the net harvested energy. In S1BF operation, i.e., S-SSHI, there is only one dissipative triangle in each half of a vibration cycle. In the S2BF operation, there are two dissipative triangles. However, different from the previous S2BF solutions [28], [29], the second intermediate voltage V_1 is not preset at any value here. The S3BF operation with three dissipative triangles is achieved under a light-load condition, as shown in Fig. 4(c). These three cases are special examples of the S-SMBF generalization [31]. A quick

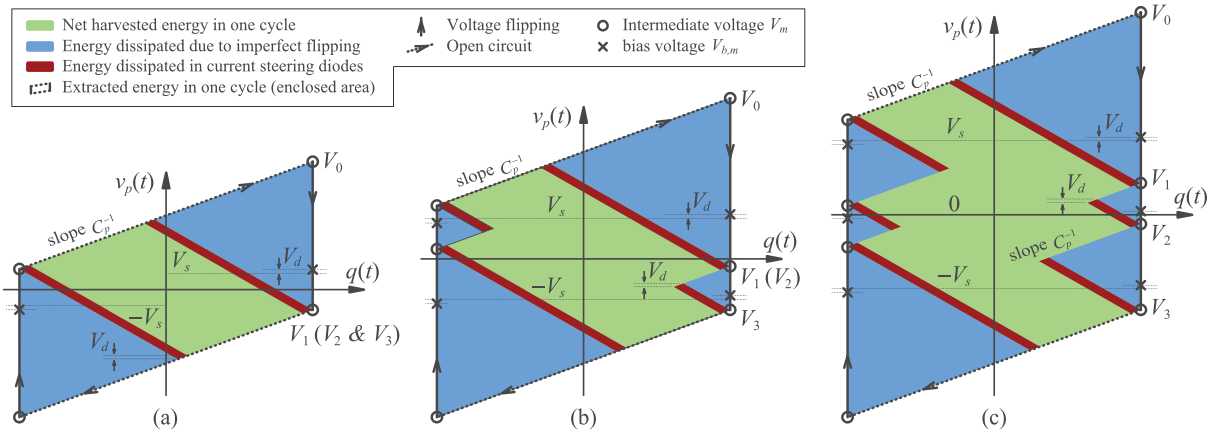

Fig. 4. Energy cycles under three steady-state modes. (a) S1BF (heavy load). (b) S2BF (medium load). (c) S3BF (light load).

qualitative conclusion can be drawn that, in order to enlarge the green area (harvested energy), we have to simultaneously increase the enclosed area (extracted energy) and reduce the sum area in blue and red (dissipated energy).

B. Voltage, Energy, and Harvesting Capability

To quantify the dynamic contribution of different energy flows, we derive their corresponding equivalent impedance. The equivalent impedance model of the C_p and interface circuit combination is derived according to the relation between the voltage v_p and current i_h. The derivation is based on two assumptions.

1) The through current i_h is regarded as a pure harmonic function.
2) For the across voltage v_p, the dynamic influence of its higher order harmonics is much weaker than that of its fundamental harmonic; therefore, it can be neglected.

Base on the first assumption, the input current is formulated as follows:

$$i_h(t) = I_h \sin(\omega t) \tag{1}$$

where I_h is the magnitude of $i_h(t)$, and ω is the vibration frequency. Given that the bias-flip actions happen almost instantaneously compared with a mechanical vibration cycle, the across voltage v_p can be formulated with a piecewise equation as follows:

$$v_p(t) = \begin{cases} V_{\text{oc}}\left[1-\cos(\omega t)\right] - V_3, & 0^+ \le \omega t \le \pi^- \\ V_3 - V_{\text{oc}}\left[1+\cos(\omega t)\right], & \pi^+ \le \omega t \le 2\pi^- \end{cases} \tag{2}$$

where $V_{\text{oc}} = I_h/(\omega Cp)$ is the nominal open-circuit voltage. V_3 is the end voltage of the third bias-flip actions in the downstairs instant. Given the inversion factors in the three bias-flip actions as γ_1, γ_2, and γ_3, the bias voltages in the three actions as $V_s + V_d$, V_d, and $-V_s + V_d$, the intermediate voltages can be formulated according to the following linear relation:

$$\begin{bmatrix} 1 & 0 & 0 & 1 \\ \gamma_1 & -1 & 0 & 0 \\ 0 & \gamma_2 & -1 & 0 \\ 0 & 0 & \gamma_3 & -1 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 2V_{\text{oc}} \\ (\gamma_1 - 1)V_{b,1} \\ (\gamma_2 - 1)V_{b,2} \\ (\gamma_3 - 1)V_{b,3} \end{bmatrix} \tag{3}$$

where $V_{b,m}$ is the bias voltage of the mth bias-flip action. In S-S3BF, $V_{b,1} = V_s + V_d$, $V_{b,2} = V_d$, and $V_{b,3} = V_d - V_s$, respectively. The expressions of V_0–V_3 can be obtained by solving the linear equation (3). Given that, in most cases, $V_d \ll V_{\text{oc}}$, therefore, V_d can be neglected, Fig. 5(a) shows the four intermediate voltages $\tilde{V}_m$ and three bias voltages $\tilde{V}_{b,m}$ under different storage voltage $\tilde{V}_s$ (all voltages are nondimensionalized by dividing V_{oc}) when the flipping factor $\gamma = -0.5$. The figure can be divided into three zones according to the $\tilde{V}_s$ value: S1BF zone in light red background, S2BF zone in light blue, and S3BF in light green, as shown in Fig. 5(a). The values of γ_1–γ_3 depend on the operation modes as listed in Table I. The transition details between the three modes were described in [32]. At the critical point between S1BF and S2BF, an additional relation $V_1 = V_2 = V_3 = -V_s + V_d$ holds. Substituting it into (3), we have the first critical storage voltage as follows:

$$V_{s,c1} = \gamma\left(V_d - V_{\text{oc}}\right). \tag{4}$$

At the second critical point between S2BF and S3BF, another relation $V_1 = V_2 = V_d$ holds. Substituting it into (3), we have the second critical storage voltage as follows:

$$V_{s,c2} = \frac{2\gamma}{1-\gamma^2}\left(V_d - V_{\text{oc}}\right). \tag{5}$$

Maximum V_s attains at zero-load condition ($R_l = \infty$). Without load energy consumption, under steady-state, the energy income in the first bias-flip action equals to the expenditure in the third bias-flip action; therefore, we have $V_0 - V_1 = V_2 - V_3$. Substituting this condition into (3), the maximum attainable V_s can be solved as follows:

$$V_{s,\max} = 2\frac{\gamma - 1}{\gamma + 1}\left(V_d - V_{\text{oc}}\right). \tag{6}$$

The three critical storage voltages divide the load conditions into three zones, as shown in Figs. 3 and 5(a)–(c).

From Fig. 4, the total extracted energy in one cycle corresponds to the area enclosed by the q–v_p trajectory, which can be formulated as follows:

$$\Delta E = 2C_p V_{\text{oc}}\left(V_0 - V_3\right). \tag{7}$$

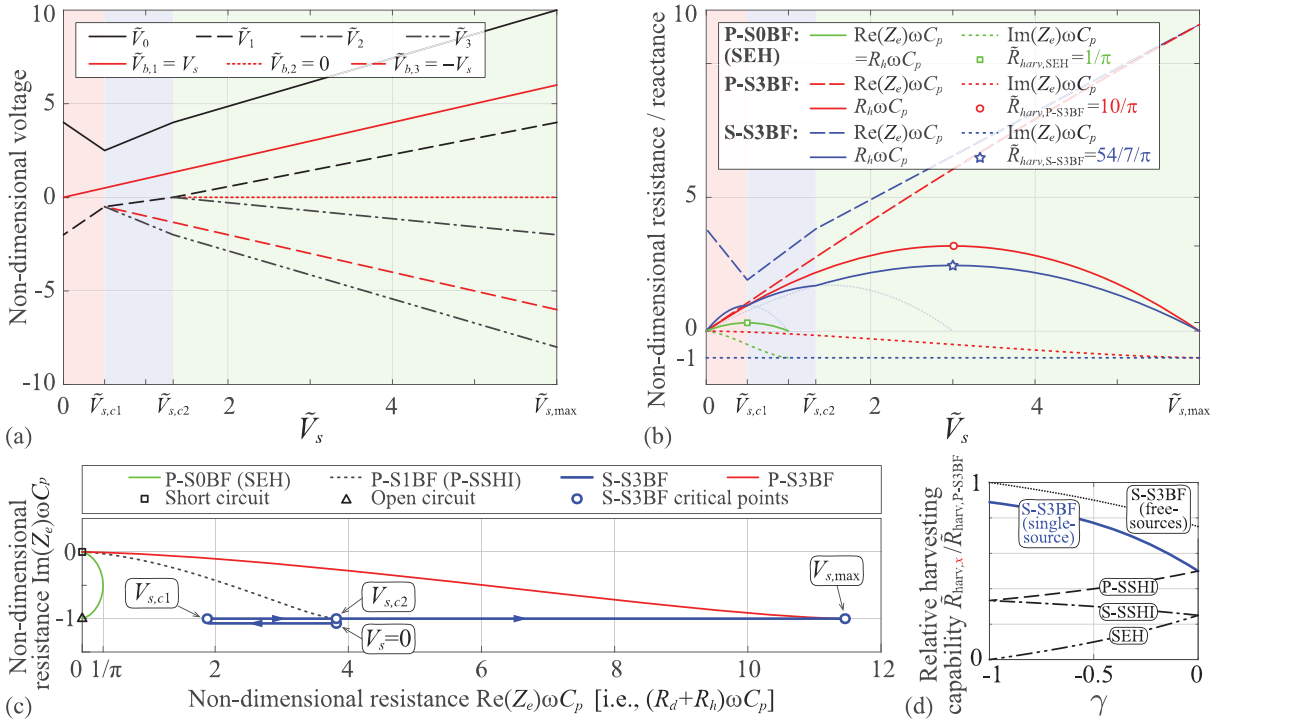

Fig. 5. Features of S-S3BF ($\gamma = -0.5$). (a) Intermediate and bias voltages. (b) Equivalent resistance and reactance as functions of the nondimensional storage voltage $\tilde{V}_s$. (c) Equivalent impedance on the normalized complex impedance plane. (d) Relative harvesting capability compared with P-S3BF.

The dissipated energy in the power conditioning can be divided into two parts. The first part is energy dissipated in the underdamped r-L_i-C_p branch during the bias-flip actions, i.e., the blue triangles in Fig. 4, which can be formulated as follows:

$$E_{d,\text{flipping}} = \sum_{m=1}^{3} C_p(1-\gamma_m^2)\left(V_{m-1}-V_{b,m}\right)^2. \tag{8}$$

The second part dissipation is consumed by the steering diodes during all bias-flip actions, i.e., the red parallelograms in Fig. 4, which can be formulated as follows:

$$\begin{aligned} E_{d,\text{steering}} &= 2\sum_{m=1}^{3} C_p\left(V_{m-1}-V_m\right)V_d \\ &= 2C_p\left(V_0-V_3\right)V_d. \end{aligned} \tag{9}$$

The total dissipated energy in each cycle can be formulated as sum of the two parts

$$E_d = E_{d,\text{flipping}} + E_{d,\text{steering}}. \tag{10}$$

According to the energy flow analysis of the PEH system [27], the net harvested energy in one cycle, i.e., the green area in Fig. 4, is the difference between energy extraction and dissipation, which is expressed as follows:

$$E_h = \Delta E - E_d = 2C_p\left[(V_0-V_1)-(V_2-V_3)\right]V_s. \tag{11}$$

E_h can also be formulated as a double of the difference between energy income during the first bias-flip action $\Delta Q_{\text{BF1}}V_s = C_p(V_0-V_1)V_s$, and energy expenditure during the third bias-flip action $\Delta Q_{\text{BF3}}V_s = C_p(V_2-V_3)V_s$, as given in (11). Given a constant V_{oc}, at the S3BF mode, E_h obtained its maximum value

$$E_{h,\max} = 2C_p(V_{\text{oc}}-V_d)^2\frac{(1-\gamma)^3}{1+\gamma^3} \tag{12}$$

under the optimal storage voltage

$$V_{s,\text{opt}} = (V_{\text{oc}}-V_d)\frac{1-\gamma}{1+\gamma}. \tag{13}$$

Neglecting the effect of the diode voltage drop V_d and according to the definition given in [31], the *harvesting capability* of the S-S3BF circuit can be formulated as follows:

$$\tilde{R}_{\text{harv,S-S3BF}} = \frac{E_{h,\max}}{\pi C_p V_{\text{oc}}^2} = \frac{2(1-\gamma)^3}{1+\gamma^3}. \tag{14}$$

Fig. 5(d) shows the relative harvesting capability of some representative bias-flip solutions by normalized their harvesting capability $\tilde{R}_{\text{harv},x}$ (subscript x stands for any specific solution) to that of P-S3BF $\tilde{R}_{\text{harv,P-S3BF}}$ under different flipping factor γ. It was mathematically proven that P-SMBF is the most capable solution when using M bias voltages [31]. From Fig. 5(d), the single-source S-S3BF introduced in this article outperforms the extensively studied SEH, P-SSHI, and S-SSHI solutions. It is not as good as the P-S3BF solution. For example, when $\gamma = -0.5$, the harvesting capability of the single-source S-S3BF is 54/70 of that of P-S3BF, as shown in Fig. 5(b). Therefore, from P-S3BF [32] to the single-source S-S3BF, the harvesting performance is sacrificed toward a simpler configuration. On the other hand, theoretically speaking, the harvesting capability of S-S3BF can be increased a little bit by removing the

single-source constraint, i.e., realizing the free-sources S-S3BF, as shown by the dot line in Fig. 5(d). However, the free-sources solution is difficult to implement, it only shows the ideal case of a general S-S3BF solution.

C. Impedance Modeling

To understand the dynamics of the S-S3BF interface circuit, we study the magnitude and phase relations between the fundamental harmonic of v_p and the sinusoidal i_h, in terms of equivalent impedance [12]

$$Z_e(j\omega) = \frac{V_{p,f}(j\omega)}{I_h(j\omega)} = \frac{4}{\pi}\frac{1-\tilde{V}_3}{\omega C_p} - \frac{j}{\omega C_p} \tag{15}$$

where $\tilde{V}_3 = V_3/V_{\rm oc}$ is nondimensionalized V_3. As we can observe from (15), the imaginary component of Z_e in S-S3BF $-j/(\omega C_p)$ is a constant, which equals to the impedance of the piezoelectric capacitance C_p, i.e., under open-circuit condition. The real part equals to that of the fundamental component of a square wave $\text{sgn}[i_h(t)](1-\tilde{V}_3)/(\omega C_p)$. Since the extracted energy is divided into two parts, harvested and dissipated energies, the real part of Z_e is composed of two portions: the dissipative resistance and harvesting resistance, which can be formulated as follows:

$$R_d = \frac{E_d}{\Delta E}\text{Re}(Z_e), \qquad R_h = \frac{E_h}{\Delta E}\text{Re}(Z_e). \tag{16}$$

Fig. 5(c) shows the picture of steady-state Z_e of different circuit solutions in the normalized complex impedance plane. The open-circuit reactance $1/(\omega C_p)$ is taken as a baseline of the equivalent impedance in all cases. From the figure, we can observe that the electrical impedance in S-S3BF moves along the S-S1BF (S-SSHI) trajectory to the left at first when $V_s \in [0, V_{s,c1})$. It shifts to the S-S2BF trajectory to the right when $V_s \in [V_{s,c1}, V_{s,c2})$. After $V_{s,c2}$, the impedance follows the S-S3BF trajectory until V_s arrives at $V_{s,\max}$. The largest end point of S-S3BF is the same as that of P-S3BF. The real part of Z_e is composed of two components: dissipative R_d and harvesting R_h, whose details cannot be shown in the complex impedance plane. Fig. 5(b) shows the harvesting performance, in terms of $R_h\omega C_p$, and the damping performance, in terms of $\text{Re}(Z_e)\omega C_p$, i.e., $(R_d + R_h)\omega C_p$ of three representative circuits. The $R_h\omega C_p$ curve of S-S3BF (blue solid) is obtained as the envelop of those curves under S1BF, S2BF, and S3BF modes. From the three solid lines in different colors, it shows that both P-S3BF (red) and S-S3BF (blue) have a much higher harvesting capability (maximum R_h) compared with SEH solution (green). S-S3BF is a little less capable than P-S3BF. On the other hand, S-S3BF gives the maximum damping effect under different storage voltage. It implies that, compared with P-S3BF, S-S3BF sends more extracted mechanical energy into heat, while turns less into useful electricity, which once again proves that S-S3BF makes the simplicity at the cost of sacrificing the harvesting capability.

The *harvesting capability*, which was coined in [31] is a figure of merit (FOM) describing the maximum attainable harvesting resistance of the C_p and interface circuit combination. It provides an intuitive index for the comparison among performances of different interface circuits. It must be pointed out that, the harvesting capability is an FOM purely related to the circuit design. It is not proportional to the harvested power. The harvested power is also influenced by the mechanical dynamics and dielectric properties [36]. The harvested power P_h is formulated as the power absorbed by R_h in the equivalent impedance network under a specific excitation condition. For example, under the constant beam deflection magnitude, $I_{\rm eq}$ is constant. The harvested power under this excitation can be formulated as follows:

$$P_{h,\text{const}X} = \frac{I_{\rm eq}^2 R_h}{2}\left|\frac{R_p}{R_p + Z_e}\right|^2. \tag{17}$$

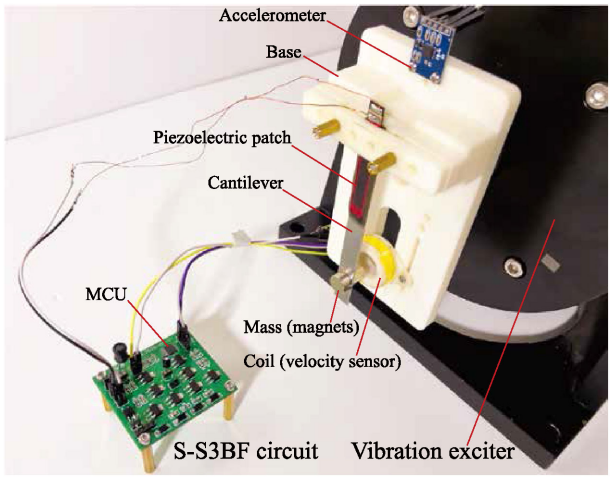

Fig. 6. Experimental setup.

IV. Experiment

In order to validate the working principle and energy harvesting ability of the proposed S-S3BF circuit, two experiments are carried out. The first experiment illustrates the working principle of S-S3BF, including the charging profiles of the storage/bias capacitor C_s and the self-adaptive shifts among single, double, and triple bias-flip operations under heavy-, medium-, and light-load conditions. The second experiment validates the harvested power performance of the S-S3BF interface circuit.

A. Setup

The experimental setup is shown in Fig. 6. The corresponding specifications are listed in Table II. A magnet is fixed at the free end of the cantilevered beam as a tip mass. The piezoelectric patch is connected to the S-S3BF interface circuit. The base vibration is provided by a vibration shaker (KDJ-20). A laser vibrometer (Polytec OFV-552/5000) provides displacement reference for maintaining a constant beam deflection magnitude. In order to generate the synchronized switch control for the S-S3BF interface circuit, a coil is used as an electromagnetic (EM) sensor. It is installed near the free-end magnet for sensing the relative velocity between the cantilever beam and the vibrating base. A low-pass filter is connected between the EM sensor and the microcontroller for filtering the noise from the sensor. Because the voltage is proportional to the equivalent current $i_{\rm eq}$,

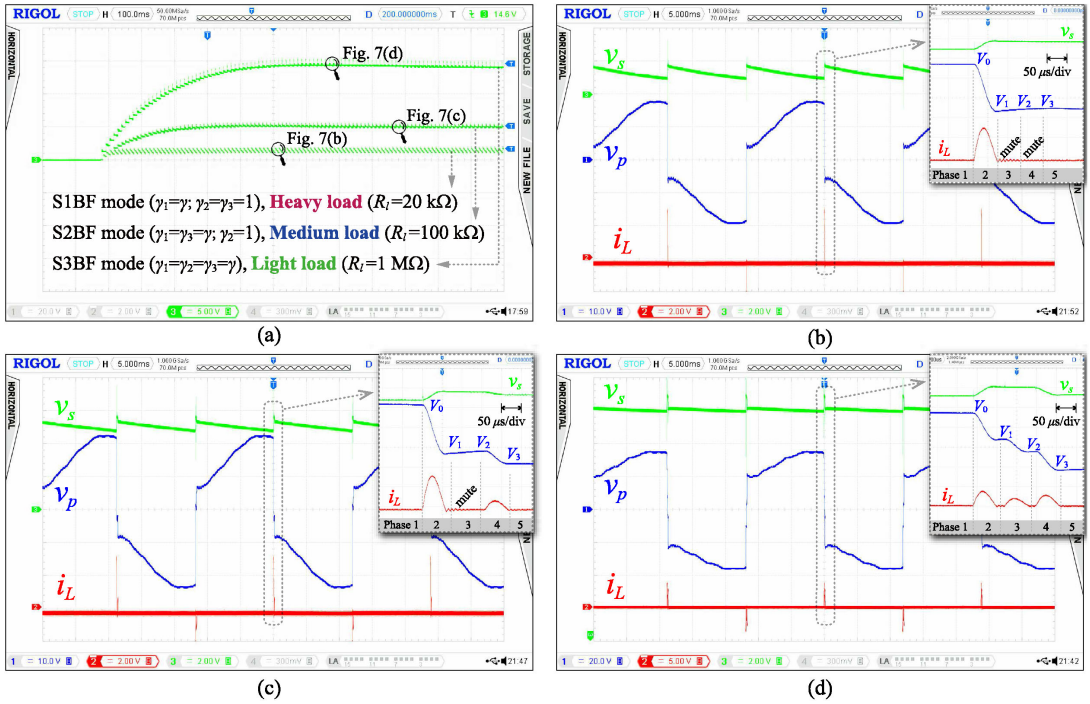

Fig. 7. Charging profiles and operating waveform under three different loading conditions. (a) Charging profiles of the storage/bias voltage v_s. (b) Heavy-load condition (S1BF mode). (c) Medium-load condition (S2BF mode). (d) Light-load condition (S3BF mode).

TABLE II
PARAMETERS IN EXPERIMENT

Parameter	Value
Piezoelectric patch (PZT)	50×7.2×0.84 (mm^3)
Cantilever (aluminum)	100×10×1.5 (mm^3)
C_p	32.16 nF
L_i	10 mH
C_s	1 μF
ω	$2\pi \times 42$ Hz
γ	-0.38
R_p	1.91 MΩ
V_{oc}	5.5 V
MOSFETs	ZVN(P)4424GTA
Diodes	SS16 ($V_d = 0.51V$)

this EM output signal can be used to generate interrupt signals at i_{eq} zero-crossing instants. Once a synchronized interrupt is caught, a microcontroller (MSP430G2553) drives the MOSFET switches to carry out the corresponding synchronized bias-flip actions. The microcontroller currently is powered by external batteries. Since S-S3BF has the same switching sequence as P-S3BF does, the power overhead of the switching actions is the same as that measured in [25], about 24 μW, which is lower than the harvested power. The implementation in this experiment is not an end product with a self-powered capability yet; we focus on the topology and functionality of S-S3BF first.

B. Charging Performance

The charging profiles and experimental waveform corresponding to heavy-load, medium-load, and light-load conditions of the S-S3BF interface circuit are shown in Fig. 7. As mentioned in Section II, the S-S3BF circuit operates at the S1BF mode under a heavy-load condition (small R_l), where only the first bias-flip action is activated, as shown in Fig. 7(b). At the current zero-crossing point, the corresponding conducting path opens an outlet to the charge stored in C_p so that the charge rapidly flows through the inductor L_i and the storage/bias capacitor C_s. C_s is selected much larger than C_p; therefore, it provides an almost constant bias voltage $V_s + V_d$ for the bias flip. After half of the L_iC_p cycle, the piezoelectric voltage v_p changes from V_0 to V_1. As there must be a current steering diode in any bias-flip conducting branch, the current can only flow through the clockwise direction at the downstairs instants, as shown in Fig. 2(n)–(p). Therefore, the second and third bias flip actions are muted, i.e., $\gamma_2 = \gamma_3 = 1$. v_p stops at V_1 after the first bias-flip action. After those actions, v_s drops quickly due to the heavy-load condition. It can be smoothed by selecting a larger C_s.

When the load resistance gets larger into the medium-load zone, the S-S3BF circuit operates at S2BF mode. In this load zone, the first and third bias-flip actions are activated, as shown in Fig. 7(c). At the current zero-crossing point, as we can observe from the enlarged view, the inductor current i_L has two peaks, which correspond to the first and third bias-flip actions. The second bias-flip action is still muted, i.e., $\gamma_2 = 1$. During the bias-flip actions, the storage/bias capacitor C_s is first charged in the first bias-flip action, then discharged in the third bias-flip action. Energy backward injection helps increase the magnitude of the piezoelectric voltage v_p, and hence, the extracted energy. After the synchronized period, v_s drops moderately due to the medium-load condition.

When the load resistance continues to increase and reach a light-load condition (large R_l), the S-S3BF circuit enters the

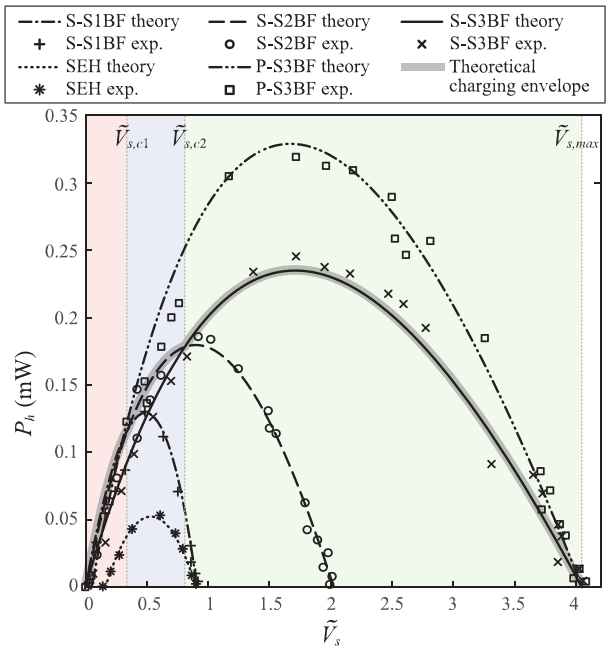

Fig. 8. Harvested power versus the nondimensional storage voltage $\tilde{V}_s$.

S3BF mode. In this mode, all bias-flip actions are activated, as shown in Fig. 7(d). At the current zero-crossing point, the inductor current i_L has three peaks, which correspond to the three bias-flip actions. The v_s levels after the first charge and the third discharge bias flips get closer under the light-load condition. They become equal in the zero-load open-circuit condition, i.e., C_s is energy neutral. During the bias-flip actions, the piezoelectric voltage v_p steps down from V_0 to V_3, further enlarging the voltage amplitude under the same piezoelectric current i_{eq}. Therefore the harvested power becomes larger compared with S1BF and S2BF modes. After the synchronized period, v_s drops slowly because of the light-load condition.

C. Harvested Power

Fig. 8 compares the harvested power as functions of the normalized rectified voltage V_s with different interface circuits, such as SEH, S-S3BF, and P-S3BF. The experimental results show a good agreement with the theoretical prediction. Comparing the maximum harvested powers in the three modes of S-S3BF and the conventional SEH solutions, we can observe that the S-S3BF outperforms the extensively studied SEH solution, as well as its S-S1BF (S-SSHI), and S-S2BF modes. With the prototyped piezoelectric structure in use, the ratios of the maximum harvested powers in P-S3BF, S-S3BF, S-S2BF, S-S1BF, and SEH are $6.25 : 4.47 : 3.42 : 2.46 : 1$. The ratios of the maximum attainable $\tilde{v}_s$ in S-S3BF, S-S2BF, and S-S1BF are $4.45 : 2.23 : 1$. The actual charging process follows the power envelope, which is shown by the bold gray line in Fig. 8. The working modes automatically shift during charging. The power curve follows the maximum power envelope of the three working modes.

V. Conclusion

This article introduced the series triple bias-flip (S-S3BF) interface circuit for the PEH. S-S3BF explored the maximum potential of a single storage capacitor toward a better energy harvesting capability. The single storage capacitor is multifunctional. It serves as an energy storage and provides bias voltages for two different bias-flip actions as well ($\pm V_s$). Combining with the free zero-volt bias voltage, three bias-flip actions were successfully achieved with the sophisticated switching network and control. Both theoretical and experimental results have shown that S-S3BF can effectively increase the harvested power under the same vibration magnitude. Compared with the previously proposed parallel-S3BF interface circuits, S-S3BF realizes the simplification by making a little scarification in harvesting capability. The special automatic mode-shifting feature of our S-S3BF implementation under heavy-, medium-, and light-load conditions was also analyzed in detail. The S-S3BF design offers one of the most concise and robust energy-investing or injecting schemes so far for the piezoelectric energy harvesting enhancement.

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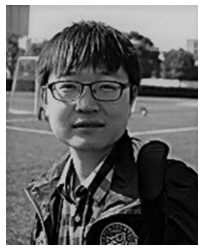

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