Operational Limits of a Cascaded Dual-Output Multilevel Converter Using Model Predictive Control

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***Abstract*—This article proposes a modified cascaded dual-output multilevel converter with a reduced number of power switches. The proposed converter can provide independent multilevel voltages across its dual-output ports, which makes it distinct when compared with the existing topologies. The mathematical model of the converter is developed for two converter cells with two output ports and is incorporated in a finite control set model predictive control algorithm for controlling the dual-output currents. Due to an inherent restriction, the converter output ports can operate independently, only during certain operating conditions. Therefore, converter operational limits in terms of voltage amplitude range are investigated for its output ports operating under various modes, such as different amplitude, different frequency, and different phase angle. The developed model is simulated for all these modes, and the operational limits of the proposed converter are obtained based on the distorted output currents. The effects of unequal dc source voltages on the operational limits are also analyzed. The determined operational limits ensure that the converter output ports operate independently without any current distortion and guarantee a safe operation. Finally, the operation of the proposed converter under different operating conditions is validated using simulation and experimental results.**

***Index Terms*—Dual-output converter, finite control set model predictive control (FCS-MPC), multilevel converter, operational limits.**

I. Introduction

MULTILEVEL converters have gained significant popularity in medium/high-voltage and high-power applications [1]–[3], as they can provide lower total harmonic distortion and reduced power losses [4]–[7], when compared to traditional two-level converters. Multilevel converters are generally classified as a neutral point clamped converter [8], a flying capacitors converter [9], and a cascaded multimodular converter [10], [11]. The topologies such as a Marx multilevel converter [12], a modular multilevel converter [13], [14], and a multilevel matrix converter [15], [16] are developed based on aforementioned multilevel converters. Among the above, the cascaded multimodular converter provides additional features such as scalability and modularity [17], [18]. Furthermore, additional voltage levels can be synthesized at the converter output port by cascading similar converter circuits. The cascaded converters also ensure smooth operation in case of failure in any of the cascaded cells [19].

The dual-output converters have been another developing trend in the domain of power electronics. As per the author's knowledge, the first dual-output converter topology was developed from a 12-switch ac–dc–ac converter through power switch reduction [20]. The topology consists of nine power switches and is capable of operating its three-phase dual-output ports under similar and/or variable frequencies [21]. However, the converter has an inherent restriction in the attainable voltage magnitude across the dual-output ports due to its reduced power switch configuration. As a result, appropriate modulation schemes were formulated for the nine-switch converter to operate its dual-output ports independently under different modes [22]. Furthermore, modifications of a nine-switch converter into single-phase (six-switch) [23] and five-phase [24] configurations to drive dual-output ports under similar and/or variable frequencies are also reported. Thus, dual-output converters gain interest in various power applications such as uninterrupted power supplies [25], grid power quality conditioning [26], and motor drives [27].

The aforementioned dual-output converter topologies provide only two voltage levels at its output port. As a result, improved topologies emerged to enhance the waveform quality of dual-output currents by generating multilevel voltages across the output ports. One way of achieving it is by providing an additional path from the output ports to the converter neutral point, through bidirectional power switches [29]. In this context, multilevel voltages ranging from three to nine levels have been generated at its dual-output ports. However, such a converter induces unbalanced dc capacitor voltages that necessitate an additional control objective to ensure better waveform quality and operational safety [30]. Another variant of the dual-output converter is the switched-capacitor-based three-level Marx inverter [31], [32], which can generate independent voltages of different amplitude (DA), different frequency (DF), and different phase angle (DP) across its dual-output ports. However, such converters are fault intolerant and nonflexible.

Therefore, a single-phase cascaded dual-output multilevel (CDOM) converter was proposed in [33] and [34]. The CDOM

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TABLE I
COMPARISON OF MODIFIED CDOM CONVERTER WITH THE AVAILABLE DUAL-OUTPUT CONVERTERS

Topology/configuration	Component count		Voltage stress	Voltage level	Port count		Modularity/Scalability
	Active	Passive			Input	Output	
Six switch dual-output [23]	6	0	V_{dc}	3	1	2	No
Dual-input dual-output Z-source [28]	6	10	$\frac{V_{dc}}{2}$	3	2	2	No
Three-level dual-output [29]	10	18	$\frac{V_{dc}}{2}$	5	1	2	No
Three-level Marx dual-output [31]	10	2	$\frac{V_{dc}}{2}$	5	1	2	No
Modular Multilevel dual-output							
Single half-bridge sub-module per arm	16	16	$\frac{V_{dc}}{2}$	5	1	2	Yes
Single full-bridge sub-module per arm	32			9			
Modified CDOM	10	0	$\frac{V_{dc}}{2}$	5	2	2	Yes

is formed by cascading multiple converter cells and can generate multilevel voltages across its dual-output ports. As a result, the converter not only enhances the power quality in terms of voltage and current but also has fault tolerance capability owing to its modular structure. A grid-connected application of the CDOM converter for a hybrid ac–dc microgrid environment is presented in [35]. The converter is capable of interfacing multiple ac and dc power sources to the grid. The grid and ac power source, connected through output ports, can operate at different magnitudes and frequencies. The CDOM converter is controlled by a model predictive controller, which enables it to operate its output ports independently to attain multiple objectives of active power control with reactive power and harmonic current compensation during its operation.

The objective of this article is to present a modified single-phase CDOM converter with a reduced number of power switches. The comparison of modified CDOM converter with available dual-output converters (scaled to a single-phase configuration) is summarized in Table I. Note that the modular multilevel dual-output topologies are added for comparison and do not exist in the literature. The converter can provide variable voltages across its dual-output ports, and each output port can generate multiple voltage levels. However, the converter possesses an inherent restriction on the attainable voltage magnitude across its output ports. Any operation beyond this restriction can lead to misoperation of equipment connected across the output ports. Therefore, converter operating limitations are investigated and analyzed, which quantifies the inherent restriction and ensures independent dual-output port operation with no distortion. In addition, the mathematical model of the converter is developed and incorporated in a finite control set model predictive control (FCS-MPC) algorithm for controlling the dual-output currents.

The CDOM converter was first introduced in [33], where its mathematical model was developed for two converter cell configurations [see Fig. 1(a)]. However, theoretical analysis of the converter operating limitations and experimental validation was not presented. Therefore, this article is an extension of the preliminary work reported in [33]. Following are the contributions overlaid in this work:

1) the CDOM converter is modified to operate with reduced power switch count;
2) a generalized modified CDOM converter is illustrated for a multiple-cell configuration;
3) theoretical analysis on the converter operational limits are provided, which quantifies the voltage amplitude range that each output port can operate without any distortion under different modes;
4) results of the proposed topology are experimentally validated pertinent to various operating conditions.

This article is organized as follows. Section II describes the CDOM converter and its mathematical modeling. Section III presents the implementation of the FCS-MPC algorithm for controlling dual-output load currents. Section IV presents the converter operational limits, which defines the minimum and maximum attainable voltages across the dual-output ports under different modes. Section V presents simulation and experimental results of the CDOM converter under different modes followed by conclusions.

II. CDOM CONVERTER

A. Topology

The CDOM converter is composed of two converter cells, each of which has two output ports, as shown in Fig. 1(a). Each converter cell consists of two legs, with each leg housing three power switches. Each converter cell is powered by individual isolated dc voltage sources V_{dc1} and V_{dc2}. The binary switching signal of the ith ($i \in \{1, 2, 3, 4, 5, 6\}$) power switch in the jth ($j \in \{1, 2\}$) converter cell is denoted as s_{ij}. The switching signal of the middle power switch in the jth converter cell is expressed

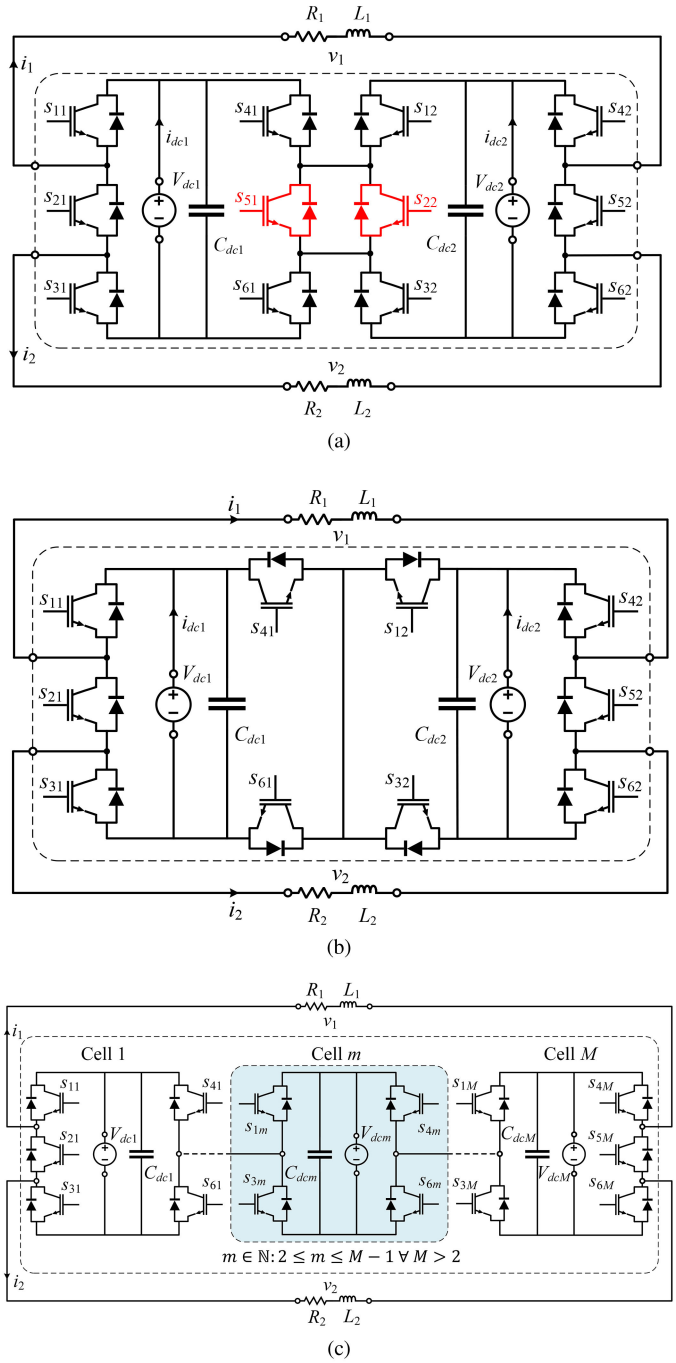


Fig. 1. CDOM converter topology: (a) CDOM converter with two converter cells [33], (b) modified CDOM converter with two converter cells, and (c) generalized modified CDOM converter with M converter cells.

in terms of its respective upper and lower power switches as

$$s_{2j} = s_{1j} \oplus s_{3j} \text{ and} \tag{1}$$

$$s_{5j} = s_{4j} \oplus s_{6j}. \tag{2}$$

On performing circuit analysis, the CDOM converter is found to operate under 36 possible switching states that are shown in Table II. It is observed that the middle power switches s_{51} and s_{22} [see Fig. 1(a)] remain switched-ON in all the switching states. These two middle power switches can be eliminated and the new modified CDOM converter with reduced power switches is formed, which is shown in Fig. 1(b). The switching signal of lower power switches s_{61} and s_{32} in the modified CDOM converter are defined as

$$s_{61} = \overline{s}_{41} \tag{3}$$

and

$$s_{32} = \overline{s}_{12}. \tag{4}$$

In summary, cascading M converter cells will eliminate a total of $2M-2$ middle power switches from the legs that interconnect each converter cell. For instance, cascading three converter cells ($M=3$) will eliminate four middle power switches s_{51}, s_{22}, s_{52}, and s_{23} from its configuration. The generalized modified CDOM converter topology with M converter cells is shown in Fig. 1(c). It can be observed that an additional count of only four power switches will be incorporated in topology with the increase in number of converter cells. As a result, the number of power switches (N_{sw}) expressed as a function of number of converter cells (M) is given as

$$N_{\text{sw}} = 4M + 2 \forall M \geq 1. \tag{5}$$

It is to be noted that a six-switch dual-output converter [23] is formed when $M=1$. The possible switching states of the modified CDOM converter with their respective voltage levels at

TABLE II
SWITCHING STATES AND THE OUTPUT VOLTAGES

State	***Output***	
(Decimal)	$\boldsymbol{v_1}$	$\boldsymbol{v_2}$
37	$V_{dc1}+V_{dc2}$	$V_{dc1}+V_{dc2}$
39	V_{dc1}	$V_{dc1}+V_{dc2}$
53	$V_{dc1}+V_{dc2}$	V_{dc2}
21,45	V_{dc2}	V_{dc2}
55	V_{dc1}	V_{dc2}
33,38	V_{dc1}	V_{dc1}
23,47	0	V_{dc2}
35	$V_{dc1}-V_{dc2}$	V_{dc1}
49,54	V_{dc1}	0
61	V_{dc2}	$-V_{dc1}+V_{dc2}$
29	$-V_{dc1}+V_{dc2}$	$-V_{dc1}+V_{dc2}$
34	$V_{dc1}-V_{dc2}$	$V_{dc1}-V_{dc2}$
17,22,41,46	0	0
51	$V_{dc1}-V_{dc2}$	0
63	0	$-V_{dc1}+V_{dc2}$
19,43	$-V_{dc2}$	0
31	$-V_{dc1}$	$-V_{dc1}+V_{dc2}$
57,62	0	$-V_{dc1}$
50	$V_{dc1}-V_{dc2}$	$-V_{dc2}$
18,42	$-V_{dc2}$	$-V_{dc2}$
59	$-V_{dc2}$	$-V_{dc1}$
25,30	$-V_{dc1}$	$-V_{dc1}$
27	$-V_{dc1}-V_{dc2}$	$-V_{dc1}$
58	$-V_{dc2}$	$-V_{dc1}-V_{dc2}$
26	$-V_{dc1}-V_{dc2}$	$-V_{dc1}-V_{dc2}$

the output ports are shown in Table II. For the sake of simplicity, the switching states are represented in decimal format. The switching states are obtained by converting the states to binary format. For example, switching state 55 is equivalent to 6-b binary format, where the switching signals of the power switch are defined as $[s_{11}, s_{31}, s_{41}, s_{12}, s_{42}, s_{62}] = [1, 1, 0, 1, 1, 1]$. The switching signal for remaining power switches are computed from (1)–(4).

The modified CDOM converter output voltages v_1 and v_2 in terms of binary switching signals are expressed as

$$v_1 = (s_{11} - s_{41})V_{\text{dc1}} - (s_{42} - s_{12})V_{\text{dc2}} \text{ and} \tag{6}$$

$$v_2 = (s_{11}s_{21} - s_{41})V_{\text{dc1}} - (s_{42}s_{52} - s_{12})V_{\text{dc2}} \tag{7}$$

where V_{dc1} and V_{dc2} are the voltages of the dc source that powers individual cells of the modified CDOM converter.

B. Continuous-Time Model

The CDOM converter shown in Fig. 1(b) is modeled using a simple circuit analysis. The continuous-time domain equation of the current at converter output port x is given as

$$\frac{di_x}{dt} = \frac{1}{L_x}\left(v_x - R_x i_x\right) \forall\, x \in \mathbb{N} : 1 \le x \le 2 \tag{8}$$

where i_x represent the output current of the CDOM converter at port x, whereas terms L_x and R_x are the load inductance and resistance connected across the output port x.

C. Discrete-Time Model

The continuous-time model of the output current i_x is transformed into discrete time by using a forward Euler method and is given as

$$i_x^{k+1} = \left(1 - \frac{R_x T_s}{L_x}\right) i_x^k + \frac{T_s}{L_x} v_x^k \tag{9}$$

where T_s is the sampling period of the controller.

The current i_x^k at instant k is measured by the current sensors. It is used to predict the future values of current at instant $k+1$. The discrete-time models of the converter output voltages v_1^k and v_2^k are expressed as

$$v_1^k = (s_{11}^k - s_{41}^k)v_{\text{dc1}}^k - (s_{42}^k - s_{12}^k)v_{\text{dc2}}^k \text{ and} \tag{10}$$

$$v_2^k = (s_{11}^k s_{21}^k - s_{41}^k)v_{\text{dc1}}^k - (s_{42}^k s_{52}^k - s_{12}^k)v_{\text{dc2}}^k \tag{11}$$

where v_{dc1}^k and v_{dc2}^k are measured voltages of dc sources V_{dc1} and V_{dc2} at time instant k, respectively.

III. FCS-MPC Implementation

In this section, FCS-MPC [36] implementation for the CDOM converter is presented. The FCS-MPC runs at a sampling period of T_s and its implementation in a block diagram and a flowchart are shown in Figs. 2 and 3, respectively. The FCS-MPC algorithm begins by measuring the variables—output currents (i_1^k and i_2^k) and dc source voltages (v_{dc1}^k and v_{dc2}^k) at every instant k. The measured variables are subject to a prediction model (9) that predicts 36 possible output currents (i_1^{k+1} and i_2^{k+1}) for instant $k+1$ using the switching states shown in Table II. In order to

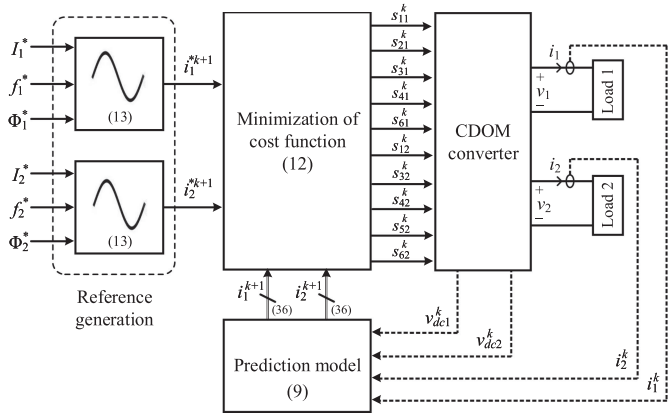


Fig. 2. Block diagram of the FCS-MPC implementation.

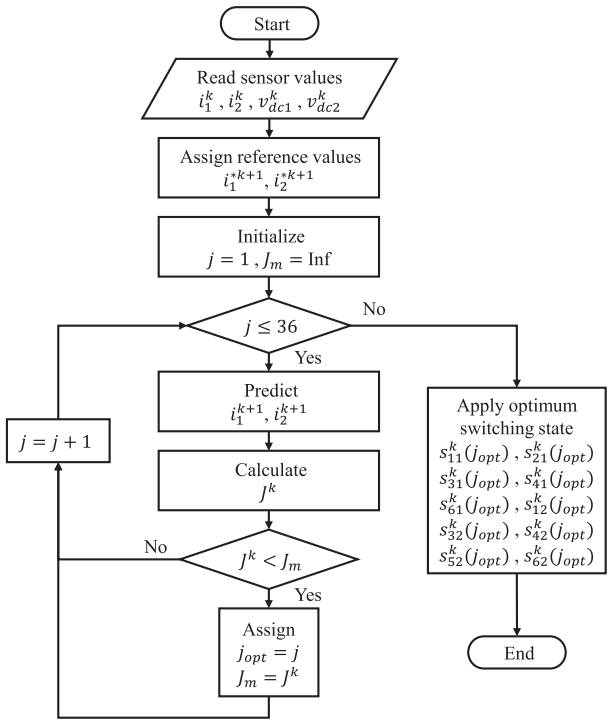


Fig. 3. Flowchart of the FCS-MPC algorithm.

identify the optimum switching state during a sampling period, a quadratic cost function is formulated as follows:

$$J^k = \sum_{x=1}^{2} \left(i_x^{*k+1} - i_x^{k+1}\right)^2. \tag{12}$$

The term, i_x^{*k+1} is the reference current for the converter output port x and is required to be sinusoidal. The reference current is controlled using three parameters—amplitude I_x^*, frequency f_x^*, and phase angle ϕ_x^* (see Fig. 2). The reference current for the converter output port x in a continuous-time domain is expressed as

$$i_x^*(t) = I_x^* \sin\left(2\pi f_x^* t + \phi_x^*\right). \tag{13}$$

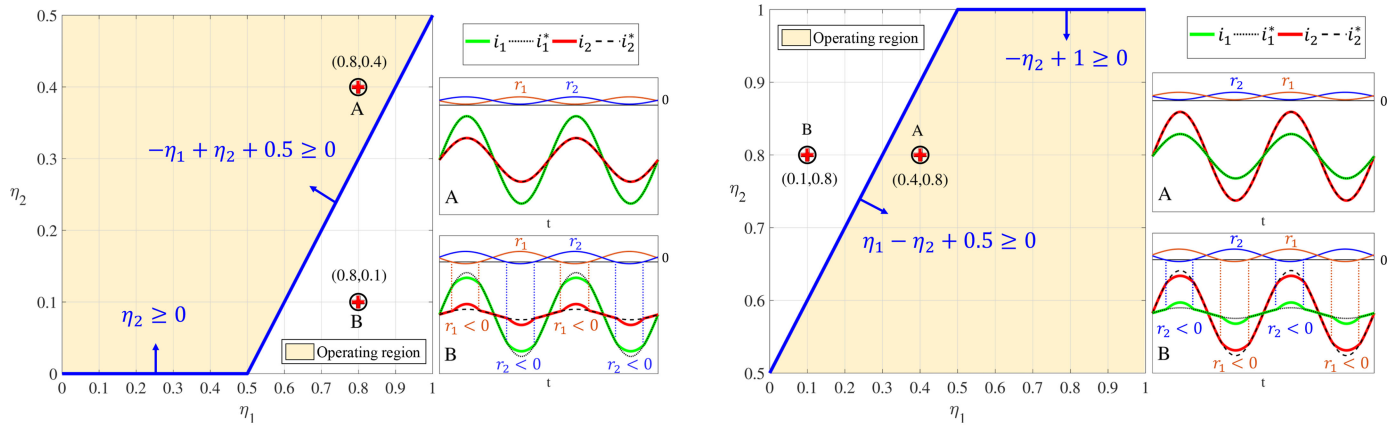


Fig. 4. Operational limits under DA mode: (a) variations in minimum value of η_2 with respect to η_1 and (b) variations in maximum value of η_2 with respect to η_1.

The reference currents i_x^* are transformed into discrete-time domain as i_x^{*k+1} for FCS-MPC implementation.

The quadratic cost function J^k is computed for 36 predicted output currents during a sampling period T_s (see Fig. 3). Finally, an optimum switching state that has a minimum value of J^k is applied to the converter at time instant k (see Fig. 2).

IV. Operational Limits of the CDOM Converter

In this section, operational limits of the CDOM converter under DA, DF, and DP modes are studied. The converter operational limits are defined as the region bounded by a range of voltage, which the converter can generate across its output ports simultaneously without distortion. As a result, the converter output ports can operate independently only when the operating point is within the defined operational limits, as shown in Figs. 4–6. Any operation beyond these limits will deteriorate the output current waveform, leading to unsafe operation of the load.

The converter operational limits can be obtained by using valid switching states that correspond to the minimum and maximum output voltages. This can be accomplished by defining a reference sinusoidal voltage signal $\bar{v}_x$ for the converter output port x as

$$\bar{v}_x(t) = \eta_x \sin\left(2\pi f_x^* t + \psi_x\right) \tag{14}$$

where f_x^* is the reference frequency of output port x and ψ_x is the phase angle associated with the load connected across output port x. The phase angle ψ_x can be defined as

$$\psi_x = \tan^{-1}\left(\frac{2\pi f_x^* L_x}{R_x}\right) \tag{15}$$

where R_x and L_x are the parameters of load connected across output port x. The term η_x is the voltage index for output port x and is expressed as

$$\eta_x = \frac{\mid z_x \mid}{V_{\text{dc1}} + V_{\text{dc2}}} I_x^* \,\forall\, \eta_x \in \mathbb{R} : 0 \leq \eta_x \leq 1 \tag{16}$$

where I_x^* is the reference current amplitude of output port x and $\mid z_x \mid$ is the magnitude of the load impedance connected across output port x. Note that the dc source voltages V_{dc1} and V_{dc2} are assumed to be equal throughout the analysis. It can be noted from (14) that η_x, f_x^*, and ψ_x are the key parameters that determine the voltage across the converter output port x. Therefore, analyzing these parameters will quantify the converter operational limits under different modes. For the sake of simplicity, the frequencies (f_1^* and f_2^*) are expressed as frequency difference ($\Delta f = f_1^* - f_2^*$) and phase angles (ψ_1 and ψ_2) are expressed as phase angle difference ($\Delta\psi = \psi_1 - \psi_2$). This simplifies the analysis to four parameters: $\eta_1, \eta_2, \Delta f$, and $\Delta\psi$. Therefore, obtaining minimum and maximum values of η_1 and η_2, with $\Delta f = 0$ and $\Delta\psi = 0$, quantifies the converter operational limits for DA mode. On the other hand, acquiring minimum and maximum values of η_1 and η_2 for different Δf and $\Delta\psi$ computes the converter operational limits for DF and DP modes, respectively.

The operational limits are obtained by simulating the FCS-MPC algorithm on the developed converter model. The simulation is run for all possible combinations of η_1 and η_2 under different values of Δf and $\Delta\psi$. The parameter η_x is varied from 0 to 1, and its corresponding reference current amplitude I_x^* is calculated from (16). The other reference current parameters f_x^* and ϕ_x^* are calculated based on the mode of operation and are explained in respective sections. Note that the load parameters R_x and L_x are kept constant throughout the analysis. Therefore, phase angle difference $\Delta\psi$ between the output voltage is introduced by varying reference current phase angle ϕ_x^*. Finally, the converter dual-output current responses for all possible combinations of η_1 and η_2 are recorded, and their deviations from the reference output currents are monitored. The minimum and maximum values of η_x are determined based on the current waveform deviation from its reference. The results of analysis under different modes are discussed in the respective sections.

A. DA Mode

In DA mode, the converter output ports are operating with same frequency and phase angle. In this analysis, η_1 and η_2 are

varied from 0 to 1, whereas Δf and $\Delta\psi$ are kept zero. Thus, the converter model is simulated for all combinations of I_1^* and I_2^*, which are calculated from (16). The reference frequencies f_1^* and f_2^* are set to 50 Hz, whereas the reference phase angles ϕ_1^* and ϕ_2^* are set to 0°. As a result, the variations in minimum and maximum values of η_2, with respect to η_1, is shown in Fig. 4(a) and (b), respectively. It can be observed from Fig. 4(a) that the minimum value of η_2 remains 0 until $\eta_1 = 0.5$, whereas it increases linearly with unity slope for $\eta_1 > 0.5$. Similarly, the maximum value of η_2 increases linearly with unity slope until $\eta_1 = 0.5$, and remains 1 for $\eta_1 > 0.5$ [see Fig. 4(b)]. Therefore, the converter output ports can operate independently without any distortion [operating point A in Fig. 4(a) and (b)] only when it is operating at a voltage index pair (η_1, η_2) that is localized within the area bounded by the following linear equations:

$$0 \le \eta_1 \le 1 \tag{17}$$

$$0 \le \eta_2 \le 1 \tag{18}$$

$$-\eta_1 + \eta_2 + 0.5 \ge 0 \tag{19}$$

and

$$\eta_1 - \eta_2 + 0.5 \ge 0. \tag{20}$$

The distortion in both output currents can be observed for operating point B [see Fig. 4(a) and (b)], which is outside the area bounded by the linear equations (17)–(20). In order to examine the instance of distortion in output current waveforms, (19) and (20) can be rewritten in terms of the reference sinusoidal voltages $\bar{v}_1$ and $\bar{v}_2$ (14) as

$$r_1(t) = -\bar{v}_1(t) + \bar{v}_2(t) + 0.5 \tag{21}$$

and

$$r_2(t) = \bar{v}_1(t) - \bar{v}_2(t) + 0.5. \tag{22}$$

The resulting equations r_1 and r_2 define the evolution of the converter operating point. Note that r_1 and r_2 should always be greater than or equal to zero for an independent output port operation. It is observed in Fig. 4(a) and (b) that the current waveforms distort during the interval when either r_1 or r_2 is less than zero. The mathematical expression defining the permissible range of η_2 in terms of η_1 for an independent output port operation can be simplified from (17)–(20) as

$$(\eta_1 - 0.5) \le \eta_2 \le 1, \forall\, \eta_1 \ge 0.5,\ \Delta f = 0,\ \Delta\psi = 0^\circ \tag{23}$$

and

$$0 \le \eta_2 \le (\eta_1 + 0.5),\ \forall\, \eta_1 < 0.5,\ \Delta f = 0,\ \Delta\psi = 0^\circ. \tag{24}$$

Equations (23) and (24) define the converter operational limits under DA mode. It can be observed that one of the output ports can operate at the full range of voltage index (0 to 1) only when another output port is operating at a voltage index of 0.5.

B. DF Mode

In this analysis, η_1 and η_2 are varied from 0 to 1 for all values of Δf, ranging from 0 to 200 Hz. The parameter $\Delta\psi$ is kept zero throughout the analysis. Thus, the converter model is simulated

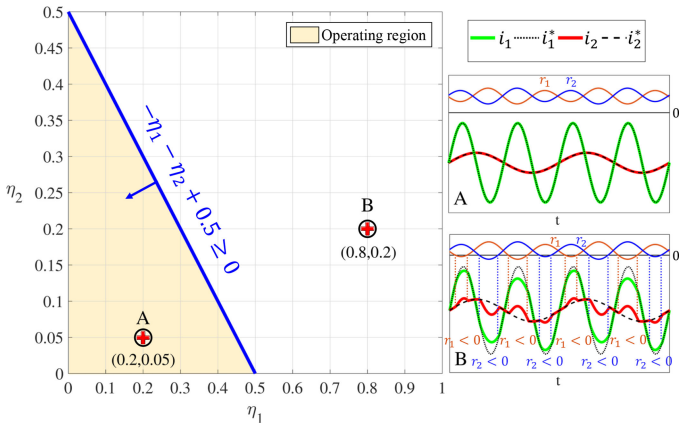


Fig. 5. Operational limits under DF mode: variations in η_2 with respect to η_1.

for all combinations of I_1^* and I_2^*, which are calculated from (16). The reference frequency is calculated as $f_1^* = \Delta f + f_2^*$, where f_2^* is set to a constant value (50 Hz), and reference current phase angles ϕ_1^* and ϕ_2^* are set to 0°. As a result, the variations in maximum η_2 with respect to η_1 is shown in Fig. 5. It is observed that the maximum value of η_2 reduces linearly with the increase in η_1 for all $\Delta f > 0$. Therefore, the converter output ports can operate independently without any distortion (operating point A in Fig. 5) only when it is operating at a voltage index pair (η_1, η_2) that is localized within the region bounded by the following linear equations:

$$0 \le \eta_1 \le 0.5 \tag{25}$$

$$0 \le \eta_2 \le 0.5 \tag{26}$$

and

$$-\eta_1 - \eta_2 + 0.5 \ge 0. \tag{27}$$

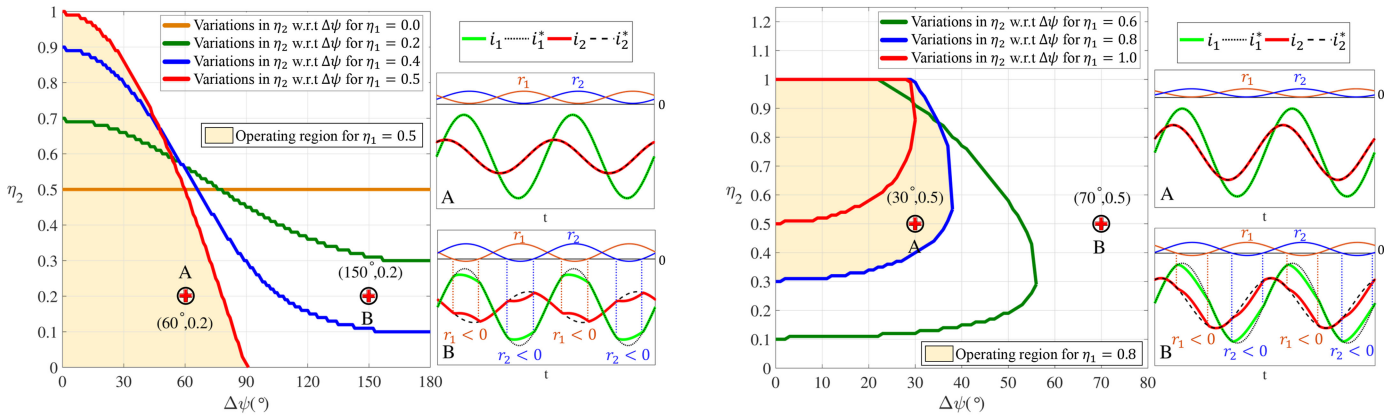
The distortion in both output currents can be noted for operating point B (see Fig. 5), which is outside the region bounded by the linear equations (25)–(27). The distortion is observed in Fig. 5 for instances when either of r_1 or r_2 is less than zero. The output currents track its references without any deviation for all r_1 and r_2 greater than or equal to zero. The mathematical expression defining the permissible range of η_2 in terms of η_1 can be expressed as

$$0 \le \eta_2 \le (0.5 - \eta_1)\ \forall\, \eta_1 \le 0.5,\ \Delta f > 0,\ \Delta\psi = 0^\circ. \tag{28}$$

Equation (28) defines the converter operational limits under DF mode. It can be noted that the converter output ports can operate only at a voltage index of less than 0.5.

C. DP Mode

In this analysis, the phase angle difference between the output voltage is introduced by varying the reference current phase angles ϕ_1^* and ϕ_2^*. The parameters η_1 and η_2 are varied from 0 to 1 for all values of $\Delta\psi$, ranging from 0° to 180°. The parameter Δf is kept zero throughout the analysis. Thus, converter model is simulated for all combinations of I_1^* and I_2^*, which are calculated from (16). The reference current phase angles are calculated



(a) (b)

Fig. 6. Operational limits under DP mode: (a) variations in η_2 with respect to $\Delta\psi$ for $\eta_1 \leq 0.5$ and (b) variations in η_2 with respect to $\Delta\psi$ for $\eta_1 > 0.5$.

as: $\phi_1^* = \Delta\psi + \phi_2^*$, where ϕ_2^* is set to a constant value (0°), and the reference frequencies f_1^* and f_2^* are set to 50 Hz. As a result, the variation in maximum η_2 with respect to $\Delta\psi$ for $\eta_1 \leq 0.5$ is shown in Fig. 6(a). It can be observed that with the increase in η_1, the maximum attainable value of η_2 decreases for higher values of $\Delta\psi$, while increases for lower values of $\Delta\psi$. For instance, consider the converter operating one of its output ports at half voltage index ($\eta_1 = 0.5$). The other output port can operate independently without any distortion [operating point A in Fig. 6(a)] only when it is operating at point $(\Delta\psi, \eta_2)$ bounded by the following equation:

$$0 \leq \eta_2 \leq 1 \tag{29}$$

$$0 \leq \Delta\psi \leq 90^\circ \tag{30}$$

and

$$-\eta_2 + \cos(\Delta\psi) \geq 0. \tag{31}$$

The distortion in both output currents from its reference can be noted for operating point B, which is outside the area bounded by (29)–(31). The distortion occurs during the instances when either of r_1 or r_2 is less than zero [see Fig. 6(a)]. The output currents are free from distortion for all r_1 and r_2 greater than or equal to zero. The mathematical expression defining the permissible range of η_2 in terms of $\Delta\psi$ for an independent output port operation can be expressed as

$$0 \leq \eta_2 \leq \cos(\Delta\psi) \,\forall\, \eta_1 = 0.5,\ \Delta f = 0,\ \Delta\psi \leq 90^\circ. \tag{32}$$

Equation (32) defines the converter operational limits under DP mode for $\eta_1 = 0.5$. Similar constraints can be derived for other values of η_1 from Fig. 6(a). Likewise, variation in minimum and maximum attainable values of η_2 with respect to $\Delta\psi$ for $\eta_1 > 0.5$ is shown in Fig. 6(b). It is observed that with the increase in $\Delta\psi$, the converter output ports lose their capability to operate independently at higher voltage indices. This is demonstrated by considering converter operating at $\eta_1 = 0.8, \eta_2 = 0.5$, and $\Delta\psi = 30^\circ$. It can be seen from Fig. 6(b) that the converter is operating within the region defined for $\eta_1 = 0.8$. Therefore, the converter output ports operate independently without any distortion. If $\Delta\psi$ is increased to 70°, the converter output port loses independent operation and distorts the output current waveforms (operating point B). The distortion is observed during instances when r_1 or r_2 is less than zero [see Fig. 6(b)]. The output currents track its references without any distortion for all r_1 and r_2 greater than or equal to zero. Therefore, in order to ensure independent output port operation under DP mode, the operating point must be chosen such that it falls within the area bounded by the respective curves.

D. *Effect of DC Source Voltages on the Operational Limits*

The converter operational limits determined in the previous sections are under the assumption of having dc sources with equal voltages ($V_{\text{dc1}} = V_{\text{dc2}}$). Therefore, this section presents the effect on operational limits under unequal dc source voltages ($V_{\text{dc1}} \neq V_{\text{dc2}}$). The operation of the converter with unequal dc source voltages can increase the output voltage levels without needing to increase the number of converter cells [37]. However, the converter operational limits vary with unequal dc source voltages, as shown in Fig. 7. The variation is dependent on the scaling factor C, which is expressed in terms of dc source voltages as

$$C = \frac{\min(V_{\text{dc1}}, V_{\text{dc2}})}{V_{\text{dc1}} + V_{\text{dc2}}}. \tag{33}$$

It is noted from (33) that C is always less than or equal to 0.5, and the converter operational limits are dependent on the dc source with minimum voltage value. The effect on operational limits when $C = 0.3$ is demonstrated in Fig. 7. As a result, the operational limits for DA mode are generalized in terms of C from Fig. 7(a), and (b) as

$$0 \leq \eta_2 \leq (\eta_1 + C) \,\forall\, \eta_1 \leq C \tag{34}$$

$$(\eta_1 - C) \leq \eta_2 \leq (\eta_1 + C) \,\forall\, C \leq \eta_1 \leq 1 - C \tag{35}$$

and

$$(\eta_1 - C) \leq \eta_2 \leq 1 \,\forall\, \eta_1 \geq 1 - C \tag{36}$$

where $\Delta f = 0$ and $\Delta\psi = 0$. The operating region is observed to shrink depending on the value of C. Similarly, operational limits

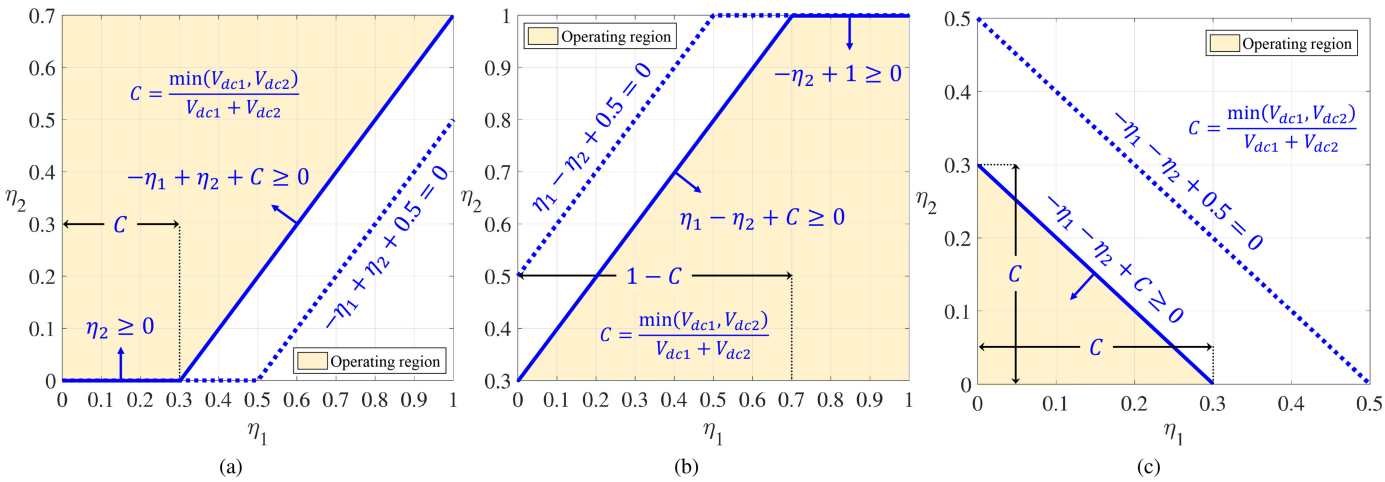


Fig. 7. Effect of dc source voltages on the operational limits: (a) variations in the minimum value of η_2 with respect to η_1 for $C = 0.3$ (DA mode), (b) variations in the maximum value of η_2 with respect to η_1 for $C = 0.3$ (DA mode), and (c) variations in η_2 with respect to η_1 for $C = 0.3$ (DF mode).

TABLE III
SYSTEM PARAMETERS FOR SIMULATION AND EXPERIMENTAL TEST

Parameter	V_{dc1} V_{dc2} (V)	R_1 R_2 (Ω)	L_1 L_2 (mH)	C_{dc1} C_{dc2} (mF)	T_s (μs)
Value	50	18	6	2.2	50

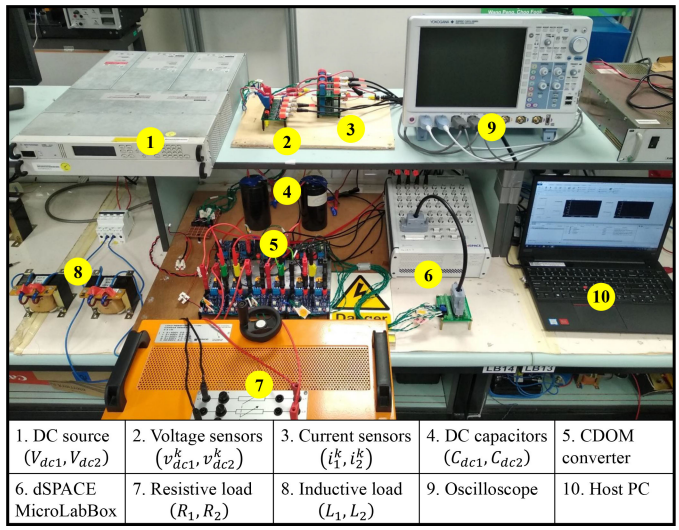
for DF mode are generalized in terms of C from Fig. 7(c) as

$$0 \leq \eta_2 \leq (C - \eta_1) \forall \eta_1 \leq C,\ \Delta f > 0,\ \Delta\psi = 0^\circ. \quad (37)$$

A similar analysis can be extended for DP mode, and its operational limits in terms of C can be generalized. It is observed that the converter with equal dc source voltages is the case when $C = 0.5$. In conclusion, converter operational limits are dependent on the voltage values of its dc sources. The converter operating region is compromised if a voltage difference exists between the dc source connected across each cell. Therefore, a converter with equal dc source voltages will have a broader operating region (area enclosed by dotted lines in Fig. 7) than the converter with unequal dc source voltages.

V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental tests are performed on a low-power CDOM converter as shown Fig. 1(b). The CDOM converter operation has been simulated using the MATLAB/Simulink environment. The FCS-MPC algorithm is programmed using a function block with a sampling time of 50 μs. The simulation results are validated experimentally using a dSPACE MicroLabBox. The converter prototype and hardware setup are shown in Fig. 8. The system parameters are given in Table III. The case studies on dynamic behavior of a CDOM converter during mode transitions and step-load change are demonstrated in the following section.



1. DC source (V_{dc1}, V_{dc2})	2. Voltage sensors (v^k_{dc1}, v^k_{dc2})	3. Current sensors (i^k_1, i^k_2)	4. DC capacitors (C_{dc1}, C_{dc2})	5. CDOM converter
6. dSPACE MicroLabBox	7. Resistive load (R_1, R_2)	8. Inductive load (L_1, L_2)	9. Oscilloscope	10. Host PC

Fig. 8. Experimental prototype of a single-phase CDOM converter.

A. DA Mode

In this study, the converter output ports operate under different current amplitudes. The frequency and phase angle of both output currents are set to 50 Hz and 0°, respectively. The behavior of converter output voltages and currents are shown in Fig. 9. The simulation results under these operating conditions are shown in Fig. 9(a). Until time $t = 50$ ms, the current amplitudes I_1^* and I_2^* are set to 4.7 and 1.9 A, respectively. It is observed that the converter output ports operate independently under different voltage levels. This is because the resulting converter operating point ($\eta_1 = 0.85$, $\eta_2 = 0.35$) is within the operational limits defined in (23). At time $t = 50$ ms, I_1^* and I_2^* are set to 1.9 and 4.7 A, respectively. It is observed that the converter output ports 1 and 2 operate at $\eta_1 = 0.35$ and $\eta_2 = 0.85$, respectively. Since the resulting operating point is within the operational limits (24), the output ports operate independently. A reduction in the output voltage level of port 1 (from 5 to 3 level) is observed, which is due to the decrease in I_1^*. The same results are observed experimentally [see Fig. 9(b)]. The converter power

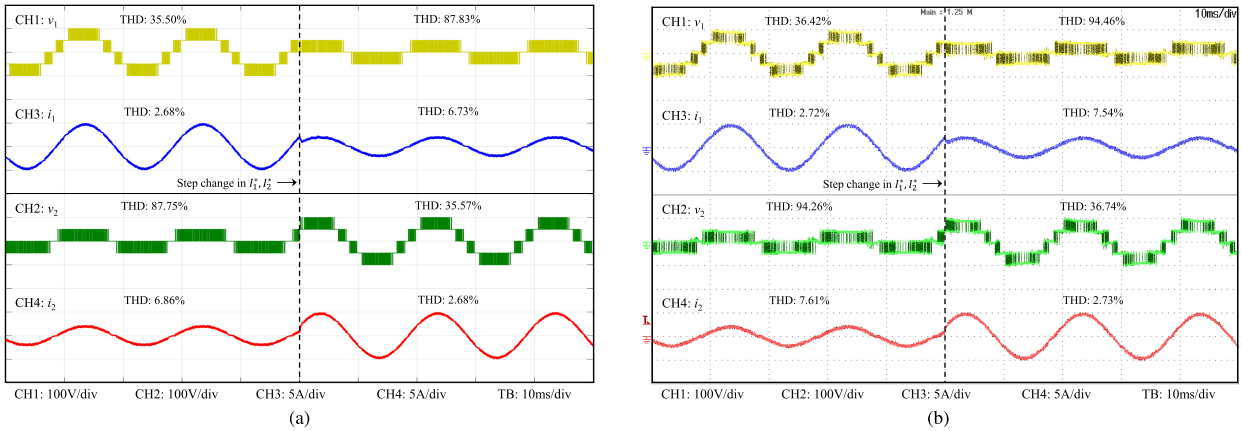


Fig. 9. Operation of CDOM converter under DA mode: (a) simulation and (b) experimental results.

TABLE IV
CONVERTER POWER BALANCE AND EFFICIENCY UNDER DIFFERENT OPERATING CONDITIONS

Operating conditions	Input power (W)		Output power (W)		Efficiency(%)
	P_{dc1}	P_{dc2}	P_1	P_2	
$\eta_1 = 0.85, \eta_2 = 0.35$ $f_1^* = 50$Hz, $f_2^* = 50$Hz $\phi_1^* = 0^\circ$, $\phi_2^* = 0^\circ$	140.5	138.5	196.8	36.03	83.4
$\eta_1 = 0.35, \eta_2 = 0.85$ $f_1^* = 50$Hz, $f_2^* = 50$Hz $\phi_1^* = 0^\circ$, $\phi_2^* = 0^\circ$	140.5	138.5	36.03	196.8	83.4
$\eta_1 = 0.6, \eta_2 = 0.8$ $f_1^* = 50$Hz, $f_2^* = 50$Hz $\phi_1^* = 0^\circ$, $\phi_2^* = 0^\circ$	159.15	159.75	99.6	176.76	86.6
$\eta_1 = 0.3, \eta_2 = 0.2$ $f_1^* = 100$Hz, $f_2^* = 50$Hz $\phi_1^* = 0^\circ$, $\phi_2^* = 90^\circ$	23.23	24.17	26.46	11.07	79

balance and its efficiency under these operating conditions are shown in Table IV. The FCS-MPC algorithm enhances the dynamic performance of the converter operation by tracking the step-reference change instantly without introducing any delay. Hence, the CDOM converter output ports are capable of operating independently, at different current amplitudes.

B. DP Mode

In this study, the converter output ports operate at different phase angles. The frequency at both the ports are set to 50 Hz. The current amplitudes I_1^* and I_2^* are set to 3.3 and 4.4 A, respectively. Until time $t = 50$ ms, the current phase angles ϕ_1^* and ϕ_2^* are set to 0°. The evolution of converter output voltages and currents are shown in Fig. 10. The simulation results under these operating conditions are shown in Fig. 10(a). It can be observed that the converter output currents are in-phase and operate independently. This is because the resulting converter operating point ($\eta_1 = 0.6$, $\eta_2 = 0.8$) is within the operational limits defined in (23). At time $t = 50$ ms, the current phase angle ϕ_2^* is changed to 35°. It can be seen that the converter output ports operate independently with a phase angle difference of 35°. This is because the resulting converter operating point ($\Delta\psi = 35^\circ, \eta_2 = 0.8$) resides within the operational limits for $\eta_1 = 0.6$ given in Fig. 6(b). The same results are seen experimentally in Fig. 10(b). The converter power balance and its efficiency under these operating conditions are shown in Table IV. Hence the CDOM converter is capable of operating its two output ports independently, with different phase angles.

C. Different Output Modes

In this study, the output currents at ports 1 and 2 of the converter are operating under DA, DF, and DP. Until time $t = 50$ ms, the current parameters of output ports 1 and 2 are set as $I_1^* = 3.3$ A, $f_1^* = 50$ Hz, $\phi_1^* = 0^\circ$ and $I_2^* = 4.4$ A, $f_2^* = 50$ Hz, $\phi_2^* = 0^\circ$, respectively. The evolution of converter output voltages and currents is shown in Fig. 11. The simulation and experimental results under these operating conditions are shown in Fig. 11(a) and (b), respectively. The converter output ports 1 and 2 are observed to operate independently at $\eta_1 = 0.6$ and $\eta_2 = 0.8$, respectively. At time $t = 50$ ms, the current parameters of output ports 1 and 2 are changed to $I_1^* = 1.6$ A, $f_1^* = 100$ Hz, $\phi_1^* = 0^\circ$ and $I_2^* = 1.1$ A, $f_2^* = 50$ Hz, $\phi_2^* = 90^\circ$,

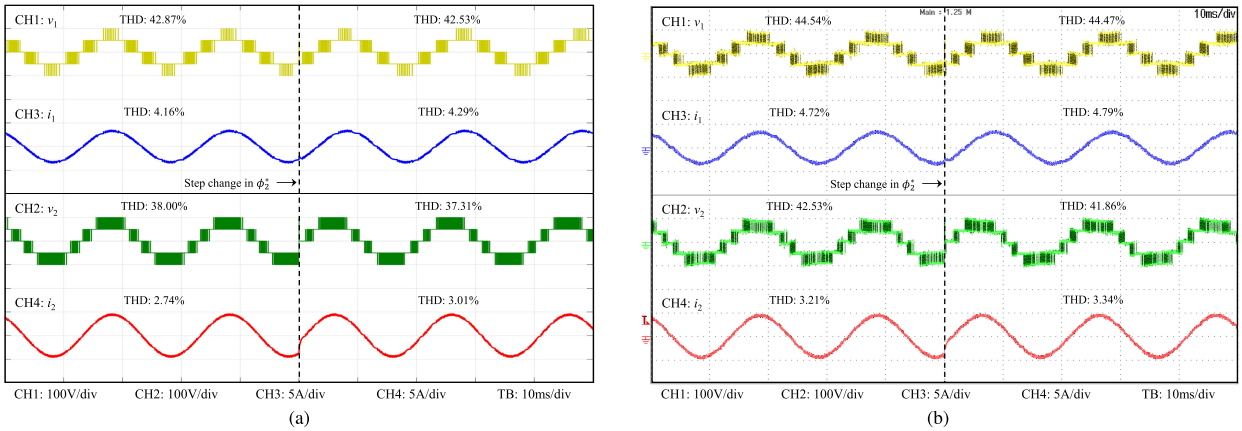


Fig. 10. Operation of CDOM converter under DP mode: (a) simulation and (b) experimental results.

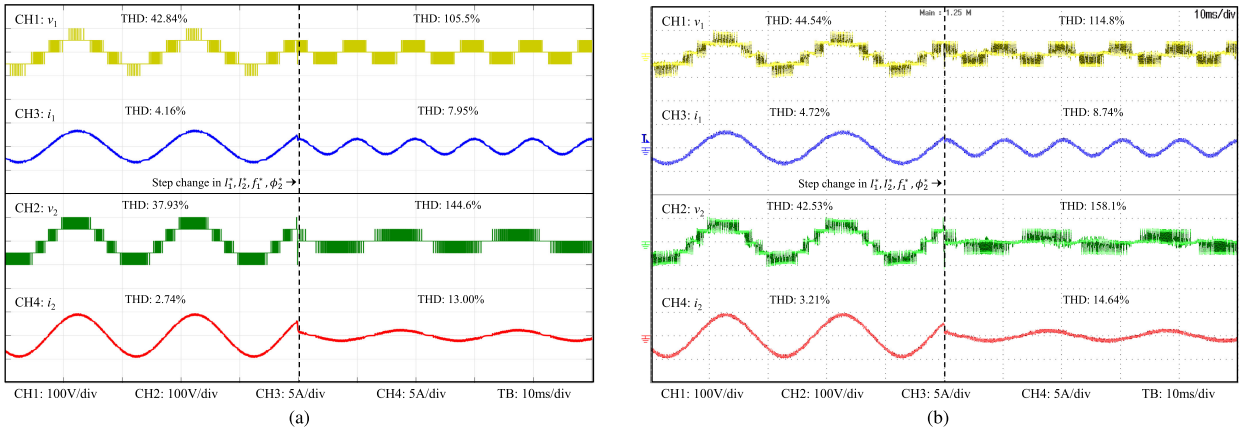


Fig. 11. Operation of the CDOM converter under different output modes: (a) simulation and (b) experimental results.

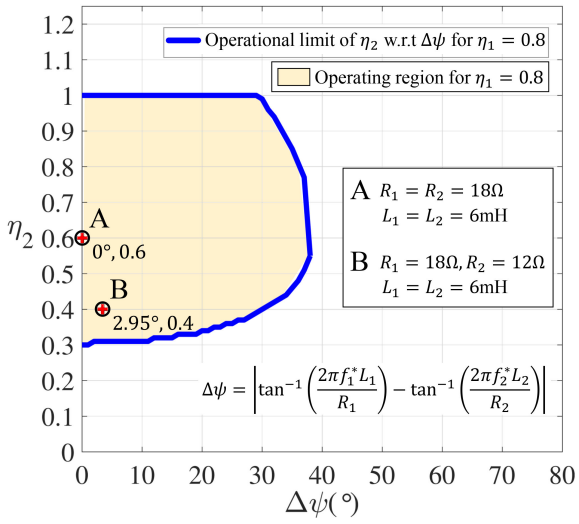


Fig. 12. Effect on the converter operating point during a step-load change.

respectively. It can be observed that the converter output ports operate independently, at DA, DF, and DP. This is because the resulting operating point ($\eta_1 = 0.3$, $\eta_2 = 0.2$) is within the operational limits defined in (28). The experimental results are also found to comply with the simulation. The converter power balance and its efficiency under these operating conditions are shown in Table IV.

D. *Effect of Load Parameters on the Operating Point*

In this study, the effect on the converter operating point during step-load change is presented. The load parameters given in Table III are considered for the study. Simulation and experimental results on the dynamic behavior of the converter for a step-load change are shown in Fig. 13(a) and (b), respectively. The reference current parameters of FCS-MPC are set as $I_1^* = 4.4$ A, $I_2^* = 3.3$ A, $f_1^* = f_2^* = 50$ Hz, and $\phi_1^* = \phi_2^* = 0°$ throughout the study. It can be observed from Fig. 13 that until time $t = 50$ ms, the converter output ports 1 and 2 operate under DA mode with $\eta_1 = 0.8$ and $\eta_2 = 0.6$, respectively. Since both the output ports are connected to loads with equal parameters, the phase angle difference between the output voltages is zero ($\Delta\psi = 0$). The resulting operating point is denoted as A in Fig. 12. At time $t = 50$ ms, load across output port 2 is subjected a step change to $R_2 = 12\,\Omega$. This introduces a load parameter mismatch between the output ports. The mismatch can be quantified as magnitude mismatch $\Delta z = ||z_1| - |z_2||$

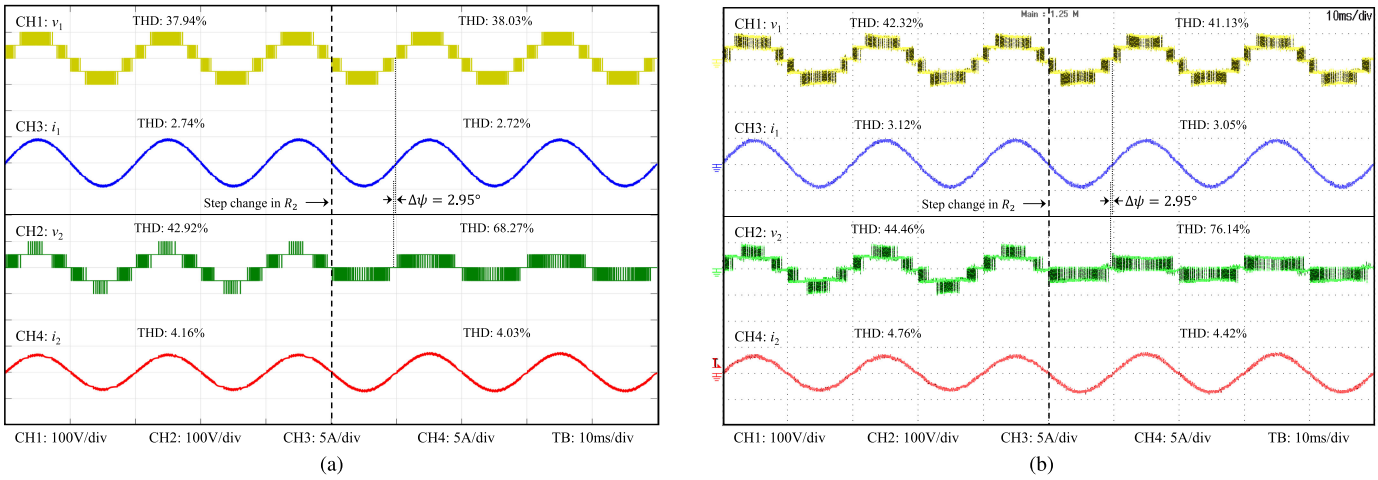


Fig. 13. Dynamic behavior of a CDOM converter for a step-load change: (a) simulation and (b) experimental results.

and phase angle mismatch $\Delta\psi = |\psi_1 - \psi_2|$. The magnitude mismatch introduces a change in voltage index η_2 (16) and a phase angle mismatch introduces a phase angle difference $\Delta\psi$ between the output voltages. Since the reference currents are kept constant, output port 2 operates at $\eta_2 = 0.4$ and a phase angle difference $\Delta\psi = 2.95°$ is introduced between the output voltages (see Fig. 13). Therefore, the converter operates under DP mode, and its resulting operating point is denoted as B in Fig. 12. It is noted that the converter operating point is dependent on the parameters of load connected across the output ports. Since operating points A and B resides within the operating region, the converter output ports are observed to operate independently (see Fig. 13). However, if the load parameter variations go beyond the operational limits, the output ports will lose its independent operation and introduce distortion in the current waveform, as discussed in Section IV.

VI. Conclusion

In this article, a modified CDOM converter with a reduced number of power switches was presented. Unlike other dual-output converter topologies, the proposed converter can generate independent multilevel voltages across its dual-output ports. The mathematical model for the CDOM converter was developed, and an FCS-MPC algorithm was devised to control its dual-output ports. The algorithm enhances the converter performance without introducing any delay during step changes in mode. In addition, analysis of the converter operational limit under various modes are also investigated and summarized as: 1) In DA mode, the converter can have one of its output ports operate at a full range only when another output port operates at half voltage index. 2) In DF mode, the converter can only operate its output ports at a voltage index of less than 0.5, and, thereby, restricts the output ports operation to only three voltage levels. 3) In DP mode, the converters ability to drive the output ports with five voltage levels reduces with the increase in phase angle difference between the output voltages.

Furthermore, the effects of dc source voltages on the operational limits were also presented. The converter operating region was reduced when dc sources with unequal voltages were connected across each converter cell. Both simulation and experimental results were demonstrated to validate the converter operation. In the industry, the CDOM converter finds its application in electric vehicles, where two motors can be driven independently for similar and variable speeds. In a hybrid microgrid environment, it can interface two ac systems operating with DAs and DFs. Thus, the future scope of this work would be to develop its three-phase configuration and analyze its application in various real-time industrial problems, preferably electric drives and microgrids.

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