Letters

Modeling of N-Parallel Full-SiC AC–DC Converters by Four Per-Phase Circuits

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***Abstract*—Due to the limit in current-rating of SiC MOSFETs, a number of SiC-based modular ac–dc converters needs to be paralleled to increase power capacity. The number of modular converters (N) may vary depending on the customer's requirement. On the other hand, paralleling diversifies paths of current, and complex filter topologies such as integrated inductors may complicate analysis. To enhance understanding of N-paralleled ac–dc converters and to provide an insight for filter design, four per-phase equivalent circuits are proposed. Any voltage on the frequency spectrum can be classified into four groups by two criteria; first, positive sequence and negative sequence versus zero sequence, and, second, circulating, versus in-phase. By extending symmetrical component theory to the parallel converters, the N-paralleled three-phase converters can be represented by four single-phase circuits for any N. Thanks to the simplicity, complex issues such as an impact of the magnetic integration or change of harmonic attenuation for different N can be easily understood for any N by single-phase equivalent circuits.**

***Index Terms*—AC–DC converters, coupled inductors, interleaving, modeling, paralleling.**

I. Introduction

WIDE bandgap devices are significantly improving the performance of power electronics systems. Efficiencies of three-phase ac–dc converters are reported to go beyond 99% with improved power density. However, current capacity of matured Si-IGBT reaches a few kA, and paralleling is required to match comparable current capacity with SiC devices.

Multiple modular ac–dc converters can be paralleled to meet the desired power level, while benefitting from enhanced manufacturability and cost reduction on maintenance. An interleaving among the modular converters can help reduce the size of the filters, thanks to ripple cancelation with cost of circulating current.

Various filter topologies can be a candidate for the modular converters. However, two difficulties present to design a filter for N-parallel converter. First, level of attenuation for harmonics may change according to N. Especially, in practice, the number of modular converters is determined by the customer's requirement and, in general, not known at the design stage. A state-space representation through $N \times N$ matrix offers an accurate mathematical description [1]. However, an approach with equivalent circuits can provide a physical insight for filter designers. Second, literature has investigated different filter topologies for paralleled converters, such as convention coupled inductor [2], integration between boost inductor and coupled inductor [3]–[5], or integrated coupled inductors [6], [7]. For a comparative evaluation, a design has to find filter parameters which can provide similar harmonic attenuation. This may not be straightforward considering flux-coupling of different structures. Furthermore, definition of terminologies such as circulating current or interpretation of flux-coupling vary depending on literature and may confuse the readers.

In an effort to deepen the understanding of parallel ac–dc converters, four equivalent per-phase circuits are proposed to provide an intuitive understanding for N-paralleled ac–dc converters. Based on symmetrical component theory, any voltage in three-phase can be decomposed into three symmetrical components, and the per-phase circuit simplifies the circuit analysis. In this letter, the symmetrical component theory is extended into N-parallel converters, and a per-converter analysis is proposed. A combination of per-phase analysis and per-converter analysis transforms N-paralleled converters into four single-phase circuits. Thanks to the simplicity, the proposed per-phase circuits provide an insight into the paralleled three-phase converters such as the change in harmonic attenuation for different N and comparison of different filter topologies including integrated inductors.

II. Symmetrical Theory and Per-Phase Circuit Model for a Three-Phase System

Holmes and Lipo [8] showed an analytical solution of carrier-based modulation as (1) when output frequency is $f_0(=\omega_0/2\pi)$ and carrier frequency is $f_c(=\omega_c/2\pi)$. The phase of f_0 term

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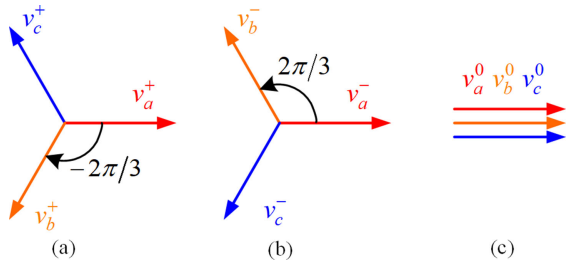


Fig. 1. Phasor diagrams for (a) positive-, (b) negative-, and (c) zero-sequence components for three-phase system.

is noted as θ_0, and the phase of the carrier is noted as θ_c. The magnitude of voltage at $mf_c + nf_0$ is labeled as $V_{m,n}$. Modulation index (MI) is defined as in (2)

$$v_x(t) = \sum_{n=1}^{\infty} V_{0,n}\cos(n\omega_0 t + n\theta_0) + \sum_{m=1}^{\infty} V_{m,0}\cos(m\omega_c t + m\theta_c) + \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} V_{m,n}\cos([m\omega_c + n\omega_0]t + m\theta_c + n\theta_0]) \tag{1}$$

$$\text{MI} = \frac{V_{0,1}}{V_{\text{dc}}/2}. \tag{2}$$

A symmetrical theory is commonly used for power system analysis [9], [10]. Any asymmetrical set of N phasors can be expressed as a linear combination of N symmetrical set of phasors as shown in Fig. 1. In the three-phase system, positive-$(v_x^+(t))$, negative-$(v_x^-(t))$, and zero-sequence components$(v_x^0(t))$ form this symmetrical set as

$$v_x(t) = v_x^+(t) + v_x^-(t) + v_x^0(t), x \in a, b, c. \tag{3}$$

Equation (1) shows that $\theta_0(=0, 2\pi/3, -2\pi/3)$ impacts the phase of harmonics. When $n = 3p \pm 1$ (p is a nonzero integer), these frequency components form $v_x^{\pm}(t)$. When $n = 3p$, three-phase voltages are in-phase and form $v_x^0(t)$. Therefore, any frequency component of pulsewidth modulation (PWM) voltage can be classified according to symmetrical component theory [7]. A frequency spectrum of PWM voltage with three-level space vector PWM (SVPWM) is shown in Fig. 2.

On time-domain waveform, (4) holds for both $v_a^+(t)$ and $v_a^-(t)$, and the response of the circuit is similar between the two. They are often labeled as differential-mode (DM) components

$$v_a^{\pm}(t) + v_b^{\pm}(t) + v_c^{\pm}(t) = 0. \tag{4}$$

Equation (5) holds for $v_x^0(t)$. The high-frequency parts may disturb other equipment, and electromagnetic interference (EMI) standards refer to this as common-mode (CM) noise of three-phase system

$$v_a^0(t) = v_b^0(t) = v_c^0(t). \tag{5}$$

When the impedance is balanced, per-phase analysis simplifies the circuit. An example circuit is shown in Fig. 3. For DM

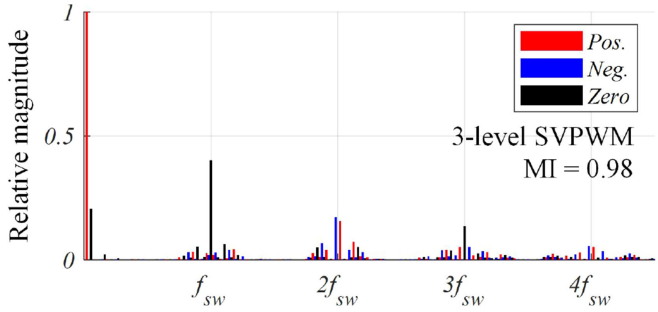


Fig. 2. Three symmetrical components on frequency spectrum of three-level PWM voltage.

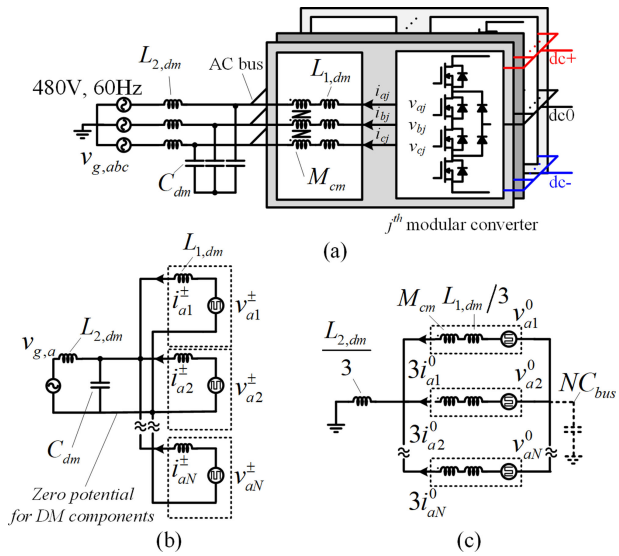


Fig. 3. Per-phase circuit for N-parallel converter. (a) Full circuit. (b) Per-phase circuit for positive- and negative-sequence components. (c) Per-phase circuit for zero-sequence component.

currents $(i_x^{\pm}(t))$, there is no path for neutral nodes, and these nodes are considered as the zero-potential as shown in Fig. 3(b). Note that the leakage inductance of CM choke is neglected in Fig. 3(b). The circuit for zero-sequence current$(i_x^0(t))$ can be similarly derived as Fig. 3(c). Note that $i_x^0(t)$ is defined as the zero-sequence current per-phase, and $3i_x^0(t)$ flows in the equivalent circuit. The phase-x current will be combination of these two components as

$$i_x(t) = i_x^{\pm}(t) + i_x^0(t). \tag{6}$$

III. Per-Converter Circuit for Interleaved AC-DC Converters

With the symmetrical interleaving, θ_c in (1) is set to $(j-1)\frac{2\pi}{N}$ for jth converter. As an example, the phasor diagram at f_{sw} is drawn in Fig. 4(a). Only at multiple of Nf_{sw}, the phase of harmonic voltages are in-phase as Fig. 4(b).

The symmetrical component theory can be extended to any poly-phase system including paralleled converters [9]. With N paralleled converters, there exist N symmetrical components as shown in Fig. 4. Among them, $N-1$ components are classified as circulating component $(v_{\text{cir},xj}(t))$, and (7) holds similar to (4).

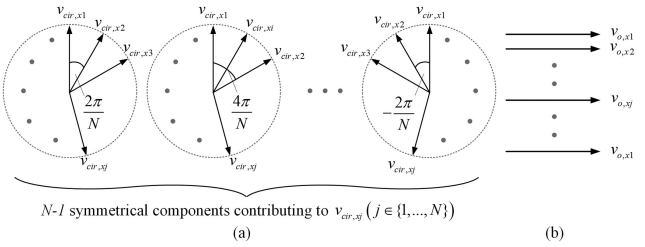


Fig. 4. Phasor diagrams for (a) circulating and (b) in-phase components in interleaved converters.

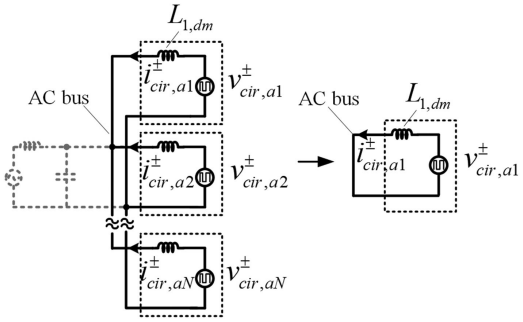


Fig. 5. Derivation of per-converter circuit for positive- and negative-sequence circulating currents ($i^{\pm}_{\text{cir},a1}$).

Only harmonics at qNf_{sw} (q is a positive integer) are in-phase ($v_{\text{out},xj}(t)$), and (8) holds similar to (5)

$$\sum_{j=1}^{N} v_{\text{cir},xj}(t) = 0, x \in a, b, c \tag{7}$$

$$v_{\text{out},x1}(t) = v_{\text{out},x2}(t) = \cdots v_{\text{out},xN}(t). \tag{8}$$

Therefore, per-converter circuit can be derived using symmetrical component theory similar to the per-phase circuit. For positive, and negative sequence circulating component ($v^{\pm}_{\text{cir},xj}(t)$), node of ac bus in Fig. 5 is zero-potential if the impedance of each converter is balanced. It can be converted into a single-phase circuit as shown in Fig. 5. In a similar manner, the same for zero sequence circulating component ($v^{0}_{\text{cir},xj}(t)$) can be derived from Fig. 3(c). The per-converter circuit for $v^{\pm}_{\text{out},xj}(t)$ and $v^{0}_{\text{out},xj}(t)$ can also be easily derived.

Combining the per-phase circuits and per-converter circuit, the proposed per-phase circuits are as shown in Fig. 6. Using (4), (5), (7), and (8), the voltage source for each circuit can be derived from PWM voltage. Then, the current of jth converter can be analyzed by these four single-phase circuits as

$$i_{xj}(t) = i^{\pm}_{\text{out},xj}(t) + i^{\pm}_{\text{cir},xj}(t) + i^{0}_{\text{out},xj}(t) + i^{0}_{\text{cir},xj}(t). \tag{9}$$

Thanks to the simplicity by single-phase representation, the proposed per-phase circuits provide intuitive understanding on the paralleled ac–dc converter. Based on four per-phase circuits, impact of each passive filter component on four groups of currents or change of circuit response depending on N can be easily understood. Related issues are also summarized in the same figure.

Note that the derivation of per-phase circuits assumes ideal symmetry between the paralleled ac–dc converters, such as

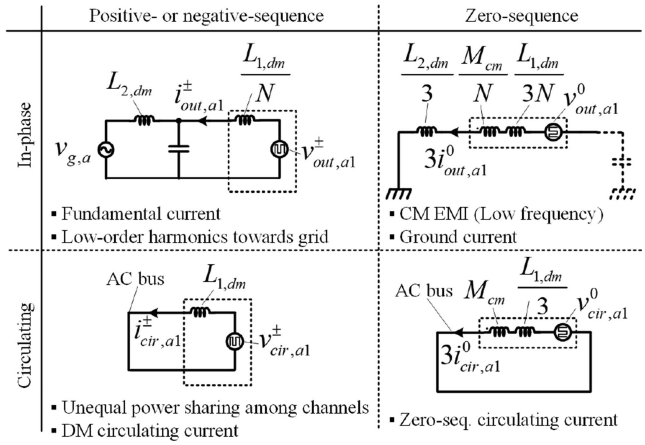


Fig. 6. Four per-phase equivalent circuits to interpret three-phase N-parallel converters.

the balanced impedance, identical load-sharing, and accurate interleaving. In practice, this is not feasible, and there exists coupling between four per-phase circuits. For example, by unbalanced impedance, a part of $i^{0}_{\text{out},xj}(t)$ can be generated from $v^{\pm}_{\text{out},xj}(t)$ or a part of $v^{\pm}_{\text{cir},xj}(t)$ may contribute to $i^{\pm}_{\text{out},xj}(t)$, thus, total harmonic distortion (THD) of grid-side current. Also, derivation of the modeling starts from classification of voltage harmonics on frequency domain. Therefore, prediction of high-frequency current may not be valid as similar to the other frequency-domain modelings to cover EMI phenomena. However, at a relatively low frequency range, the modeling can provide insight on circulating current and grid-side current for any N.

IV. Example of Analysis Based on Four Per-Phase Circuits

A. Estimation of Peak Value for $i^{\pm}_{cir,xj}$, and $i^{0}_{cir,xj}$ for Any N

While the low frequency components of $i^{\pm}_{\text{cir},xj}$ or $i^{0}_{\text{cir},xj}$ are mitigated by control, the peak value of the high-frequency components impacts the design of intercell transformers. The analytical solutions are derived for $N = 2$ [5], [6], [11] and $N = 3$ [4] for a specific topology and modulation. However, it is not easy to derive the peak values for any N or each of topology and modulation schemes. Thanks to simplicity of the proposed equivalent circuit approach, this can be easily estimated.

With interleaving, all harmonics will become $v^{\pm}_{\text{cir},xj}(t)$ or $v^{0}_{\text{cir},xj}(t)$ in Fig. 7 when $N \to \infty$. For $v^{\pm}_{\text{out},xj}(t)$ and $v^{0}_{\text{out},xj}(t)$, DM voltage reference ($v^{\pm *}_{xj}$) from kVA command, and zero-sequence voltage reference (v^{0*}_{xj}) will determine the magnitude and phase

$$\begin{cases} \lim_{N\to\infty} v^{0}_{\text{cir},xj}(t) = v^{0}_{xj}(t) - v^{0*}_{xj}(t) \\ \lim_{N\to\infty} v^{\pm}_{\text{cir},xj}(t) = v^{\pm}_{xj}(t) - v^{\pm *}_{xj}(t). \end{cases} \tag{10}$$

The integration of (10) is the flux-linkage corresponding to the circulating current when $N \to \infty$ ($\lim_{N\to\infty} \lambda^{0}_{\text{cir},xj}$, $\lim_{N\to\infty} \lambda^{\pm}_{\text{cir},xj}$). Based on PLECS simulation result, Fig. 7 compares the peak of $\lambda^{0}_{\text{cir},xj}$ and $\lambda^{\pm}_{\text{cir},xj}$ from $N = 2$–9 to that of $N \to \infty$ under three-level SVPWM. For any N, the peak value of $\lambda^{0}_{\text{cir},xj}$ stays

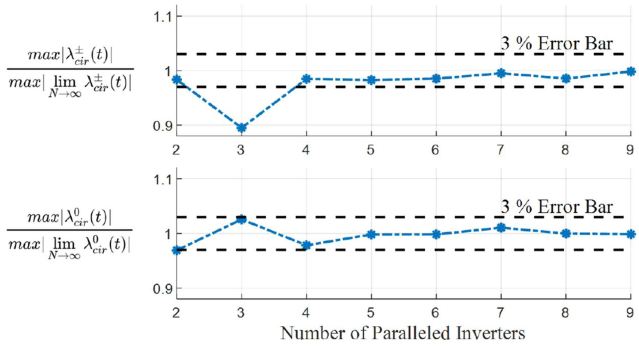


Fig. 7. Comparison of peak of voltage*sec corresponding to $i^{\pm}_{\mathrm{cir},x1}$ and $i^{0}_{\mathrm{cir},x1}$.

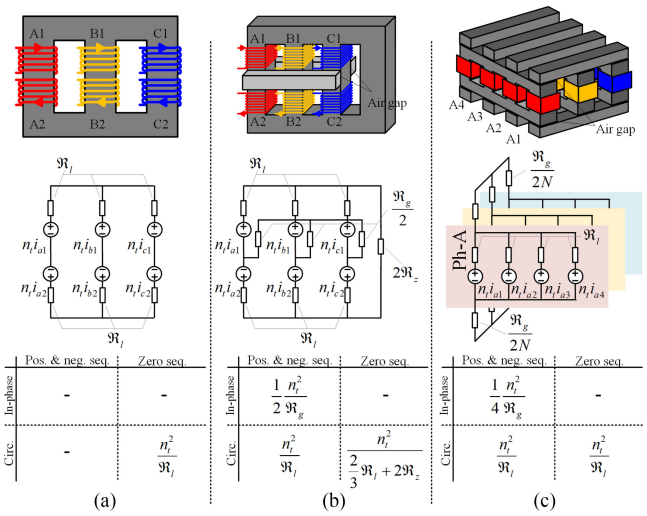


Fig. 8. Structure, magnetic circuit, and effective impedance table for $i^{\pm}_{\mathrm{out},x}$, $i^{0}_{\mathrm{out},x}$, $i^{\pm}_{\mathrm{cir},x1}$, and $i^{0}_{\mathrm{cir},x1}$. (a) DM coupled inductor [6]. (b) Four-limb coupled inductor with integrated boost inductance [5]. (c) Monolithic configuration of coupled inductor with integrated boost inductance [4].

within 3% error. Therefore, the peak values with the filter in Fig. 3 can be approximated for any N as an example as follows:

$$\begin{cases} \max|i^{\pm}_{\mathrm{cir},x1}(t)| \approx \frac{1}{L_{1,\mathrm{dm}}} \int (v^{\pm}_{x1}(\tau) - v^{\pm *}_{x1}(\tau))d\tau \\ \max|i^{0}_{\mathrm{cir},x1}(t)| \approx \frac{1}{3M_{\mathrm{cm}}+L_{1,\mathrm{dm}}} \int (v^{0}_{x1}(\tau) - v^{0*}_{x1}(\tau))d\tau. \end{cases} \tag{11}$$

B. Effective Inductance for Comparison of Different Integrated Magnetic Methods

Literature reported various magnetic integration methods to reduce total size of filter. The proposed model can be extended to the magnetic circuits. Then, effective impedance of the different integration methods by flux-coupling can be easily compared.

As an example, three structures of integrated inductors [4]–[6] and their magnetic circuits are shown in Fig. 8. n_t refers to turns number. $\Re_c$ and $\Re_g$ are reluctance of a magnetic limb and air gap, respectively. $\Re_z$ refers to reluctance of fourth limb in Fig. 8(b). The effective inductance table for groups of voltage can be derived based on four per-phase circuits. From (11) and the effective inductance, $\max|i^{\pm}_{\mathrm{cir},x1}(t)|$ and $\max|i^{0}_{\mathrm{cir},x1}(t)|$ can be estimated.

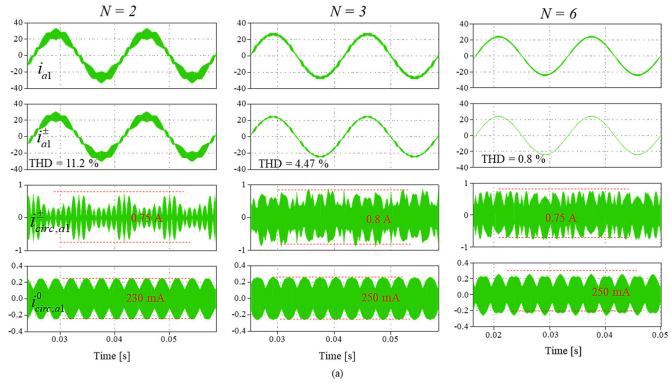


Fig. 9. (a) Simulation waveforms of $i^{\pm}_{\mathrm{out},x1}$, $i^{\pm}_{\mathrm{cir},x1}$, and $i^{0}_{\mathrm{cir},x1}$ for different N.

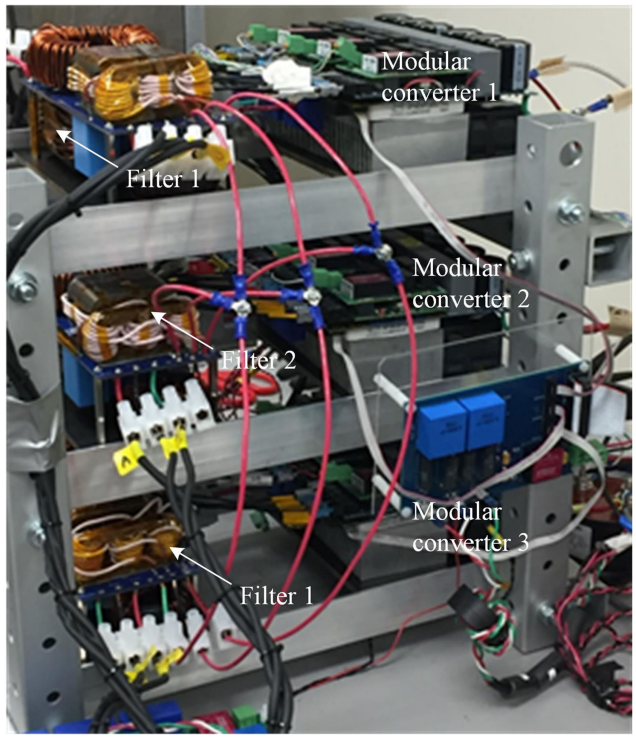
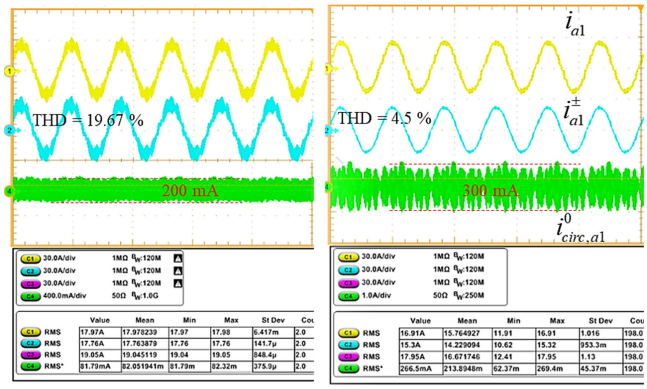


Fig. 10. Experimental setup with three paralleled NPC converters.

A filter designer can determine magnetic circuit parameters to have similar harmonic attenuation, and then size and loss of each filter topology can be compared after design optimization.

V. Simulation Result

To verify the proposed modeling approach, a PLECS simulation has been performed for the circuit in Fig. 3(a). SVPWM is used. DC-link voltage is 750 V, and f_{sw} is set to 32 kHz. The filter parameters are $L_{1,\mathrm{dm}} = 100\,\mu$H, $M_{1,\mathrm{cm}} = 4$ mH. No filters exist on the grid side. The waveform of $i^{\pm}_{\mathrm{out},x1}(t)$, $i^{\pm}_{\mathrm{cir},x1}(t)$, and $i^{0}_{\mathrm{cir},x1}(t)$ are compared in Fig. 9 for different N at 13.3 kW. The estimated value based on (11) is shown using red line. As Fig. 7, the peak of $i^{\pm}_{\mathrm{cir},x1}(t)$ and $i^{0}_{\mathrm{cir},x1}(t)$ remains similar to the estimation for $N = 2$, 3, and 6.



(b)

Fig. 11. Experimental waveform of currents for $N = 2$ and $N = 3$.

VI. Experimental Result

To verify the modeling, three paralleled modular converters are built as shown in Fig. 10. Neutral point clamped (NPC) converters are paralleled. The operating condition is as the same as Section IV. Time-domain waveform for total circulating current under active front end mode were experimentally verified as per Fig. 11 for two and three channels. Due to the lack of real estate and complexity, the experimental setup could not be extended to more than three channels. It can be observed that the peak circulating current does not change significantly between two and three parallel channels. The difference between simulation and experiment is originated by low-frequency circulating current. This low-frequency effect is severe with a larger number of parallel converters. The experimental results validates that a modeling approach by four per-phase circuits can predict circuit behavior of N parallel converters.

VII. Conclusion

By extending symmetrical component theory, four per-phase equivalent circuits for N paralleled three-phase ac–dc converters are proposed. Thanks to its simplicity, the proposed circuit can provide an intuitive insight N-parallel converters. Also, the modeling can be easily extended for any filter topology and help to evaluate different filter topologies including integrated inductors. This would help filter designers to understand dynamics of different groups of harmonic currents and their impacts on filter design. Analysis on an impact of unbalance or asymmetry based on the per-phase circuits remains a future work.

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