Improved Maximum Boost Control and Reduced Common-Mode Voltage Switching Patterns of Three-Level *Z*-Source Inverter

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***Abstract*—The maximum boost control (MBC) technique of voltage boosting offers the highest output voltage gain among other boost control techniques of *Z*-source inverter (ZSI). But, this technique suffers from the major drawback of sixth fundamental frequency (6^{th}F1) ripple components of the impedance network inductor current. Due to this, the size/cost of the impedance network increases, which limits the practical applications of MBC. This article proposes an improved version of MBC via appropriate modification in the conventional space vector pulse width modulation of three-level ZSI (3L-ZSI). The improved MBC eliminates the problem of the 6^{th}F1 impedance network inductor current ripple of 3L-ZSI without affecting its input/output gain and switching stress across power switches as compared to the existing MBC. Also, two new improved reduced common-mode voltage (RCMV) switching patterns have been proposed. As compared to the existing ones, the proposed RCMV switching patterns of 3L-ZSI offers reduced size of the impedance network while limiting the common-mode voltage magnitude to one-sixth of the available dc-link voltage. The above-mentioned findings have been successfully validated using theoretical analysis, simulation, and experimental results.**

***Index Terms*—Common-mode voltage (CMV), controlled diode bridge clamped (CDBC) *Z*-source inverter (ZSI), maximum boost control (MBC), space vector pulse width modulation (SVPWM), three-level ZSI (3L-ZSI).**

I. Introduction

THE arrangement of impedance network-based single-stage buck–boost dc to ac power conversion is popular in distributed power generation applications [1]–[2]. This arrangement offers reduced cost, increased reliability, and improved power quality features as compared to the conventional voltage source inverters (VSIs). From the aspect of power quality and *dv*/*dt* across power switches, multilevel inverter configurations are a better option [3]. Impedance network-based various three-level buck–boost inverter topologies present in the literature are: *Z*-source/qZ-source inverters [4]–[18], *LC* switching based neutral-point clamped inverters [19], LCCT-derived three-level inverters [20], switched boost inverters [21]–[23], and topology of those presented in [24]. The major difference between these topologies is the type of an impedance network used before the inverter switches. The common aspect of these inverters is the integration of the shoot-through (ST) state into the pulsewidth modulation (PWM) switching pattern. ST state is used to short circuit the impedance network. Normally, the null interval of the PWM technique is used for ST insertion.

Depending upon the utilization of the null interval as ST state, three main voltage boosting techniques in ZSI are as follows: simple boost control (SBC) [15], maximum boost control (MBC) [25], and maximum constant boost control (MCBC) [30]. Out of SBC, MBC, and MCBC, the maximum utilization of the null interval has been done in MBC to increase the output voltage gain of the inverter and to reduce the switching stress across the power switches. Whether two-level or three-level VSI/ZSI, the null interval always changes with frequency equals to six times the fundamental frequency. Since the null interval of each carrier cycle is fully replaced by ST states in MBC, it causes lower order ripple components in the impedance network inductor current. This drawback limits the practical applications of the MBC technique.

Next, the magnitude and the rate of change of common-mode voltage (CMV) is an important concern when inverters are used in motor drives or any distributed power generation application. The major problems associated with CMV are ground leakage current in photo voltaic (PV) power generation, shaft voltage, bearing currents, and electromagnetic interference in motor drive application [2], [7], [15], [16]. The existing reduced CMV (RCMV) techniques of 3L-ZSI/q-ZSI have been analyzed based on some important factors. Their detailed analysis is summarized in Table I.

In this article, first, an improved MBC (IMBC) has been proposed by modifying the conventional space vector pulse width modulation (SVPWM) switching diagram of three-level ZSI (3L-ZSI). The modified SVPWM doubles the frequency of the null interval as compared to the conventional SVPWM. This helps in eliminating the problem of 6th F1 ripple components of inductor current prevailed in existing MBC. After that, two new RCMV switching patterns have been proposed for a 3L-ZSI. The following major demerits (see Table I) have been considered to avoid in the proposed RCMV switching patterns:

1) unbalanced inductor voltage boosting per carrier cycle as in origin shifted 60° discontinuous of [4];

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TABLE I
ANALYSIS OF EXISTING RCMV PWM TECHNIQUES OF 3L-ZSI /Q-ZSI

Existing techniques	Merits	Demerits	Remarks
Origin shifted 60 degree discontinuous of [4],	➢ Nearest three vector (NTV) switching ➢ CMV limited to $\pm BV_{dc}/6$	➢ Unbalanced inductor voltage boosting per carrier cycle ➢ Large inductor size requirement	➢ Used either upper or lower ST state in half carrier cycle
APOD of [5], [8]	➢ CMV limited to $\pm BV_{dc}/6$ ➢ Balanced inductor voltage boosting per carrier cycle	➢ Non -NTV switching ➢ Require synchronization of two phase legs for ST insertion if minimum six switching transitions per half carrier cycle is desired	➢ Used full dc-link ST state, 1 per half carrier cycle
RCM of [6] and [7]	➢ Ideally zero CMV ➢ Balanced inductor voltage boosting per carrier cycle	➢ Increased switching transitions (12 per half carrier cycle) ➢ Non-NTV switching ➢ Large switching vector are unused. This leads to underutilization of available dc link	➢ Used full dc-link ST state, 2 per half carrier cycle
Switching technique of [15], [16]	➢ CMV limited to $\pm BV_{dc}/6$ ➢ Balanced inductor voltage boosting per carrier cycle	➢ Increased switching transitions (8 per half carrier cycle) ➢ Non-NTV switching	➢ Used full dc-link ST state, 1 per half carrier cycle
Common demerit of sine –triangle comparison based PWM techniques ➢ Increased complexity of implementation because at least 5 reference signal and 2 triangular signal are required for the generation of gating signals. The number of reference signal increases further if the range of modulation index up to 1.15 is desired.			

2) increased number of switching transitions per carrier cycle as in RCMV technique of [6] and [7] and switching technique of [15] and [16];
3) increased complexity of implementation of ST state arises due to phase legs synchronization as in alternate phase opposition disposition (APOD) of [5] and [8];
4) increased size of the impedance network because of the lower switching frequency of the impedance network [4],[5],[8],[15],[16];
5) the complexity of overall implementation as the sine-triangle comparison approach of PWM generation requires several reference signals for the generation of gating pulses.

Depending upon the RCMV switching patterns, the proposed PWM techniques have been named as ZSVM_1TI and ZSVM_2TI. Both proposed techniques use the same modified SVPWM switching diagram and IMBC of voltage boosting. These techniques of 3L-ZSI results in reduced CMV magnitude (limited to one-sixth of available dc-link voltage), reduced size of impedance network, increased dc bus utilization, and ease of implementation of ST states.

This article is organized as follows. Section II gives a brief introduction to the 3L-ZSI. Existing and proposed modified SVPWM switching diagrams have been explained in Section III. Section IV presents a detailed explanation of the improved MBC of the 3L-ZSI. In Section V, the proposed RCMV switching patterns have been presented. Comparison of the switching techniques have been given in Section VI. Simulation and experimental results have been presented in Section VII and Section VIII gives a final discussion. Finally, Section IX concludes this article.

II. THREE-LEVEL ZSI (3L-ZSI)

The two main three-level inverter topologies popular in ZSI/q-ZSIs are neutral-point clamped configuration [4] and T-type configuration [9]. For low-voltage applications, T-type configurations are beneficial as compared to the NPC configuration [26]. This article uses alternate configuration, which is a controlled diode bridge clamped (CDBC) three-level inverter [27]. This topology is very similar to the T-type except the type of the bidirectional switch. CDBC configuration based 3L-ZSI is shown in Fig. 1. The main motive to use CDBC configuration based ZSI is given in Section VI-C. The operating principle of a CDBC ZSI can be understood from Table II. The switching states have been denoted using four letters, "P," "O," "N," and "F." The letter "P" indicates that the phase leg is connected to the positive dc bus by ON upper switch of a phase leg. Similarly, the letter "O"/ "N" indicates that the phase leg is connected to the midpoint/ negative point of the dc bus by ON middle/lower switch of a phase leg. The letter "F" indicates that the phase leg is shorted via upper and lower switches ON of the same phase

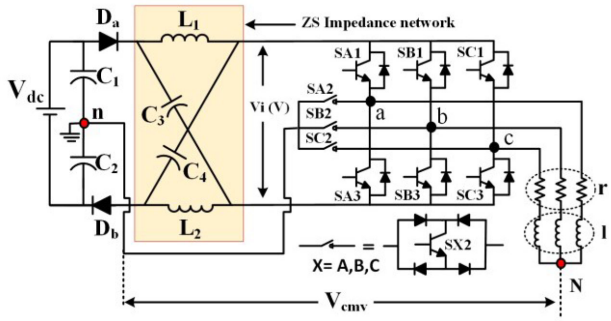


Fig. 1. Configuration of three-phase three-level controlled diode bridge clamped (CDBC) ZSI.

TABLE II
SWITCHING STATES OF CDBC ZSI

Switching state type	ON switch	V_{Yn}(pole voltage)	States/switches position
NST	SX1	$0.5.BV_{dc}$	P/100
NST	SX2	0	O/010
NST	SX3	$-0.5.BV_{dc}$	N/001
FST	SX1, SX3	0	F/101

X = A, B, C and Y = a, b, c

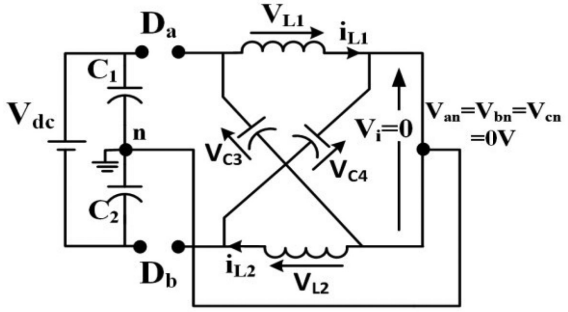


Fig. 2. Equivalent circuit diagram of 3L-ZSI during FST state.

TABLE III
DESCRIPTION OF USED ST VECTORS

ST vectors	Pole Voltage	Line Voltage	CMV
FON, OPF, NFO, FOP, ONF, PFO, POF, OFN, FPO, NOF, OFP, FNO	$V_{an} = V_{bn} = V_{cn} = 0$	$V_{ab} = V_{bc} = V_{ca} = 0$	$V_{cmv} = 0$

leg. The position of power switches during switching states P, O, N, and F is shown in Table II.

In this article, the approach of full dc-link ST (FST) [5] has been used. The equivalent circuit diagram of the 3L-ZSI during the FST state is shown in Fig. 2.

Used ST switching vectors and their generated pole/line voltage and CMV have been tabulated in Table III. These vectors produce zero pole/line voltage and zero CMV irrespective of the switching position of the individual phase legs.

A quick review of the applicable formulas for the 3L-ZSI operating under FST approach (considering $L_1 = L_2 = L;\ C_3 = C_4 = C$) is given as follows [25].

Peak dc-link voltage ($\hat{v}_i$):

$$\hat{v}_i = \left(\frac{1}{1-2\cdot D}\right)\ V_{dc} = BV_{dc} \tag{1}$$

$$B = \frac{1}{1-2\cdot D} \tag{2}$$

where "*D*" and "*B*" are ST duty ratio and boost factor, respectively.

The voltage gain "*G*" of the inverter and the switching stress across inverter switches "V_s"can be expressed as

$$G = M\cdot B \tag{3}$$

where "*M*" is the modulation index

$$V_s = BV_{dc}. \tag{4}$$

The CMV is defined as

$$V_{cmv} = \frac{V_{an}+V_{bn}+V_{cn}}{3} \tag{5}$$

where $V_{an}, V_{bn}, \text{and } V_{cn}$ are the pole voltages.

III. Proposed Modified SVPWM Switching State Diagram

The conventional and the proposed modified SVPWM switching diagrams differ in the length and dwell time duration of switching vectors. This is illustrated as follows.

A. Brief Review of the Conventional SVPWM Switching Diagram

The conventional SVPWM switching state diagram is shown in Fig. 3(a). For the reference sinusoidal line-voltage signals of peak equal to $1\cdot BV_{dc}$, the magnitude of the resultant signal is always constant (i.e., $1\cdot BV_{dc}$). This is shown in Fig. 4. Mathematically, these reference line-voltage signals can be written as

$$V_{ab} = \sin\left(2\pi/3 + \alpha\right) \tag{6}$$

$$V_{bc} = \sin(\alpha) \tag{7}$$

$$V_{ca} = \sin\left(4\pi/3 + \alpha\right). \tag{8}$$

As per Clark's transformation, the calculated lengths (line quantities) of large (V1–V6) and medium (V13–V18) switching vectors are $1.154\cdot BV_{dc}$ and $1\cdot BV_{dc}$, respectively.

As seen in Fig. 3(a), the maximum value of the reference vector (V_{ref}) in linear operating region is equal to the length of the medium vector

$$V_{ref,\ max} = 1\cdot BV_{dc}. \tag{9}$$

The modulation index, in this case, is defined as per [28]

$$M_{ex} = \frac{2\cdot V_{ref}}{\sqrt{3}\cdot BV_{dc}}. \tag{10}$$

The maximum modulation index can be found by substituting (9) into (10), which is given as follows:

$$M_{ex,\ (max)} = 1.154. \tag{11}$$

The maximum available rms value of the fundamental line voltage can be expressed as

$$V_{ab,\ rms}\ (\max) = \frac{\sqrt{3}}{2\sqrt{2}}\ M_{ex,(max)}\cdot BV_{dc}. \tag{12}$$

Substituting (11) into (12), we get

$$V_{ab,\ rms}\ (\max) = 0.707\cdot BV_{dc}. \tag{13}$$

The conventional SVPWM approach has been used in [15] for 3L-ZSI where the dwell time of switching vectors in triangle T1 have been calculated using the following formulas:

$$T_{a\_ex} = \left(\frac{V_{ref}}{1.15.BV_{dc}}\right)\left(\frac{\text{Sin}\left(\pi/6-\alpha\right)}{\text{Sin}\left(\pi/6\right)}\right).T_s \tag{14}$$

$$T_{b\_ex} = \left(\frac{V_{ref}}{1.BV_{dc}}\right)\left(\frac{\text{Sin}\left(\alpha\right)}{\text{Sin}\left(\pi/6\right)}\right).T_s \tag{15}$$

$$T_{z\_ex} = T_s - T_{a\_ex} - T_{b\_ex} \tag{16}$$

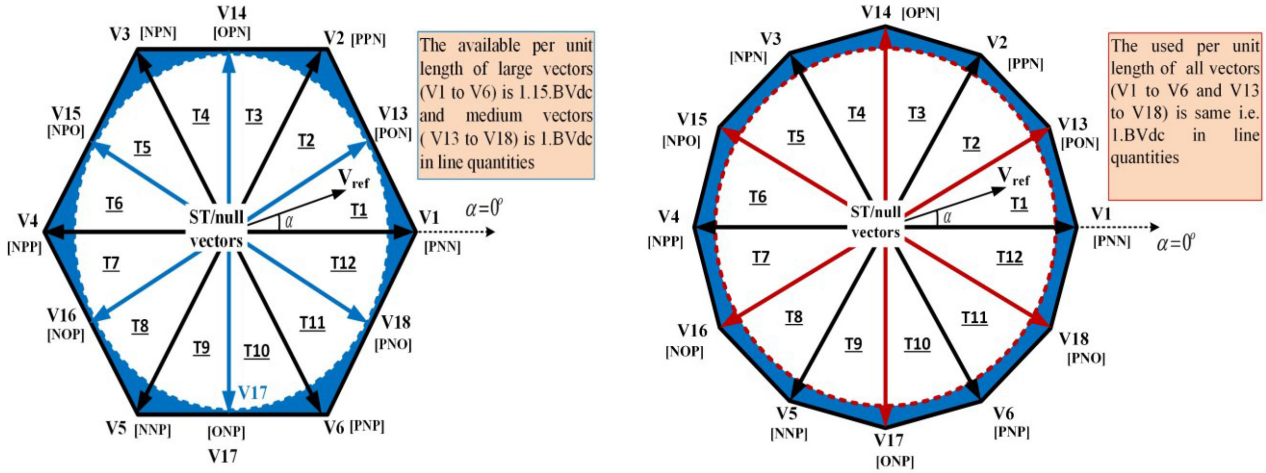


Fig. 3. SVPWM switching diagram of 3L-ZSI. (a) Conventional space vector hexagon [15]. (b) Proposed 12-sided polygon.

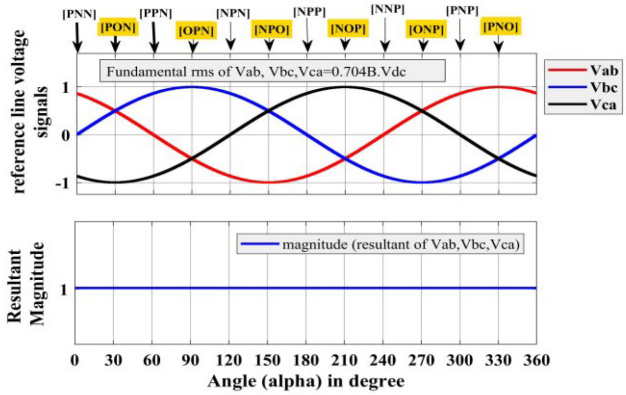


Fig. 4. Reference line voltages and their resultant magnitude signal of the conventional SVPWM.

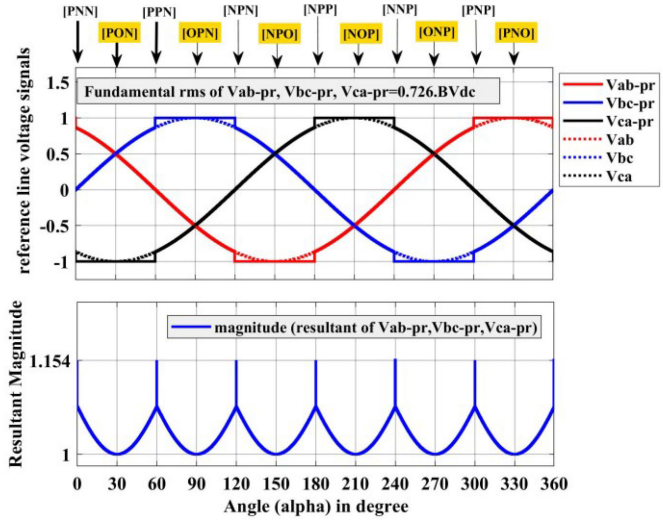


Fig. 5. Proposed modified reference line-voltage signals and their instantaneous resultant signal magnitude (IRSM).

where T_{a_ex}, and T_{b_ex} are the active vector time durations, T_{z_ex} is the time duration of the null vector, and T_s is the time duration of the half carrier cycle. The null interval (T_{z_ex}) changes six times the fundamental frequency in this case.

B. Proposed Modified SVPWM Switching Diagram

The modified SVPWM switching diagram is shown in Fig. 3(b). The objective of the proposed SVPWM is to double the frequency of the null interval as compared to the conventional. It is possible only if the length of large and medium switching vectors are equal. For this purpose, the required reference line-voltage signals have been modified, which are shown in Fig. 5. Mathematically the proposed modified reference line-voltage signals can be written as

$$\begin{aligned} V_{ab,pr} = &\left[\left\{\sin\left(2\pi/3+\alpha\right)\right\}\right]_{\alpha=0 \text{ to } \frac{2\pi}{3};\ \pi \text{ to} \frac{5\pi}{3};} \\ &+ \left[\left\{\sin\left(3\pi/2\right)\right\}\right]_{\alpha=\frac{2\pi}{3} \text{ to } \pi} \\ &+ \left[\left\{\sin\left(\pi/2\right)\right\}\right]_{\alpha=\frac{5\pi}{3} \text{ to } 2\pi} \end{aligned} \tag{17}$$

$$\begin{aligned} V_{bc,pr} = &\left[\left\{\sin\left(\alpha\right)\right\}\right]_{\alpha=0 \text{ to } \frac{\pi}{3};\ \frac{2\pi}{3} \text{ to} \frac{4\pi}{3};\ \frac{5\pi}{3} \text{ to } 2\pi} \\ &+ \left[\left\{\sin\left(\pi/2\right)\right\}\right]_{\alpha=\frac{\pi}{3} \text{ to } \frac{2\pi}{3}} \\ &+ \left[\left\{\sin\left(3\pi/2\right)\right\}\right]_{\alpha=\frac{4\pi}{3} \text{ to } \frac{5\pi}{3}} \end{aligned} \tag{18}$$

$$\begin{aligned} V_{ca,pr} = &\left[\left\{\sin\left(4\pi/3+\alpha\right)\right\}\right]_{\alpha=\frac{\pi}{3} \text{ to } \pi;\ \frac{4\pi}{3} \text{ to } 2\pi;} \\ &+ \left[\left\{\sin\left(3\pi/2\right)\right\}\right]_{\alpha=0 \text{ to } \frac{\pi}{3}} \\ &+ \left[\left\{\sin\left(\pi/2\right)\right\}\right]_{\alpha=\pi \text{ to } \frac{4\pi}{3}}. \end{aligned} \tag{19}$$

Fig. 5 also shows the IRSM of the modified reference line-voltage signals.

In contrast to the conventional SVPWM, the IRSM of modified reference line-voltage signals has frequency equals six times

TABLE IV
CALCULATIONS OF THE LENGTH OF SWITCHING VECTORS

Switching vectors	Length (per 1.BVdc)	Used length (as per available IRSM of Fig.5
Large, (V1 to V6)	$1.154 \times (1.\mathrm{BV_{dc}}) = 1.154.\mathrm{V_{dc}}$	$1.15 \times \left(\frac{1}{1.154}.\mathrm{BV_{dc}}\right) = 1.\mathrm{BV_{dc}}$
Medium, (V13 to V18)	$1 \times (1.\mathrm{BV_{dc}}) = 1.\mathrm{BV_{dc}}$	$1 \times (1.\mathrm{BV_{dc}}) = 1.\mathrm{BV_{dc}}$

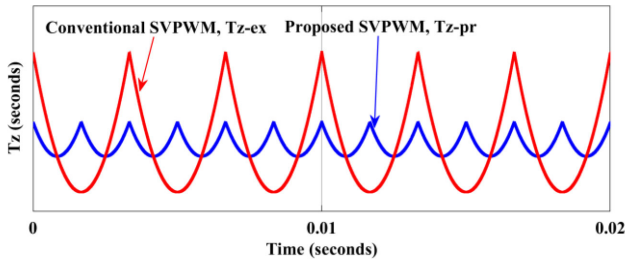


Fig. 6. Variation of the null interval over the fundamental cycle using the conventional and proposed SVPWM.

the fundamental frequency (50 Hz). Also, the resultant signal has the maximum IRSM of $1.15 \cdot BV_{\mathrm{dc}}$ at the position of large vectors (i.e., at $\alpha = 0°, 60°, 120°, 180°, 240°, 300°$).

The lengths of the switching vectors have been calculated based on the maximum available IRSM of reference line-voltage signals at the position of respective switching vector. The calculations of switching vector lengths have been provided in Table IV.

The reduction in the length of large switching vectors in proposed SVPWM consequently results in the modification of the dwell time duration of the switching vectors. This is shown as follows.

1) Dwell Time Calculation: Consider Fig. 3(b), the reference vector positioned in T1 can be realized using one large vector (V1), one medium vector (V13), and one or two appropriate ST vectors from Table III. The formulas used for the calculation of dwell time of switching vectors have been mentioned as follows:

$$T_{\mathrm{a\_pr}} = \left(\frac{V_{\mathrm{ref}}}{1 \cdot BV_{\mathrm{dc}}}\right)\left(\frac{\mathrm{Sin}\,(\pi/6 - \alpha)}{\mathrm{Sin}\,(\pi/6)}\right).T_{\mathrm{s}} \tag{20}$$

$$T_{\mathrm{b\_pr}} = \left(\frac{V_{\mathrm{ref}}}{1 \cdot BV_{\mathrm{dc}}}\right)\left(\frac{\mathrm{Sin}\,(\alpha)}{\mathrm{Sin}\,(\pi/6)}\right).T_{s} \tag{21}$$

$$T_{\mathrm{z\_pr}} = T_{\mathrm{s}} - T_{\mathrm{a\_pr}} - T_{\mathrm{b\_pr}} \tag{22}$$

where $T_{\mathrm{a\_pr}}$ and $T_{\mathrm{b\_pr}}$ are the active vector time durations, $T_{\mathrm{z\_pr}}$ is the time duration of the null vector, and T_{s} is the time duration of the half carrier cycle. From (20)–(22)

$$T_{\mathrm{a\_pr}}{}_{\alpha = \pi/12} = T_{\mathrm{b\_pr}}{}_{\alpha = \pi/12} \text{ and } T_{\mathrm{a\_pr}}{}_{\alpha\,=\,0} = T_{\mathrm{b\_pr}}{}_{\alpha = \pi/6}. \tag{23}$$

As shown in Fig. 6, the frequency of the null interval ($T_{\mathrm{z\_pr}}$) is 12 times the fundamental frequency, which is double as compared to $T_{\mathrm{z\_ex}}$ (16) of the conventional SVPWM.

From Fig. 3(b), since large and medium vectors are of unity length, the simple mathematical calculation gives the maximum value of reference vector ($V_{\mathrm{ref,\ max}}$) as

$$V_{\mathrm{ref,\ max}} = 0.96 \cdot BV_{\mathrm{dc}}. \tag{24}$$

The modulation index in the case of proposed SVPWM is defined as

$$M_{\mathrm{pr}} = \frac{4 \cdot V_{\mathrm{ref}}}{3 \cdot BV_{\mathrm{dc}}} \cdot (\mathrm{CF}). \tag{25}$$

The correction factor (CF) is

$$\mathrm{CF} = \frac{V_{\mathrm{ref,max}}}{\text{Average value of maximum IRSM}}. \tag{26}$$

The average value of the maximum IRSM is (see Fig. 5)

$$\text{Average value of maximum IRSM} = 1.028 \cdot BV_{\mathrm{dc}}. \tag{27}$$

Substituting (24) and (27) into (26) gives the value of CF as

$$\mathrm{CF} = 0.933. \tag{28}$$

The maximum modulation index using the proposed SVPWM can be found by substituting (24) and (28) into (25)

$$M_{\mathrm{pr,\ (max)}} = 1.19. \tag{29}$$

The maximum available rms value of the fundamental line voltage can be found using (12) and (29)

$$V_{\mathrm{ab}}\ (\mathrm{rms}) = (0.612 \times 1.19)\ \cdot B\ V_{\mathrm{dc}} = 0.728 \cdot BV_{\mathrm{dc}}. \tag{30}$$

Comparing (29) and (30) with (11) and (13), respectively, shows that the modulation index and available fundamental rms line voltage using the proposed modified SVPWM is 3% more as compared to that by the conventional SVPWM.

IV. PROPOSED IMBC

The null interval (22) of the modified SVPWM is completely replaced by ST states to realize IMBC. The analysis of the IMBC is given as follows.

A. Available ST Duty Ratio

The average value of the ST duty ratio using IMBC ($\bar{D}_{\mathrm{IMBC}}$) can be calculated using (20)–(22) as

$$(\bar{D}_{\mathrm{IMBC}}) = \frac{6}{\pi}\int_0^{\pi/6}\left(\frac{T_{\mathrm{z\_pr}}}{T_{\mathrm{s}}}\right)$$

$$= \frac{6}{\pi}\int_0^{\pi/6}\left[1 - \left\{\frac{\sin\,(\pi/6 - \alpha)}{\sin\,(\pi/6)} + \frac{\sin\,(\alpha)}{\sin\,(\pi/6)}\right\}\left(\frac{V_{\mathrm{ref}}}{BV_{\mathrm{dc}}}\right)\right] d\alpha. \tag{31}$$

Solving (31), we get

$$(\bar{D}_{\mathrm{IMBC}}) = 1 - \frac{12.\left(2 - \sqrt{3}\right) \cdot V_{\mathrm{ref}}}{\pi \cdot BV_{\mathrm{dc}}}. \tag{32}$$

From (25), we get

$$\frac{V_{\mathrm{ref}}}{BV_{\mathrm{dc}}} = \frac{3 \cdot M_{\mathrm{pr}}}{4 \cdot (\mathrm{CF})}. \tag{33}$$

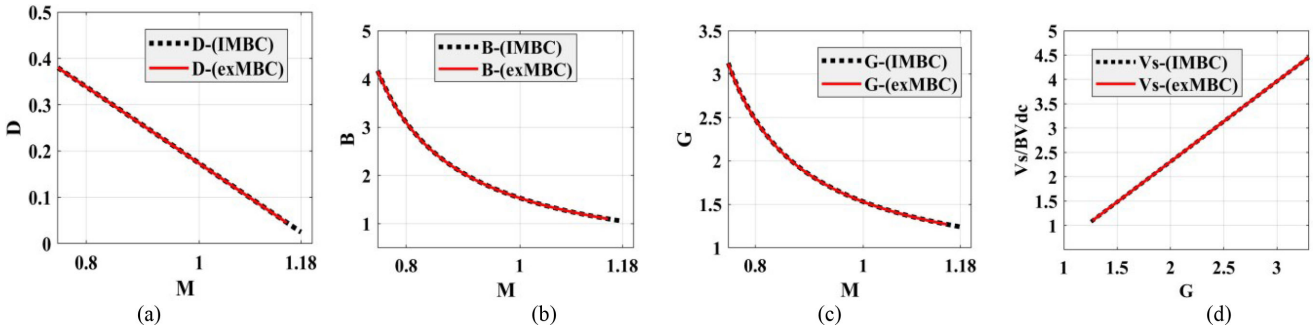


Fig. 7. Comparison of existing MBC [25] and improved MBC. (a) ST duty ratio versus modulation index. (b) Boost factor versus modulation index. (c) Gain versus modulation index. (d) Switching stress versus gain.

TABLE V
PROPOSED RCMV SWITCHING STATES PATTERN

T	ZSVM_1TI		ZSVM_2TI	
	Switching pattern	*	Switching pattern	*
T1	PON-FON-PNN	a	FON-PON-POF-PNN	a, c
T2	PON-FON -PPN	a	FON-PON-POF-PPN	a, c
T3	OPN- OPF-PPN	c	OPF-OPN-OFN-PPN	c, b
T4	OPN- OPF-NPN	c	OPF-OPN-OFN-NPN	c, b
T5	NPO- NFO-NPN	b	NFO-NPO-FPO-NPN	b, a
T6	NPO- NFO-NPP	b	NFO-NPO-FPO-NPP	b, a
T7	NOP- FOP-NPP	a	FOP-NOP-NOF-NPP	a, c
T8	NOP- FOP-NNP	a	FOP-NOP-NOF-NNP	a, c
T9	ONP- ONF-NNP	c	ONF-ONP-OFP-NNP	c, b
T10	ONP- ONF-PNP	c	ONF-ONP-OFP-PNP	c, b
T11	PNO- PFO-PNP	b	PFO-PNO-FNO-PNP	b, a
T12	PNO- PFO-PNN	b	PFO-PNO-FNO-PNN	b, a

*ST phase leg.

Substituting (33) into (32), the relationship between ST duty ratio and modulation index can be found

$$\left(\bar{D}_{\mathrm{IMBC}}\right) = \frac{\pi \cdot (\mathrm{CF}) - 9 \cdot M_{\mathrm{pr}} \cdot \left(2 - \sqrt{3}\right)}{\pi \cdot (\mathrm{CF})}. \quad (34)$$

On the other hand, the relationship between the ST duty ratio and the modulation index when the existing MBC [25] is applied in 3L-ZSI is

$$\bar{D}_{\mathrm{ex\_MBC}} = \frac{\left(2\pi - 3\sqrt{3} \cdot \mathrm{M_{ex}}\right)}{2\pi}. \quad (35)$$

The plots of ST duty ratio, boost factor, and gain versus modulation index and switching stress versus gain have been shown in Fig. 7 to illustrate the comparison between existing MBC and IMBC. Both, existing MBC and IMBC, give the same performance in terms of available ST duty ratio, boost factor, gain, and switching stress except the higher range of modulation index available with IMBC.

V. PROPOSED RCMV SWITCHING PATTERNS

Depending upon the number of ST states per half carrier cycle, the proposed switching patterns have been categorized under ZSVM_1TI and ZSVM_2TI PWM techniques. ZSVM_1TI and ZSVM_2TI are characterized by the use of one and two ST states per half carrier cycle, respectively. The switching states pattern per half carrier cycle for each triangle is tabulated in Table V for both techniques. The ST states have been equally distributed in all three phase legs. The important features of these switching patterns have been discussed in the next section.

TABLE VI
SWITCHING FREQUENCY OF THE IMPEDANCE NETWORK

Switching freq. of impedance network	Category 1(1 ST)		Category 2(2 ST)	
	ZSVM_1TI	M2= M3	ZSVM_2TI	M1
$F_{sw(imp)}$	$2F_s$	F_s	$3F_s$	$2F_s$

$F_s = 1/(2T_s)$.

VI. COMPARISON

It is the characteristic of MBC that it completely replaces the null states via ST states. This affects the switching frequency of the power switches. Therefore, to have a fair comparison, existing RCMV switching techniques have been also considered with completely replaced null states. After modification using existing MBC, the abbreviations used for the existing RCMV switching techniques are as follows:

M1 = RCMV switching technique of [6] and [7]
M2 = APOD technique of [5] and [8]
M3 = switching technique of [15].
ZSVM_1TI and ZSVM_2TI are the proposed switching techniques that use the IMBC approach of voltage boosting.

A. Switching Frequency of the Impedance Network

The switching frequency of the impedance network is an important consideration while designing the size of its inductors and capacitors. Fig. 8 shows the graphical representation of switching patterns, pole voltage, and CMV using ZSVM_1TI, ZSVM_2TI, M1, M2, and M3. The position of the ST state affects the switching frequency of the impedance network. For example, ZSVM_1TI, M2, and M3 have only one ST state per half carrier cycle but the switching frequency of the impedance network is double in the case of ZSVM_1TI as compared to those of M2 and M3. Depending upon the number of ST states per half carrier cycle, all switching techniques have been classified into two categories in Table VI. Table VI also contains the expressions of switching frequency of the impedance network. A plot between the carrier frequency and the switching frequency

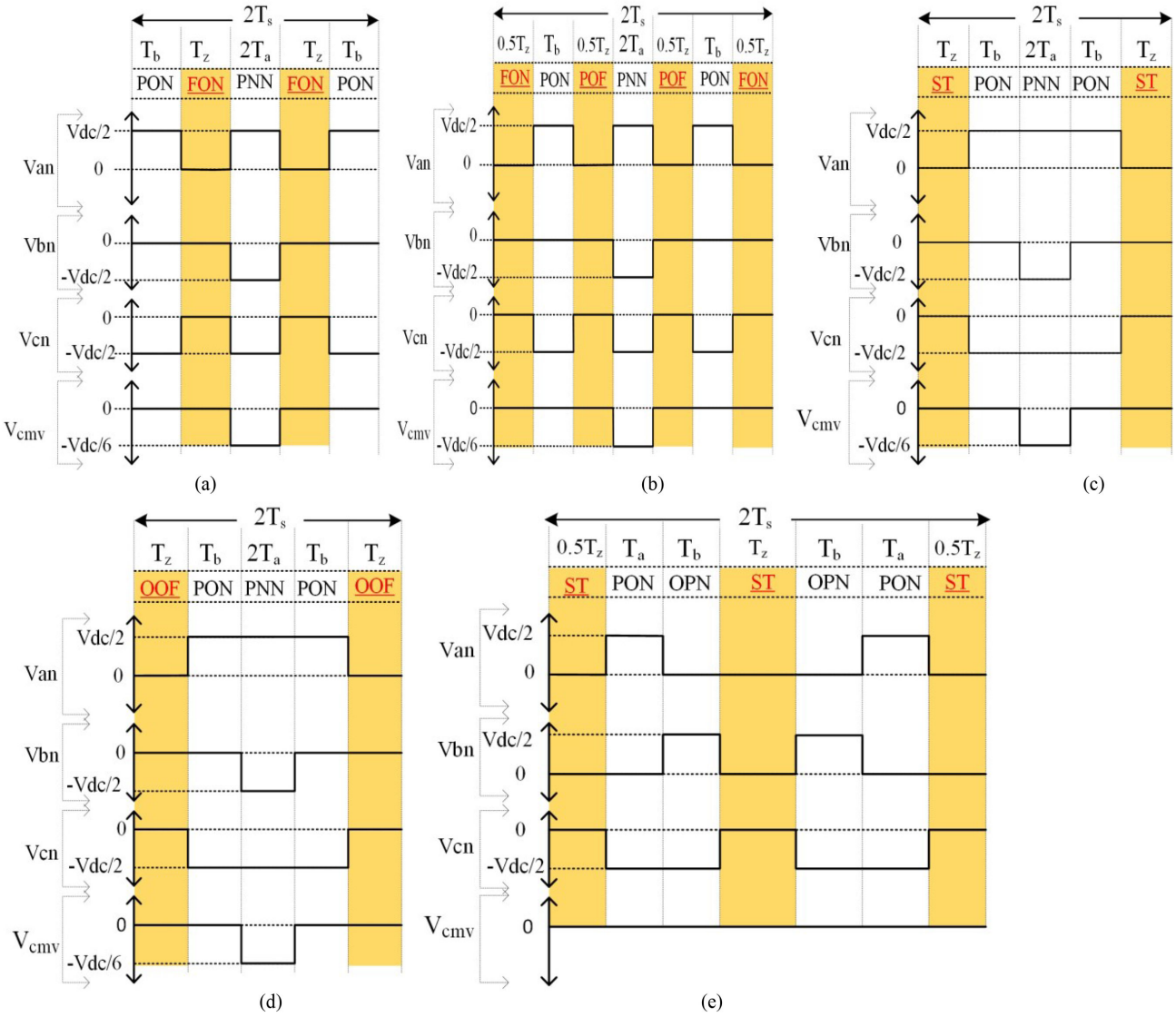


Fig. 8. Graphical description of the switching pattern, pole voltages, and CMV of the different RCMV PWM techniques. (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M2. (d) M3. (e) M1. Note—M2 and M3 differ only in the applied way of ST state. In M2, the ST state is applied via synchronization of two phase legs, whereas in M3, only one phase leg at a time is used for the ST state insertion. However, output waveforms of both are same.

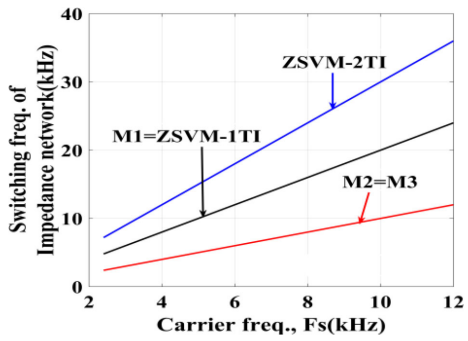


Fig. 9. Plot between carrier frequency and switching frequency of the impedance network using various RCMV switching techniques.

of the impedance network using considered PWM techniques is shown in Fig. 9.

B. Switching Frequency of the Power Switches

The inverter circuitry of a CDBC ZSI (see Fig. 1) has been taken for comparison. It is the characteristic of a CDBC ZSI/VSI [32] configuration that the switching frequency of the middle bidirectional switch (SX2) is different from the upper power switch (SX1) and lower power switch (SX3) in each phase leg $\{X = A, B, C\}$. The upper and lower switches (SX1 and SX3) of the CDBC ZSI have equal switching frequency. Here, the total average switching frequency (power switches) of the inverter has been compared using various PWM techniques. The formula used for calculating total average switching frequency (W) is

$$W = \frac{3\left(\sum\left(F_{\mathrm{sw}}\left(\mathrm{SX1}\right) + F_{\mathrm{sw}}\left(\mathrm{SX2}\right) + F_{\mathrm{sw}}(\mathrm{SX3})\right)\right)}{9}. \quad (36)$$

The switching frequencies of the power switches calculated using all PWM techniques at the various values of carrier frequency are tabulated in Table VII. In category 1 of the PWM

TABLE VII
SWITCHING FREQUENCY OF POWER SWITCHES USING VARIOUS RCMV PWM TECHNIQUES IN 3L-ZSI (CDBC)

Carrier Freq in KHz	Switching frequency of the power switches (IGBTs) in Hz									
	ZSVM_1TI		ZSVM_2TI		M1		M2		M3	
	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**
2.4	1250, 900	**1133**	1700, 900	**1433**	850, 4800	**2166**	450, 2400	**1100**	1400, 1800	**1533**
4.8	2450, 1700	**2200**	3300, 1700	**2766**	1650, 9600	**4300**	850, 4800	**2166**	2600, 3400	**2866**
7.2	3650,2500	**3266**	4900, 2500	**4100**	2450, 14400	**6433**	1250, 7200	**3233**	3800, 5000	**4200**
9.6	4850,3300	**4333**	6500, 3300	**5433**	3250, 19200	**8566**	1650, 9600	**4300**	5000, 6600	**5533**
12	6050,4100	**5400**	8100, 4100	**6766**	4050, 24000	**10700**	2050, 12000	**5366**	6200, 8200	**6866**

W is defined in (36), and X = (A, B, C).

techniques (defined in Table VI), the minimum "*W*" is offered by switching technique of M2, which is slightly (33 Hz) less than that of the proposed ZSVM_1TI. But it should be noted that the switching frequency of the impedance network is double in ZSVM_1TI as compared to that in M2 (see Table VI). In category 2, the proposed ZSVM_2TI offers 1.5 times more switching frequency of the impedance network even at reduced switching frequency of the power switches "*W*" as compared to the M1.

C. Important Feature of CDBC ZSI

The main drawback of a CDBC ZSI/VSI reported in [32, Tables III and IX] is that the switching frequency of the middle bidirectional switch is more as compared to that of upper and lower power switches of a phase leg. But this is not true with the proposed PWM techniques. As illustrated in Table VII, the switching frequency of the middle bidirectional switch is even lower than those of the upper and lower power switches of a phase leg when the proposed PWM techniques have been used in the CDBC ZSI configuration. In the existing RCMV PWM techniques, the switching frequency of the middle bidirectional power switch (SX2) is always greater than those of the upper and lower switches of each phase leg. It is also noted from Table VII that the switching frequency of the bidirectional switch (SX2) of CDBC ZSI is the same with those of the proposed ZSVM_1TI and ZSVM_2TI.

D. Comparison of Impedance Network Components Size

The switching frequency of the impedance network and the presence of the lower order harmonic components significantly affect the size of the impedance network. It is indicated in Fig. 9 that the switching frequency of the impedance network has the following order: ZSVM_2TI > ZSVM_1TI > (M2 = M3). First of all, consider important relationships of the existing MBC and IMBC. In the case of existing MBC, the ST duty ratio varies six times the fundamental frequency. The ST duty ratio as a function of α using existing MBC is given by [using (14)–(16)]

$$D(\alpha)_{\_\mathrm{exMBC}} = 1 - \frac{V_{\mathrm{ref}}}{BV_{\mathrm{dc}}}\left\{\sqrt{3}.\sin\left(\frac{\pi}{6}-\alpha\right) - 2\cdot\sin(\alpha)\right\};\quad \left(0<\alpha<\frac{\pi}{6}\right). \tag{37}$$

To be more specific, the null intervals $T_{\mathrm{z\_ex}}$ of (16) and $T_{\mathrm{z\_pr}}$ of (22) are denoted by $T_{\mathrm{z\_exMBC}}$ and $T_{\mathrm{z\_IMBC}}$ for the existing MBC and IMBC, respectively. Similarly, the modulation index denoted by M_{ex} of (10) and M_{pr} of (25) are denoted by $M_{\mathrm{ex\_MBC}}$ and $M_{\mathrm{pr\_IMBC}}$ for the existing MBC and proposed IMBC, respectively.

In (37), $D(\alpha)_{\_\mathrm{exMBC}}$ has the maximum value at $\alpha = 0^\circ$. Substituting $\alpha = 0^\circ$ in (37) and using (10), we get

$$D(\alpha = 0^\circ)_{\_\mathrm{exMBC\_max}} = \frac{T_{\mathrm{z\_exMBC\_max}}}{T_{\mathrm{s}}} = \left(1 - \frac{3}{4}M_{\_\mathrm{exMBC}}\right). \tag{38}$$

The modulation index of the existing MBC can be written in terms of boost factor using (2) and (35) as

$$M_{\_\mathrm{exMBC}} = \frac{(1+B)\,\pi}{3\sqrt{3}\,B}. \tag{39}$$

Using (39) in (38), the maximum null interval in a half carrier cycle can be written in terms of "*B*" as

$$T_{\mathrm{z\_exMBC\_max}} = \left\{1 - \frac{(1+B)\,\pi}{4\sqrt{3}\cdot\,B}\right\}T_{\mathrm{s}}. \tag{40}$$

On the other hand, in IMBC, the ST duty ratio as a function of angle (α) is given by (using 31)

$$D(\alpha)_{\_\mathrm{IMBC}} = \left[1 - \frac{2\cdot V_{\mathrm{ref}}}{BV_{\mathrm{dc}}}\left\{\sin\left(\frac{\pi}{6}-\alpha\right) + \sin(\alpha)\right\}\right];\quad \left(0<\alpha<\frac{\pi}{6}\right) \tag{41}$$

where $D(\alpha)_{\_\mathrm{IMBC}}$ of (41) has the maximum value at $\alpha = 0^\circ$

$$D(\alpha = 0^\circ)_{\_\mathrm{IMBC\_max}} = \left(1 - \frac{V_{\mathrm{ref}}}{BV_{\mathrm{dc}}}\right). \tag{42}$$

Substituting (33) into (42)

$$D(\alpha = 0^\circ)_{\_\mathrm{IMBC\_max}} = \frac{T_{\mathrm{z\_IMBC\_max}}}{T_{\mathrm{s}}} = \left(1 - \frac{3\cdot M_{\mathrm{pr\_IMBC}}}{4\cdot(\mathrm{CF})}\right). \tag{43}$$

The modulation index in terms of boost factor can be found using (2) and (34)

$$M_{\mathrm{pr\_IMBC}} = \frac{(1+B)\cdot(\mathrm{CF})\cdot\pi}{18\cdot B\cdot\left(2-\sqrt{3}\right)}. \tag{44}$$

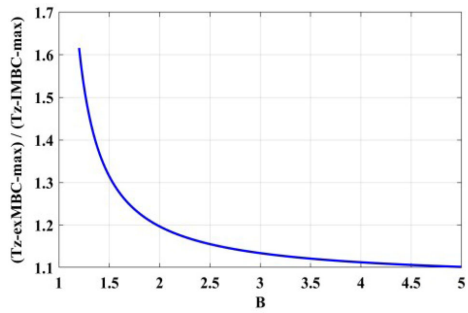


Fig. 10. Ratio of max duration of ST/null interval in a half carrier cycle using existing MBC and proposed IMBC [using (40) and (45)].

Using (43) and (44), the maximum null interval in a half carrier using IMBC can be expressed in terms of "*B*" as

$$T_{\mathrm{z\_IMBC\_max}} = \left\{1 - \left(\frac{(1+B)\,\pi}{24 \cdot \mathrm{B} \cdot \left(2-\sqrt{3}\right)}\right)\right\} T_{\mathrm{s}}. \quad (45)$$

For the range of "*B*" from $(1.2 \leq B \leq 5)$, the relationship between $T_{\mathrm{z\_exMBC\_max}}$ and $T_{\mathrm{z\_IMBC\_max}}$ is plotted in Fig. 10.

Mathematically, it can be written as [using (40) and (45)]

$$\left(1.10 \leq \frac{T_{\mathrm{z\_exMBC\_max}}}{T_{\mathrm{z\_IMBC\_max}}} \leq 1.61\right);\ \{5 \geq B \geq 1.2\}. \quad (46)$$

Next, the impedance network inductor current ripple ($\Delta\, I_{\mathrm{L1}} = \Delta\, I_{\mathrm{L2}} = \Delta I_{\mathrm{L}}$) and capacitor voltage ripple $\Delta\, V_{\mathrm{C3}} = \Delta\, V_{\mathrm{C4}} = \Delta V_{\mathrm{C}}$) can be written as a sum of high-frequency and low-frequency components of inductor current and capacitor voltage ripple as

$$\Delta\, I_{\mathrm{L}} = \Delta I_{\mathrm{Lh}} + \Delta I_{\mathrm{Ll}} \quad (47)$$

$$\Delta\, V_{\mathrm{C}} = \Delta V_{\mathrm{Ch}} + \Delta V_{\mathrm{Cl}}. \quad (48)$$

Now, consider the PWM techniques as follows.

1) Switching Techniques M2 and M3: From Fig. 8, the maximum duration of ST state seen by the impedance network using M2 and M3 is twice of the null interval (i.e., $2T_{\mathrm{z\_exMBC\_max}}$.). The high-frequency ripple components of impedance network inductor current and capacitor voltage using M2 and M3 can be written as [29]–[31]

$$\Delta\, I_{\mathrm{Lh\_exMBC}} = \frac{V_{\mathrm{C\_exMBC}}}{\mathrm{L_{exMBC}}} \cdot 2 \cdot T_{\mathrm{z\_exMBC\_max}} \quad (49)$$

$$\Delta\, V_{\mathrm{Ch\_exMBC}} = \frac{I_{\mathrm{L\_exMBC}}}{C_{\mathrm{exMBC}}} \cdot 2 \cdot T_{\mathrm{z\_exMBC\_max}}. \quad (50)$$

The sixth frequency components of inductor current and capacitor voltage using exiting MBC can be written as

$$\Delta\, I_{\mathrm{Ll\_exMBC}} = \frac{V_{\mathrm{pk2pk}}}{6\omega \cdot L_{\mathrm{exMBC}}} \quad (51)$$

$$\Delta\, V_{\mathrm{Cl\_exMBC}} = \frac{I_{\mathrm{pk2pk}}}{6\omega \cdot C_{\mathrm{exMBC}}} \quad (52)$$

where V_{pk2pk} and I_{pk2pk} are the peak-to-peak ripples across the inductor voltage and capacitor current, respectively. Using (47)–(52), the final expression for "*L*" and "*C*" for M2 and M3 can be written as

$$L_{\mathrm{exMBC}} = \underbrace{\frac{V_{\mathrm{C\_exMBC}}}{\Delta I_{\mathrm{Lh\_exMBC}}} \cdot 2 \cdot T_{\mathrm{z\_exMBC\_max}}}_{\text{high freq. component}} + \underbrace{\frac{V_{\mathrm{pk2pk}}}{6\omega \cdot (\Delta I_{\mathrm{Ll\_exMBC}})}}_{\text{sixth freq. component}} \quad (53)$$

$$C_{\mathrm{exMBC}} = \underbrace{\frac{I_{\mathrm{L\_exMBC}}}{\Delta V_{\mathrm{Ch\_exMBC}}} \cdot 2 \cdot T_{\mathrm{z\_exMBC\_max}}}_{\text{high freq. component}} + \underbrace{\frac{I_{\mathrm{pk2pk}}}{6\omega \cdot (\Delta V_{\mathrm{Cl\_exMBC}})}}_{\text{sixth freq. component}} \quad (54)$$

2) Proposed ZSVM_1TI and ZSVM_2TI: The low-frequency ripple component of the inductor current ripple and capacitor voltage ripple greater than 6th F1 have not been considered. From the spectra of inductor current shown in Fig. 13, it is clear that the 6$^{\mathrm{th}}$F1 components are absent in these PWM techniques. From Fig. 8, the maximum duration of the ST interval seen by the impedance network using these techniques is equal to the maximum null interval ($T_{\mathrm{z\_IMBC\_max}}$). The high-frequency ripple components seen by inductor current and capacitor voltage can be written as [29]–[31]

$$\Delta\, I_{\mathrm{Lh\_IMBC}} = \frac{V_{\mathrm{C\_IMBC}}}{L_{\mathrm{IMBC}}} \cdot T_{\mathrm{z\_IMBC\_max}} \quad (55)$$

$$\Delta\, V_{\mathrm{Ch\_IMBC}} = \frac{I_{\mathrm{L\_IMBC}}}{\mathrm{C_{IMBC}}} \cdot T_{\mathrm{z\_IMBC\_max}}. \quad (56)$$

Using (47), (48), (55), and (56), the final expression for "*L*" and "*C*" considering only high-frequency components can be written as

$$L_{\mathrm{IMBC}} = \frac{V_{\mathrm{C\_IMBC}}}{\Delta I_{\mathrm{Lh\_IMBC}}} \cdot T_{\mathrm{z\_IMBC\_max}} \quad (57)$$

$$C_{\mathrm{IMBC}} = \frac{I_{\mathrm{L\_IMBC}}}{\Delta V_{\mathrm{Ch\_IMBC}}} \cdot T_{\mathrm{z\_IMBC\_max}}. \quad (58)$$

For equal output power (i.e., same boost factor), the average voltage across the impedance network capacitors using proposed and existing PWM techniques can be written as

$$V_{\mathrm{C\_exMBC}} = V_{\mathrm{C\_IMBC}}. \quad (59)$$

Consider $\Delta\, I_{\mathrm{Lh\_exMBC}} = \Delta I_{\mathrm{Lh\_IMBC}}$, neglecting the sixth frequency component of (53) and (54) and then comparing (53) with (57) and (54) with (58), we get

$$\frac{L_{\mathrm{exMBC}}}{L_{\mathrm{IMBC}}} = \frac{C_{\mathrm{exMBC}}}{C_{\mathrm{IMBC}}} = \frac{2 \cdot T_{\mathrm{z\_exMBC\_max}}}{T_{\mathrm{z\_IMBC\_max}}}. \quad (60)$$

Using (46) and (60), for $(5 \geq B \geq 1.2)$, the ratio (even neglecting the 6$^{\mathrm{th}}$F1 components of M2 and M3 techniques) of the requirement of "*L*" and "*C*" comes out to be

$$\left(2.2 \leq \frac{L_{\mathrm{exMBC}}}{L_{\mathrm{IMBC}}} = \frac{C_{\mathrm{exMBC}}}{C_{\mathrm{IMBC}}} \leq 3.2\right);\ \{5 \geq B \geq 1.2\}. \quad (61)$$

TABLE VIII
DISTRIBUTION OF SWITCHING AND CONDUCTION LOSSES

Losses	Switches /diodes	ZSVM_1TI	ZSVM_2TI	M2	M3
Switching losses (W)	SX1+SX3	27.39	34.36	4.57	21.4
	SX2	0.45	0.2	19.3	1.41
	Da + Db	0.09	0.17	0.051	0.049
Conduction losses (W)	SX1+SX3	24.74	35.23	7.54	20.5
	SX2	0.47	0.53	17.8	0.58
	Da + Db	12.71	13.39	11.4	12.9
Total (W)		65.85	83.88	60.66	56.8

X = A, B, C.

TABLE IX
PARAMETERS USED FOR SIMULATION/EXPERIMENTATION

Parameter	Value/name
Input dc source (V_{dc})	130V
Inductors (L_1, L_2)	6mH
Capacitor C_3, C_4	330uF
Three phase load parameters	25 Ω, 4mH 50 Ω, 2mH
Fundamental Frequency (F_1)	50Hz
Half carrier cycle duration	208usec.
Carrier frequency (F_s)	2.4kHz

Finally, the size of the impedance network "*L*" and "*C*" using M2 and M3 switching techniques is around two to three times more than that of the proposed ZSVM_1TI and ZSVM_2TI techniques.

E. Switching and Conduction Losses

To calculate the switching and conduction losses of the power switches and diodes, the PWM techniques have been simulated using the datasheet parameters. The IGBT power switch used is "KGT25N120NDH," which has an inbuilt antiparallel diode. The "MUR 1560" diodes have been used in the bidirectional power switch and impedance network. For the rated output power of around 1 kW, the simulated values of switching and conduction losses have been tabulated in Table VIII. In category 1 of the PWM techniques defined in Table VI, ZSVM_1TI has slightly increased power loss as compared to the M2 and M3. The power losses due to ZSVM_2TI (category 2) are the highest among the considered PWM techniques.

VII. RESULTS

As shown in Fig. 8, the switching state patterns of M2 and M3 are the same except that by the used combination of power switches for the ST state insertion. The output waveforms of both (M2 and M3) are the same. Therefore, only M3 has been taken from the existing PWM technique for comparison with the proposed techniques.

A. Simulation Results

MATLAB/Simulink software has been used for simulation with the parameters mentioned in Table IX. For the same output power, the modulation index requirement of M3 and proposed PWM techniques are same. The boost factor B is set to 2.5 and load parameters are $r = 25\ \Omega$ and $l = 4$ mH.

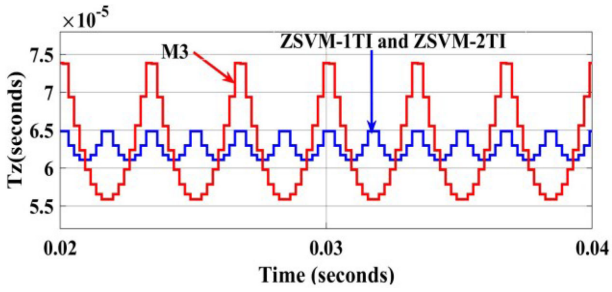


Fig. 11. Simulated waveform of ST/null time interval over fundamental cycle using ZSVM_1TI, ZSVM_2TI, and M3.

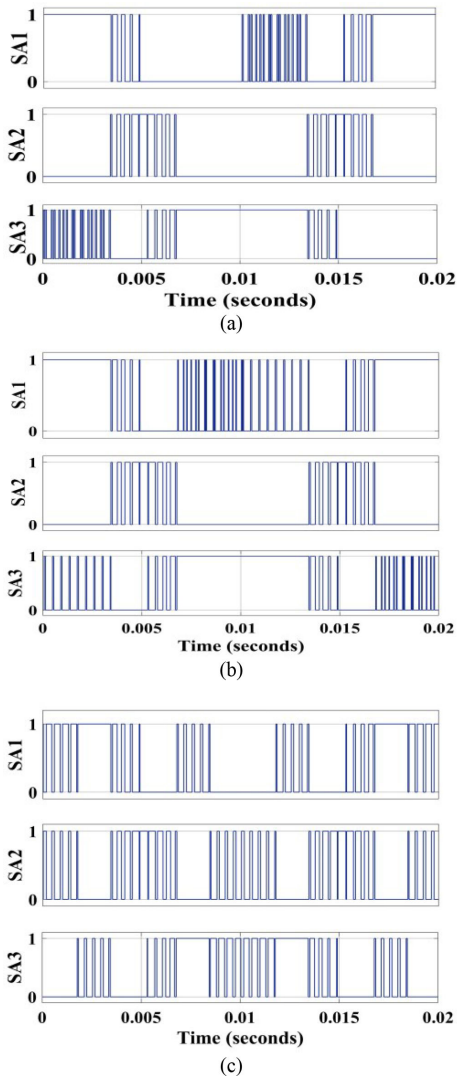


Fig. 12. Simulation waveforms of gating signal at $B = 2.5$. (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3.

The simulation waveforms of null/ST interval are shown in Fig. 11. The ST/null time duration using the M3 technique changes six times the fundamental frequency, which is half as compared to those of ZSVM_1TI and ZSVM_2TI. Fig. 11 also justifies the theoretical calculation illustrated in Fig. 6.

The gating pulse waveforms are shown in Fig. 12 to illustrate the switching frequency of the power switches at the carrier

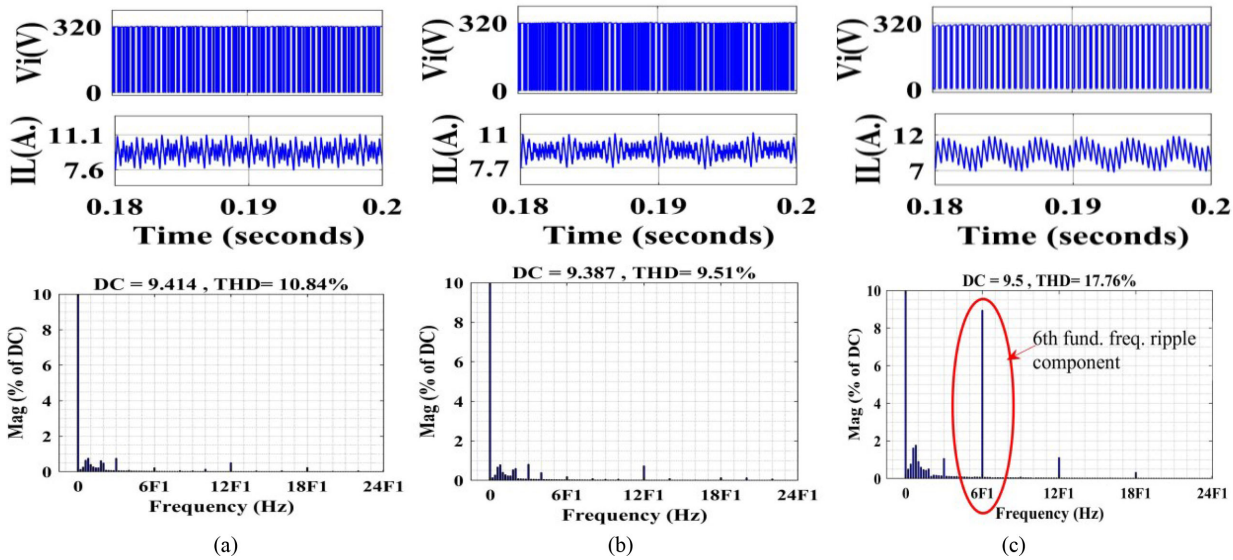


Fig. 13. Simulation waveforms of dc-link voltage (V_i) , inductor current (i_L), and the spectra of inductor current at "*B*=2.5." (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3. Note: DC-link voltage of ZSVM_1TI and ZSVM_2TI look denser just because of the increased switching frequency of the impedance network (see Table VI). The total average switching frequency of the power switches "*W*" using ZSVM_1TI and ZSVM_2TI is actually lower as compared to M3. See Table VII first row for the switching frequency of the power switches using ZSVM_1TI, ZSVM_2TI, and M3 and waveforms of gating pulses in Fig. 12.

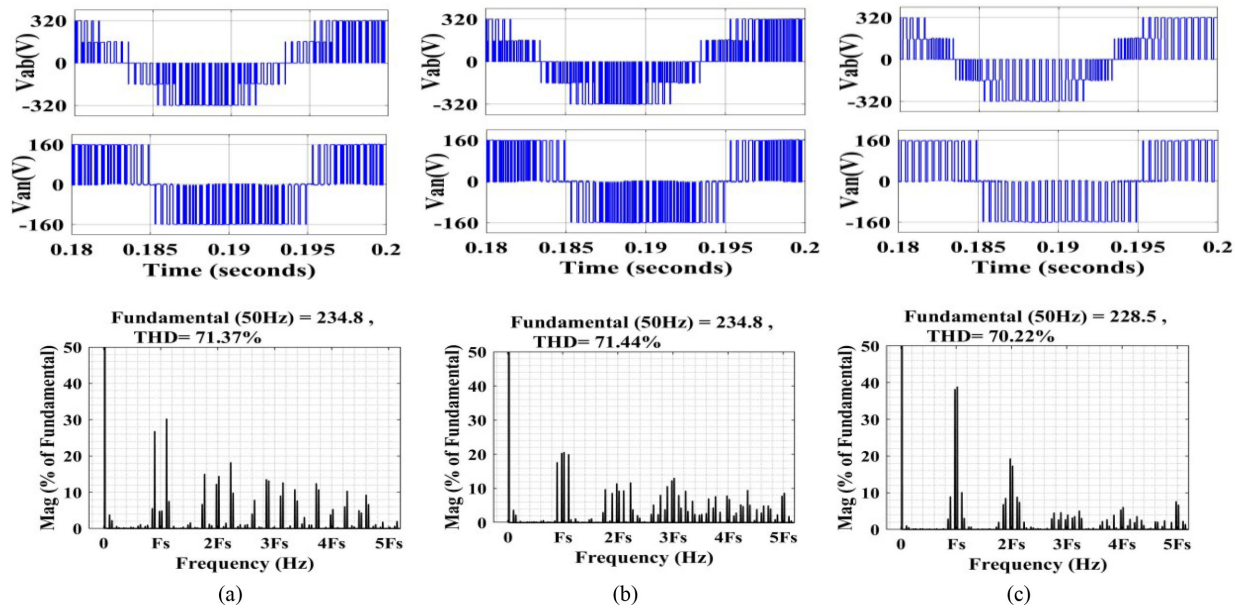


Fig. 14. Simulation waveforms of line voltage $(V_{\rm ab})$, pole voltage $(V_{\rm an})$, and THD spectra of line voltage at "B=2.5." (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3. Note—The total average switching frequency "W" of the power switches using ZSVM_1TI and ZSVM_2TI is lower as compared to that of M3. See first row of Table VII and Fig. 12 of the gating pulses.

frequency of 2.4 kHz (as of the first row of Table VII). As seen in Fig. 12(a) and (b), the middle bidirectional switch has the same switching frequency using ZSVM_1TI and ZSVM_2TI.

Fig. 13 shows the dc-link voltage (V_i), inductor current (i_L) and spectra of the inductor current waveform. The dc-link voltage peak (320 V) has good agreement with the theoretically predicted value as per the relation $(B \cdot V_{\rm dc})$. The inductor current is smooth using proposed PWM techniques; but when the M3 technique is used, the inductor current contains the 6th F1 components, which are visible in Fig. 13(c). The harmonic spectra of inductor currents have been also shown in Fig. 13 to strengthen the claim that the 6$^{\rm th}$F1 ripples are absent when proposed PWM techniques are applied. The simulation results of the line voltage $(V_{\rm ab})$, pole voltage $(V_{\rm an})$, and total harmonic distortion (THD) of line voltage have been shown in Fig. 14. Since "*B*" is the same, the peak magnitude of line voltage $(V_{\rm ab})$ is approximately same using all techniques (i.e., 320 V, which is as per the relation $B \cdot V_{\rm dc}$.). Similarly, the peak magnitude of pole voltage is also same (i.e., 160 V) for all techniques and in accordance with the relation $0.5 \cdot B \cdot V_{\rm dc}$. The THD plots

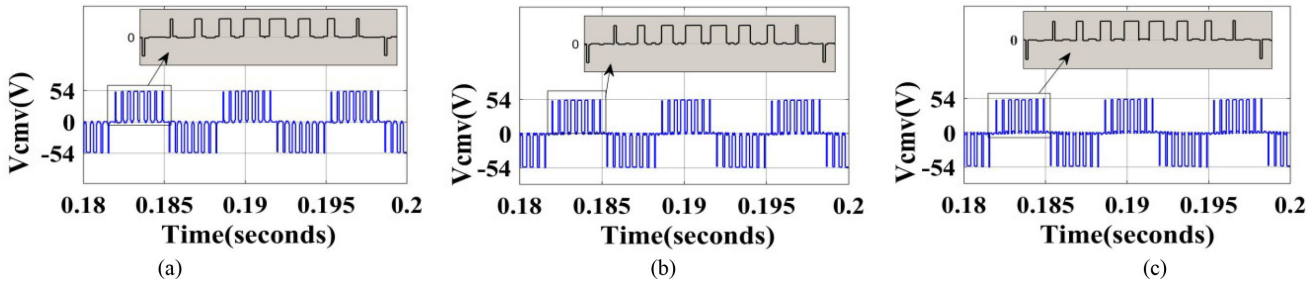


Fig. 15. Simulation waveforms of CMV ($V_{\rm cmv}$) at B=2.5. (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3.

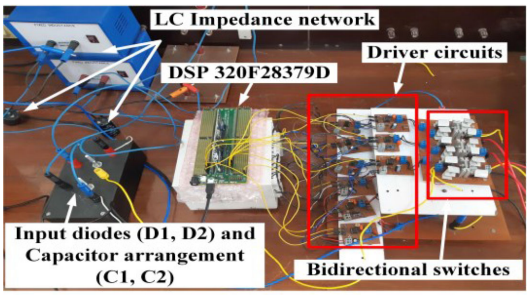


Fig. 16. Photograph of a CDBC ZSI prototype.

indicate that the harmonic distortion of the line voltage is also approximately same. It should be noted from THD plot that the fundamental rms component of line voltage is less using the M3 technique as compared to the proposed techniques. This is due to the low-frequency ripple of the inductor current present in M3.

The waveforms of the CMV ($V_{\rm cmv}$) are shown in Fig. 15. The peak magnitude of CMV using all PWM techniques is around $\pm$54 V, which is the one-sixth of the available dc-link voltage (V_i). It is also clear from the zoomed portion of Fig. 15 that all PWM techniques have the same number of commutation in CMV, i.e., slew rate of the CMV is unaffected with the proposed PWM techniques.

B. Experimental Results

The laboratory prototype of a CDBC ZSI is shown in Fig. 16. Texas Instruments DSP, TMS320F28379D, has been used for the generation of gating pulses. Two different cases of load parameters have been considered for experimental verification.

1) $B = 2.5$, $r = 25\ \Omega$, $l = 4$ mH: The gating pulse waveforms for this case are shown in Fig. 17. These waveforms have the exact match as with the simulation waveforms of Fig. 12. For "B = 2.5," the required modulation index value is 0.846 for all techniques. Fig. 18 shows the experimental waveforms of the line voltage, pole voltage, and CMV. The peak value of the line voltage ($V_{\rm ab}$) and pole voltage ($V_{\rm an}$) are 320 and 160 V, respectively, for all techniques. This satisfies the theoretical relation of $BV_{\rm dc}$ for line voltage peak and $0.5 \cdot BV_{\rm dc}$ for pole voltage peak value. The magnitude of CMV is around $\pm$54 V, which satisfies the relationship $\pm BV_{\rm dc}/6$. The zoomed view of pole voltage and CMV is provided in Fig. 19 to indicate the number of commutation in the CMV. Fig. 19 proves that the rate of change of CMV is unaffected with the proposed PWM techniques. The measured rms values of the CMV for the various values of the boost factor are provided in Table X. The rms value of CMV is approximately the same using all PWM techniques.

TABLE X
MEASURED VALUES OF CMV

V_{ab}(rms), B	RMS value of CMV (V)		
	ZSVM_1TI	ZSVM_2TI	M3
135, 1.5	20.8	20.9	20.1
169, 2	26.1	26.2	25.3
204, 2.5	31.5	31.5	30.5

The dc-link voltage (V_i) and the inductor current (i_L) waveforms are shown in Fig. 20. The peak value of the dc-link voltage satisfies the predicted theoretical value as per the relationship $B \cdot V_{\rm dc}$. It can be noticed from Fig. 20 that there are 6th F1 ripple components in the inductor current using the M3 PWM technique. On the other hand, inductor current using proposed techniques is smooth. This validates the claim that the IMBC technique of voltage boosting offers the elimination of the 6th F1 inductor current ripple component.

2) $B = 2$, $r = 50\ \Omega$, $l = 2$ mH: In this case, the modulation index is set to 0.906. The waveforms of dc-link voltage and inductor current for this case are shown in Fig. 21. The dc-link voltage has been boosted to around 250 V. Again, it is visible from the inductor current waveforms in Fig. 21 that the 6th F1 inductor current ripples are absent with the proposed techniques.

The tested efficiencies of the prototype using proposed and existing PWM techniques have been plotted in Fig. 22. ZSVM_1TI and M3 techniques come in the category of one ST state per half carrier cycle and ZSVM_2TI comes in the category of two ST state per half carrier cycle (see Table VI).

Comparing the PWM techniques of category 1, it has been admitted that the efficiency offered by ZSVM_1TI is slightly less (around 1%) as compared to that of M3, which can be compromised while seeing at the advantages of ZSVM_1TI. The efficiency of the inverter suffers more when the ZSVM_2TI technique is used.

VIII. DISCUSSION

The proposed PWM techniques (ZSVM_1TI and ZSVM_2TI) are a combination of three important findings. These findings are, modified SVPWM switching state diagram, IMBC technique of voltage boosting, and new RCMV switching patterns. The modified SVPWM doubles the frequency of the null interval based on which the IMBC has been proposed to eliminate the 6$^{\rm th}$F1 ripple component of the impedance

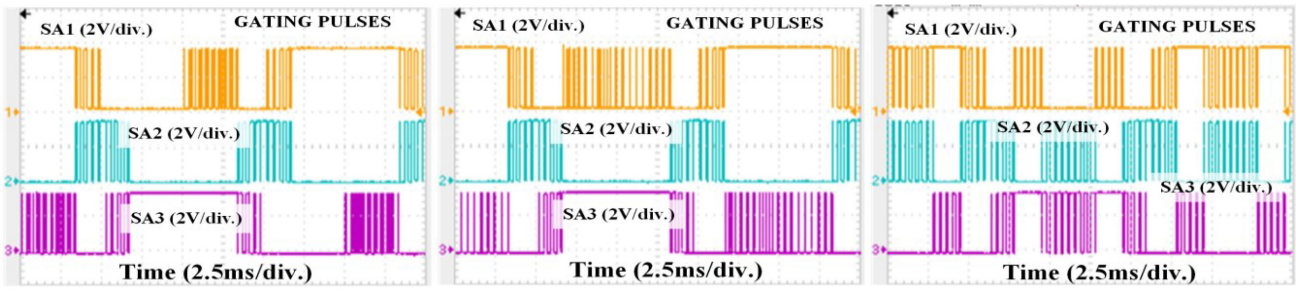


Fig. 17. Experimental waveforms of gating pulses at "*B*=2.5." (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3.

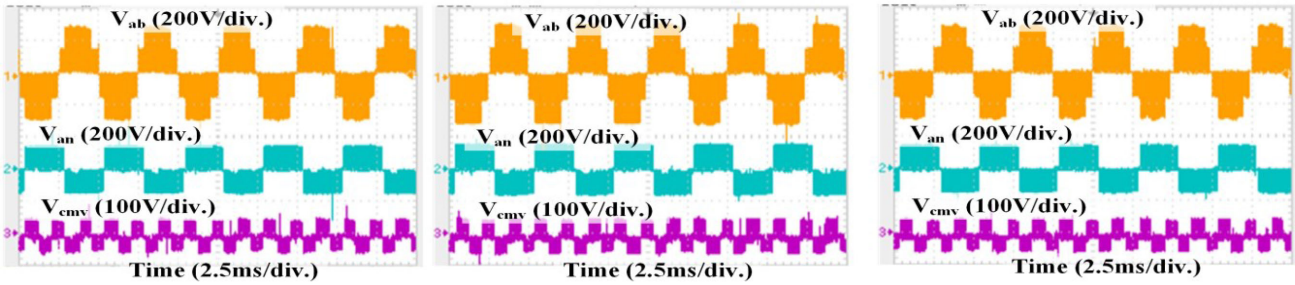


Fig. 18. Experimental waveforms of line voltage $(V_{\rm ab})$, pole voltage $(V_{\rm an})$, and CMV $(V_{\rm cmv})$ at "B=2.5." (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3.

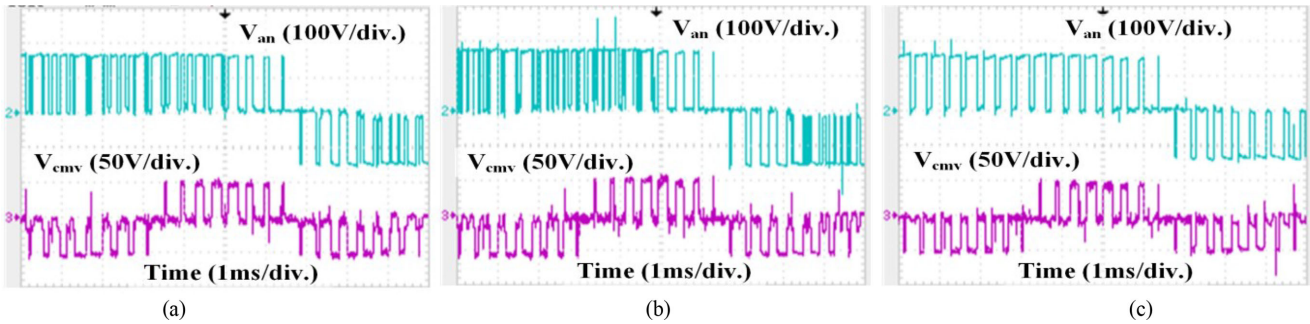


Fig. 19. Experimental waveforms (zoomed view) of pole voltage $(V_{\rm an})$ and CMV $(V_{\rm cmv})$ at "*B*=2.5." (a) ZSVM_1TI. (b) ZSVM_2TI. (c) M3.

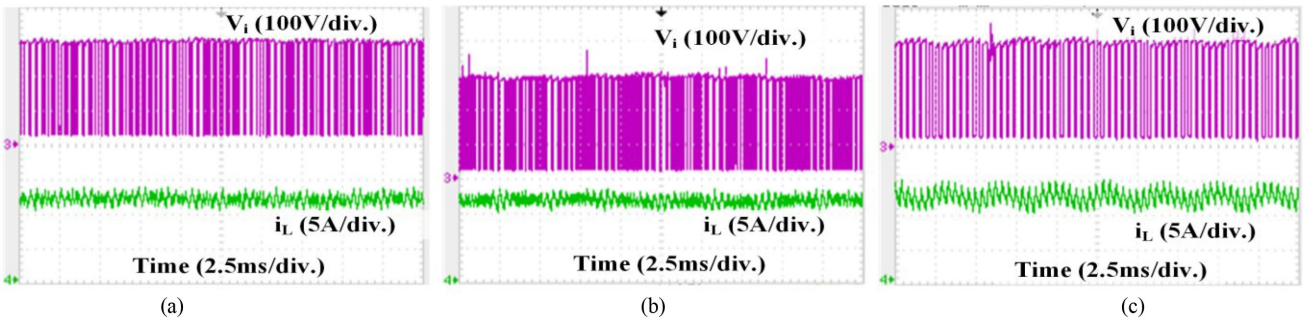
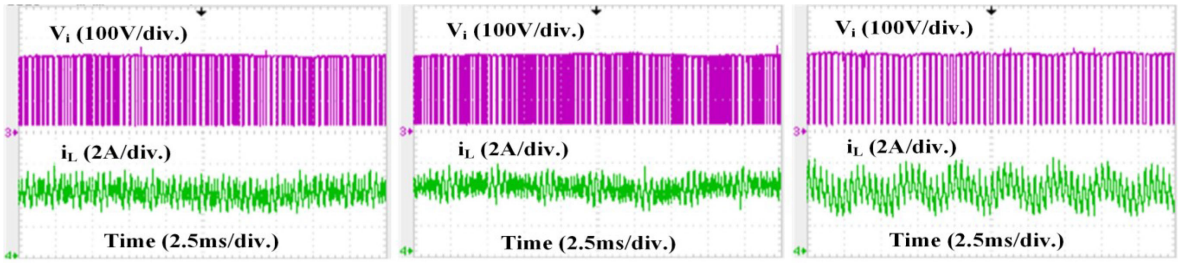


Fig. 20. Experimental waveforms of dc-link voltage (V_i) and inductor current (i_L) at "*B*=2.5" for (a) ZSVM_1TI, (b) ZSVM_2TI, and (c) M3.

network inductor current. The proposed SVPWM switching diagram also offers an increased range of modulation index and improved dc bus utilization. The new pattern of switching states limits the CMV magnitude to one-sixth of the available dc-link voltage without affecting the slew rate of CMV. Furthermore, the proposed 12-sided polygon shown in Fig. 3(b) is equally valid for the case of a three-level VSI. Similarly, the proposed IMBC can also be used with other PWM switching patterns of the 3L-ZSI. The important aspects of the proposed and existing RCMV techniques have been summarized in Table XI.



(a) (b) (c)

Fig. 21. Experimental waveforms of dc-link voltage (V_i) and inductor current (i_L) at "B=2" for (a) ZSVM_1TI, (b) ZSVM_2TI, and (c) M3.

TABLE XI
IMPORTANT ASPECTS OF PROPOSED AND EXISTING RCMV PWM TECHNIQUES OF 3L-ZSI

Aspect	Proposed (with improved MBC approach) ZSVM_1TI and ZSVM_2TI	Existing (with existing MBC approach) M2 and M3
Elimination of 6th F1 ripple components of impedance network inductor current	Yes, (see Fig. 6, Fig. 13, Fig. 20 and Fig. 21)	No, (see Fig. 6, Fig. 13, Fig. 20 and Fig. 21)
Max range of modulation index	1.19, (Fig. 3(b) and equation (29))	1.15, (Fig. 3(a) and equation (11))
Boost factor	Both (proposed and existing) offers same boost factor in the range of M from 0.6 to 1.15. In addition, the proposed techniques also offers the enhanced utilization of the dc-link potential up to the range of M =1.19.	
Fundamental rms line voltage magnitude	$0.728.BV_{dc}$, (see equation (30))	$0.707.BV_{dc}$, (see equation (13))
Size of the impedance network components	As shown in (61), for the particular range of 'B', the size of impedance network using proposed PWM techniques is 2 to 3 times lower than the existing (M2, M3) techniques.	
Magnitude of CMV	Maintained within $\pm BV_{dc}/6$, (Fig. 15 and Fig. 19)	
Slew rate of CMV	Same (Fig. 15 and Fig. 19)	
THD of line voltage	Almost same (Fig. 14)	
Switching frequency of the impedance network and power switches	See Table VI and Table VII, The proposed ZSVM_1TI and ZSVM_2TI doubles and triples the switching frequency of the impedance network as compared to the existing (M2, M3) SVPWM techniques at competitive total average switching frequency of the power switches. This results in reduced impedance network size requirements using proposed techniques.	
Neutral point voltage (NPV) oscillation control	Mostly, the dwell time duration of the small vectors is used for balancing the upper/lower capacitors (C_1 and C_2) of the dc source in three-level inverters. But when the small vectors are not available either because they are not used or completely replaced by ST states for the implementation MBC technique, then it is not possible to apply those NPV oscillation control algorithm with proposed (ZSVM_1TI and ZSVM_2TI) as well as in existing (M2, M3) PWM techniques of 3L-ZSI. ZSVM_1TI, ZSVM_2TI, M2, and M3 PWM techniques does not use small vectors. This means that these techniques are suitable only for those applications where fixed dc sources are used at the input side of 3L-ZSI.	
Power losses and efficiency	The proposed switching pattern increases the switching frequency of the impedance network. See Table VI and Table VII for details regarding the switching frequency of impedance network and power switches. As shown in Fig. 22 that the efficiency using ZSVM_1TI suffers slightly (around 1 percent) as compared to the M3. In addition to the advantages offered by ZSVM_1TI, the ZSVM_2TI technique has a better inductor current profile (Fig. 13) but the efficiency using ZSVM_2T suffers more as compared to the ZSVM_1TI and M3.	

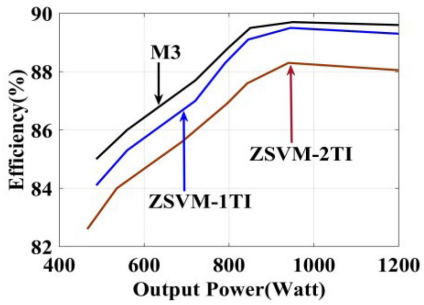


Fig. 22. Prototype efficiency curve.

IX. CONCLUSION

The conventional SVPWM switching diagram of a 3L-ZSI has been successfully modified to propose the IMBC of voltage boosting. Modified SVPWM offers a 3% increase in the modulation index and fundamental rms line voltage as compared to the conventional SVPWM. Most importantly, the IMBC resolves the problem of 6th F1 inductor current ripple components that prevailed in existing MBC without affecting the gain and switching stress across the power switches. The proposed improved RCMV switching patterns increase the switching frequency of the impedance network at a competitive switching frequency of the power switches as compared to the existing RCMV techniques. This results in reduced size of the impedance network while limiting the magnitude of CMV to one-sixth of the available dc-link voltage. The rate of change of CMV was also unaffected when compared to the existing RCMV techniques of 3L-ZSI. However, a decrease in efficiency has been noticed using proposed techniques. The main demerit of the proposed as well as existing considered RCMV PWM technique is that the neutral-point voltage balancing algorithms which adjust the small vector duration for balancing the upper and lower capacitors of dc source are not applicable as these techniques do not use small vectors at all.

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