Improved Finite Control Set Model Predictive Current Control for Five-Phase VSIs

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***Abstract*—Model predictive current control (MPCC) is widely studied and applied in five-phase VSIs, and virtual voltage vectors (V^3s) are constructed to improve steady state performance and simplify computation complexity. However, V^3s in five-phase VSIs were initially constructed using one large and one medium voltage vectors, and all existing works employed this method, which goes against the common-mode voltage (CMV) reduction. To address this problem, two improved MPCC (IMPCC) methods are proposed in this article. Firstly, the V^3s are constructed in a new way using four adjacent large vectors, which enables the proposed IMPCC methods to reduce CMV and low-order harmonic currents inherently. Thus, there are no harmonic and CMV terms in the cost function. Secondly, the duty ratio optimization is introduced and dwell time of the optimal V^3 is estimated to reduce current ripples. Then, in order to achieve superior steady state performance, two switching patterns are designed, namely the asymmetrical and symmetrical ones. The asymmetrical pattern aims to reduce the switching frequency while the symmetrical one focuses on harmonics suppression. Finally, experimental comparisons between the proposed IMPCC methods and conventional methods are presented. Experimental results have verified that the proposed schemes can mitigate CMV, suppress current harmonics and reduce computation complexity, simultaneously.**

***Index Terms*—Common-mode voltage (CMV), predictive control, voltage source inverter (VSI).**

I. Introduction

COMMON-MODE voltage (CMV) is known to cause winding insulation damages, affect the lifetime and produce deteriorations [1]–[4]. Thus, CMV reduction has attracted widespread attention in the recent years. CMV reduction techniques have been applied for different power converters, such as three-phase voltage source inverters (VSIs) [5], [6], multiphase VSIs [7], [8], matrix converters [9]–[12] etc. There are typically two types of CMV reduction methods, namely the hardware-based and software-based methods. Passive filters and special topologies are usually required in the hardware-based method [13]–[15], which makes it cost-inefficient. To reduce CMV without additional passive filters, the software-based methods, which are dependent on the control strategy, are more popular in industry applications.

The basic idea of software-based CMV reduction is to avoid using the high-CMV switching states in the modulation methods. Phase-shifted sinusoidal PWM (PSPWM) methods have been presented to reduce CMV, but CMV spikes caused by dead-time are not avoided [16]. Carrier-based PWM (CBPWM) method with opposite carriers for specific phases has been proposed to reduce CMV for five-phase VSIs [17]. Two SVPWM methods with 40% and 80% CMV reduction have been proposed for five-phase motor drives in linear modulation zone [18] and over-modulation zone [19]. The SVPWM are extended to multilevel multiphase VSIs, and only the switching states that generate zero CMV are utilized to synthesize the reference voltages [20]. The double-sided and central leg distributions have been applied alternately for two-level multiphase VSIs, and the minimum CMV PWM (MCMV-PWM) is proposed [21].

Model predictive current control (MPCC) has been widely reported and applied in power converters and drive systems [22]–[25]. As different control variables can be included in the cost function, it is feasible for MPCC methods to deal with multiple control goals. And weighting factors are often tuned to realize a trade-off between the desired control targets [26]. To reduce CMV in three-phase VSIs, the cost function is redesigned with an additional constraint, considering the CMV reduction by adding the term proportional to CMV values [27]. By adding the CMV term, the switching states that generate high CMV values are penalized. The same principle is adopted in a matrix converter [28]. The MPCC methods using modified cost function with CMV term have been extended to multiphase applications [29]. Two additional objective terms are included in the cost function, to penalize the voltage vectors that generate medium and large CMV in five-phase inverters. However, the steady state performance is deteriorated inevitably, which is the price paid for CMV reduction as some switching states are not adopted in this type of control methods. Moreover, weighting factors tuning is a key issue of these MPCC methods, which is not an easy task due to the lack of theoretical design procedure [30], [31]. The performance is highly dependent on the cost function, weighting factors, and the specific operation point [32], thus it is a big challenge to find the optimal weighting factors, especially when the control objectives are more than two [33].

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To simplify the weighting factors tuning, some modified MPCC methods with CMV reduction have been studied in [34]–[37]. In [34], zero voltage vectors that generate large CMV are not used and only the six active voltage vectors are utilized to conduct the enumeration optimization. The CMV is restricted within $\pm V_{\rm dc}/6$ without using zero voltage vectors, and two active voltage vectors are applied during each sampling interval to achieve the desired current waveforms. In [35], only four active voltage vectors are employed to carry out the optimization procedure during each sampling interval. The steady state performance is deteriorated due to eliminating zero vectors. A hybrid voltage vector preselection-based MPCC method with CMV reduction has been proposed to improve the steady state performance for three-phase VSIs [36], where six synthesized voltage vectors are defined and involved in the optimization procedure. Although these schemes can reduce CMV effectively for three-phase VSIs, they are not universal for multiphase VSIs.

In five-phase VSIs, to suppress low-order harmonic currents and achieve sinusoidal current waveforms, the current components in both α-β and x-y subspace need to be controlled. In other words, the prediction model, cost function and control set are relatively more complex compared with three-phase applications, leading to heavy computation cost. Besides, it becomes worse when CMV reduction is taken into account. In order to reduce the computation cost and improve the steady state performance, virtual voltage vectors (V^3s) based MPCC methods have been studied [37]–[39]. The V^3s in existing works are initially defined using one large and one medium voltage vectors, and the dwell time ratio between the medium and large voltage vectors is fixed at 0.618. In this way, the low order harmonic currents are eliminated. Unfortunately, it leads to high CMV values due to the absence of CMV reduction.

In this article, two improved MPCC methods (IMPCC1 and IMPCC2) are proposed for five-phase VSIs. First, CMV in five-phase VSIs is analyzed and V^3s are redefined with four adjacent large vectors, which mitigates CMV and reduces low-order harmonic currents inherently. Then, the V^3s are adopted in the enumeration optimization, and the optimal V^3 is selected with the simplified prediction model and cost function, leading to computation cost reduction. Moreover, to further improve steady state performance, the duty ratio optimization is introduced. The dwell time of the optimal V^3 is estimated in such a way that minimizes the current ripples. In order to achieve superior steady state performance, two optimized switching patterns are designed. Therefore, the main contribution of the proposed methods is to reduce CMV and achieve excellent steady state performance simultaneously. Moreover, the computation cost is also reduced, which makes it easy to be implemented.

This article is organized as follows: Section II illustrates the modeling of five-phase VSI and CMV analysis. The conventional MPCC method with CMV reduction is briefly introduced in Section III. The proposed two IMPCC schemes are described in Section IV. An experimental comparison of the proposed and conventional methods is presented and analyzed in Section V. The conclusions are summarized in Section VI.

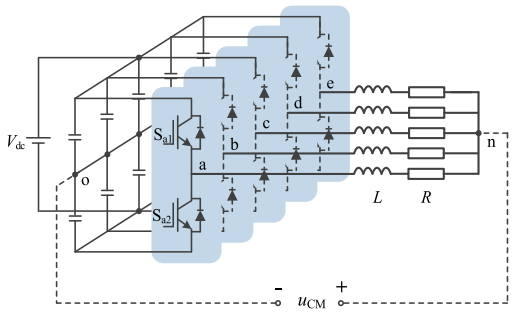

Fig. 1. Topology of five-phase VSI with start-connected *RL* loads.

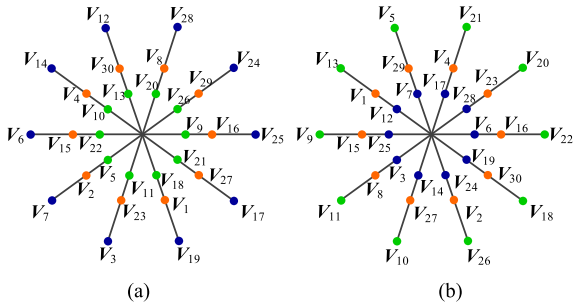

Fig. 2. Space voltage vectors distribution in (a) α-β subspace and (b) x-y subspace.

II. Five-Phase VSI Modeling and CMV Analysis

A. Five-Phase VSI Modeling

The main circuit of a two-level five-phase VSI with passive star-connected *RL* loads is shown in Fig. 1. Switching function $S_{\rm k}$ is defined to represent the switching states of phase k (k = a, b, c, d, e), where $S_k = 1$ means the upper insulated gate bipolar translator (IGBT) is ON and the lower one is OFF, and vice versa.

The phase voltage of phase k is expressed as

$$u_{k\rm n} = \left(S_k - \frac{S_{\rm a} + S_{\rm b} + S_{\rm c} + S_{\rm d} + S_{\rm e}}{5}\right) V_{\rm dc} \tag{1}$$

where $V_{\rm dc}$ is the dc-bus voltage.

The space voltage vector in the α-β and x-y subspace are expressed as

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_x \\ u_y \end{bmatrix} = \frac{2}{5} \begin{bmatrix} 1 & \cos\alpha & \cos 2\alpha & \cos 3\alpha & \cos 4\alpha \\ 0 & \sin\alpha & \sin 2\alpha & \sin 3\alpha & \sin 4\alpha \\ 1 & \cos 3\alpha & \cos 6\alpha & \cos 9\alpha & \cos 12\alpha \\ 0 & \sin 3\alpha & \sin 6\alpha & \sin 9\alpha & \sin 12\alpha \end{bmatrix} \begin{bmatrix} u_{\rm an} \\ u_{\rm bn} \\ u_{\rm cn} \\ u_{\rm dn} \\ u_{\rm en} \end{bmatrix} \tag{2}$$

where $\alpha = 2\pi/5$.

The phase voltages can be mapped into two orthogonal coordinates, namely α-β and x-y subspace, as shown in Fig. 2. The voltage vectors $\boldsymbol{V}_i$ are numbered according to the binary number of the switching functions.

$$i = S_{\rm a} \cdot 2^4 + S_{\rm b} \cdot 2^3 + S_{\rm c} \cdot 2^2 + S_{\rm d} \cdot 2^1 + S_{\rm e} \cdot 2^0 \tag{3}$$

TABLE I
VOLTAGE VECTORS AND SWITCHING STATES

Large vectors		Medium vectors		Small vectors	
V_{25}	11001	V_{16}	10000	V_9	01001
V_{24}	11000	V_{29}	11101	V_{26}	11010
V_{28}	11100	V_8	01000	V_{20}	10100
V_{12}	01100	V_{30}	11110	V_{13}	01101
V_{14}	01110	V_4	00100	V_{10}	01010
V_6	00110	V_{15}	01111	V_{22}	10110
V_7	00111	V_2	00010	V_5	00101
V_3	00011	V_{23}	10111	V_{11}	01011
V_{19}	10011	V_1	00001	V_{18}	10010
V_{17}	10001	V_{27}	11011	V_{21}	10101

TABLE II
CMV OF DIFFERENT VOLTAGE VECTORS

Groups	Voltage vectors					CMV
Zero vectors	V_0, V_{31}					$\pm 0.5V_{\rm dc}$ large CMV
Large vectors	V_{25}	V_{24}	V_{28}	V_{12}	V_3	$\pm 0.1V_{\rm dc}$
	V_6	V_7	V_{19}	V_{14}	V_{17}	Small CMV
Medium vectors	V_{16}	V_{29}	V_8	V_{30}	V_4	$\pm 0.3V_{\rm dc}$
	V_{15}	V_2	V_{23}	V_1	V_{27}	Medium CMV
Small vectors	V_9	V_{26}	V_{20}	V_{13}	V_{10}	$\pm 0.1V_{\rm dc}$
	V_{22}	V_5	V_{11}	V_{18}	V_{21}	Small CMV

The voltage vectors and switching states are shown in Table I.

According to the amplitudes, the active voltage vectors can be classified into three groups: large vectors ($\boldsymbol{V}_{\rm L}$, 0.6472 $V_{\rm dc}$), medium vectors ($\boldsymbol{V}_{\rm M}$, 0.4 $V_{\rm dc}$) and small vectors ($\boldsymbol{V}_{\rm S}$, 0.2472 $V_{\rm dc}$).

The mathematical model of *RL* loads in α-β and *x*-*y* subspace can be expressed as

$$\begin{cases} u_{\alpha\beta} = Ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} \\ u_{xy} = Ri_{xy} + L\frac{di_{xy}}{dt} \end{cases} \tag{4}$$

where $u_{\alpha\beta}$ and u_{xy} are the voltage in α-β and *x*-*y* subspace, $i_{\alpha\beta}$ and i_{xy} are load currents in α-β and *x*-*y* subspace.

B. CMV in Five Phase VSIs

CMV in five-phase VSIs is defined as the voltage between the neutral point and the midpoint of the dc-bus, as expressed

$$u_{\rm CM} = \frac{V_{\rm dc}}{5}(S_{\rm a} + S_{\rm b} + S_{\rm c} + S_{\rm d} + S_{\rm e}) - \frac{V_{\rm dc}}{2} \tag{5}$$

where $u_{\rm CM}$ is the common-mode voltage.

According to (5), the 32 voltage vectors produce six CMV values, namely: ± 0.5 $V_{\rm dc}$, ± 0.3 $V_{\rm dc}$ and ± 0.1 $V_{\rm dc}$, as shown in Table II. It can be summarized that

1) zero voltage vectors generate large CMV;
2) medium vectors generate medium CMV;
3) small and large voltage vectors generate small CMV.

III. CONVENTIONAL MPCC METHOD WITH CMV REDUCTION

In the classical finite control set (FCS) MPCC methods, the currents prediction model is deduced using first-order Forward Euler approximation, with the assumption that the sampling interval is small enough

$$\begin{cases} i_{\alpha\beta}^{k+1} = \frac{T_{\rm s}}{L}u_{\alpha\beta}^{k} + (1 - \frac{RT_{\rm s}}{L})i_{\alpha\beta}^{k} \\ i_{xy}^{k+1} = \frac{T_{\rm s}}{L}u_{xy}^{k} + (1 - \frac{RT_{\rm s}}{L})i_{xy}^{k} \end{cases} \tag{6}$$

where $T_{\rm s}$ is the sampling interval, the superscripts k and $k+1$ represent the variable values at kth and $(k+1)$th sampling instant.

In order to compensate the inherent one-step digital delay in MPCC methods, a digital compensation method is widely employed in MPCC methods. The prediction model is conducted to estimate the currents at $(k+1)$th sampling interval, which serve as the initial values for the enumeration optimization. The modified prediction model can be deduced

$$\begin{cases} i_{\alpha\beta}^{k+2} = \frac{T_{\rm s}}{L}u_{\alpha\beta}^{k+1} + (1 - \frac{RT_{\rm s}}{L})i_{\alpha\beta}^{k+1} \\ i_{xy}^{k+2} = \frac{T_{\rm s}}{L}u_{xy}^{k+1} + (1 - \frac{RT_{\rm s}}{L})i_{xy}^{k+1} \end{cases} \tag{7}$$

In conventional FCS-MPCC schemes, the cost function is usually defined as

$$\begin{aligned} G = &\left|i_{\alpha}^{*} - i_{\alpha}^{k+2}\right|^2 + \left|i_{\beta}^{*} - i_{\beta}^{k+2}\right|^2 \\ &+ \lambda_{xy}(\left|i_{x}^{*} - i_{x}^{k+2}\right|^2 + \left|i_{y}^{*} - i_{y}^{k+2}\right|^2) \end{aligned} \tag{8}$$

where the superscript $*$ represents the reference values, λ_{xy} is the weighting factor of harmonic currents.

In the conventional MPCC method with CMV reduction for five-phase VSIs, additional terms corresponding to CMV are directly included in the cost function to reduce the CMV by penalizing the voltage vectors that generate medium and large CMV. The modified cost function is defined as

$$\begin{aligned} G = &\left|i_{\alpha}^{*} - i_{\alpha}^{k+2}\right|^2 + \left|i_{\beta}^{*} - i_{\beta}^{k+2}\right|^2 \\ &+ \lambda_{xy}(\left|i_{x}^{*} - i_{x}^{k+2}\right|^2 + \left|i_{y}^{*} - i_{y}^{k+2}\right|^2) \\ &+ \lambda_{\rm M}(V_i \in G_{\rm M}) + \lambda_{\rm L}(V_i \in G_{\rm L}) \end{aligned} \tag{9}$$

where $\lambda_{\rm M}$ and $\lambda_{\rm L}$ are weighting factors to penalize medium- and large-CMV voltage vectors respectively, $\boldsymbol{V}_i \in G_{\rm M}$ and $\boldsymbol{V}_i \in G_{\rm L}$ are logic functions, which provide one if the voltage vector $\boldsymbol{V}_i$ generate medium or large CMV and zero if otherwise.

It is obvious that there are three weighting factors in the modified cost function, which complicates the weighting factors tuning [30].

IV. PROPOSED MPCC METHODS WITH V^{3}S

A. Virtual Voltage Vectors Construction

In this section, a new definition of V^{3}s is proposed. As analyzed in Section II, zero vectors generate large CMV and medium vectors generate medium CMV, so CMV can be mitigated by eliminating zero and medium vectors. In the new

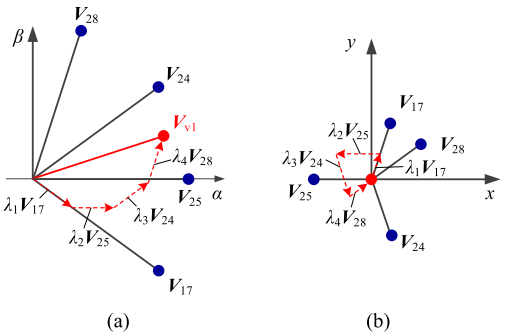

Fig. 3. The schematic diagram of V^{3}s construction. (a) α-β subspace and (b) x-y subspace.

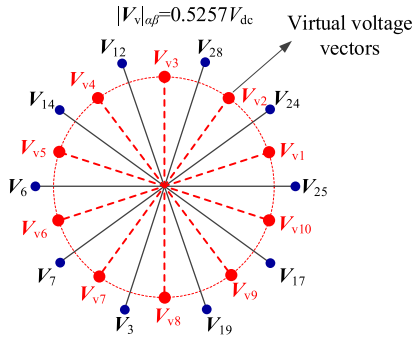

Fig. 4. Trajectories of V^{3}s and the large voltage vectors in α-β subspace.

definition, four adjacent large vectors are selected to construct V^{3}s, and $\boldsymbol{V}_{v1}$ is taken as an illustration, as shown in Fig. 3.

In order to eliminate low-order harmonic currents, the duty ratios are determined in such a way that zero-mean volt-second value is provided in x-y subspace. In other words, x- and y-axis components should be zero.

$$\begin{cases} 0.2472V_{dc}(\lambda_1\cos\frac{2\pi}{5}+\lambda_2\cos\pi+\lambda_3\cos(-\frac{2\pi}{5}) \\ \qquad\qquad +\lambda_4\cos\frac{\pi}{5})=0 \\ 0.2472V_{dc}(\lambda_1\sin\frac{2\pi}{5}+\lambda_2\sin\pi+\lambda_3\sin(-\frac{2\pi}{5}) \\ \qquad\qquad +\lambda_4\sin\frac{\pi}{5})=0 \end{cases} \tag{10}$$

where λ_1, λ_2, λ_3, and λ_4 are duty ratios of $\boldsymbol{V}_{17}$, $\boldsymbol{V}_{25}$, $\boldsymbol{V}_{24}$, and $\boldsymbol{V}_{28}$ respectively. Assuming $\lambda_1=\lambda_4$, the duty ratios can be calculated

$$\begin{cases} \lambda_1=0.191 \\ \lambda_2=0.309 \\ \lambda_3=0.309 \\ \lambda_4=0.191 \end{cases} \tag{11}$$

The amplitude of $\boldsymbol{V}_{v1}$ in α-β subspace can be expressed as

$$\begin{aligned} |\boldsymbol{V}_{v1}|_{\alpha\beta}= & \ 0.6472V_{dc}\cos\tfrac{\pi}{10}(\lambda_2+\lambda_3) \\ & +0.6472V_{dc}\cos\tfrac{3\pi}{10}(\lambda_1+\lambda_4) \end{aligned} \tag{12}$$

Substituting (11) into (12), yields

$$|\boldsymbol{V}_{v1}|_{\alpha\beta}=0.5257V_{dc} \tag{13}$$

In a similar way, ten V^{3}s are constructed in total, as shown in Fig. 4. The blue dots represent the large voltage vectors and the red dots represent V^{3}s.

B. Simplification of Cost Function and Prediction Model

The purpose of cost function definition is to select the optimal voltage vector, in order to achieve the best reference tracking performance. For five-phase VSIs, in order to eliminate low-order harmonic currents and achieve sinusoidal current waveforms, the harmonic current references in conventional MPCC methods are both set to zero. To reduce CMV in five-phase VSIs, CMV terms are also included, as shown in (9), which complicates the cost function.

In the proposed method, CMV and harmonic currents are reduced inherently with the utilization of V^{3}s. Therefore, it is unnecessary to include the harmonic currents i_x and i_y, as well as CMV terms in the cost function. In other words, the empirical weighting factors tuning is avoided. Moreover, the cost function simplification contributes to reducing the computation complexity. The simplified cost function is expressed as

$$G=\left|i_\alpha^*-i_\alpha^{k+2}\right|^2+\left|i_\beta^*-i_\beta^{k+2}\right|^2 \tag{14}$$

As the harmonic currents i_x and i_y are cancelled in the cost function, so it is not necessary to predict the evolution of harmonic currents in the future sampling interval. In this way, the prediction model is also simplified, which makes a further contribution to computation cost reduction.

C. Duty Ratio Estimation

In most cases, it is not necessary to apply the optimal V^3 during the entire sampling interval to force the actual currents to reach its references. Thus, to achieve accurate reference tracking, the optimal dwell time should be estimated, zero voltage vectors are applied for the remaining part of the sampling interval. The optimal dwell time is determined to minimize the tracking error between the actual currents and the reference values.

Assuming that the optimal V^3 will be applied for dT_s, where d is defined as the duty ratio of the selected V^3, the currents at (k+2)th sampling instant can be calculated as

$$i_{\alpha\beta}^{k+2}=\frac{dT_s}{L}u_{\alpha\beta}^{k+1}+\left(1-\frac{RT_s}{L}\right)i_{\alpha\beta}^{k+1} \tag{15}$$

The optimal duty ratio is determined by minimizing the cost function, which yields

$$\frac{\partial G}{\partial d}=0 \tag{16}$$

According to (14), d can be calculated as

$$d=\frac{\left[Li_\alpha^*-(L-RT_si_\alpha^{k+1})\right]V_\alpha+\left[Li_\beta^*-(L-RT_si_\beta^{k+1})\right]V_\beta}{T_s|\boldsymbol{V}_{opt}|^2} \tag{17}$$

where $\boldsymbol{V}_{opt}$ is the selected V^3, V_α and V_β are the α- and β-axis components of $\boldsymbol{V}_{opt}$. The duty ratio should be limited at $0\le d\le 1$.

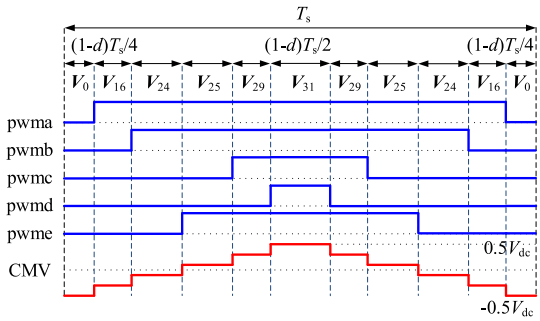

Fig. 5. Conventional switching pattern.

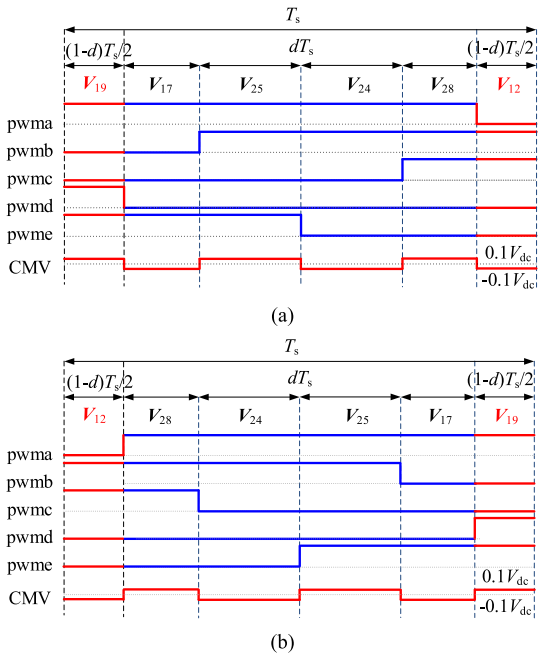

Fig. 6. Asymmetrical switching patterns in (a) counterclockwise order and (b) clockwise order.

D. Switching Patterns Designation

In the conventional MPCC methods with duty ratio optimization, the selected optimal active voltage vector is applied for dT_s, and zero voltage vectors ($\boldsymbol{V}_0$ and $\boldsymbol{V}_{31}$) are applied for the remaining part (1-d)T_s. A symmetrical switching pattern is shown in Fig. 5, which is widely utilized in the conventional MPCC methods [34]. It is obvious that, six CMV values are generated, including $\pm 0.1\ V_{dc}$, $\pm 0.3\ V_{dc}$ and $\pm 0.5\ V_{dc}$, where the maximum CMV is produced by zero voltage vectors.

In order to reduce CMV, zero voltage vectors are replaced with two phase-opposed large vectors, and two optimized switching patterns are designed, including the asymmetrical and symmetrical one. The asymmetrical switching patterns exhibit reduced switching frequency while the symmetrical patterns achieve better steady state performance. The large vectors in the asymmetrical patterns can be applied in the counterclockwise order or the clockwise order, as shown in Fig. 6. In order to avoid additional switching actions between two adjacent sampling intervals, the counterclockwise and clockwise patterns are applied alternatively.

When $\boldsymbol{V}_{v1}$ or $\boldsymbol{V}_{v6}$ is the optimal voltage vector, the phase-opposed large vectors $\boldsymbol{V}_{19}$ and $\boldsymbol{V}_{12}$ are selected to replace zero voltage vectors and regulate the volt-second value during each sampling interval. The specific combinations of phase opposed large vectors are determined according to the optimal V[3], as listed in Table III.

TABLE III
PHASE OPPOSED VECTORS IN ASYMMETRICAL PATTERN

$\boldsymbol{V}_{opt}$	Combinations
$\boldsymbol{V}_{v1}$, $\boldsymbol{V}_{v6}$	$0.5\boldsymbol{V}_{19}$+$0.5\boldsymbol{V}_{12}$
$\boldsymbol{V}_{v2}$, $\boldsymbol{V}_{v7}$	$0.5\boldsymbol{V}_{17}$+$0.5\boldsymbol{V}_{14}$
$\boldsymbol{V}_{v3}$, $\boldsymbol{V}_{v8}$	$0.5\boldsymbol{V}_{25}$+$0.5\boldsymbol{V}_{6}$
$\boldsymbol{V}_{v4}$, $\boldsymbol{V}_{v9}$	$0.5\boldsymbol{V}_{24}$+$0.5\boldsymbol{V}_{7}$
$\boldsymbol{V}_{v5}$, $\boldsymbol{V}_{v10}$	$0.5\boldsymbol{V}_{28}$+$0.5\boldsymbol{V}_{3}$

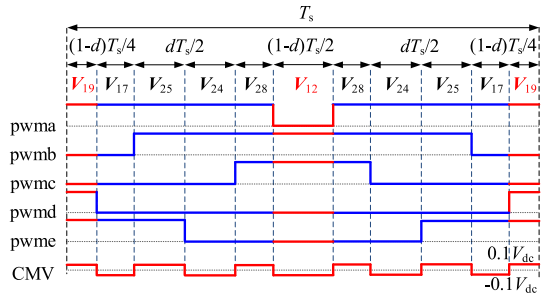

Fig. 7. Symmetrical switching patterns.

TABLE IV
PHASE OPPOSED VECTORS IN SYMMETRICAL PATTERN

$\boldsymbol{V}_{opt}$	Combinations	$\boldsymbol{V}_{opt}$	Combinations
$\boldsymbol{V}_{v1}$	$0.25\boldsymbol{V}_{19}$+$0.5\boldsymbol{V}_{12}$+$0.25\boldsymbol{V}_{19}$	$\boldsymbol{V}_{v6}$	$0.25\boldsymbol{V}_{12}$+$0.5\boldsymbol{V}_{19}$+$0.25\boldsymbol{V}_{12}$
$\boldsymbol{V}_{v2}$	$0.25\boldsymbol{V}_{17}$+$0.5\boldsymbol{V}_{14}$+$0.25\boldsymbol{V}_{17}$	$\boldsymbol{V}_{v7}$	$0.25\boldsymbol{V}_{14}$+$0.5\boldsymbol{V}_{17}$+$0.25\boldsymbol{V}_{14}$
$\boldsymbol{V}_{v3}$	$0.25\boldsymbol{V}_{25}$+$0.5\boldsymbol{V}_{6}$+$0.25\boldsymbol{V}_{25}$	$\boldsymbol{V}_{v8}$	$0.25\boldsymbol{V}_{6}$+$0.5\boldsymbol{V}_{25}$+$0.25\boldsymbol{V}_{6}$
$\boldsymbol{V}_{v4}$	$0.25\boldsymbol{V}_{24}$+$0.5\boldsymbol{V}_{7}$+$0.25\boldsymbol{V}_{24}$	$\boldsymbol{V}_{v9}$	$0.25\boldsymbol{V}_{7}$+$0.5\boldsymbol{V}_{24}$+$0.25\boldsymbol{V}_{7}$
$\boldsymbol{V}_{v5}$	$0.25\boldsymbol{V}_{28}$+$0.5\boldsymbol{V}_{3}$+$0.25\boldsymbol{V}_{28}$	$\boldsymbol{V}_{v10}$	$0.25\boldsymbol{V}_{3}$+$0.5\boldsymbol{V}_{28}$+$0.25\boldsymbol{V}_{3}$

Similarly, the symmetrical switching pattern is designed mainly focused on harmonics reduction. The phase-opposed large vectors are distributed at the center and both sides of the sampling interval, as shown in Fig. 7. $\boldsymbol{V}_{19}$ and $\boldsymbol{V}_{12}$ are selected to provide zero-mean volt-second value when $\boldsymbol{V}_{v1}$ is the selected V[3], and the switching pattern is $\boldsymbol{V}_{19}\rightarrow\boldsymbol{V}_{17}\rightarrow\boldsymbol{V}_{25}\rightarrow\boldsymbol{V}_{24}\rightarrow\boldsymbol{V}_{28}\rightarrow\boldsymbol{V}_{12}\rightarrow\boldsymbol{V}_{28}\rightarrow\boldsymbol{V}_{24}\rightarrow\boldsymbol{V}_{25}\rightarrow\boldsymbol{V}_{17}\rightarrow\boldsymbol{V}_{19}$. The specific combinations of phase-opposed large vectors are listed in Table IV. Although the switching frequency will be a little higher than the sampling frequency due to unfixed state (0 or 1) in the border of each switching period, it can be easily implemented with DSP, which is widely used in industrial applications.

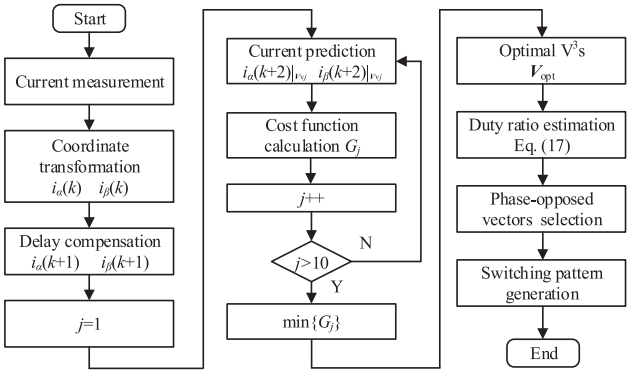

Fig. 8. Flowchart of the proposed IMPCC methods.

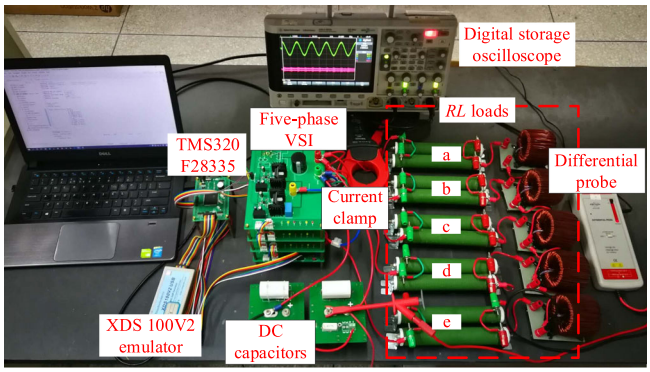

Fig. 9. An experimental prototype of the five-phase VSI.

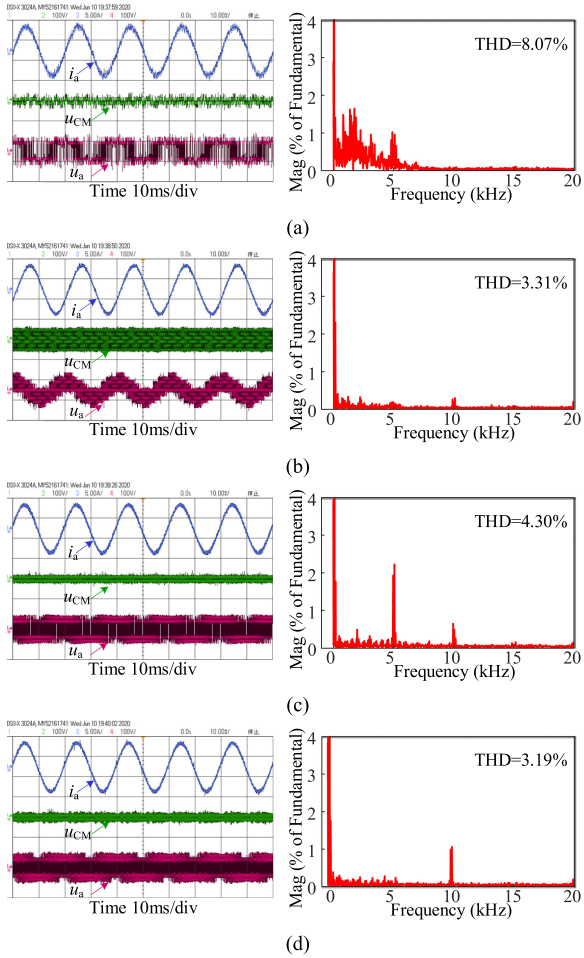

Fig. 10. Steady state performance of four control methods at the same sampling frequency. (a) CMPCC1, (b) CMPCC2, (c) IMPCC1, and (d) IMPCC2. (i_a: 5 A/div, u_{CM}: 100 V/div and u_a: 100 V/div).

E. Improved MPCC Method

The improved MPCC schemes are proposed based on the predefined V^{3}s and the optimized switching patterns, to reduce CMV and harmonic currents simultaneously. The proposed MPCC method with asymmetrical switching pattern is named as IMPCC1, and the one utilizing symmetrical pattern is named as IMPCC2. The prediction model, cost function as well as delay compensation are simplified, and only ten V^{3}s are evaluated during each sampling interval. As a result, the computation cost is reduced dramatically. Therefore, the proposed schemes using the V^{3}s as control set are easy to be implemented with DSP. The flowchart of the proposed IMPCC methods are shown in Fig. 8.

V. Experimental Results

The experimental prototype of the five-phase VSI is shown in Fig. 9. The Infineon IHW50N65 IGBT is adopted as power module. A TI DSP TMS320F28335 is adopted to implement the control methods. The phase current, CMV and phase voltage waveforms are measured using a current clamp (Tektronix A621), two differential probes (PINTECH N1015B) and a digital storage oscilloscope (Agilent Technologies InfiniiVision DSO-X 3024A). The resistance and inductance for experiments are 5Ω and 8 mH, and the dc-bus voltage is set as 100 V. In this article, the conventional MPCC method with CMV mitigation is named as CMPCC1 [31], and the conventional MPCC method based on the existing V^{3}s definition is named as CMPCC2 [39].

A. Steady Performance at the Same Sampling Frequency

In order to verify the effectiveness of the proposed IMPCC methods at the same sampling frequency (10 kHz), the experimental results of phase current, phase voltage, CMV and current spectrum are presented in Fig. 10. The peak current reference is 6 A in the steady state tests. It is obvious that the CMV is restricted within $\pm 0.1V_{dc}$ in IMPCC1 and IMPCC2, reduced by 80% compared with CMPCC2 ($\pm 0.5V_{dc}$).

It can be easily found that the total harmonic distortion (THD) value in CMPCC1 is the largest (8.07%), which is the main limitation of this method. THD values in IMPCC2 and CMPCC2 are much similar, being 3.19% and 3.31%, respectively. THD in IMPCC1 is 4.30%, slightly higher than that in IMPCC2, due to the asymmetrical switching pattern. Therefore, the current THDs in the proposed IMPCC methods are lower than that in CMPCC1 at the same sampling frequency.

The current trajectories in α-β and x-y subspaces are shown in Fig. 11. It is clear that the current ripples in IMPCC1 and

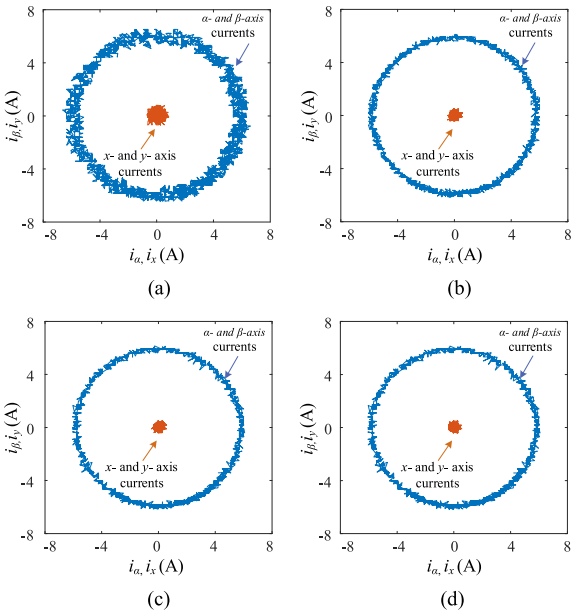

Fig. 11. Current trajectories in α-β and x-y subspaces at the same sampling frequency. (a) CMPCC1, (b) CMPCC2, (c) IMPCC1, and (d) IMPCC2.

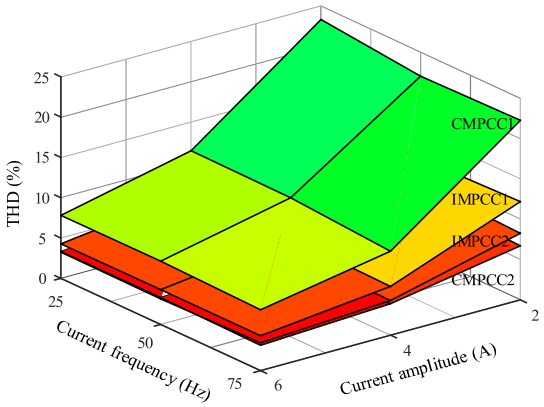

Fig. 12. THD comparison of the studied methods under different conditions.

IMPCC2 are similar to CMPCC2, and smaller than that in CMPCC1.

In order to compare the studied methods under different conditions, the THD values with respect to different amplitude and frequency of the reference current in the four control schemes are shown in Fig. 12.

Unsurprisingly, CMPCC1 behaves the worst current performance, IMPCC2 and CMPCC2 have approximately same performance, and IMPCC1 has slightly worse performance than IMPCC2.

Moreover, the average switching frequency of the studied methods at different conditions are also compared, as shown in Fig. 13. The average switching frequency is defined as

$$f_{\mathrm{sw}} = \frac{1}{5T_{\mathrm{w}}} \sum_{k=\mathrm{a}}^{\mathrm{e}} N_k \tag{18}$$

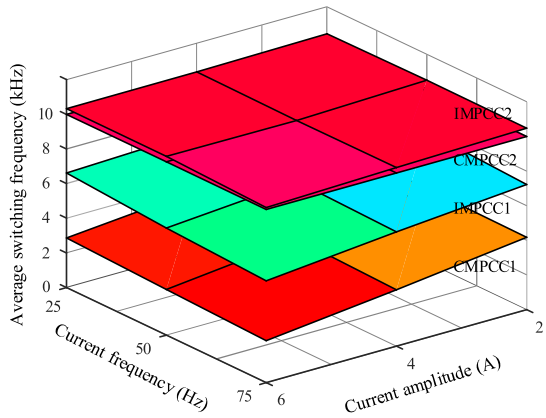

Fig. 13. Average switching frequency of the four methods at different conditions.

TABLE V
COMPARISON OF THE STUDIED METHODS AT APPROXIMATELY SAME SWITCHING FREQUENCY

Control methods	Switching frequency	Sampling frequency	Sampling period	THD
PI-SVPWM	2.5kHz	2.5kHz	400us	7.22%
CMPCC1	2.69 kHz	10 kHz	100 us	8.07%
CMPCC2	2.50 kHz	2.5 kHz	400 us	5.38%
IMPCC1	2.71 kHz	5 kHz	200 us	7.71%
IMPCC2	2.62 kHz	2.5 kHz	400 us	7.86%

where T_{w} is time window in which the ON-OFF times of IGBTs are counted, and T_{w} is set to 1s in this test. N_k represents the ON-OFF times of leg k (k = a, b, c, d, e).

The average switching frequency in CMPCC2 and IMPCC2 are both 10 kHz approximately. The switching frequency is lower in IMPCC1, due to the asymmetrical switching pattern. And the conventional CMPCC1 has the lowest average switching frequency at the same sampling frequency.

B. Steady State Performance at the Same Switching Frequency

In order to verify the feasibilities of the proposed methods at the same switching frequency, supplementary experiments are carried out. The average switching frequency in CMPCC1 is about 2.69 kHz when the sampling frequency is 10 kHz. In order to achieve similar switching frequency, the sampling frequency of CMPCC2 and the proposed IMPCC schemes are adapted, as listed in Table V. Besides, the experimental results of conventional PI-SVPWM with CMV reduction method is also presented. The switching frequency is 2.5 kHz and the parameters of the PI controllers are designed according to the solution reported in [40].

The experimental results of phase current, phase voltage, CMV and current spectrum at the same average switching frequency are shown in Fig. 14. IMPCC1 and IMPCC2 still have better steady state performance over the conventional CMPCC1 at the same average switching frequency. The PI-SVPWM should have the best steady state performance, but

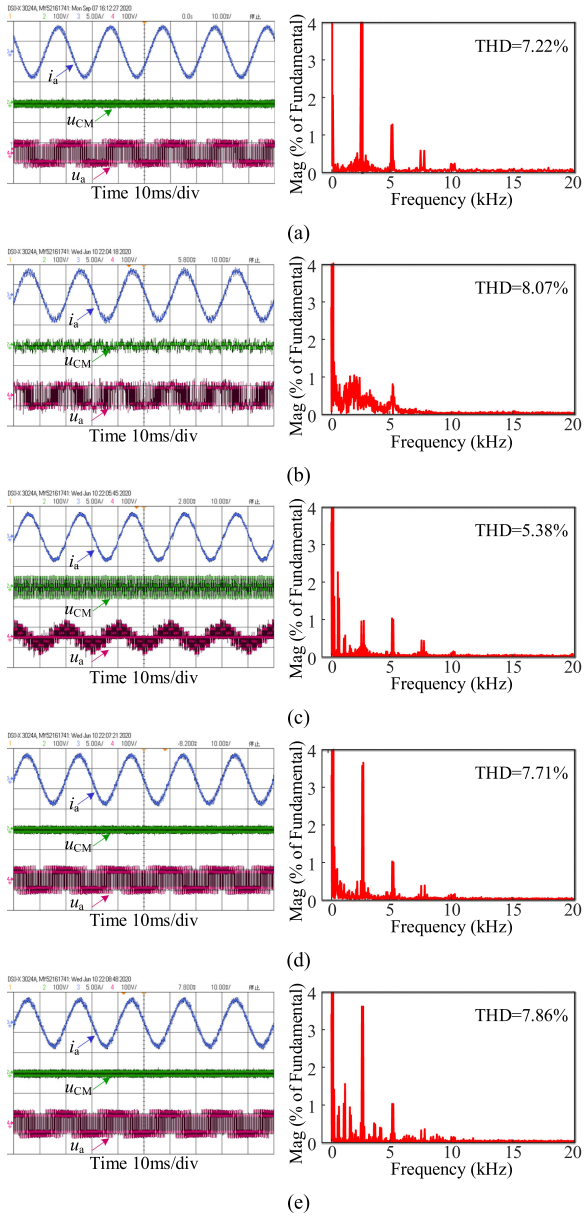

Fig. 14. Steady state performance of the studied methods at the same switching frequency. (a) PI-SVPWM, (b) CMPCC1, (c) CMPCC2, (d) IMPCC1 and (e) IMPCC2. (i_a: 5A/div, u_{CM}: 100V/div and u_a: 100V/div).

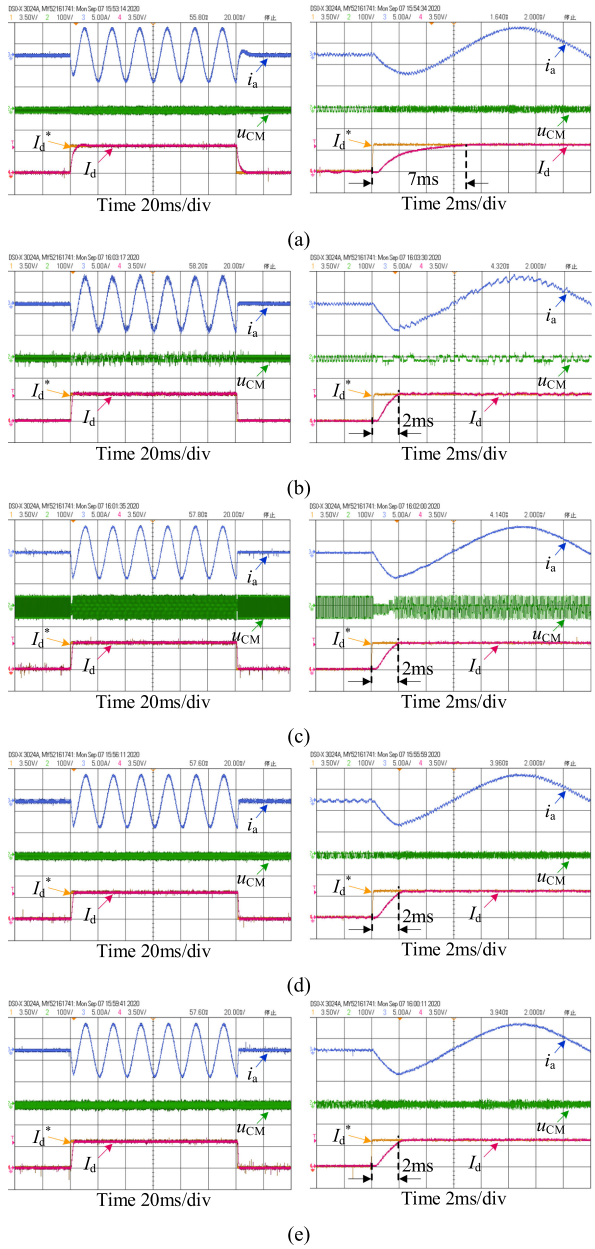

Fig. 15. Dynamic performance comparisons of (a) PI-SVPWM, (b) CMPCC1, (c) CMPCC2, (d) IMPCC1 and (e) IMPCC2. (i_a: 5A/div, I_d: 5A/div and u_{CM}: 100V/div).

the SVPWM with CMV reduction generates additional current ripples [18], resulting in higher THD than CMPCC2. As a result, the proposed methods have the approximately same THD values with the PI-SVPWM method. Moreover, IMPCC1 (5 kHz) and IMPCC2 (2.5 kHz) reduce the sampling frequencies compared with CMPCC1, significantly. Therefore, cheaper controllers can be used to implement the proposed schemes, which makes it cost-efficient.

C. Dynamic Performance

In order to evaluate the dynamic performance of the studied methods, Fig. 15 shows the dynamic waveforms when the current reference step changes from 0 A to 6 A. It can be noticed that the phase current can track the reference accurately and achieve fast dynamic performance in both IMPCC1 and IMPCC2 (2 ms), while the PI-SVPWM method shows much slower dynamic performance (7 ms). Therefore, the proposed IMPCC methods keep fast dynamic performance of MPCC, which is the salient feature compared with the PI-SVPWM method.

D. Sensitivity to Parameters Mismatches

The above experimental evaluations are carried out with accurate parameters. To investigate the performance of the proposed IMPCC methods with parameter mismatches, further experimental tests are presented, as shown in Fig. 16. And only

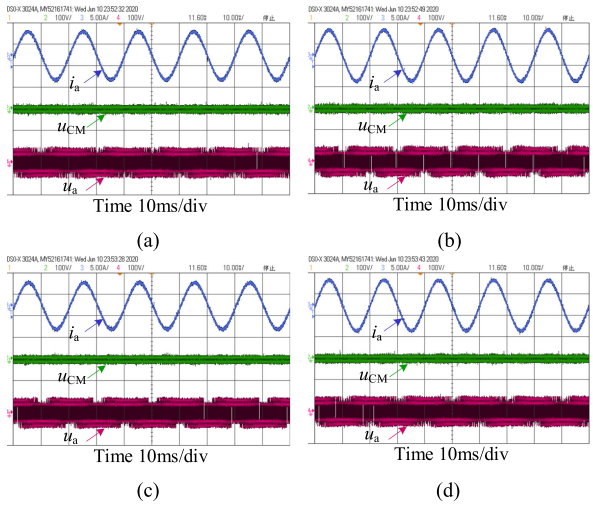

Fig. 16. Steady state performance of IMPCC1 with different parameter mismatches. (a) $\eta_R = -50\%$, $\eta_L = 0\%$, (b) $\eta_R = 50\%$, $\eta_L = 0\%$, (c) $\eta_R = 0\%$, $\eta_L = -50\%$, and (d) $\eta_R = 0\%$, $\eta_L = 50\%$. (i_a: 5A/div, u_{CM}: 100V/div and u_a: 100V/div).

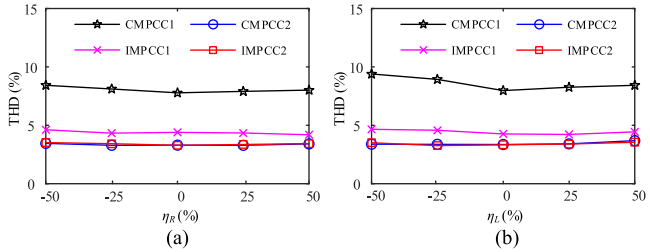

Fig. 17. THD values of the four methods with different parameter mismatches. (a) Resistance mismatches. (b) Inductance mismatches.

the waveforms of IMPCC1 are presented for simplicity. The parameter mismatch ratio η_x is defined as

$$\eta_x = \frac{X' - X}{X} \times 100\% \tag{19}$$

where X represent the accurate parameter, while X' is the mismatched parameter in the control methods.

Four cases of parameter mismatch are presented in Fig. 16, namely: (a) $\eta_R = -50\%$, $\eta_L = 0\%$; (b) $\eta_R = 50\%$, $\eta_L = 0\%$; (c) $\eta_R = 0\%$, $\eta_L = -50\%$; (d) $\eta_R = 0\%$, $\eta_L = 50\%$. It is clear that the CMV reduction is not affected by parameter mismatches, and current waveforms are still sinusoidal.

Fig. 17 shows the current THD values of the studied methods with different parameter mismatch ratios. It is clear that the load resistance and inductance mismatches have negligible effects on the performance of the studied methods. Moreover, the proposed IMPCC1 and IMPCC2 still have lower harmonics and THD values with different parameter mismatches compared with CMPCC1.

E. Comparison of Computation Cost

The detailed execution time of these four MPCC methods are shown in Fig. 18. High computation cost requires more

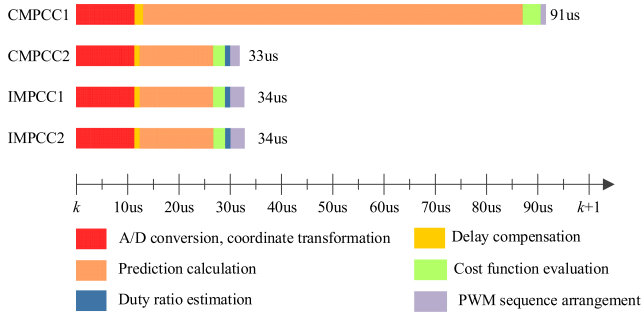

Fig. 18. Detailed execution time of the studied MPCC methods in TMS320F28335.

TABLE VI
OVERALL COMPARISON OF THE PROPOSED METHODS WITH THE EXISTING METHODS

Performances	CMPCC1	CMPCC2	IMPCC1	IMPCC2
CMV	$\pm 0.1 V_{dc}$	$\pm 0.5 V_{dc}$	$\pm 0.1 V_{dc}$	$\pm 0.1 V_{dc}$
Computation cost	Heavy	Easy	Easy	Easy
Steady-state performance	General	Excellent	Good	Excellent
Dynamic performance	Fast	Fast	Fast	Fast
Switching frequency	Low	High	Medium	High
Maximum output voltage	$0.6472 V_{dc}$	$0.5527 V_{dc}$	$0.5257 V_{dc}$	$0.5257 V_{dc}$

expensive controllers to implement the control method, which makes it cost-inefficient. In the conventional CMPCC1, all the basic voltage vectors are utilized to execute the enumeration optimization procedure, leading to heavy computation cost. Moreover, the predictive model, cost function and even the delay compensation are complex, hence, the execution time of CMPCC1 is the highest (91us). With the utilization of V^3s, the harmonic currents and CMV are reduced inherently, leading to simplified enumeration procedure. As a result, computation complexity is simplified in IMPCC1 and IMPCC2. The execution time of the proposed methods is 34 us, reduced by about 63%.

F. Overall Comparison of the Studied Methods

In order to evaluate the proposed IMPCC methods clearly, the performances of the studied control methods are listed in Table VI. It is clear that CMPCC2 has superior steady state performance and low computation cost, but CMV amplitude is large ($\pm 0.5\ V_{dc}$); Although CMV is reduced in CMPCC1, the steady state performance is the worst, and the computation cost is the heaviest. The proposed methods achieve CMV reduction and harmonic currents suppression, simultaneously. In addition, compared with CMPCC1, the proposed methods reduce computation complexity significantly, which can be easily implemented in digital controllers. Regarding to the proposed two methods, IMPCC1 has a little worse steady state performance and lower switching frequency, while IMPCC2 has better steady state performance and higher switching frequency.

Moreover, IMPCC1 and IMPCC2 keep fast dynamic performance as the inherent characteristic of FCS-MPC. However, it should be noticed that the maximum available output voltage of the proposed IMPCC is reduced compared with CMPCC1, which is the cost of low-order harmonics suppression [34].

VI. Conclusion

In this article, a new definition of virtual voltage vectors (V^3s) is firstly proposed by selecting four adjacent large vectors as candidates, which is quite different from the existing definition. CMV and harmonic terms are cancelled in the cost function, and the empirical weighting factors tuning is avoided. Secondly, the duty ratio optimization is introduced to reduce current ripples. Dwell time of the optimal V^3 is estimated and phase-opposed large vectors are utilized to adjust the volt-second value. Then, to achieve satisfactory steady state performance, two optimized switching patterns are designed. Finally, on the basis of the predefined V^3s and the redesigned switching patterns, two improved model predictive current control methods (IMPCC1 and IMPCC2) are proposed to mitigate CMV, suppress low-order harmonic currents and reduce calculation complexity simultaneously. The feasibilities of the proposed IMPCC methods are validated by experimental results. For clarity, the salient superiorities of the proposed IMPCC methods are summarized.

1) CMV is restricted within $\pm 0.1 V_{\mathrm{dc}}$, reduced by 80% compared with CMPCC2.
2) Superior steady state performance is achieved, the current THD and ripples are reduced.
3) Fast dynamic response is kept as the inherent characteristic of FCS-MPC.
4) The weighting factors are not required in the cost function, and the empirical parameters tuning is avoided.
5) Computation cost is reduced by about 63% compared with the CMPCC1, which makes it cost-efficient.

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