High-Reliability and Reduced Switch Count Single-Phase Dual-Output Current Source Inverter Using Switching-Cell Structure

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***Abstract*—In this article, a novel high-reliability single-phase dual-output current source inverter is presented. By using the switching-cell (SC) structure in the proposed topology, the overlap-time between switching transition can be minimized or eliminated. This improves the quality of ac output currents, efficiency, and dc-source utilization. Additionally, the capacitors in SC structure can help to reduce *dv/dt* of power switches and clamp the overshoot voltage under open-circuit problems, thus improving reliability. Two modes of common and different frequency operations are considered and detailed pulsewidth modulation schemes are presented. A 650-W hardware prototype was built and tested to verify the performance of the proposed inverter, and the results are compared with conventional single-phase dual-output current source inverters.**

***Index Terms*—Current source inverter, dual-output, high-reliability, overlap-time, single-phase inverter, switching-cell, voltage overshoot.**

I. Introduction

When compared to voltage source inverter (VSI), current source inverter (CSI) has the following advantages:

1) VSI requires the use of a boosting circuit when the input voltage is smaller than the output voltage, whereas CSI has an inherent voltage boosting function [1]–[3].
2) Power decoupling in CSI is realized by an inductor, which has a longer lifetime than electrolytic capacitors used in VSI [4], [5].
3) A rapid controlling system can be achieved owing to intrinsic short-circuit protection and direct-current control capability [6].
4) CSI can achieve high power factor operation because it has an ability to inject current with known magnitude to the grid [7], [8].
5) The development of superconducting magnetic energy storage systems can provide better power decoupling efficiency in CSI [9], [10].

From these advantages, CSIs are attractive in applications such as photovoltaic grid-connected systems [11]–[16] and others.

In many industrial applications, there is a need to supply energy to two ac autonomous loads at the same time. For example, two separate inverters with the conventional method of controlling two ac loads are used. However, this method increases both the cost and volume of the whole system. Similarly, dual-output (DO) CSIs sharing the same dc-bus yield high conduction loss due to the series connection of many semiconductor devices. As can be seen in Fig. 1(a), the topology of two H-bridge (2HB) single-phase CSIs always has eight conducting devices (i.e., four active switches and four diodes). To reduce the conduction loss, the topology shown in Fig. 1(b) is proposed in [17]. However, it still has six conducting devices at the same time. Besides, like other CSIs, these topologies still suffer from the open-circuit problem. An overlap-time must be inserted between switching transitions to ensure the continuity of dc current [18]–[21]. This overlap-time causes distortions in output waveforms, reduces both efficiency and dc-source utilization, as analyzed in [20] and [21].

In [22] and [23], the basic p- and n-switching cells (SCs) shown in Fig. 2 were presented, and the topology of the SC-CSI was introduced to resolve the commutation problem. Although the feasibility of this configuration was proved, a detailed analysis of the operation principle was omitted.

To overcome the disadvantages of the conventional ones, this article proposes a single-phase DO-SC-CSI. The proposed topology uses only six active switches instead of eight and only four devices (i.e., two switches and two diodes) are conducting during the operation. Therefore, compared to the conventional DO-CSIs, it can reduce the number of switches and conduction loss. Moreover, the two SC capacitors C_1 and C_2 connected between the switches and diodes provide continuous current paths for the input current source ($I_{\rm dc}$). Therefore, the overlap-time can theoretically be eliminated completely or at least minimized, which leads to better output waveform quality. Similar to the conventional DO-CSIs, the proposed DO-SC-CSI can be used in two-phase open-end winding induction motor drive [24], smart microgrid applications [25], and photovoltaic grid-connected

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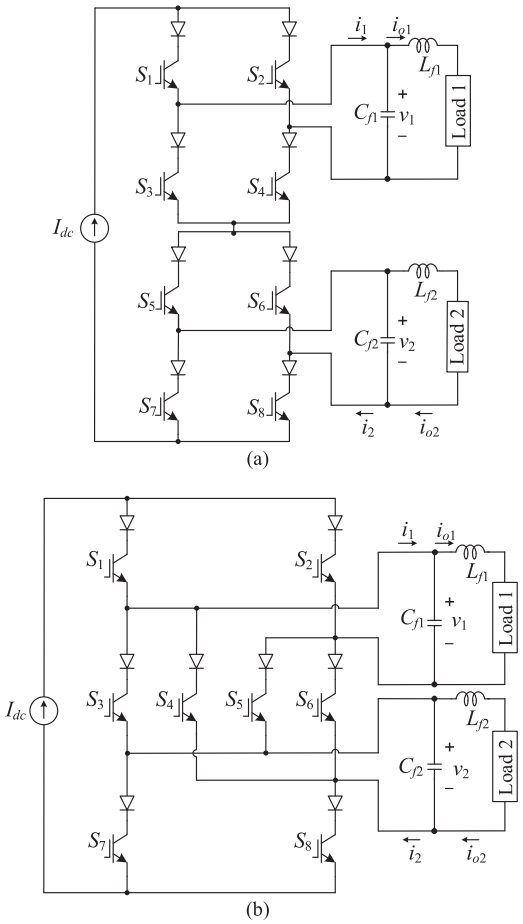

Fig. 1. Conventional single-phase DO CSIs. (a) 2HB single-phase CSIs connected in series. (b) Proposed in [17].

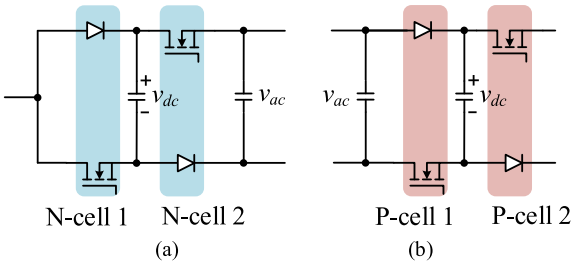

Fig. 2. Series connection of two (a) n-cells and (b) p-cells.

systems. Also, the proposed inverter can be used as an ac–ac current source converter in [27], a power decoupling for current source converters [5], [28], etc.

II. Topology and Operation Principle

Fig. 3 shows the proposed single-phase DO-SC-CSI. It has three two-switch phase legs (leg a, leg b, and leg c), two single-phase output loads, and two SC capacitors (C_1 and C_2) combined with four diodes (D_1, D_2, D_4, and D_5) to form the paths to the current source. The two outputs share the middle phase leg. Therefore, the switching states of two outputs affect each other.

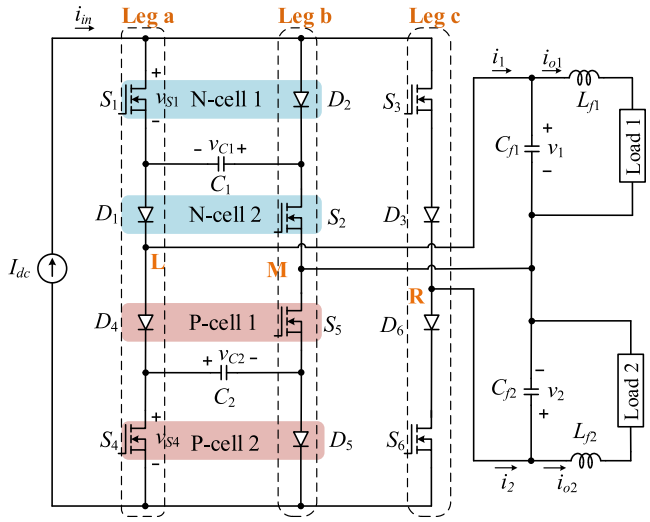

Fig. 3 Proposed single-phase DO-SC-CSI.

A. Carrier-Based PWM With Offset Function

The operation of the proposed inverter is divided into two modes: different-frequency (DF) and common-frequency (CF) modes. In the CF mode, the two outputs have the same fundamental frequencies, and the amplitudes of them can be different. Depending on the phase difference between the references, the two outputs have modulation indices up to one. When the output current references are in-phase, the total magnitude of them can go up to two.

In the DF mode, the two outputs are independent of each other in both amplitude and frequency, the sum of the magnitude of their reference signals must be less than one.

The CSI outputs are modulated by two references (m_1 and m_2) as follows:

$$\begin{cases} m_1 = 0.5M_1 \sin(2\pi f_{o1} t + \varphi_{o1}) \\ m_2 = 0.5M_2 \sin(2\pi f_{o2} t + \varphi_{o2}). \end{cases} \tag{1}$$

In (1), M_1 and M_2 represent modulation indices. f_{o1} and f_{o2} are output frequencies. φ_{o1} and φ_{o2} are phase angles of m_1 and m_2, respectively.

In order to avoid modulating wave interference, the appropriate offsets ($i_{o1.\text{off}}$, $i_{o2.\text{off}}$) should be added to the references. Therefore, modulating references are determined as follows:

$$\begin{cases} i_{o1.u} = i_{o1.\text{off}} + 0.5M_1 \sin(2\pi f_{o1} t + \varphi_{o1}) \\ i_{o1.d} = i_{o1.\text{off}} - 0.5M_1 \sin(2\pi f_{o1} t + \varphi_{o1}) \end{cases} \tag{2}$$

$$\begin{cases} i_{o2.u} = i_{o2.\text{off}} + 0.5M_2 \sin(2\pi f_{o2} t + \varphi_{o2}) \\ i_{o2.d} = i_{o2.\text{off}} - 0.5M_2 \sin(2\pi f_{o2} + \varphi_{o2}) \end{cases} \tag{3}$$

where $i_{o1.u}$, $i_{o2.u}$, $i_{o1.d}$, and $i_{o2.d}$ are the modulating references for upper and lower terminals, L and R, respectively. Hence, output references ($i_{o1.\text{ref}}$, $i_{o2.\text{ref}}$) can be determined as

$$\begin{cases} i_{o1.\text{ref}} = i_{o1.u} - i_{o1.d} = M_1 \sin(2\pi f_{o1} t + \varphi_{o1}) \\ i_{o2.\text{ref}} = i_{o2.u} - i_{o2.d} = M_2 \sin(2\pi f_{o2} t + \varphi_{o2}). \end{cases} \tag{4}$$

The sum of the modulation indices must ensure the following conditions:

$$\begin{cases} M_1 + M_2 \le 2, & \text{CFmode} \\ M_1 + M_2 \le 1, & \text{DFmode.} \end{cases} \tag{5}$$

By adding appropriate offset values, references in the CF and DF modes are shifted in modulation space, as shown in Fig. 4(a) and (b). The modulating waveform of output 1 should always be greater than that of output 2, as given by

$$i_{o1.u} \ge i_{o2.u}, i_{o1.d} \ge i_{o2.d}. \tag{6}$$

Therefore, the additional offsets should ensure the following conditions:

$$i_{o1.\text{off}} \le 1 - 0.5M_1, i_{o2.\text{off}} \ge 0.5M_2. \tag{7}$$

Fig. 4(c) shows the gate signal generation logic of the proposed single-phase DO-SC-CSI. Modulating waveforms and gate signals over a switching cycle are shown in Fig. 4(d).

B. Switching-State Analysis

Fig. 5 shows current paths for each switching state, which are as follows.

1) *States 1, 8, and 9:* One of the legs has all switches in the ON state. Thus, two output currents i_1 and i_2 are zero, as shown in Fig. 5(a), (h), and (i), respectively.
2) *State 2:* S_2 and S_6 are ON. The output current i_1 is zero, and the output current i_2 becomes $-I_{\text{dc}}$, as shown on the right-hand side of Fig. 5(b). However, when the voltage of the capacitor C_2 is lower than the total output voltage, i.e., $v_{C2} < (v_1 + v_2)$, the capacitor C_2 is charged through D_4 and D_5, as shown in the left-hand side of Fig. 5(b).
3) *States 3 and 6:* All switches of the phase leg b are OFF. Therefore, one of the two output currents is I_{dc}, and the other one is $-I_{\text{dc}}$, as shown in Fig. 5(c) and (f).
4) *States 4 and 5:* All switches of the leg c are OFF. The i_2 is zero, and i_1 is $-I_{dc}$ or I_{dc}, as shown in Figs. 5(d) and (e), respectively.
5) *State 7:* S_3 and S_5 are ON. i_1 is zero, and i_2 becomes I_{dc}, as shown in the right-hand side of Fig. 5(g). However, the capacitor is charged through D_2 and D_1 when the voltage of the capacitor C_1 is lower than the total negative output voltage, i.e., $v_{C1} < -(v_1 + v_2)$, as shown on the left-hand side of Fig. 5(g).

From the switching-state analysis, it can be seen that the maximum voltage of SC capacitors ($V_{C1.\max}$, $V_{C2.\max}$) is given as

$$V_{C1.\max} = V_{C2.\max} = V_{1P} + V_{2P} \tag{8}$$

where V_{1P} and V_{2P} are the peak values of the output voltages 1 and 2, respectively.

C. Overlap-Time

Fig. 6 shows the gate signals and simplified equivalent circuit of the proposed single-phase DO-SC-CSI during overlap-time. The capacitor C_1 discharges during overlap-time between S_1 and S_2. As shown in Fig. 6(a), the capacitor C_1 discharges through

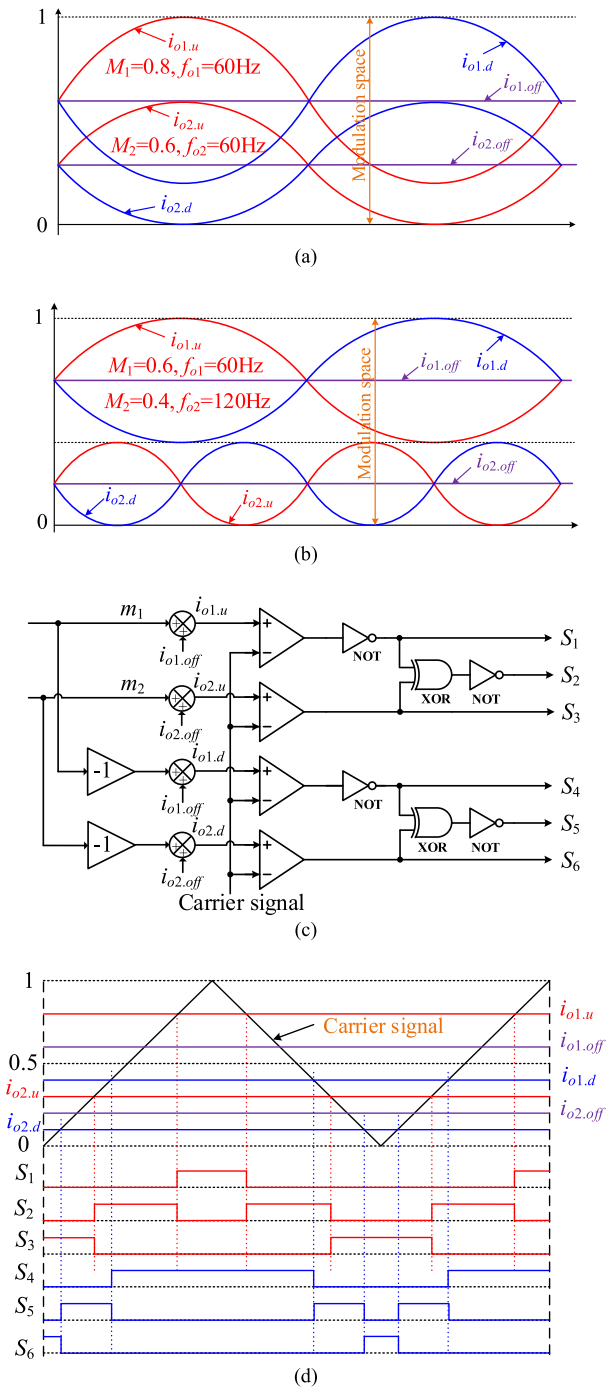

Fig. 4. (a) Modulation space division in the CF mode. (b) Modulation space division in the DF mode. (c) Gate signal generation logic of the proposed inverter. (d) Modulating waveforms and gate signals over one switching cycle.

the loop S_2, load 2, D_6, S_6, and S_1 when switches S_1, S_2, and S_6 are ON. When switches S_1, S_2, and S_4 are ON, the capacitor C_1 discharges through the loop load 1, diode D_4, and switches are in ON state, as shown in Fig. 6(b). The capacitor C_2 discharges during overlap-time between S_4 and S_5. When switches S_1, S_4, and S_5 are ON, the capacitor C_2 discharges through the loop S_4, S_1, D_1, load 1, and S_5, as shown in Fig. 6(c). When S_3, S_4, and S_5 are ON, the capacitor C_2 discharges through S_4, S_3, D_3, load 2, and S_5, as shown in Fig. 6(d).

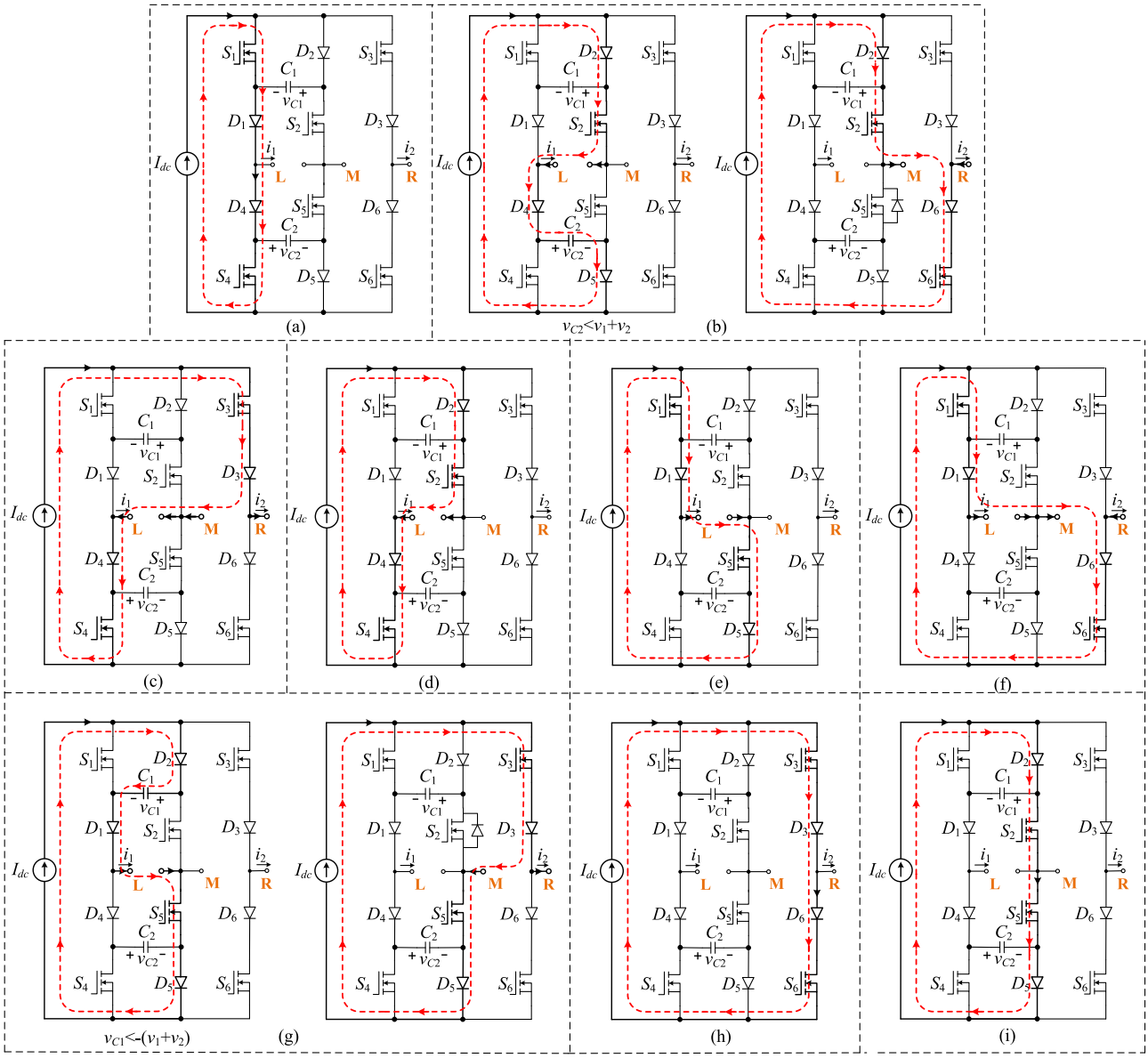

Fig. 5. Switching states of the proposed single-phase DO-SC-CSI.

As mentioned before, the SC capacitors C_1 and C_2 in the proposed inverter can help to reduce *dv/dt* of power switches and clamp the overshoot voltage under open-circuit problems in power switches. Therefore, the overlap-time between gate signals can be minimized. While the conventional DO-CSI, the overlap-time must be large enough to guarantee a safe transition. The overlap-time effect in the DO-CSI is presented as follows.

Take output current i_1 as an example, Fig. 7 shows the impact of overlap-time on i_1. It can be seen that some parts of output current pulses (ΔI) are lost due to the overlap-time. The total current pulse losses are

$$\Delta I_{o1} = 2 \cdot \Delta t_{\rm ov} \cdot f_s \cdot I_{\rm dc}. \tag{9}$$

In (9), $\Delta I_{\rm ol}$ is the total current pulse losses over one period of output fundamental frequency, $\Delta t_{\rm ov}$ is the overlap-time, f_s is the frequency of carrier signal, and $I_{\rm dc}$ is the magnitude of the dc source.

As presented in [20], the overlap-time will result in a deviation of the output current for both negative and positive parts. Applying Fourier decomposition, the output current wave deviation is given as

$$\Delta I_{o1}(t) = \frac{2\sqrt{3}}{\pi} \cdot \Delta t_{\rm ov} \cdot f_s \cdot I_{\rm dc} \left(\sin \omega t - \frac{\sin 5\omega t}{5} - \frac{\sin 7\omega t}{7} \dots \right). \tag{10}$$

Therefore, additional odd harmonics components in the output current waveform can be found in (10). The harmonics are affected proportionally by $\Delta t_{\rm ov}$, dc source $I_{\rm dc}$, and switching frequency f_s.

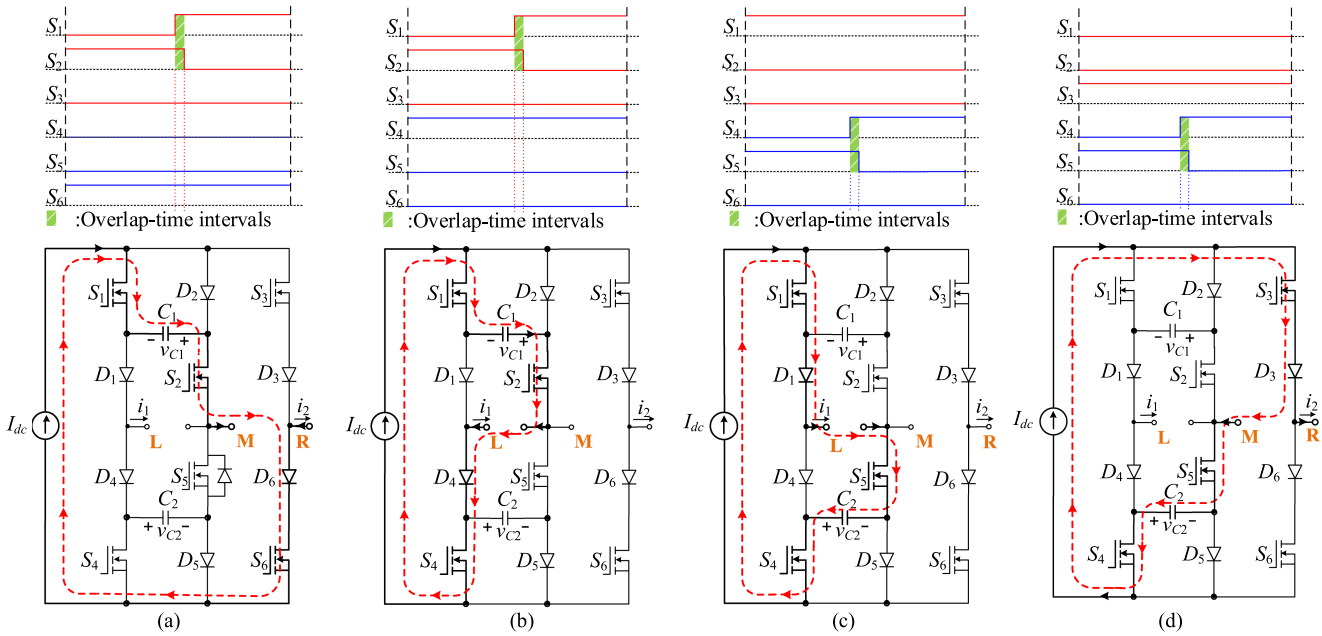

Fig. 6 Gate signals and simplified equivalent circuits of the proposed single-phase DO-SC-CSI during overlap-time. (a) and (b) Overlap-time between S_1 and S_2. (c) and (d) Overlap-time between S_4 and S_5.

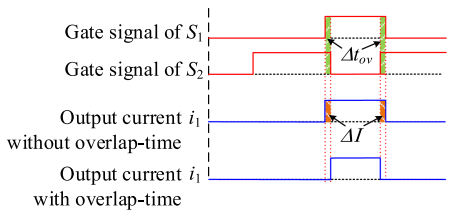

Fig. 7. Effects of overlap-time on output current.

D. Reliability Analysis

As explained before, CSIs generally require finite overlap-time for safe commutation. However, if there are some delays or mismatches in gate drive signals, there is an open-circuit problem and the switching devices are damaged by overvoltage because the input inductor current is blocked suddenly. The open-circuit problem may also be caused by EMI noise's misgating-off. For example, in the conventional single-phase DO-CSIs [see Fig. 8(a) and (b)], either the two top switches (S_1 and S_2) or bottom switches (S_7 and S_8), or all switches are accidentally turned-OFF, high *di/dt* will appear in the input inductor, generating high voltage spikes, which may damage power devices. On the other hand, in the proposed inverter as depicted in Fig. 8(c), the two capacitors C_1 and C_2 with four diodes (D_1, D_2, D_4, and D_5) can always provide a path for the input inductor. As shown in Fig. 8(c), the capacitors C_1 and C_2 are charged during the dead-time (Δt_d) and the increase in the capacitor voltages (ΔV_{C1} and ΔV_{C2}) is given by the following equation. For the sake of simplicity, C_1 and C_2 values are assumed to have the same capacitance C

$$\Delta V_{C1} = \Delta V_{C2} = \frac{I_{\rm dc}}{C}\Delta t_d. \tag{11}$$

The SC capacitor value C can be chosen to guarantee that the voltage stress of switches is always lower than the switch breakdown voltage ($V_{\rm sw.max}$) under fault conditions. The value of the SC capacitor is chosen by

$$C = \frac{I_{\rm dc}}{\Delta V_C}\Delta t_d. \tag{12}$$

In (12), the increase of the capacitor voltage (ΔV_C) is given as

$$\Delta V_C = V_{\rm sw.max} - (V_{1P} + V_{2P}). \tag{13}$$

E. Common-Mode Voltage

Fig. 9(a) shows the proposed DO-SC-CSI for grid-connected photovoltaic (PV) systems. C_{p1} and C_{p2} represent parasitic capacitances between PV panel and the earth terminal. The value of C_{p1} and C_{p2} are estimated to be 1μF/kW for thin and 50–150 nF/kW for the crystalline silicon module film module [12]. The common-mode voltage (CMV) $v_{{\rm cm}i}$ ($i = 1, 2$) can be obtained as

$$v_{\rm cm1} = \frac{v_{LN} + v_{MN}}{2}, v_{\rm cm2} = \frac{v_{RN} + v_{MN}}{2} \tag{14}$$

where v_{LN}, v_{MN}, and v_{RN} are the voltages between points L, M, R, and the point N, respectively. The relationship between CMVs and switching states of the proposed inverter is shown in Table I. S_x ($x = 1, 2, 3, 4, 5, 6$) represents the ON-state when $S_x = 1$, and OFF-state when $S_x = 0$. As can be seen, in Fig. 9(a), $v_{{\rm cm}i}$ ($i = 1, 2$) varies with high frequency, the ground leakage current exists in the DO-SC-CSI. To solve this issue, a modified DO-SC-CSI for grid-connected PV system is shown in Fig. 9(b). In Fig. 9(b), a common-mode choke ($L_{\rm dc1}$ and $L_{\rm dc2}$), and a split capacitor arrangement ($C_{\rm dc1}$ and $C_{\rm dc2}$) are used to reduce the

TABLE I
SWITCHING STATES AND CMV OF THE PROPOSED DO-SC-CSI

State	S_1	S_2	S_3	S_4	S_5	S_6	i_1	i_2	Fig. 9(a)		Fig. 9(b)	
									v_{cm1}	v_{cm2}	v_{cm1}	v_{cm2}
1	1	0	0	1	0	0	0	0	$-v_1/2$	$(v_2-v_1)/2$		
2	0	1	0	0	0	1	0	$-I_{dc}$	$(v_1-v_2)/2$	$-v_2/2$		
3	0	0	1	1	0	0	$-I_{dc}$	I_{dc}	$-v_1/2$	$(v_2-v_1)/2$		
4	0	1	0	1	0	0	$-I_{dc}$	0	$-v_1/2$	$(v_2-v_1)/2$		
5	1	0	0	0	1	0	I_{dc}	0	$v_1/2$	$v_2/2$	$(v_1+2V_{dc2})/2$	$(v_2+2V_{dc2})/2$
6	1	0	0	0	0	1	I_{dc}	$-I_{dc}$	$(v_1-v_2)/2$	$-v_2/2$		
7	0	0	1	0	1	0	0	I_{dc}	$v_1/2$	$v_2/2$		
8	0	0	1	0	0	1	0	0	$(v_1-v_2)/2$	$-v_2/2$		
9	0	1	0	0	1	0	0	0	$v_1/2$	$v_2/2$		

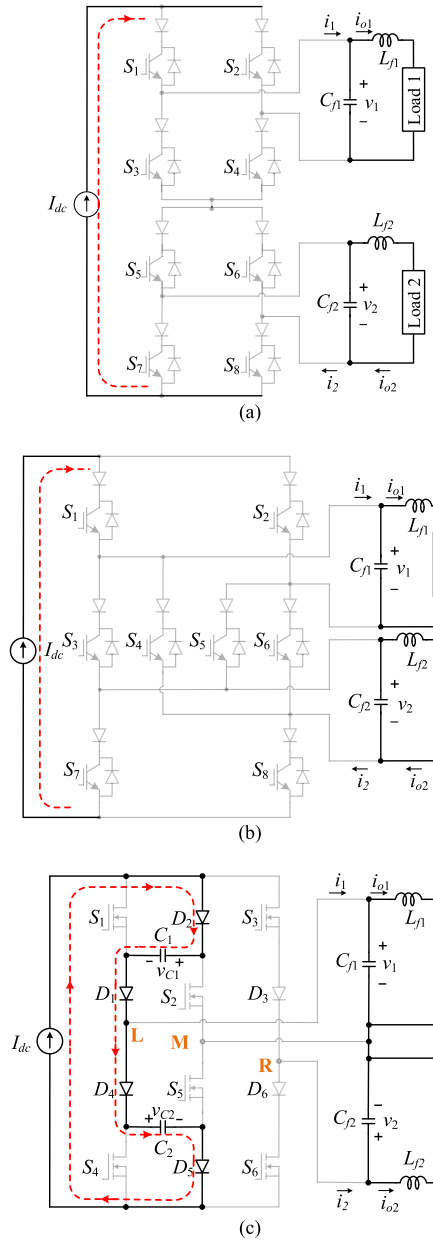

Fig. 8. Simplified equivalent circuits of the conventional and proposed inverter during dead-time. (a) 2HB CSIs. (b) DO-CSI in [17]. (c) Proposed DO-SC-CSI.

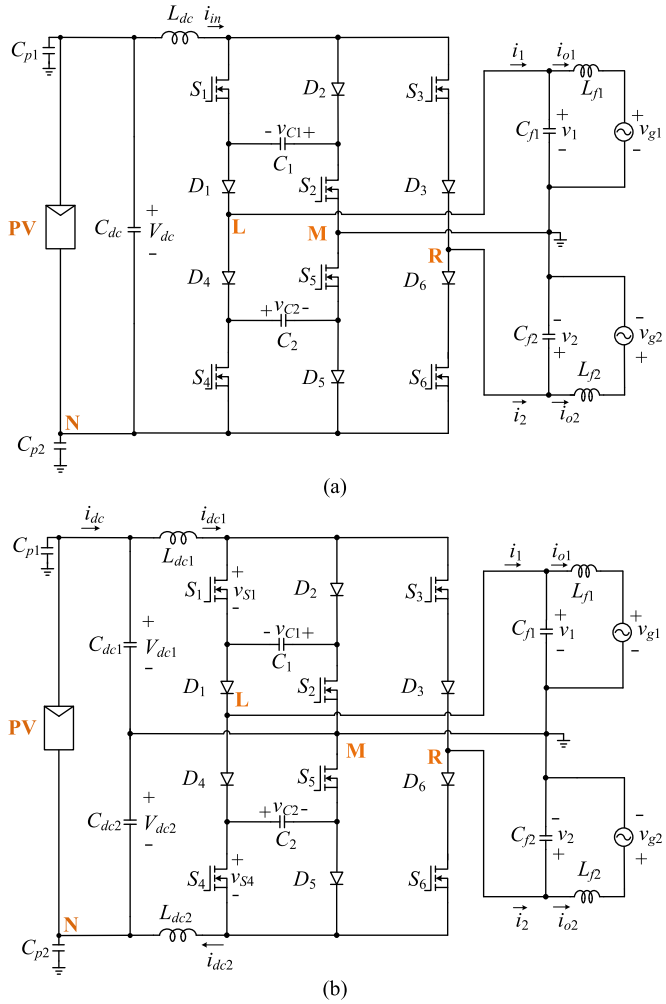

Fig. 9. (a) DO-SC-CSI for grid-connected PV system. (b) Modified DO-SC-CSI for grid-connected PV system.

leakage current for transformerless PV inverter system. As can be seen in Table I, the CMVs in Fig. 9(b) are always constant regardless of switching state and are expressed as

$$v_{\mathrm{cm1}} = \frac{v_1 + 2V_{\mathrm{dc2}}}{2}, \quad v_{\mathrm{cm2}} = \frac{v_2 + 2V_{\mathrm{dc2}}}{2} \tag{15}$$

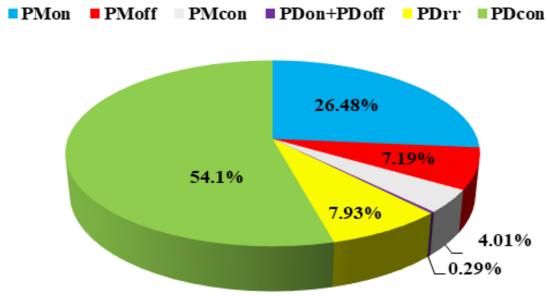

Fig. 10. Power loss of MOSFETs and diodes of the proposed inverter.

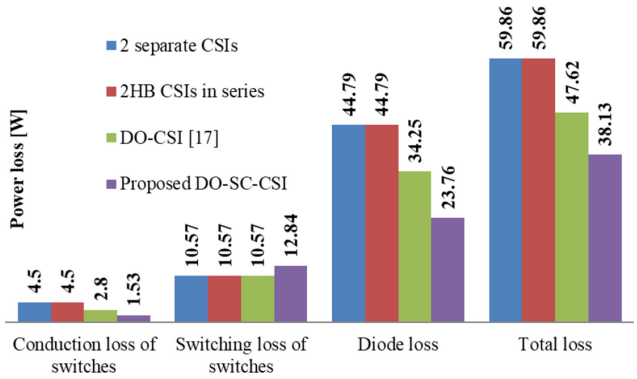

Fig. 11 Semiconductor loss comparison in the proposed and other conventional CSIs.

where v_1 and v_2 have sinusoidal variation at grid frequency. Therefore, $v_{\rm cm1}$ and $v_{\rm cm2}$ also have sinusoidal variation at the grid frequency. Thus, the ground leakage current is small and negligible because the impedance of C_{p1} and C_{p2} at the grid frequency is high.

III. Semiconductor Loss Analysis

Power loss of semiconductor devices includes conduction and switching losses of MOSFET and diode. In this article, the power loss equations in [26] is used for the loss calculation and the additional power losses in input inductor and others are not considered because they are small. The percentage of switching and conduction losses of diode and MOSFET is shown in Fig. 10. $P_{\rm Doff}$, $P_{\rm Drr}$, $P_{\rm Don}$, and $P_{\rm Dcon}$ are turn-OFF, reverse-recovery, turn-ON, and conduction losses of diode, respectively. $P_{\rm Mcon}$, $P_{\rm Moff}$, and $P_{\rm Mon}$ are conduction, turn-OFF, and turn-ON losses of MOSFET, respectively. The total semiconductor loss calculated by equations in [26] is 38.13 W at the rated output power 550 W. As expected, more than half of the loss comes from diode conduction loss. The semiconductor loss comparison among the proposed and other CSIs under the same condition of $P_{\rm o} = 550$ W, $I_{\rm in} = 7.5$ A, and $f_{\rm sw} = 30$ kHz is shown in Fig. 11 .

IV. Simulation and Experimental Results

A. Simulation Results

PSIM simulation is used to verify the operation of the proposed inverter. The system operates with two resistive loads of

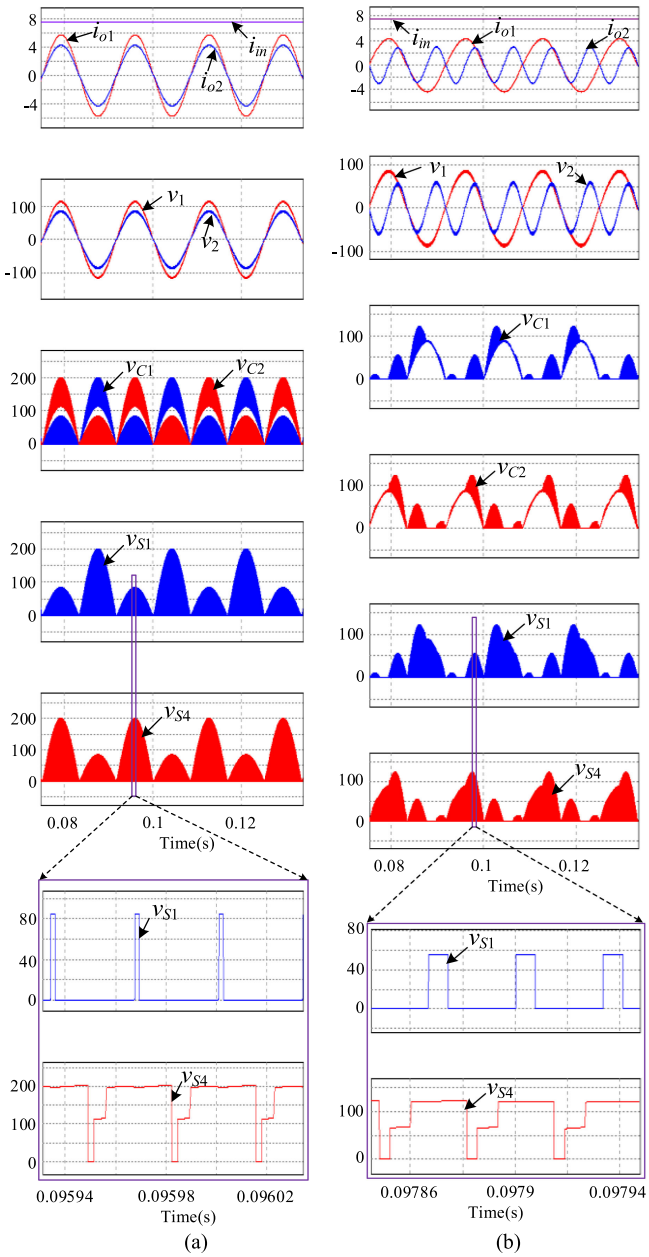

Fig. 12. Simulation waveforms of the proposed single-phase DO-SC-CSI with overlap-time of 0.3 μs. (a) CF mode. (b) DF mode.

20 Ω. The inductance and capacitance values of the ac filters are $L_{f1} = L_{f2} = 0.74$ mH and $C_{f1} = C_{f2} = 10$ μF, respectively. A 7.5 A ideal current source is used for the input and the switching frequency is 30 kHz. In the CF mode, two outputs are modulated using the additional offsets ($i_{o1.\rm off} = 0.55$, $i_{o2.\rm off} = 0.35$) with modulation indices ($M_1 = 0.8$, $M_2 = 0.6$) at the same frequency of 60 Hz. In the DF mode, $i_{o1.\rm off}$ and $i_{o2.\rm off}$ are 0.65 and 0.25 with modulation indices ($M_1 = 0.6$, $M_2 = 0.4$) at frequencies ($f_{o1} = 60$ Hz, $f_{o2} = 120$ Hz), respectively.

Fig. 12(a) shows the simulation results in the CF mode. In the simulation results, $i_{\rm in}$ is the input current, i_{o1} and i_{o2} are load currents, v_1 and v_2 are the output voltages, v_{C1} and v_{C2} are the voltages of SC capacitors (C_1 and C_2), and v_{S1}

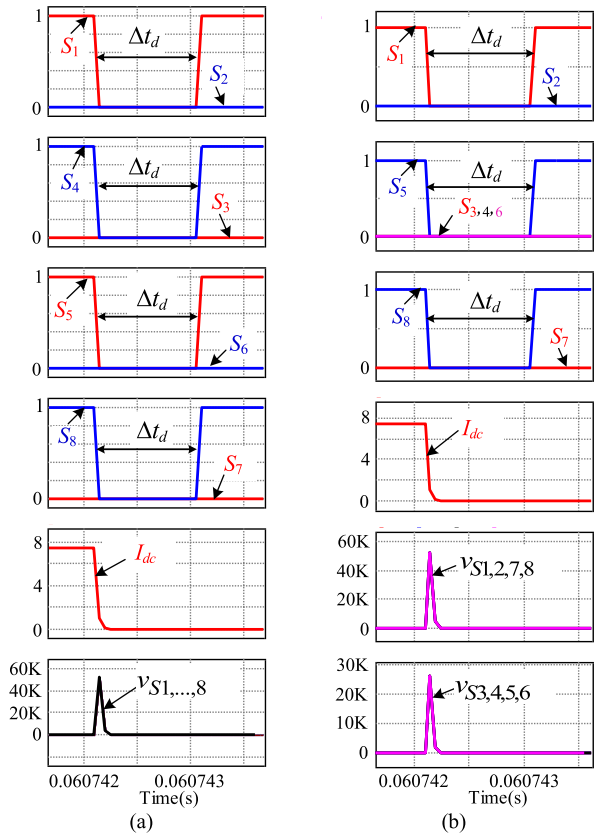

Fig. 13. Switch voltage stresses under fault condition during 1 μs dead-time. (a) 2HB CSIs. (b) DO-CSI in [17].

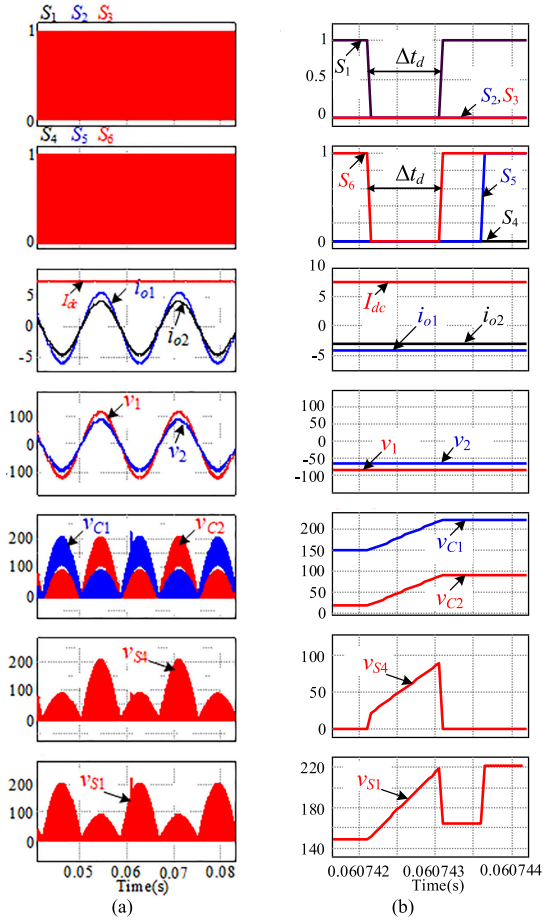

Fig. 14. (a) Simulation waveform of the proposed DO-SC-CSI under fault condition. (b) Magnification of (a) around the time interval when appearing fault.

and v_{S4} are the voltage stresses on the switches (S_1 and S_4), respectively. Similarly, simulation results in the DF are shown in Fig. 12(b). As can be seen, the inverter is able to generate the two currents i_{o1} and i_{o2} independently. The simulation results in Fig. 12 are consistent with the theoretical analysis.

To verify the operation under fault conditions, it is assumed that all the switching devices are accidentally turned-OFF during 1 μs. Under the fault conditions, in the conventional DO-CSIs, the inductor current has no path to flow, the high *di/dt* will appear in the inductor, and huge voltage spikes are generated across the switches. Fig. 13(a) shows the drain-to-source voltage waveforms of the switches of 2HB CSIs. It can be seen that a huge voltage spike of about 50 kV is generated across the switches. Similarly, as shown in Fig. 13(b), the switches of DO-CSI [17] also suffer from excessive voltage spikes.

On the other hand, in the proposed DO-SC-CSI, no significant voltage spike is generated and the switch voltages are well clamped, as shown in Fig. 14(a). The waveforms of Fig. 14(a) are magnified around the time interval when all the switching devices are accidentally turned OFF, as shown in Fig 14(b). It can be seen that SC capacitors (C_1 and C_2) are charged during this time. The relationship between ΔV_{C1} (or ΔV_{C2}) and Δt_d is given by (11). The change in capacitor voltages (ΔV_{C1}, and ΔV_{C2}) is 75 V (where $C = 0.1$ μF; $I_{\rm dc} = 7.5$ A; $\Delta t_d = 1$ μs). From Figs. 13 and 14, it can be concluded

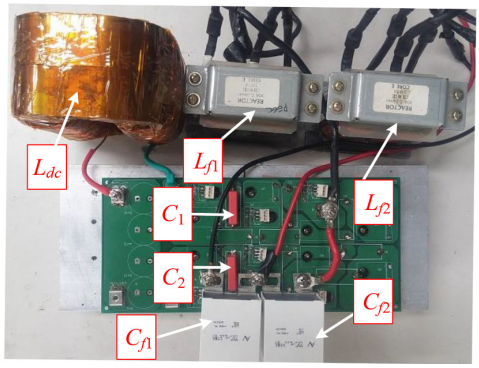

Fig. 15. Prototype photo of the proposed single-phase DO-SC-CSI.

that conventional DO-CSIs suffer from open-circuit problems, whereas the proposed DO-SC-CSI does not have such a problem and can work properly.

B. Experimental Results

In the experiment, 650-W prototypes of single-phase DO-SC-CSI and other CSIs were built and tested. A dc voltage source is

TABLE II
EXPERIMENTAL PARAMETER OF THE PROPOSED INVERTER

Symbol	Value	Symbol	Value	Symbol	Value
P_o	650 W	f_{sw}	30 kHz	C_{f1}, C_{f2}	10 μF
I_{dc}	7.5 A	C_1, C_2	0.1 μF	L_{f1}, L_{f2}	0.74 mH
L_{dc}	55 mH	R_1, R_2	20 Ω		

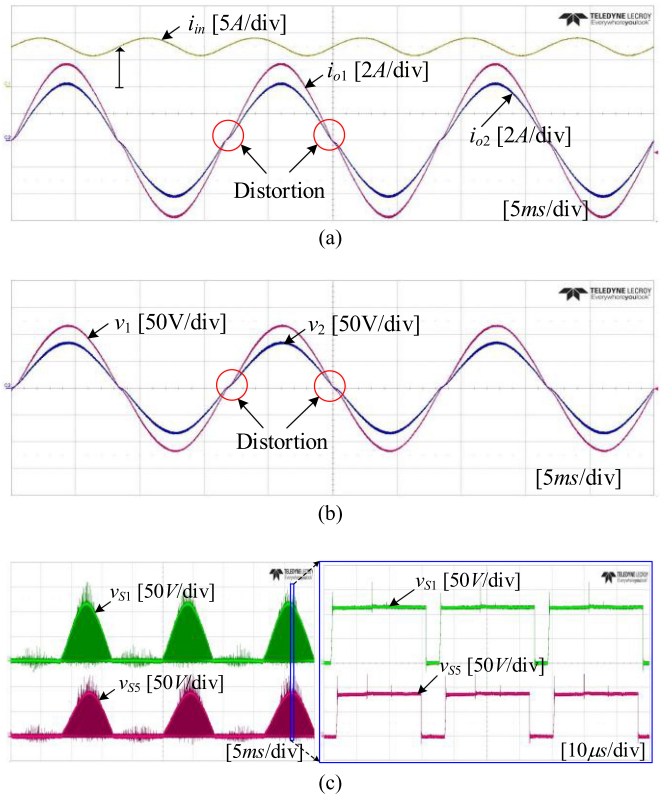

Fig. 16. Experimental waveforms of the 2HB CSIs with overlap-time of 0.8 μs. (a) Input and load currents. (b) Output voltages. (c) Switch voltages.

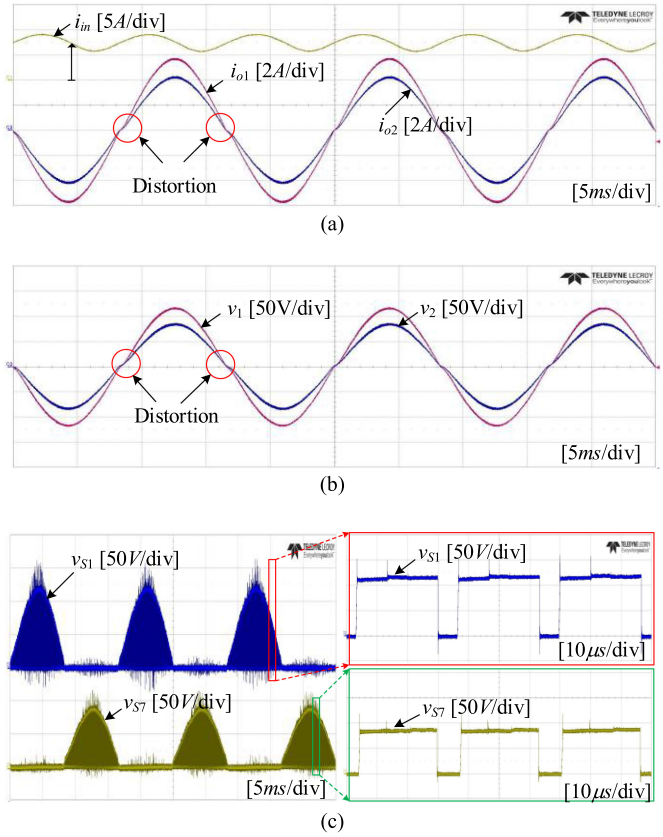

Fig. 17. Experimental waveforms of the DO-CSI [17] with overlap-time of 0.8 μs. (a) Input and load currents. (b) Output voltages. (c) Switch voltages.

connected with an inductance of 55 mH to represent the current source in the dc side. The input current on the dc side has the second-order harmonic of the output frequency. Therefore, the nonlinear modulation technique with functions, m_1 and m_2, in [7] is employed to improve the quality of both input and output currents. The 60C7040 MOSFETs and RHRG3060 diodes were used in both the conventional DO-CSIs and proposed DO-SC-CSI for fair comparison. The other experimental parameters are the same as simulation parameters, as shown in Table II. The photo of the proposed topology is shown in Fig. 15.

To verify the operation under normal conditions, 0.8 μs switch overlap-time is used for the control signals of the conventional DO-CSI. Fig. 16 shows the waveforms of 2HB CSIs. Fig. 16(a) shows the output currents with the total harmonic distortion (THD) of injected load currents i_{o1} and i_{o2} measured to be 4.3% and 4.7%, respectively. The output voltages v_1 and v_2 are shown in Fig. 16(b). Fig. 16(c) shows the voltage stress of switches S_1 and S_5. Similarly, Fig. 17 shows the experimental results of the DO-CSI [17]. Fig. 17(a) shows output currents i_{o1} and i_{o2} with the THD measured to be 4.2% and 4.6%, respectively. Fig. 17(b) shows the output voltages v_1 and v_2. The voltage stress of the switches S_1 and S_7 are shown in Fig. 17(c).

With the proposed inverter, overlap-time intervals can be minimized. Fig. 18 shows the experimental results in the CF mode of the proposed inverter with overlap-time intervals of 0.3 μs. Fig. 18(a) shows the input and load current waveforms. As shown, the input has a peak-to-peak ripple of about 3.5 A with the average dc component of 7.5 A. The THD of injected load currents i_{o1} and i_{o2} are 2.4% and 2.6%, which are lower than those of the conventional single-phase DO-CSIs, respectively. Table III shows the amplitude of the harmonics of the output currents of the DO-CSI topologies. Fig. 18(b) depicts the output voltages v_1 and v_2. The voltages of capacitors (v_{C1} and v_{C2}) are presented in Fig. 18(c). The voltage stress of the switches (S_1 and S_4) are shown in Fig. 18(d). Experimental results in the DF mode are also shown in Fig. 19. The input current has the peak-to-peak ripple of about 1.5 A with the average dc component of 7.5 A, as shown in the top of Fig. 19(a). The bottom of Fig. 19(a) shows the load current i_{o2} at the frequency of 120 Hz and the load current i_{o1} at the frequency of 60 Hz. The output voltage v_2 at the frequency of 120 Hz is shown at the top of Fig. 19(b), whereas the bottom of Fig. 19(b) presents the output voltage v_1 at the frequency of 60 Hz. The voltages of capacitors (v_{C1} and v_{C2}) are depicted in Fig. 19(c). Fig. 19(d) indicates the voltage stress of the switches S_1 and S_4. It can be seen that the results

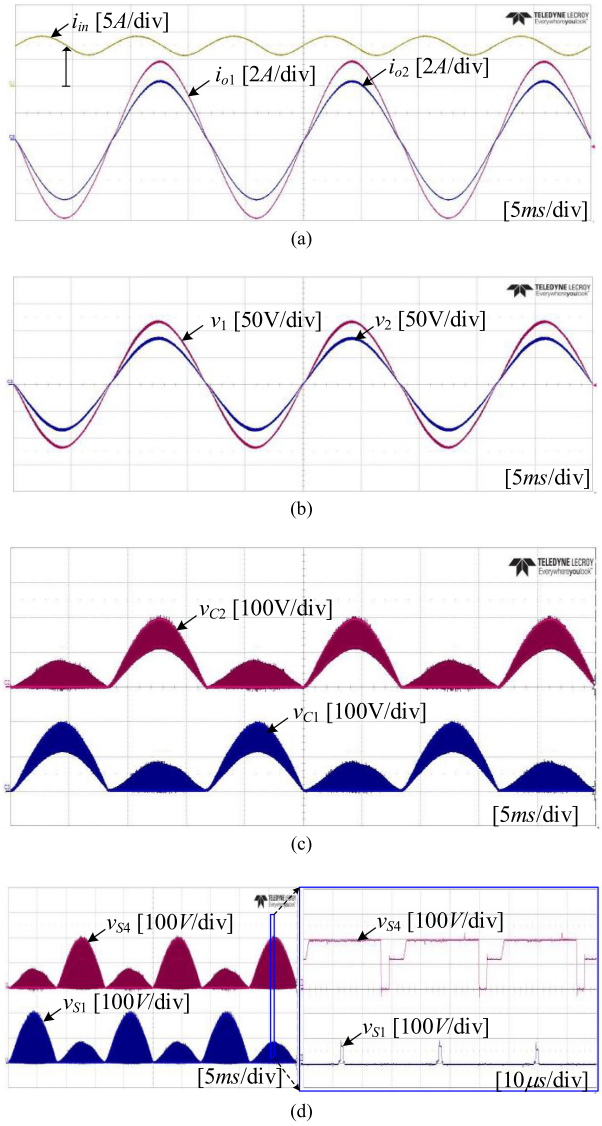

Fig. 18. Experimental waveforms of the proposed inverter in the CF mode with overlap-time of 0.3 μs. (a) Input and load currents. (b) Output voltages. (c) Capacitor voltages. (d) Switch voltages.

TABLE III
AMPLITUDES OF HARMONICS OF THE OUTPUT CURRENT OF THE SINGLE-PHASE DO-CSI TOPOLOGIES

Harmonics (n)	2HB CSIs		DO-CSI [17]		Proposed DO-SC-CSI	
	i_{o1}	i_{o2}	i_{o1}	i_{o2}	i_{o1}	i_{o2}
1	5.78	4.308	5.75	4.302	5.85	4.35
3	0.223	0.181	0.225	0.178	0.144	0.114
5	0.043	0.051	0.048	0.044	0.005	0.005
7	0.061	0.054	0.057	0.047	0.004	0.017
9	0.051	0.035	0.042	0.036	0.001	0.001
11	0.037	0.029	0.032	0.027	0.003	0.009
13	0.027	0.024	0.025	0.022	0.002	0.007
15	0.023	0.015	0.02	0.017	0.006	0.006
17	0.018	0.013	0.016	0.014	0.005	0.005
19	0.014	0.012	0.013	0.011	0.005	0.004
21	0.01	0.009	0.01	0.009	0.004	0.003
23	0.009	0.007	0.008	0.008	0.003	0.003
THD (%)	4.3	4.7	4.2	4.6	2.4	2.6

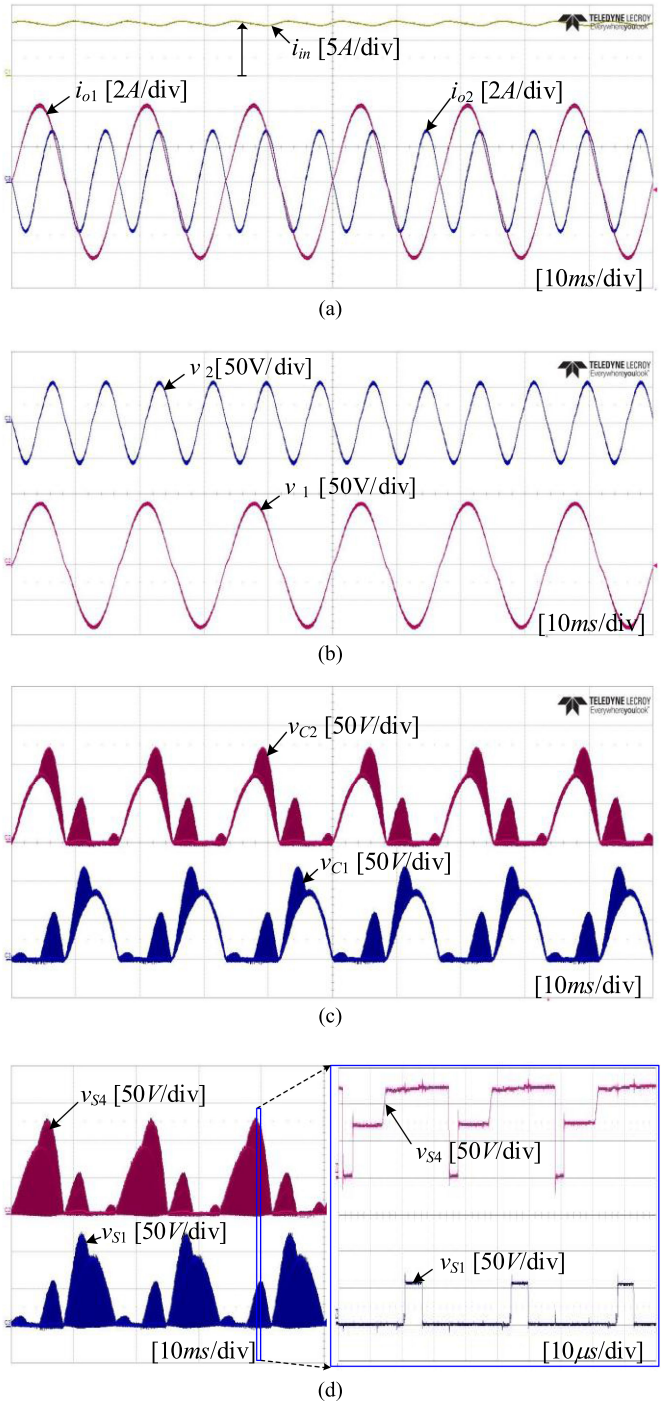

Fig. 19. Experimental waveforms of the proposed inverter in the DF mode with overlap-time of 0.3 μs. (a) Input and load currents. (b) Output voltages. (c) Capacitor voltages. (d) Switch voltages.

shown in Figs. 18 and 19 are similar to the ones presented in Fig. 12(a)and (b), respectively.

As shown in Figs. 18(d) and 19(d), because SC capacitors (C_1 and C_2) in the proposed inverter perform a role in reducing *dv/dt* of high-speed switching switches, the voltage spikes of the switch are reduced when compared with those of the conventional DO-CSIs shown in Figs. 16(c) and 17(c).

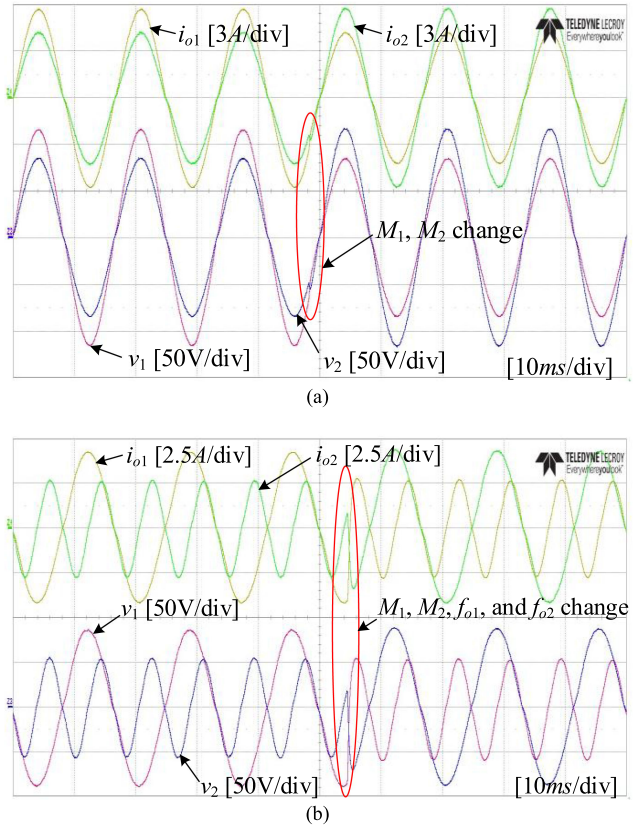

Fig. 20. Experimental waveforms of the proposed inverter. (a) Modulation indices variation. (b) Both modulation indices and frequencies variation.

TABLE IV
COMPARISON AMONG SINGLE-PHASE DO-CSI TOPOLOGIES

Parameter	2 separate CSIs	2HB CSIs	DO-CSI [17]	Proposed DO-SC-CSI
No. of switches	8	8	8	6
No. of conducting switches	4	4	3	2
Reliability	Low	Low	Low	High
Efficiency (%)	86.1	86.4	89.2	92.5
Overlap-time in gate signals	Large	Large	Large	Can be minimized or eliminated

Fig. 20(a) shows the output waveforms when modulation indices (M_1 and M_2) are changed. Where $i_{o1.\mathrm{ref}}$ and $i_{o2.\mathrm{ref}}$ start with $M_1 = 0.8$ at 60 Hz and $M_2 = 0.6$ at 60 Hz, respectively. Then, the $i_{o1.\mathrm{ref}}$ and $i_{o2.\mathrm{ref}}$ change to $M_1 = 0.6$ and $M_2 = 0.8$, respectively. Fig. 20(b) shows the output waveforms when both modulation indices and frequencies are changed. Where $i_{o1.\mathrm{ref}}$ and $i_{o2.\mathrm{ref}}$ start with $M_1 = 0.6$ at 60 Hz and $M_2 = 0.4$ at 120 Hz, respectively. Then, $i_{o1.\mathrm{ref}}$ and $i_{o2.\mathrm{ref}}$ change to $M_1 = 0.4$ at 120 Hz and $M_2 = 0.6$ at 60 Hz, respectively. The efficiency comparison of the topologies is plotted for different values of output power, as shown in Fig. 21. Table IV shows a brief comparison among the single-phase DO-SC-CSI and other single-phase DO-CSI topologies.

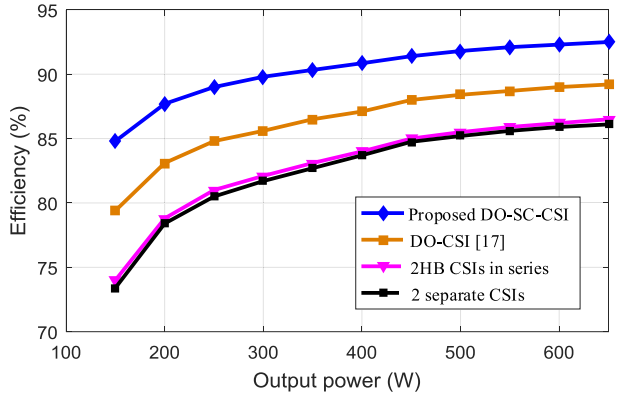

Fig. 21. Efficiency comparison.

V. CONCLUSION

This article proposes a novel highly reliable single-phase DO-CSI using SC structure. With sharing the middle phase leg, the proposed topology has less semiconductor count and conduction loss compared with the conventional single-phase DO-CSIs. The SC capacitors (C_1 and C_2) in the proposed inverter can help to reduce *dv/dt* of power switches and clamp the overshoot voltage under open-circuit faults. Additionally, the overlap-time of gate signals in the proposed DO-SC-CSI can be minimized or eliminated. Thus, the THD of the output current is reduced. The proposed inverter can be used in many applications, such as two-phase open-end winding induction motor drive, smart microgrid applications, photovoltaic grid-connected systems, etc. Both the simulation and experiment results were in good agreement with theoretical analyses.

REFERENCES

[1] B. Sahan, A. Vergara, N. Henze, A. Engler, and P. Zacharias, "A single stage PV module integrated converter based on a low-power current-source inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2602–2609, Jul. 2008.
[2] Y. K. Wu, J. H. Lin, and H. J. Lin, "Standards and guidelines for grid-connected photovoltaic generation systems: A review and comparison," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3205–3216, Jul./Aug. 2017.
[3] H. Komurcugil, "Steady-state analysis and passivity-based control of single-phase PWM current-source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1026–1030, Mar. 2010.
[4] Y. Ohnuma, K. Orikawa, and J.-i. Itoh, "A single-phase current-source PV inverter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 531–538, Jan./Feb. 2015.
[5] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Correa, "Low-frequency power decoupling in single-phase applications: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.
[6] Q. Guo, H. Liu, D. Peng, Q. Liu, and Y. Zhang, "A multi-loop control strategy and parameter design for current-source PWM rectifiers," *Proc. Chin. Soc. Elect. Eng.*, vol. 35, no. 5, pp. 1193–1202, Mar. 2015.
[7] R. T. H. Li, H. S.-H. Chung, and T. K. M. Chan, "An active modulation technique for single-phase grid-connected CSI," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1373–1382, Jul. 2007.
[8] B. S. Prasad, S. Jain, and V. Agarwal, "Universal single-stage grid-connected inverter," *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 128–137, Mar. 2008.

[9] X. T. Peng, S. J. Cheng, S. R. Wang, and Y. J. Tang, "A novel PWM control for current source converter and its application in a superconducting magnetic energy storage unit," *Proc. Chin. Soc. Elect. Eng.*, vol. 26, no. 22, pp. 60–66, Nov. 2006.
[10] Z. Wang, L. Jiang, Z. Zou, and M. Cheng, "Operation of SMES for the current source inverter fed distributed power system under islanding mode," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013, Art. no. 5700404.
[11] S. Kjaer, J. Pedersen, and F. Blaabjerg, "A review of single-phase grid connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
[12] M. Rajeev and V. Agarwal, "Single phase current source inverter with multiloop control for transformerless grid–PV interface," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2416–2424, May/Jun. 2018.
[13] C. R. Baier *et al.*, "Analysis and design of a control strategy for tracking sinusoidal references in single-phase grid-connected current-source inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 819–832, Jan. 2018.
[14] N. S. Ahmad, T. Tsai, and Y. Chen, "Single-phase grid-connected inverters with simplified SPWM control," *IEEE Open J. Power Electron.*, vol. 1, pp. 170–179, May 2020.
[15] H. Wu, Y. Liu, and Z. Wang, "Implementation of a new high-power current-source single-stage PV grid-connected system with reactive power compensation," *IET Renewable Power Gener.*, vol. 13, no. 11, pp. 1873–1881, 2019.
[16] L. A. Costa, M. A. Vitorino, M. B. R. Correa, F. A. C. Bahia, and F. Blaabjerg, "Two-phase x-type current source rectifier with reduced active switch count for open-end permanent-magnet synchronous generator," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 2446–2453.
[17] M. Vitorino, M. Correa, L. Costa, L. Hartmann, and D. Fernandes, "Double four-quadrants single-phase current source converter sharing the same dc-bus," in *Proc. Energy Convers. Congr. Expo.*, Sep. 2014, pp. 2801–2808.
[18] H. Qin, X. Zhang, Z. Zhu, C. Ma, and H. Xu, "Influence of overlap-time on the ac grid-side current of current source PWM rectifier and restraining method," *Trans. Chin. Electrotech. Soc.*, vol. 31, no. 12, pp. 142–152, Jul. 2016.
[19] Y. Geng, R. Deng, W. Dong, K. Wang, H. Liu, and X. Wu, "An overlap-time compensation method for current-source space-vector PWM inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3192–3203, Apr. 2018.
[20] W. Suroso and T. Noguchi, "Overlap-time compensation technique for current-source power inverter," *IET Power Electron.*, vol. 13, no. 4, pp. 854–862, 2020.
[21] E. Lorenzani, F. Immovilli, C. Iianchini, and A. Bianchini, "Performance analysis of a modified current source inverter for photovoltaic microinverter applications," in *Proc. 39th Ann. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 1809–1814.
[22] F. Z. Peng, L. M. Tolbert, and F. H. Khan, "Power electronics' circuit topology-the basic switching cells," in *Proc. IEEE Power Electron. Educ. Workshop*, Jun. 2005, pp. 52–57.
[23] L. M. Tolbert, F. Z. Peng, F. H. Khan, and S. Li, "Switching cells and their implications and applications in power electronic circuits," in *Proc. IEEE Power Electron. Educ. Workshop*, Jun. 2005, pp. 52–57.
[24] L. A. L. d. A. C. Costa, M. A. Vitorino, E. R. Braga-Filho, M. B. R. Corrêa, and D. A. Fernandes, "Two-phase open-end winding induction motor drive using improved current source inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1304–1210.
[25] K. Senthilnathan and I. Annapoorani, "Multi-port current source inverter for smart microgrid applications: A cyber physical paradigm," *Electronics*, vol. 8, no. 1, 2019, Art. no. 1.
[26] G. Dusan, P. Macro, and K. Andreas, "MOSFET power losses calculation using the datasheet parameters," Infineon, Neubiberg, Germany, Appl. Note V1.1, Jul. 2006.
[27] L. A. Costa, M. A. Vitorino, and M. B. R. Correa, "Improved single-phase AC–DC–AC current source converter with reduced DC-link oscillation," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2506–2516, May/Jun. 2018.
[28] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

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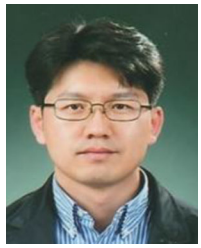

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