High-Efficiency Multilevel Multimode Dynamic Supply Switching Modulator for LTE Power Amplifier

Sungjae Oh, Hansik Oh, Jongseok Bae, *Student Member, IEEE*, Jaekyung Shin, Keum Cheol Hwang, *Senior Member, IEEE*, Kang-Yoon Lee, *Senior Member, IEEE*, and Youngoo Yang, *Senior Member, IEEE*

***Abstract*—A high efficiency multilevel multimode (MLMM) dynamic supply switching (DSS) modulator using a single-inductor multiple-output (SIMO) dc–dc converter is presented to improve the efficiency of power amplifiers (PAs) for a 900 MHz band. The efficiency improvements from the DSS PA were analyzed according to the number of switching levels using the probability density function of the modulation signal. Based on the analysis results, the proposed DSS modulator was configured to give four optimal switching levels in relation to efficiency improvement of the overall DSS PA, efficiency of the modulator itself, and circuit complexity. The SIMO dc–dc converter, which newly adopts a duty skip method, was designed to generate multiple dc voltages. In addition, the four voltage levels were reconfigured according to the average output power to further improve the efficiency of the PA through a wide output power range. The proposed MLMM DSS PA was fabricated using a 0.18 μm CMOS process. For 16-quadrature amplitude modulation long-term evolution (LTE) signals, the proposed MLMM DSS modulator exhibited an efficiency of no less than 80% in the supply power range of 0.1–1 W. Using LTE signal with 10 MHz and peak to average power ratio of 7.58 dB, the MLMM DSS PA showed power added efficiency (PAE) of 41.7% at an average power of 25 dBm with an adjacent channel leakage ratio (ACLR) of −30 dBc.**

***Index Terms*—CMOS power amplifier (PA), dynamic supply switching (DSS), multilevel, multimode, single-inductor multiple-output (SIMO) dc–dc converter, supply modulator.**

I. Introduction

FOR the current mobile handsets, battery time is one of the very important parts to determine user convenience. Since power amplifiers (PAs) in mobile devices consume the largest amount of power in the transmitter, design for high efficiency characteristics in mobile devices is strongly necessary. However, due to the increasing demand for higher data rates, the signal bandwidth and peak to average power ratio (PAPR) of modulated signals have been increased. The efficiency of PAs can be significantly decreased due to the large output power back-off (OPBO or OBO) in order to comply with stringent linearity specification for modulated signals with high PAPR. In order to improve the low efficiency for the large OBO, supply modulation techniques, such as envelope tracking (ET), average power tracking (APT), and dynamic supply switching (DSS), have been introduced [1]–[29].

The efficiency of conventional supply modulators can be further decreased for large OBO at average power levels due to the increased gap between the dc input and output voltage levels. For the ET supply modulator, efficiency degradation arises mainly from the linear amplifier. In order to mitigate this decrease in efficiency of the linear amplifier, adaptive supply of the appropriate dc voltage to the linear amplifier according to the average output power was proposed in [14]. However, an additional dc–dc converter was required to generate the dc voltage for the linear amplifier, which resulted in increased circuit size and complexity. A dual-mode technique was proposed to increase efficiency at low power levels by applying APT [15], [16]. The dc–dc converter for the APT mode was realized using a switching amplifier of the ET supply modulator with an optimized switch size and additional inductor [15]. An additional buck–boost dc–dc converter for the switching and linear amplifiers was adopted for APT mode at large OBO levels [16]. In order to improve the efficiency of the ET supply modulator, a switching amplifier based on three-level buck converter was proposed [11], [21], [26]. However, the modulators did not maintain high efficiency even at low output power levels. Though these methods are helpful in improving the efficiency of the modulator at large OBO levels, significantly increased circuit size and complexity are inevitable.

The efficiency of the PAs can be improved using a DSS modulator by switching the multilevel supply voltages according to the envelope [17]. The DSS modulator consists of one or multiple dc–dc converters and switching circuit. Since the dc–dc converters and switching circuit have relatively low power consumption compared to the linear amplifier of the ET supply modulator, the DSS modulator has a higher efficiency especially under large OBO conditions than the ET modulator experiences. The relatively low potential for efficiency improvements of the

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The authors are with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea (e-mail: dhtjdwowo@gmail.com; 5hansike@gmail.com; baeyas0@gmail.com; shaq2442@skku.edu; khwang@skku.edu; klee@skku.edu; yang09@skku.edu).

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DSS method can be mitigated by the higher efficiency of the DSS modulator compared to the ET supply modulator. In [18], a DSS modulator with a single-inductor dual-output (SIDO) dc–dc converter was introduced. The converter generates two dc voltages which are gradually reduced as the average power level decreases. Even though switching two voltage levels potentially makes the circuit simple and efficient, the amount of efficiency improvement becomes limited.

In this article, a CMOS multilevel multimode (MLMM) DSS modulator integrated circuit (IC) using a single-inductor multiple-output (SIMO) dc–dc converter is proposed. Compared to the conventional DSS modulators that require two dc–dc converters with two external inductors to generate two dc voltage levels [17], the proposed MLMM DSS modulator can have higher efficiency especially for large OBO conditions and can have a very simple structure by employing a SIMO dc–dc converter which generates multilevel voltages for dynamic switching only with a single external inductor.

It is important to determine the number of voltage levels for the multilevel DSS modulator. Through the use of the probability density function (PDF) of the modulated signal and simulated loss of the switching circuit which is a dominant factor for the efficiency of the modulator, the overall efficiency was analyzed according to the number of voltage levels for the ideal class-B PA. Considering the results of this analysis and circuit complexity of the DSS modulator, an optimal number of four voltage levels was determined for this article.

In addition, the proposed four-level DSS modulator has four operation modes according to the average output power levels so as to further improve the efficiency at a large OBO condition for the average output power. At a high output power level, full four-level voltages should be used for DSS operation to maximally improve the efficiency. As the output power decreases, the efficiency of the DSS modulator becomes degraded due to the static power consumption of the modulator. To reduce the static power consumption, the number of voltage levels can be gradually reduced from four levels to two levels according to the average output power level. This is to ensure that the efficiency degradation of the modulator can be mitigated. For a very low output power level, the modulator can just have a one-level operation that is the same as an APT mode.

Different from the conventional dc–dc converters, the load regulation characteristics becomes more important because the load condition of each output voltage of the SIMO dc–dc converter in the DSS modulator can be abruptly changed due to the switching of the output voltage levels according to the envelope. This abrupt change in the load condition makes it difficult to constantly maintain the output voltages of the converter. In this article, a duty skip method is proposed for the SIMO dc–dc converter to maintain the output voltage levels at a constant level, even for abruptly changing load conditions. Using the duty skip method, an undesired voltage overshoot due to abruptly changed load can be avoided by instantly suppressing the current through the inductor.

The proposed MLMM DSS modulator IC was designed and fabricated using a 0.18-μm CMOS process. The fabricated modulator IC was verified experimentally using an uplink long-term evolution (LTE) signal with a signal bandwidth of 10 MHz in conjunction with a CMOS differential PAIC designed for the 900-MHz band through the same process. The experimental results are summarized and compared to previously published state-of-the-art devices.

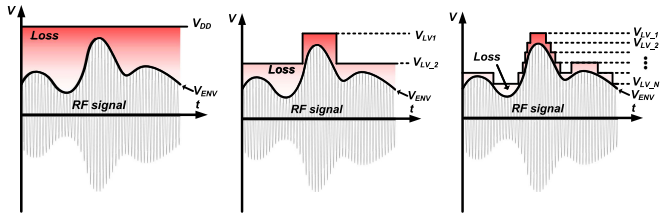


Fig. 1. Waveforms for the DSS method. (a) Fixed V_{DD}. (b) Conventional two-level DSS. (c) Proposed multilevel DSS.

II. Multilevel Multimode DSS Modulator

A. Multilevel Operation

Fig. 1 shows the waveforms of the PA for the modulated signal to explain the operation of the DSS method. Fig. 1(a) shows a conventional PA with a fixed supply voltage. The gap between the envelope signal and fixed V_{DD} results in power loss that can increase as the PAPR of the modulated signal increases. In some previous studies [17]–[19], a two-level DSS was proposed to reduce power loss by switching between two constant voltages according to the envelope, as shown in Fig. 1(b). Fig. 1(c) shows the waveforms of the proposed multilevel DSS method which can further improve the efficiency by switching between multiple constant voltages. As the number of available voltage levels increases, greater efficiency improvements become available in ideal conditions. However, there are some practical issues; various factors such as the efficiency of the switches and circuit complexity should be considered to determine an appropriate number of voltage levels.

The efficiency of the DSS PA was analyzed using an ideal class-B PA and the PDF of the modulated signal. Since the PA has a matched load, the peak fundamental current and voltage to the load can be expressed according to the envelope signal as follows:

$$I_{\text{fund}}(\nu) = \nu \cdot I_{\max} \tag{1}$$

$$V_{\text{fund}}(\nu) = \nu \cdot V_{\max} \tag{2}$$

where ν is the normalized envelope voltage going from 0 to 1. $I_{\max}$ and $V_{\max}$ are the magnitudes of the fundamental current and voltage, respectively, for the peak envelope level. When PA is supplied by constant voltage for the modulation signal, the supply current of the PA changes according to the magnitude of the modulation signal's envelope input to the PA, while the supply voltage is a constant value. As a result, the supply current can also be expressed according to the envelope signal as

$$I_{\text{supply}}(\nu) = \nu \cdot \frac{2I_{\max}}{\pi}. \tag{3}$$

By using (1) and (2), the peak output power for the fundamental signal of the DSS PA can be calculated as a function of

the envelope as

$$P_{\text{fund}}(\nu) = \frac{V_{\text{fund}}(\nu) \cdot I_{\text{fund}}(\nu)}{2} = \frac{\nu^2 V_{\max} I_{\max}}{2}. \quad (4)$$

For N voltage levels of the DSS PA, the i-th discrete supply voltage ($V_{LV,i}$) to the PA can be expressed as

$$V_{LV,i} = V_{th,i} \cdot V_{dc} \text{ for } V_{th,i+1} < \nu < V_{th,i} \quad (5)$$

where i is an integer from 1 to N and $V_{th,i}$ is the threshold voltage which is no larger than 1 (or $V_{th,1}$). $V_{LV,i}$ should be selected according to the preselected threshold levels and the instantaneous envelope voltage. One of the $V_{LV,i}$'s should be dynamically supplied to the PA. Through use of (3) and (5), the supplied power of the N-level DSS PA can be derived as

$$P_{\text{supply},i}(\nu) = V_{LV,i} \cdot I_{\text{supply}}(\nu) = V_{LV,i} \cdot \nu \cdot \frac{2I_{\max}}{\pi}. \quad (6)$$

Considering (4) and the PDF of the envelope signal, the average output power of the fundamental signal for the DSS PA using the modulated signal is given by

$$P_{\text{fund}}, \text{avg} = \int_0^1 p(\nu) \cdot P_{\text{fund}}(\nu) d\nu \quad (7)$$

where $p(\nu)$ is the PDF of the envelope signal. The DC power consumption can be calculated as the average supplied power of the N-level DSS PA for the modulated signal as follows.

$$\begin{aligned} P_{dc} = P_{\text{supply}}, \text{avg} = & \int_{V_{th,2}}^{V_{th,1}} p(\nu) \cdot P_{\text{supply},1}(\nu) d\nu \\ & + \int_{V_{th,3}}^{V_{th,2}} p(\nu) \cdot P_{\text{supply},2}(\nu) d\nu \\ & + \cdots + \int_0^{V_{th,N}} p(\nu) \cdot P_{\text{supply},N}(\nu) d\nu. \end{aligned} \quad (8)$$

Using (7) and (8), the efficiency of the N-level DSS PA based on the ideal class-B PA using the number of supply voltage levels and threshold voltages can be derived as in (9), shown at the bottom of this page.

Fig. 2(a) shows the PDF of the envelope signal for the uplink LTE signal with a signal bandwidth of 10 MHz and PAPR of 7.58 dB. Fig. 2(b) shows the maximum efficiency of the N-level DSS PA using the ideal class-B PA according to the number of supply voltage levels. The maximum efficiency was calculated using (9) and the PDF shown in Fig. 2(a) for various numbers of supply voltage levels. Threshold voltages of (9) for each number of voltage levels were optimized using MATLAB to have the maximum efficiency. The calculated efficiency gradually increased as the number of levels increased. It showed an efficiency of 78.5%, a peak efficiency of the ideal class-B PA, with an infinite number of voltage levels for the modulated signal.

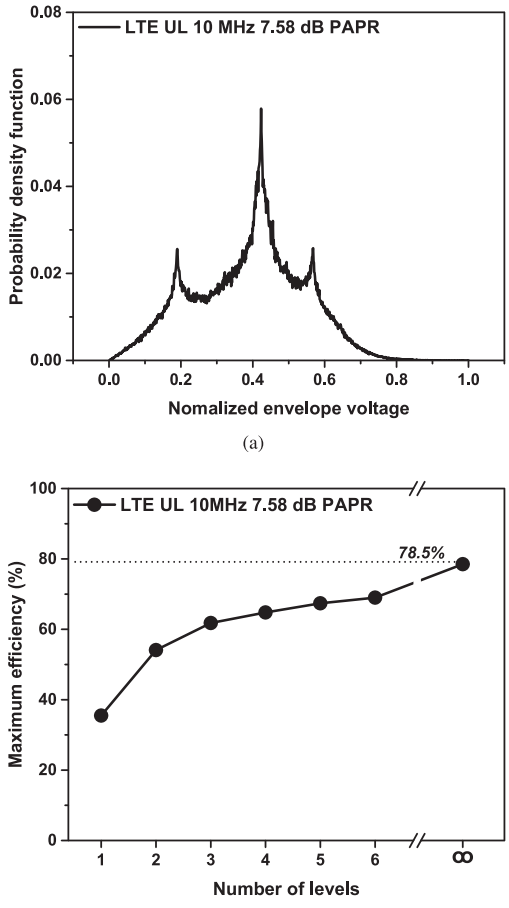


Fig. 2. (a) PDFs of the envelope signals. (b) Maximum efficiency of the N-level DSS PA using an ideal class-B PA according to the number of supply voltage levels.

However, as the number of the supply voltage levels increases, the efficiency of the supply modulator decreases due to the switching loss of the supply switch. Also, this occurs along with an increase circuit complexity. The overall efficiency considering the efficiency of the DSS modulator ($\eta_{\text{DSS,overall}}$) should be revised from (9) to be as

$$\eta_{\text{DSS,overall}} = \eta_{\text{DSS,PA}} \times \eta_{\text{mod}} \quad (10)$$

where η_{mod} is the efficiency of the DSS modulator which becomes $\eta_{\text{dc-dc}} \times \eta_{\text{switch}}$ since the DSS modulator consists of a dc–dc converter and switching circuit.

Table I shows the calculated efficiencies of the N-level DSS PA including the efficiency of the modulator according to the number of levels for the 16-quadrature amplitude modulation (16-QAM) LTE signal with a signal bandwidth of 10 MHz and PAPR of 7.58 dB. Threshold voltages were optimized by iteration to achieve the maximum calculated efficiency. $\eta_{\text{dc-dc}}$

$$\begin{aligned} \eta_{\text{DSS}}, \text{PA} &= \frac{P_{\text{fund}}, \text{avg}}{P_{\text{supply}}, \text{avg}} \\ &= \frac{\int_0^1 p(\nu) \cdot P_{\text{fund}}(\nu) d\nu}{\int_{V_{th,2}}^{V_{th,1}} p(\nu) \cdot P_{\text{supply},1}(\nu) d\nu + \int_{V_{th,3}}^{V_{th,2}} p(\nu) \cdot P_{\text{supply},2}(\nu) d\nu + \cdots + \int_0^{V_{th,N}} p(\nu) \cdot P_{\text{supply},N}(\nu) d\nu} \end{aligned} \quad (9)$$

TABLE I
SIMULATED OVERALL EFFICIENCY OF THE *N*-LEVEL DSS PA ACCORDING TO THE NUMBER OF THE SUPPLY VOLTAGE LEVELS

# of level	Threshold voltages	$\eta_{DSS,PA}$ (%)	η_{DC-DC} (%)	η_{switch} (%)	$\eta_{DSS,overall}$ (%)
1	1	35.5	90	100	32.0
2	1, 0.59	54.1	90	97.5	47.5
3	1, 0.65, 0.47	61.7	90	95.7	53.1
4	1, 0.70, 0.58, 0.45	64.8	90	94.7	55.2
5	1, 0.70, 0.59, 0.47, 0.34	67.4	90	91.6	55.7
6	1, 0.70, 0.60, 0.51, 0.44, 0.32	69.0	90	88.9	55.2

was just assumed to be 90% since the efficiency of the SIMO dc–dc converter is not strongly dependent on the number of output voltages. η_{switch} is the simulated results for the switches that were used in the design using SPICE. p-channel metal-oxide semiconductor (PMOS) switches have a length of 0.3 μm and width of 40 000 μm, while n-channel metal-oxide semiconductor (NMOS) switches have a length of 0.35 μm and width of 35 000 μm. The sizes of the switches were determined to have minimized overall loss (sum of conduction and switching losses) for the output power of 1 W or more. The value of switch gradually decreased as the number of voltage levels increased. The overall efficiency was calculated using (10). A maximum value can be found from the five levels. However, since there was just a small difference (of 0.5%) in efficiency between four and five levels, a four-level DSS modulator seemed to be the best selection to achieve very high efficiency improvement while maintaining relatively low circuit complexity. For these reasons, a four-level DSS modulator was proposed as the best choice.

B. Multimode Operation

The efficiency of the supply modulator can be degraded due to the loss of the circuits. For the DSS modulator, the efficiency was mainly affected by the loss at a switch that supplied one of the dc outputs of the SIMO dc–dc converter to the PA according to the envelope and loss at the switch in the SIMO dc–dc converter. When the output power becomes low, the efficiency improvements of the PA can be reduced due to the degraded efficiency of the modulator. Therefore, there is a need for a method that can maintain efficiency at the low power levels. Fig. 3(a) shows the switches of the proposed DSS modulator. SW_P, SW_N, $\text{SW}_{\text{LV\_1}}$, ..., and $\text{SW}_{\text{LV\_4}}$ are the switches of the SIMO dc–dc converter, while SW_{DSS1}, ..., SW_{DSS4} are switches of the switching circuit.

The efficiency of the DSS modulator can be directly improved by reducing the losses of the switches in the SIMO dc–dc converter and switching circuit. There is a proposal for a method that can be used to reduce the switch operation so as to avoid excessive increases of the loss as the output power is decreased. Along with the average power of the PA, the switches operate according to the modes, as illustrated in Fig. 3(a). Fig. 3(b) shows the expected efficiencies according to the output power level for the four different operation modes: four-level DSS, three-level DSS, two-level DSS, and APT (one-level). By changing the mode of the DSS modulator according to the output power level, high efficiency is expected to be maintained over a wide output power range as shown in Fig. 3(b).

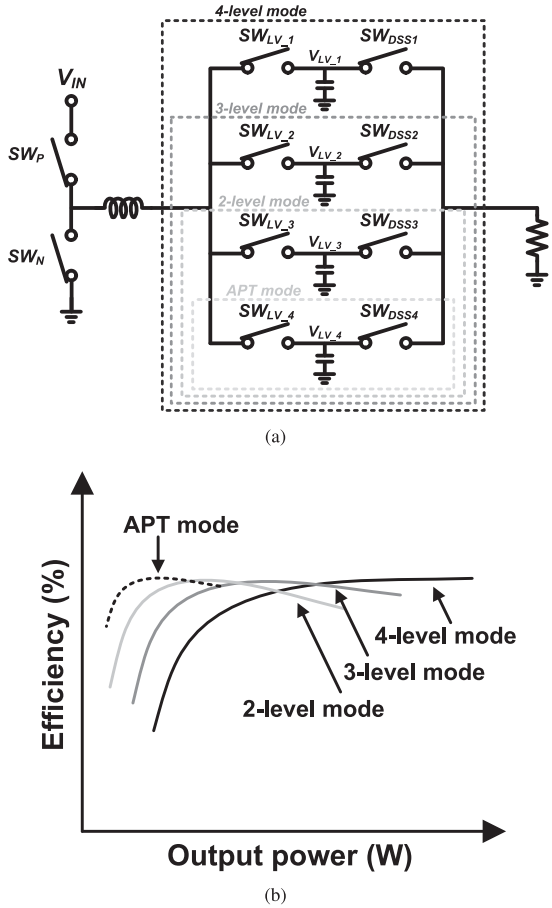


Fig. 3. (a) Switch configurations for the different modes of the proposed DSS modulator. (b) Expected efficiencies for the different modes.

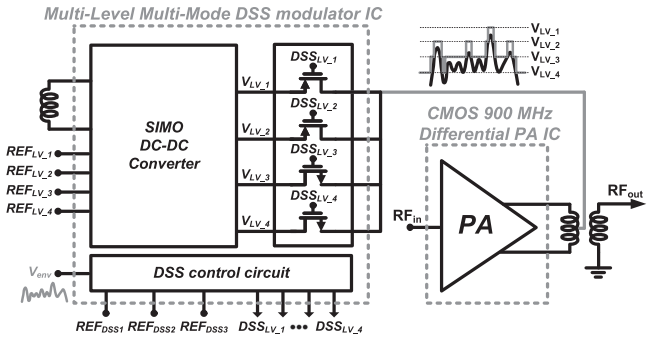


Fig. 4. Block diagram of the MLMM DSS PA.

III. CIRCUIT DESIGN

Fig. 4. shows a block diagram of the proposed MLMM DSS PA. The MLMM DSS modulator IC consists of a SIMO dc–dc converter, DSS control circuits, and DSS switches. The MLMM DSS modulator IC switches multilevel voltages according to the envelope signal and dynamically supplies one of them to the 900-MHz CMOS differential PA. In addition, efficiency can

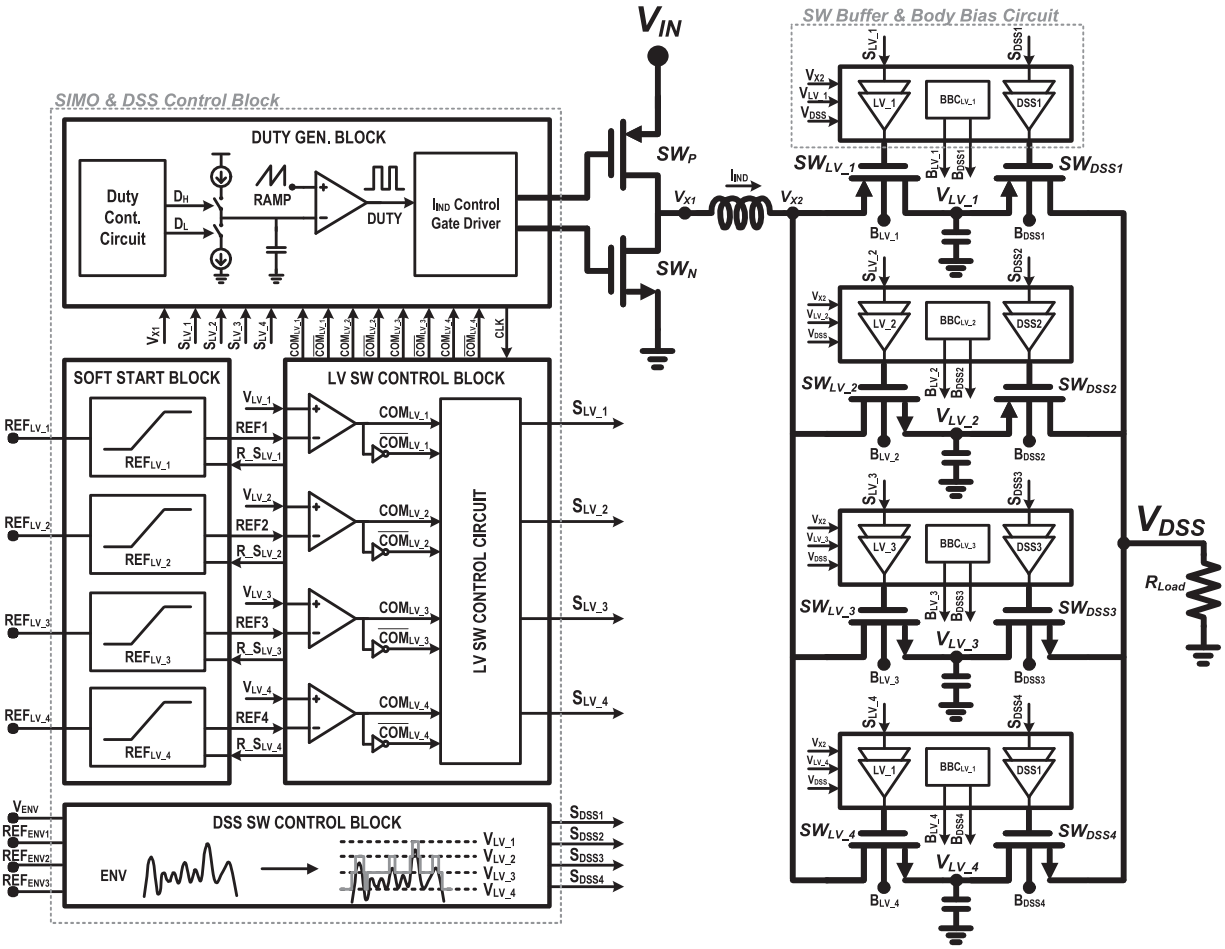


Fig. 5. Top-level architecture of MLMM DSS modulator.

be improved over a wide power range by changing the modes according to the average power. The output matching network of the differential PA consists of an external balun. The output voltage of the DSS modulator IC is supplied through the center-tap of the balun.

A. MLMM DSS Modulator

Fig. 5 shows the top-level architecture of the MLMM DSS modulator. The control block of the modulator consists of a duty generation, level switch control, soft start, and DSS switch control block. The duty generation block receives $S_{\mathrm{LV\_}N}$ and $\mathrm{COM_{LV\_}}_N$ signals, which are generated from the level switch control block. Moreover, it adjusts the inductor current so that $V_{\mathrm{LV\_}N}$'s can be kept constant. The LV switch control block receives $V_{\mathrm{LV\_}N}$ and REFN signals. It then generates $S_{\mathrm{LV\_}N}$ for the output which is a signal that controls the switches ($\mathrm{SW_{LV\_}}_N$) of the SIMO dc–dc converter. $S_{\mathrm{LV\_}N}$'s are used to charge the capacitors for constant $V_{\mathrm{LV\_}N}$'s. The DSS switch control block receives V_{ENV} and $\mathrm{REF_{ENV}}N$ signals. It generates S_{DSSN} as an output signal, which is a signal that controls DSS switches ($\mathrm{SW_{DSSN}}$) and makes the modulator to output V_{DSS}. The switches for high output voltages were designed using PMOS, while the switches for relatively low output voltages were designed using NMOS. The switches for intermediate voltages use both PMOS and NMOS together so as to increase the efficiency of the modulator. The body bias circuit supplies appropriate body biases to reduce the body effect for $\mathrm{SW_{LV\_}}_N$ and $\mathrm{SW_{DSSN}}$.

1) Duty Generation Block for Duty Skipping Operation: Fig. 6 shows a schematic of the duty generation block for the SIMO dc–dc converter. The duty generation block controls the current through an external inductor, I_{IND}. The duty control circuit and gate driver control I_{IND}, the inductor current. The duty control circuit adjusts the duty cycle according to $V_{\mathrm{LV\_}N}$. Fig. 7 shows the timing diagram of the duty control operation. $\mathrm{COM_{LV\_}}_N$ signals are the outputs generated by comparing $V_{\mathrm{LV\_}N}$ and REFN using the comparator. REFN is the reference voltage for $V_{\mathrm{LV\_}N}$. $\mathrm{COM_{LV\_}}_N$ is enabled if there is need for capacitor charging for each $V_{\mathrm{LV\_}N}$. The frequency of the ramp signal was selected to be 0.5 MHz. The duty cycle is increased when the capacitor for $V_{\mathrm{LV\_}N}$ needs to be charged within one cycle or when it is being charged. The duty cycle is decreased when the capacitor for $V_{\mathrm{LV\_}N}$ does not need to be charged within one cycle and when there is no need to increase the duty cycle. Thus, D_{REF} is generated from the charge pump circuit using D_H and D_L. Through this way, the duty cycle can be dynamically controlled.

The difference compared to the conventional SIMO dc–dc converter is that only one of the outputs is connected to the load while the others are disconnected from the load. This switching

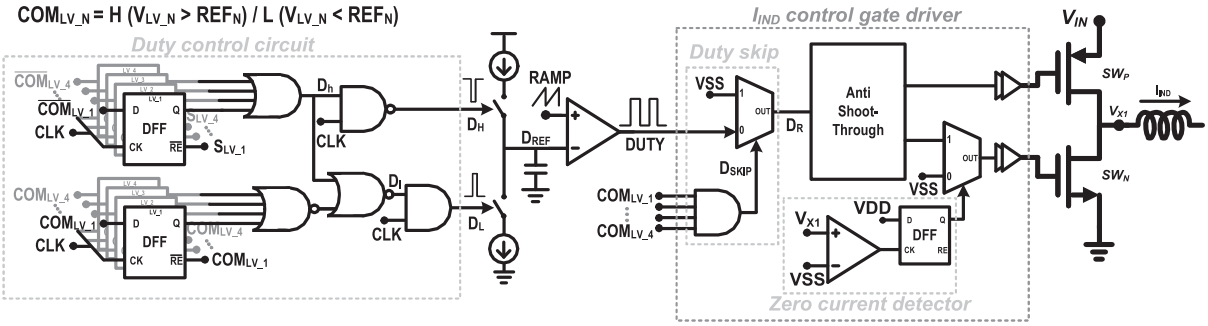


Fig. 6. Schematic of the duty generation block.

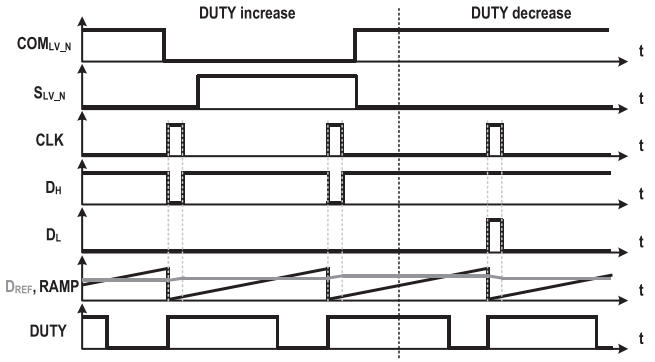


Fig. 7. Timing diagram of duty control operation.

operation causes abrupt change of the load condition for each output voltage level. Due to the abrupt change of the load, the output current to the load through each connected output voltage should be abruptly changed as well according to the envelope signal. This abrupt change of current can cause large current ripples, i.e., load regulation issues. In order to reduce the output ripples from the converter, the inductor current should be immediately controlled. The gate driver, including the duty skip circuit and zero-current detector, operates to immediately control I_{IND} by skipping the duty of the control signal. The duty skip circuit reduces I_{IND} by skipping the duty when all capacitors for the $V_{\mathrm{LV\_}N}$'s dont need charging. Fig. 8 shows the timing diagram for the duty skip operation. The D_{SKIP} signal is generated when all $\mathrm{COM_{LV\_}}_N$ signals are high, which indicates that all the capacitors for the $V_{\mathrm{LV\_}N}$'s do not require to be charged. This means that all the capacitors for the $V_{\mathrm{LV\_}N}$'s dont require charging. As such, the duty is skipped to abruptly suppress the inductor current, I_{IND}. By using the proposed duty skip technique, the ripples of the output voltages can be greatly reduced.

2) LV Switch Control Circuit: Fig. 9 shows the switch control circuit for the output switches of the dc–dc converter. The switch control circuit should run to maintain the levels of the given $V_{\mathrm{LV\_}N}$'s for DSS operation. The order of charging is fixed for the conventional SIMO dc–dc converters. However, the SIMO dc–dc converter in our DSS modulator should have a prioritized charging ability since one of the $V_{\mathrm{LV\_}N}$'s are randomly connected to the load (or the PA) in accordance with the envelope signal. In this random discharging situation, the charging priority must be determined to make all the $V_{\mathrm{LV\_}N}$'s as constant as possible. Low $\mathrm{COM_{LV\_}}_N$, which is the output of the comparator, indicates that the capacitor of the *N*th output voltage ($V_{\mathrm{LV\_}N}$) requires to be charged. Using some logic gates and *D* flip-flops, the LV charging priority control circuit determines the priority of charging according to the sequence of when each $\mathrm{COM_{LV\_}}_N$ gets low. Thus, one the signals, RE1,..., RE4, with the highest priority gets turned ON. The ON signal for the switch ($\mathrm{SW_{ON}}$) is generated through the falling edge signal of $S_{\mathrm{LV\_}N}$ or the clock signal. The output switches of the SIMO dc–dc converter are controlled using the REN signals and $\mathrm{SW_{ON}}$. Through the use of the charging priority control circuit for the output switches of the SIMO dc–dc converter, all $V_{\mathrm{LV\_}N}$'s can be maintained in spite of its random discharging characteristics.

3) Simulation Results: Fig. 10(a) shows the simulation results showing the $V_{\mathrm{LV\_}N}$'s of the proposed DSS modulator and the DSS voltage waveform according to the envelope in Fig. 10(b). The DSS voltage is generated by dynamically switching the $V_{\mathrm{LV\_}N}$'s to the load according to the envelope using the analog-to-digital converter of the control block for the DSS switches.

B. CMOS PA

Fig. 11 shows the schematic of the designed differential CMOS PA for the 900-MHz band. The designed PAIC, with two-stage common source structure, is composed of an input matching network based on an integrated balun and interstage matching network based on a high-pass *LC* network. The output matching network is based on an off-chip balun from the printed circuit board (PCB) so as to have a low loss. The input and output matching networks were designed considering the bond-wire inductance. A cross-coupled capacitor and *RC* feedback network were used to achieve better stability. The second harmonics at the source and drain of the main stage is set up to give improved linearity and efficiency. The second harmonic control circuit at the drain was implemented at the center-tap of the balun.

IV. Experimental Results

Figs. 12 and 13 depict photographs of the fabricated MLMM DSS modulator and CMOS PA. The input voltage of the designed DSS modulator was 3.3 V and the range of the output voltage was from 1.3 to 3.2 V. One off-chip inductor was used for the SIMO dc–dc converter. The chip size of the MLMM DSS modulator was $1.5 \times 1.0\,\mathrm{mm}^2$. The V_{DD} of the PA was 3.3 V. The

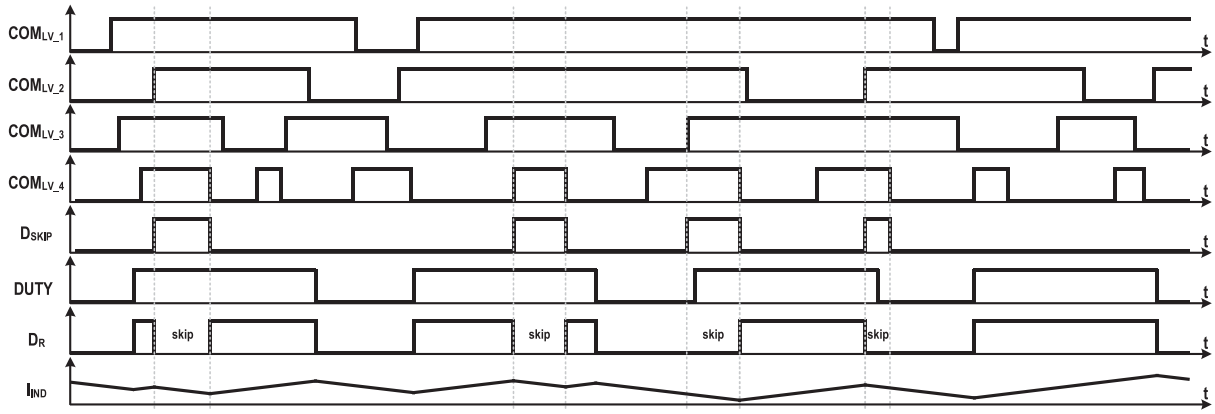


Fig. 8. Timing diagram of the duty skipping operation to control the inductor current.

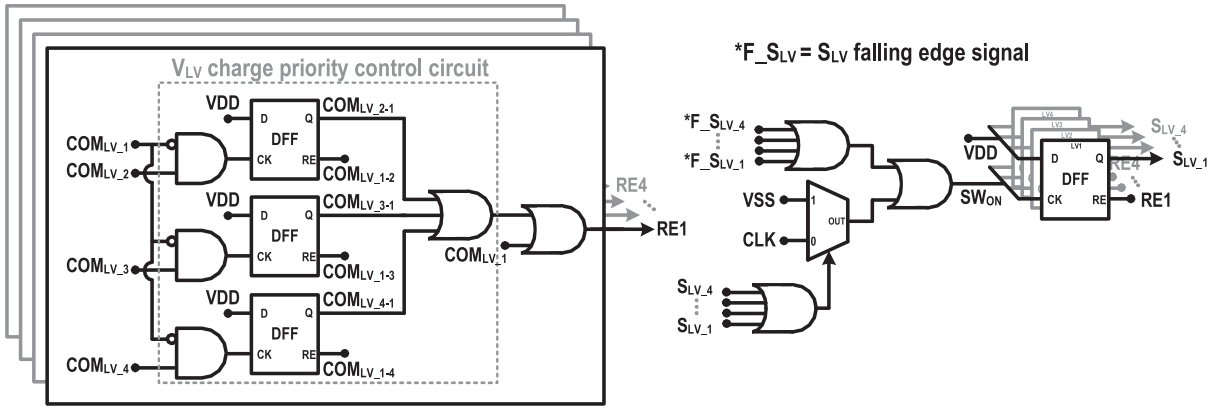


Fig. 9. Schematic of the switch control circuit for the dc–dc output switches.

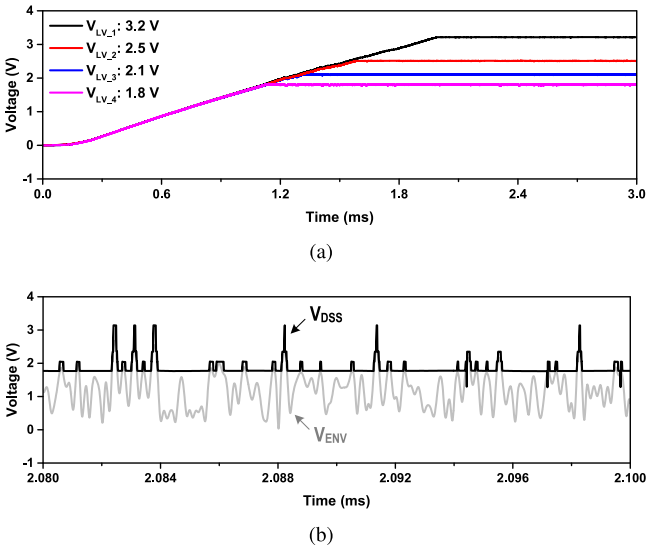


Fig. 10. Simulation results for output voltage. (a) SIMO dc–dc converter. (b) DSS modulator.

output balun was designed using a four-layer FR4 PCB. The DSS voltage was applied to the PA through the center-tap of the balun. The chip size of PAIC was 1.78×0.88 mm^2. The measurement setup includes two synchronized signal generators, E4438 C, to

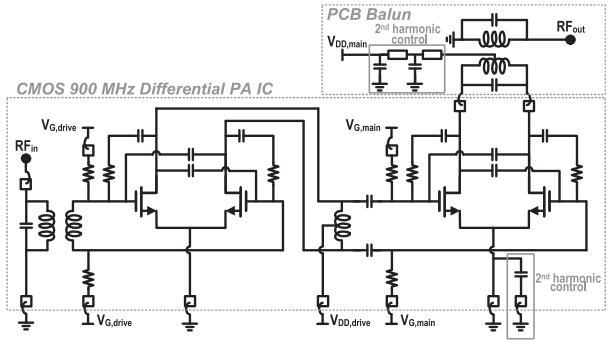
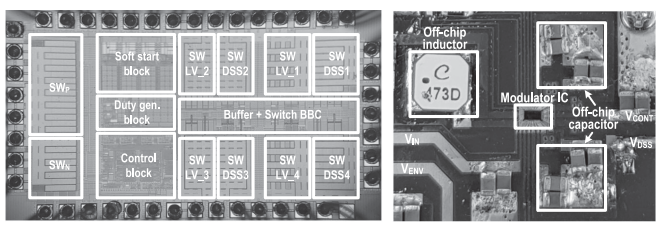


Fig. 11. Schematic of the 900-MHz differential CMOS PA.



(a) (b)

Fig. 12. Photographs of the fabricated MLMM DSS modulator. (a) IC. (b) Evaluation board.

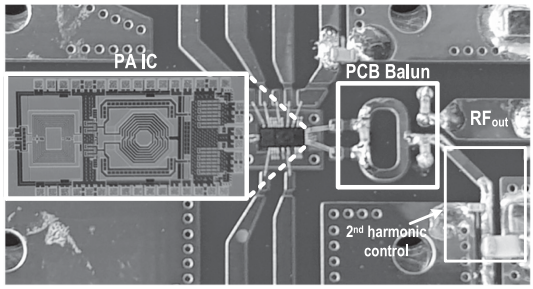


Fig. 13. Photograph of the implemented 900-MHz differential CMOS PA.

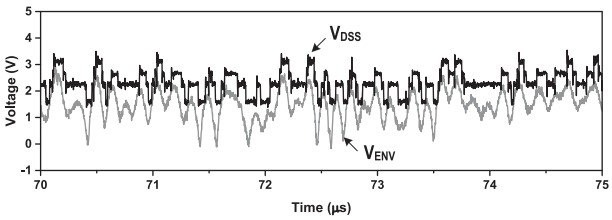


Fig. 14. Measured V_{DSS} waveforms.

generate the envelope and modulated signals. It also includes a high-speed oscilloscope, Wavepro 700, and a spectrum analyzer, E4440 A to analyze the time-domain waveforms and the output RF signal, respectively.

Fig. 14 shows the measured DSS output (V_{DSS}) waveforms according to the envelope signal of the 16-QAM LTE signal with a signal bandwidth of 10 MHz. Fig. 15(a) shows the measured efficiencies of the DSS modulator according to the output power for the LTE signal with a signal bandwidth of 10 MHz. Fig. 15(b) shows the efficiency of the DSS modulator according to the output voltage when operating with the APT mode. The efficiencies for the different modes were measured

In the four-level mode, the modulator had the highest efficiency at a high output power but suffered from efficiency degradation as the output power decreased. However, by selecting the three-level or two-level modes, high efficiency can be maintained even at lower output power levels. The MLMM DSS modulator achieves an efficiency of over 80% using the multimode operation over a wide output power range. The APT mode (or one-level mode) can be selected to further extend the efficiency improvements over the power range even for the very low output powers.

Fig. 16(a)–(c) shows the performances of the MLMM DSS PA using 16-QAM LTE signal with a signal bandwidth of 10 MHz and PAPR of 7.58 dB. For measurements, the efficiency was optimized with the output voltages for each mode of the DSS modulator at each average output power level to maintain an adjacent channel leakage ratio (ACLR) level of better than −30 dBc. Fig. 16(a) shows the measured gain and power added efficiency (PAE) of the stand-alone PA and MLMM DSS PA using the 10-MHz LTE signal. A gain of 23.5 dB and PAE of 41.7% were obtained at an average output power of 25 dBm using the 10-MHz signal. Fig. 16(b) shows the PAE improvements using the MLMM DSS modulator for the different modes. The PAE was improved by 3.4% using the 10-MHz signal at an output power of 25 dBm in the four-level

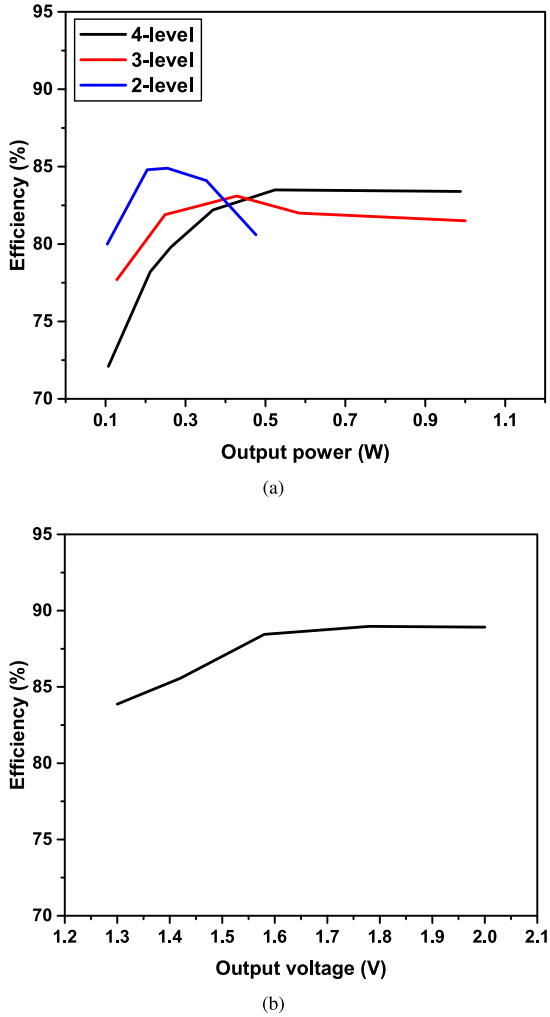
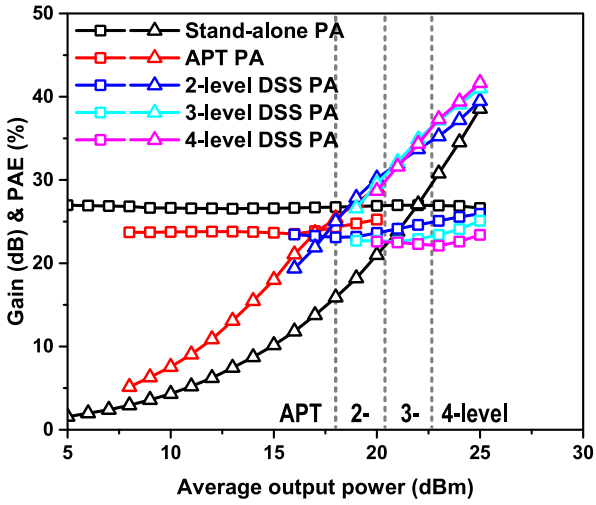


Fig. 15. Measured performances of the MLMM DSS modulator. (a) Efficiencies for the 16-QAM 10-MHz LTE signal. (c) Efficiency for the APT mode.

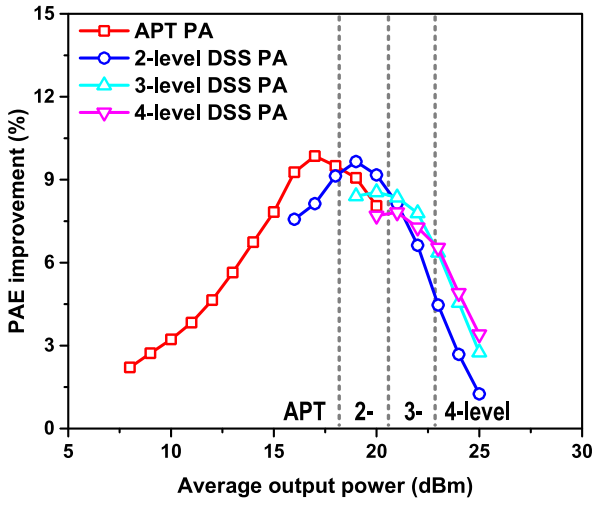
mode. The maximum PAE improvement was 9.9% at an average output power level of 17 dBm in the APT mode for the 10-MHz signal. Fig. 16(c) shows the optimized output voltages for each mode of the DSS modulator according to the average output power to give the maximum PAE improvements. The MLMM DSS PA had a higher efficiency in each mode: Average power in the range of 25–23, 23–21, 21–18, and below 18 dBm in four-level, three-level, two-level, and APT modes.

Fig. 17 shows the measured ACLR and error vector magnitude (EVM) performances of the MLMM DSS PA. An ACLR of −30 dBc and EVM of 5.57% were obtained at an output power of 25 dBm using the 10-MHz signal. Fig. 18 shows the measured signal constellation of the MLMM DSS PA at an average output power of 25 dBm using the 16-QAM LTE signal with a signal bandwidth of 10 MHz.

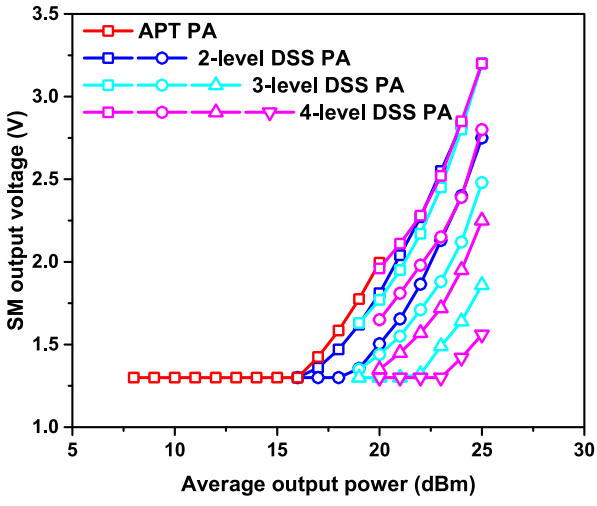
Table II shows the measured performances of the MLMM DSS PA according to the PAPRs of the 16-QAM 10-MHz LTE signal. The PAPRs of the signal were adjusted using the crest factor reduction technique. As shown, a very similar performance was obtained in spite of the broad range of PAPR variation, which went from 9.42 to 5.98 dB. For the ET supply modulator, the efficiency of the ET PA could be degraded for



(a)



(b)



(c)

Fig. 16. Measured performances of the MLMM DSS PA using the 16-QAM 10-MHz LTE signal. (a) Gain and PAE. (b) PAE improvement. (c) Optimized output voltages of the modulator for the modes according to the average output power.

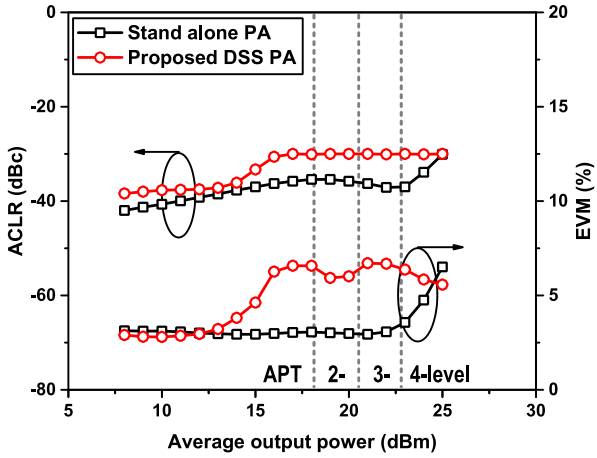


Fig. 17. ACLR and EVM of the MLMM DSS PA.

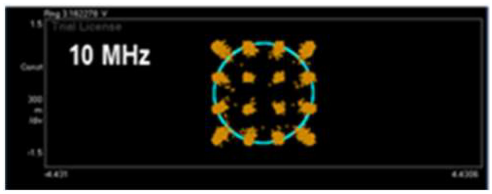


Fig. 18. Measured signal constellation of the MLMM DSS PA using the 10-MHz signal.

TABLE II
MEASURED PERFORMANCES OF THE MLMM DSS PA ACCORDING TO THE PAPRS OF THE SIGNAL

PAPR (dB)	P_{AVG} (dBm)	PAE (%)	PAE improvement (%)	Modulator efficiency (%)	Optimized output voltage (V)
5.95	25	35.5	3.4	83.7	3.20, 2.84, 2.25, 1.60
7.58	25	54.1	3.4	83.5	3.20, 2.80, 2.25, 1.56
9.42	25	61.7	3.5	84.0	3.20, 2.85, 2.20, 1.60

a signal with higher PAPR since the slew rate of the modulator should be increased for a signal with higher PAPR, which could consume more power. However, for the MLMM DSS modulator, since the switching speed cannot be increased, the efficiency could be maintained for signals with higher PAPR, as shown in Table II.

The performances of the proposed MLMM DSS modulator and the MLMM DSS PA are summarized and compared to the previous state-of-the-art devices listed in Table III. Our proposed supply modulator exhibited the highest low-power efficiency of 84.8% at five times lower output power of 0.2 W compared to the high power of 1 W. Though [21] reported the highest efficiency of 91% at a high power of 1 W, the efficiency dropped to merely 68% at a low power condition. It did not present the overall PAE in conjunction with a PA. The MLMM DSS PA in this work showed a very high improved efficiency using a simple circuit based on the SIMO dc–dc converter at the relatively high output power and especially at a low output power level.

TABLE III
PERFORMANCE COMPARISON OF THE PAs USING THE SUPPLY MODULATION TECHNIQUES

Ref.	Signal BW (MHz)	PAPR (dB)	# of off-chip ind.	Modulator high power efficiency (%)	Modulator low power efficiency (%)	Freq. (GHz)	PAE (%)	P_{AVG} (dBm)	ACLR (dBc)	V_{DD} (V)	Technique	Process technology
[6]	40	-	1	85 (1.2 W)	67* (0.5 W)	0.9	41.4**	28.5**	-	3.6	Delay-based hysteresis (ET)	SM: 180 nm CMOS PA: -
[15]	5	7.5	2	73 (0.4 W)	63* (0.1 W)	0.78	45	24.0	-31.1	3.3	Dual switch (ET, APT)	180 nm CMOS
[16]	20	5.8	2	78* (1.0 W)	-	1.747	42.6***	27.0***	-39.0***	4.6	Buck-Boost converter (ET, APT)	SM: 130 nm CMOS PA: InGaP/GaAs HBT
[21]	80	7.84	1	91 (1.0 W)	68 (0.3 W)	2.4	-	24.0	-32.5	2.4	3-level converter (ET)	SM: 130 nm CMOS PA: -
[22]	40	-	1	85 (1.8 W)	79* (0.5 W)	-	-	-	-	3.6	Dual-mode signal-delta (ET)	180 nm CMOS
[9]	5	9.38	1	76.1 (-)	-	2.4	25.3	25.0	-32.1	-	BBTPE (ET)	-
[18]	5	7.5	1	88* (0.5 W)	-	1.75	33.8	22.0	-30.1	3.3	SIDO converter (DSS)	180 nm CMOS
This work	10	7.58	1	83.6 (1.0 W)	84.8 (0.2 W)	0.9	41.7	25.0	-30.0	3.3	SIMO converter (MLMM DSS)	180 nm CMOS

*Graphically estimated.
**Measurement results for signal bandwidth (BW) of 20 MHz.
***Measurement results for signal BW of 10 MHz.

V. CONCLUSION

A MLMM DSS PA that maintains high efficiency over a wide average power range was proposed in this study. The MLMM DSS modulator was designed to deal with four levels of output voltages using a SIMO dc–dc converter. The number of output voltage levels was determined from an analysis with a class-B PA and where the loss of the switches was simulated. The SIMO dc–dc converter had four output voltages with a single inductor and was designed to minimize voltage ripples using the proposed duty skipping technique. In addition, the proposed DSS modulator can maintain high efficiency at a wide power range by changing the operation modes according to the average output power. These modes were four-, three-, and two-level DSS, and APT.

The DSS modulator was applied to a 900-MHz differential CMOS PA with an off-chip balun designed on a PCB and with second-harmonic control circuits for high linearity and efficiency. The designed MLMM DSS modulator exhibited a measured efficiency of more than 80% in the power range of 0.1–1 W. The proposed MLMM DSS PA showed a gain of 23.5 dB, PAE of 41.7%, ACLR of –30 dBc, and EVM of 5.57% at an average power of 25 dBm using a 16-QAM LTE signal with a signal bandwidth of 10 MHz and PAPR of 7.58 dB. In addition, the proposed MLMM DSS PA was proved to achieve almost the same high performances even when using signals with higher PAPR.

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Sungjae Oh was born in Gwangju, Korea, in 1992. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, Korea, in 2015. He is currently working toward the Ph.D. degree at the Department of Electrical and Computer Engineering, Sungkyunkwan University.

His research interests include the design of RF/mm-wave power amplifiers, RF/analog-integrated circuit, efficiency enhancement techniques, linearization techniques, broadband techniques, and mm-wave integration circuits and systems.

Hansik Oh was born in Seoul, Korea, in 1991. He received the B.S. degree in 2016 from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently working toward the Ph.D. degree at the Department of Electrical and Computer Engineering.

His research interests include the design of RF/mm-wave power amplifiers, RF/analog integrated circuit, efficiency enhancement techniques, linearization techniques, broadband techniques, and wireless power transfer system.

Jongseok Bae (Student Member, IEEE) was born in Suwon, Korea, in 1987. He received the B.S. degrees in electronic engineering from Chungnam University, Daejeon, South Korea, in 2014, and the Ph.D. degree from the Department of Electrical and Computer Engineering at Sungkyunkwan University, Suwon, South Korea, in 2020.

Since 2020, he has been with the Department of Electrical and Computer Engineering at Sungkyunkwan University, Suwon, South Korea, where he is currently a Postdoctoral Fellow. His research interests include the design of RF/mm-wave power amplifiers, RF and analog integrated circuits, and microwave power transfer.

Jaekyung Shin was born in Seoul, Korea, in 1993. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Korea Aerospace University, Goyang, South Korea, in 2018. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea.

His current research interests include the design of RF/mm-wave power amplifiers, efficiency-enhancement techniques, broadband techniques, and microwave power transmission.

Keum Cheol Hwang (Senior Member, IEEE) received the B.S. degree in electronics engineering from Pusan National University, Busan, Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2003 and 2006, respectively.

From 2006 to 2008, he was a Senior Research Engineer with the Samsung Thales, Yongin, Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and Cassegrain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, Korea, from 2008 to 2014. In 2015, he joined the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multiband/broadband antennas and radar antennas, and optimization algorithms for electromagnetic applications.

Dr. Hwang is a Life Member of KIEES and a member of IEICE.

Kang-Yoon Lee (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively.

From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, USA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University, Seoul, South Korea, as an Associate Professor. Since 2012, he has been with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently an Associate Professor. His research interests include implementation of power integrated circuits, CMOS RF transceivers, analog integrated circuits, and analog/digital mixed-mode VLSI system design.

Youngoo Yang (Senior Member, IEEE) was born in Hamyang, Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology (Postech), Pohang, Korea, in 2002.

From 2002 to 2005, he was with Skyworks Solutions Inc., Newbury Park, CA, USA, where he designed power amplifiers for various cellular handsets. Since 2005, he has been with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently a Professor. His research interests include RF/mm-wave power amplifiers, RF transmitters, and dc–dc converters.