GaN-Based Tri-Mode Intelligent Solid-State Circuit Breakers for Low-Voltage DC Power Networks

Yuanfeng Zhou, *Student Member, IEEE*, Risha Na, *Member, IEEE*, Yanjun Feng, *Member, IEEE*, and Zheng John Shen, *Fellow, IEEE*

***Abstract*—The purpose of this article is to provide a comprehensive and integrated discussion on the basic concept and general design methodology of a gallium nitride (GaN)-based, tri-mode, intelligent solid-state circuit breaker, referred to as iBreaker. The iBreaker concept explores the use of GaN devices in the low-voltage (<1000 V), mΩ-resistance SSCB designs and new SSCB topology and control techniques beyond the commonly used ON/OFF switch configuration in order to integrate more intelligent functions without increasing component count. The iBreaker adopts a distinct pulsewidth modulation (PWM) current limiting (PWM-CL) state in addition to the conventional ON and OFF states to facilitate soft startup, fault authentication, and fault location functions. Key design elements, such as use of wide bandgap (particularly GaN) switches, tri-mode operation, combined digital and analog control, and universal hardware/software architecture, are discussed in detail. In particular, the bidirectional buck topology, changes among operation states, variable PWM frequency control, fault locating techniques, GaN FET hardware, and thermal design are discussed. Two iBreaker prototypes, rated at 380 V/20 A and 1000 V/10 A, respectively, are built and tested to validate the proposed SSCB design concept. 99.95% transmission efficiency, passive cooling, and μs-scale response time are demonstrated experimentally.**

***Index Terms*—Solid state circuit breaker.**

I. Introduction

LOW-VOLTAGE dc power networks (up to 1000 V) such as dc data centers, PV farms, and EV charging infrastructures are gaining tractions in recent years because of their advantages in efficiency, cost, and power quality over the traditional ac power [1]–[5]. However, protecting these dc power networks from short-circuit faults remains a major technical challenge [6]–[9].

Conventional electromechanical ac circuit breakers offer a very low ON-state resistance. For example, 240 V/20 A rated molded-case circuit breakers typically offer a dc resistance of 3–5 mΩ. However, they must be significantly redesigned or derated for dc applications due to the lack of current zero crossing and the difficulty of extinguishing arcs. With a typically response time of 20–50 ms they are too slow to interrupt fast-rising dc fault currents. Various types of solid-state circuit breakers (SSCBs) have been under intensive research in recent years to address these challenges [9]–[23]. In particular, a recent publication provides a comprehensive review on the SSCBs [24]. An SSCB typically uses power semiconductor devices such as insulated gate bipolar transistors (IGBTs) or IGCTs as the main static switch, which simply switches ON and OFF in response to the current level detected by the SSCB. It typically offers a response time of 1–50 μs, more than 1000 times faster than an electromechanical circuit breaker, and fast enough to protect the network assets (cables, connectors, power converters, etc.) from excessive electrothermal stress. This is important since a dc network generally has a much smaller loop inductance than an ac network to slow down the rise of the fault current. However, the main disadvantage of SSCBs is their high conduction loss and the need to effectively remove the heat generated during normal ON-state operation. Unlike in more sophisticated HVdc or MVdc applications where active cooling (e.g., liquid or fan) on the SSCBs may be acceptable, SSCBs for low-voltage dc power applications (<1000 V) must rely on passive cooling to meet the cost and maintenance-free requirements. It is extremely challenging to limit the ON-state power loss of a silicon-based low-voltage low-current SSCB (e.g., 380 V dc/20 A for loads in 380 V dc data centers or office buildings) to several watts that can be easily dissipated with simple passive cooling.

Wide bandgap (WBG) semiconductor devices such as SiC MOSFET or junction field effect transistor (JFET) offer a much lower on-resistance and conduction power loss than silicon IGBT or MOSFET for a voltage rating over 600 V, and are highly attractive for the SSCB application [12]–[15]. For example, SSCBs using SiC JEFTs [12]–[15] or SiC MOSFETs [16] were reported to demonstrate a response time in the range of 1–10 μs with various fault current interruption capability. While WBG devices are still roughly 4–5 times more expensive than their silicon counterparts, they are expected to follow the classical semiconductor cost reduction learning curve in the future. In particular, GaN HEMT transistors, which are fabricated on low-cost silicon wafers in fully depreciated CMOS fabs stand a real chance of achieving cost parity with silicon in the near future, as indicated by the fact that 100 V-rated

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Yuanfeng Zhou, Risha Na, and Zheng John Shen are with the Illinois Institute of Technology, Chicago, IL 60616-3717 USA (e-mail: yzhou103@hawk.iit.edu; rna@iit.edu; zshen6@iit.edu).

Yanjun Feng was with the Illinois Institute of Technology, Chicago, IL 60616 USA. He is now with Canoo EV. (e-mail: yfeng25@hawk.iit.edu).

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commercial eGaN FETs are already priced comparably to silicon MOSFETs. It is an objective of this article to explore the use of commercial GaN FETs (e.g., 650 V/25 mΩ GS66516T from GaN Systems and 900 V/50 mΩ TP90H050WS from Transphorm) in various SSCB designs that offer mΩ-resistance and passive cooling, following our early work on a 300 V SSCB using a monolithic bidirectional GaN HEMT prototype device [25].

Another objective of this article is to explore new SSCB topology and control techniques beyond the commonly used simple ON/OFF switch configuration in order to integrate intelligent functions without increasing component count. It is a well-known challenge for the common ON/OFF bimode SSCBs to distinguish between a true short-circuit fault current and a load inrush current. The inrush current, often several times of the nominal current, is mostly the initial charging current for the large input capacitor of an electrical load during its startup or plugging-in phase [26]. The inrush current may cause nuisance tripping of circuit breakers or damage the electronic equipment. Conventional electromechanical circuit breakers address this problem by allowing a very high (typically 20×–30× of the nominal current) fault current tripping point as well as a wide current-time profile for overcurrent protection, neither being feasible for effective protection of the new converter-based dc microgrids.

Recently, the authors of this article proposed a tri-mode SSCB design concept that integrates current-limiting soft startup functions with basic fault shutdown functions [30]–[33]. The intelligent SSCB, referred to as *iBreaker*, explicitly identifies and exploits a distinct pulsewidth modulation (PWM) current limiting (PWM-CL) state in addition to conventional ON and OFF states in a bidirectional common-inductor buck topology without needing additional semiconductor power devices. The *iBreaker* can operate in an ON state for continuous conduction of normal load currents or an OFF state to interrupts fault currents. In addition, it can operate in the PWM-CL state with a moderate overcurrent for a short period of time to facilitate intelligent functions such as soft startup, fault authentication, and fault location. The *iBreaker* will switch from the PWM-CL to the OFF state if it deems the overcurrent condition to be a true short-circuit fault rather than a startup scenario after a short-time period. The *iBreaker* concept was first implemented on a 380 V/20 A (nominal) SSCB design using 1200 V SiC MOSFETS [30]–[32] and later on 650 V GaN FETs [33]. Switching-mode buck topologies to replace the simple ON/OFF switch configuration along with a variable frequency PWM control method were investigated to optimize both soft-start and fault protection functions. Furthermore, a new technique to identify the fault location on the connecting cable using the *iBreaker* hardware/software architecture was developed in [31].

While different aspects and design implementations were reported in the past [30]–[33], this article aims at providing a comprehensive and integrated discussion on the basic concept and general design methodology of *iBreaker*. Four key design elements will be discussed in detail: choice of WBG (particularly GaN) switches, tri-mode operation and topology, combined digital and analog control, and universal hardware/software architecture. In particular, the bidirectional common-inductor buck topology, mode changes among the three distinct states, variable PWM frequency control, fault locating techniques, GaN FET hardware, and thermal design will be discussed. Furthermore, experimental results on a new *iBreaker* prototype using stacked 900 V cascode GaN switches (Transphorm TP90H050WS) at a dc voltage of 1000 V is reported for the first time in this article. The remainder of this article is as follows. Section II reviews the general design methodology of *iBreaker* while Section III focuses on the discussion of the bidirectional buck topology. Section IV reviews different aspects of the *iBreaker* control strategy, followed by experimental results in Section V. A conclusion is provided in Section VI.

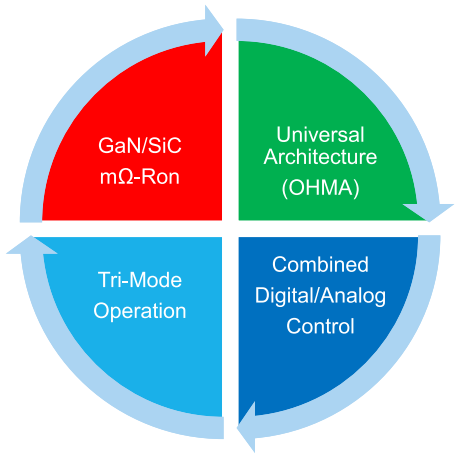


Fig. 1. *iBreaker* design methodology including four key elements: use of WBG switches, tri-mode operation, combined digital and analog control, and universal hardware/software architecture.

II. Design Methodology

The general *iBreaker* design methodology is summarized in this section. Fig. 1 shows four key design elements: use of WBG (particularly GaN) switch for on-resistance in the mΩ range, tri-mode operation for integrating intelligent functions, combined digital and analog control for both speed and flexibility, and universal hardware/software architecture for easy commercialization.

A. Choice of WBG Devices

One major limitation of today's SSCBs is their high on-resistance in comparison to that of mechanical circuit breakers (e.g., a few hundreds of mΩ of SSCB versus a few mΩ of molded-case CBs for the rating of 380 V/20 A). Even if the SSCB conduction loss is insignificant (e.g., <0.5%) comparing to the total transmitted power, self-heating of the SSCB due to the conduction loss can be a serious concern since maintenance-free passive cooling is highly preferred in low-voltage circuit breaker applications. Silicon IGBTs typically offers a forward voltage drop of 1.5–3.0 V (depending on the voltage and current ratings), and are the most commonly used power semiconductor switch type in SSCBs today. The forward voltage drop of IGBTs translates into an on-resistance of tens to hundreds of mΩ or a power loss of tens to hundreds of watts, too high for passively cooled

circuit breaker applications. Silicon superjunction MOSFETS up to 650 V typically offer an on-resistance similar to that of IGBTs. In the long run, WBG devices, such as SiC MOSFETS with a specific R_{DSON} of 2–3 mΩ-cm^2 at 1200 V or GaN HEMTs with a specific R_{DSON} of 1–2 mΩ-cm^2 at 650 V, become the only choice to reduce the SSCB on-resistance into the mΩ range for passive-cooling operation. Even though these WBG devices are still 4–5 times more expensive than their silicon counterparts, they are expected to follow the classical semiconductor cost reduction learning curve. In particular, GaN power devices, fabricated on silicon wafers with metal organic chemical vapor deposition (MOCVD) expitaxy growth techniques in fully depreciated 6 or 8 in CMOS fabs, stand a real chance of achieving cost parity with silicon in the near future if the production volume reaches a critical mass. This is indicated by the fact that commercial 100 V eGaN FETs are already in a price range comparable to their silicon MOSFET competition. It is for this reason that we focus on using commercial GaN FETs (e.g., 650 V/25 mΩ GS66516T from GaN Systems and 900 V/50 mΩ TP90H050WS from Transphorm) in this work. One concern with using GaN FETs in SSCB applications is whether or not they have sufficient device ruggedness in terms of reverse biasing safe operating area (RBSOA) to survive a stressful inductive turn-OFF with simultaneously high current and high voltage present. Comprehensive device characterization is performed to address this concern, as will be discussed later in this article.

B. Tri-mode Operation and Topology

A conventional SSCB design for interrupting fault currents is typically comprised of a semiconductor static switch, sensing and control electronics, auxiliary power and communication circuits, and energy absorption components such as metal oxide varistors (MOVs). It typically operates either in the ON (normal) or OFF (fault) state, and has a limited flexibility to deal with complex scenarios such as inrush currents during the startup of an electronic load.

In this work, a switching-mode common-inductor bidirectional buck topology is investigated to replace the simple ON/OFF switch configuration and facilitate a third operating mode of PWM-CL in addition to the basic ON and OFF operation to enhance the flexibility and intelligence of the SSCB. The tri-mode *iBreaker* will quickly limit a detected overcurrent to 2×–3× of the rated nominal current within a few microseconds, and conduct a fault authentication process within a preset time window (typically a few milliseconds) while operating at this relatively low overcurrent. This will significantly reduce the stress on the wiring and power semiconductor devices, and reduce the current rating and cost of semiconductor switches. The fault authentication algorithm will be discussed later in this article. If a short-circuit fault condition is confirmed, the *iBreaker* will transition to the OFF state from the current PWM-CL state. However, if a startup inrush condition is determined, the *iBreaker* will continue to operate in the PWM-CL state and facilitate a soft start of the load at this low overcurrent. In addition, the PWM-CL state can accommodate other intelligent functions. One example is to identify the fault location on the downstream cable connecting the load. This function can help expediting the system maintenance process after a power shutdown due to a fault. It is worth noting that an SSCB topology operating a silicon MOSFET and a freewheeling diode in a pulse (or hiccup) mode was reported to limit the startup inrush current in [9] and [10], but it somehow operated the MOSFET continuously in the saturation regime with a very high power dissipation to limit the fault current before shutting it down. A true switching-mode buck topology was simulated and modeled to limit the dc fault current by operating the semiconductor switch in a PWM ("pulse by pulse") mode in [27] and [28] while a similar buck topology was experimentally demonstrated in a dc fault current limiter [29], but none of these works integrated the type of soft-start and other intelligent functions as demonstrated in this work.

C. Combined Digital and Analog Control

Analog control provides extremely fast fault detection and reaction times (typically 1–5 μs) but lacks the flexibility and programmability offered by digital control techniques. On the other hand, the response time of digital control is limited to tens of μs by the clock or interrupt frequency of the DSP or microcontroller used. In the *iBreaker* designs, a hybrid control approach is adopted to combine digital and analog control to achieve both programmability and μs-scale response time.

D. Universal Hardware/Software Architectures

The application environment for circuit breakers is extremely diverse and complex in terms of current and voltage characteristics as well as load and fault conditions. It would be impractical to develop an *iBreaker* product for every application scenario. Instead, a universal hardware/software architecture should be considered to allow the use of one hardware but many control algorithms (OHMA) approach. The proposed OHMA approach will allow circuit breaker manufacturers to develop and support a small number of *iBreaker* products for a wide range of diverse applications, using different software programs optimized for each application scenario.

III. Circuit Topology

A bidirectional common-inductor buck topology is proposed in this work to facilitate the aforementioned tri-mode operation, as shown in Fig. 2. In the first *iBreaker* design case, the dc-bus voltage is set to 380 V and the nominal load current to 20 A. The *iBreaker* is comprised of a GaN power board (yellow box) and a control circuit board (green box). It is essentially a back-to-back bidirectional buck converter with a common inductor, which allows or blocks current flow in either direction between left and right. When current flows from left to right, GaN FET Q_2 remains in the ON state and operates in the third quadrant with a low on-resistance. GaN FET Q_1, also remains in the ON state and operates in the first quadrant under normal operation conditions. However, when an overcurrent condition is detected, Q_1, freewheeling diode D_1, and inductor L_2 together form a simple buck converter and operate in a PWM mode to limit the load current to a reasonably low level (e.g., 2× nominal). L_2

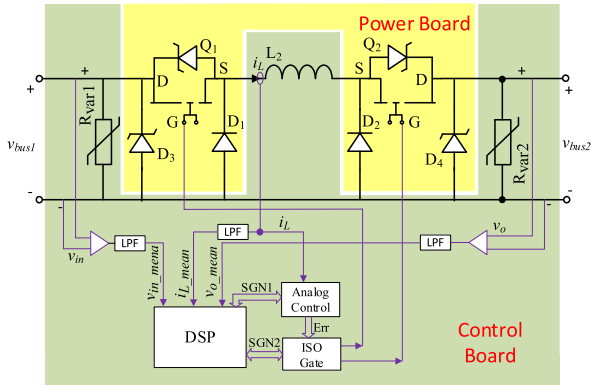


Fig. 2. Simplified schematic of the 380 V/20 A bidirectional *iBreaker* comprised of a control board (green box) and a GaN power board (yellow box). The *iBreaker* is essentially a back-to-back buck converter with a shared inductor. The control board has current, voltage, temperature sensors, a DSP, LPFs, and an analog control circuit. Five 650 V/25 mΩ GaN FETs (GaN systems GS66516T) are used in parallel for Q_1 or Q_2 to offer an equivalent on-resistance of 5 mΩ.

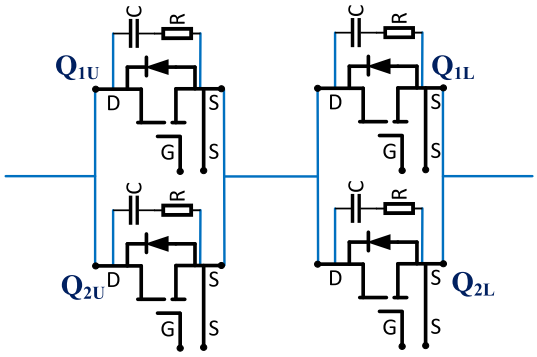


Fig. 3. Stacked 900 V GaN switches along with *RC* snubber circuit as Q_1 or Q_2 in Fig. 2 for the bidirectional 1000 V/10 A *iBreaker* design case. A total of eight 900 V/50 mΩ cascode GaN FETs (Transphorm TP90H050WS) are used in parallel/series for a total on-resistance of 25 mΩ and voltage rating of 1800 V.

also helps limit the fault current rate of change *di/dt* when a short-circuit fault occurs. The circuit operates in a similar way when the current flows from right to left since the topology is nearly symmetrical. The following discussion assumes that the current flows from left to right for the sake of simplicity. Five 650 V/25 mΩ GaN FETs (GaN Systems GS66516T) are used in parallel for Q_1 or Q_2 to offer an equivalent on-resistance of 5 mΩ in this study. The *iBreaker* total on-resistance is 10 mΩ (that of Q_1 and Q_2). The power board also includes several *RC* snubbers, MOVs, and diodes to ensure safe operation of the *iBreaker*.

The control board includes several sensors for current/voltage/temperature, a DSP, low-pass filters (LPFs), and an analog control circuit. A DSP or MCU (e.g., NUCLEO-L432KC from STMicroelectronics) is used to control the operation of the *iBreaker*, which has ADC, DAC, PWM, UART, and GPIO modules. Voltage and current sensors are used to constantly sense the dc-bus voltage v_d, node voltage v_s, and switch current i_s. Note that only the dc components of v_s, v_d, and i_s are fed to the ADC module of the DSP through the LPFs. The DSP reads these input signals once in every sampling cycle (e.g., 72 μs), and runs different control programs based on these signals. In addition, an analog control circuit is used to continuously detect and register overcurrent conditions due to either a short-circuit fault or a startup inrush current. The instantaneous switch/load current is before the LPF is constantly compared with a trip threshold I_p, which is the maximum current of the *iBreaker* set by the DSP (e.g., 40 A or 2× of the *iBreaker*'s nominal rating of 20 A). If it is less than I_p, Q_1 will be solely controlled by the DSP. If is exceeds I_p, the overcurrent analog control circuit will turn-OFF Q_1 immediately to limit the output current of the *iBreaker*, and at the same time send an overcurrent status signal to the DSP. The DSP will then initiate a PWM-CL program and find out the reason behind the overcurrent condition. If it is due to an inrush current, the *iBreaker* will charge the capacitive load to the dc-bus voltage through a PWM operation of the buck converter. The pulse width of v_s is measured using the DSP's capture function when the *iBreaker* operates in a PWM mode to limit the output current. After the successful startup, Q_1 will stay ON. If the soft startup operation cannot increase the load voltage to a preset value close to the dc-bus voltage within a specified time period, it is deemed that the overcurrent condition is due to a short-circuit fault. Therefore, Q_1 will turn-OFF and remain OFF.

Combining the flexible DSP with the analog-like overcurrent detection circuit leads to an optimal solution to maintain a μs-scale ultrafast response time while gaining digital programmability for the new *iBreaker*. The *iBreaker* also draws power from the positive and negative power buses to supply the control electronics through an isolated dc power module. An negative temperature coefficient (NTC) sensor is used to monitor the switch temperature for overtemperature protection of the *iBreaker*. A Bluetooth module is also included in the *iBreaker* to facilitate wireless communication such as status reporting or remote switching functions. Note that the *iBreaker* responds to a fault condition autonomously even without the wireless communication.

A 1000 V/10 A *iBreaker* design case is reported in this article for the first time. Since there are no 1200 V commercial GaN FETs available today, two 900 V cascode GaN switches (Transphorm TP90H050WS) are stacked in series to support the 1000 V bus voltage. It is worth noting that these stacked transistors typically need to support an inductive flyback voltage 1.5× higher than the dc-bus voltage during the SSCB shutdown. Fig. 3 shows the series/parallel 900 V GaN switches along with *RC* snubber circuits to replace Q_1 or Q_2 in Fig. 2. Note that a total of eight 900 V/50 mΩ GaN FETs are connected in parallel/series (only four are shown in Fig. 3) to offer an equivalent on-resistance of 25 mΩ and a voltage rating of 1800 V. The *iBreaker*'s total on-resistance is 50 mΩ (the sum of Q_1 and Q_2 R_{DSON}).

IV. Control Strategy

The *iBreaker* offers three distinct operation states: ON, OFF, and PWM-CL. The conventional ON state (Q_1 and Q_2 staying ON) allows continuous conduction of normal load currents while the conventional OFF state (Q_1 and Q_2 staying OFF) prohibits any current flow. The third PWM-CL state allows Q_1 or Q_2 depending on the current flow direction to switch in a PWM

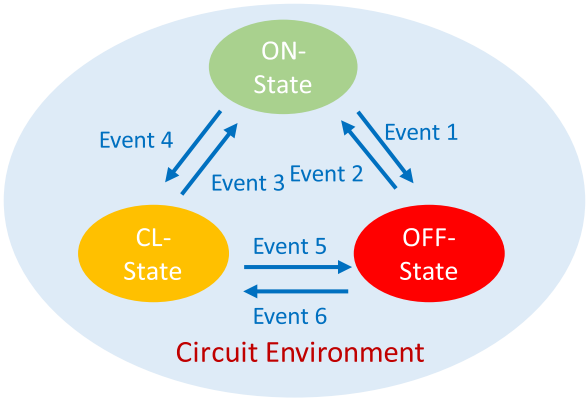


Fig. 4. *iBreaker* tri-mode control strategy.

mode with a limited peak current to distinguish an inrush current from a short-circuit fault and/or perform other intelligent functions. In the CL state, the GaN FET switches at a variable PWM frequency to optimally facilitate a soft startup process. Note that the SSCB only operates in the CL mode for a short-time period (typically several ms), and then exits to either the ON or OFF state depending on the circumstances. Such a tri-mode control strategy is described as an event-driven finite state machine in Fig. 4.

Transitions among the three operation states are driven by events, as shown in Fig. 4. Event 1 denotes the transition from ON to OFF state. It covers at least one of the following conditions: overload current (but still below the instant overcurrent shutdown threshold I_P) for an extended time period (e.g., 30 s); manual or remote shutdown command; or SSCB overtemperature. Event 2 covers the transition from OFF to ON state based on manual or remote turn-ON command. Event 4 occurs when the load current exceeds the preset overcurrent threshold I_P, due to either a true short-circuit fault or a normal inrush current during load startup. The *iBreaker* will shift from ON to CL state. In the CL state, the DSP will run a soft startup program, and operate the GaN FET with a variable frequency PWM algorithm to be discussed as follows. The root cause of the overcurrent condition will be determined by a fault authentication program to be discussed as follows. If it is deemed to be an inrush current, the *iBreaker* will return to the ON state after successfully charging the input capacitor of the load to the dc-bus voltage, as indicated by Event 3. If the overcurrent is due to a short-circuit fault, the *iBreaker* will shift to the OFF state, as indicated by Event 5. In the CL state, the average current through Q_1 is always less than I_p since the PWM duty cycle is less than 100%. The dc source and the power line, if sufficiently designed, will not be subject to thermal overstress since the *iBreaker* only operates in the CL state for a very short-time period (less than a few ms). Event 6 denotes situations such as reclosing of the *iBreaker* immediately after a short-circuit shutdown or a scheduled soft start of a load. The default operating state of the *iBreaker* is OFF, guaranteed by a large gate-source shorting resistor in the hardware design. The *iBreaker* will be powered up once being connected to the dc power source, a process taking no more than tens of μs to complete. After initialization, the DSP may choose to turn-ON Q_1 or keep it OFF depending on the user command. If the *iBreaker* enters the ON state, its output current i_o will be monitored by both the DPS and the overcurrent analog control circuit. If an overcurrent condition (i.e., i_o exceeding I_p) is detected, the *iBreaker* will shift to the CL state, otherwise it will remain in the ON state. The *iBreaker* operating in the CL state will continue its operation if the soft start process is still on-going, or exit to the ON state if the soft start process is finished. However, if the DSP determines that the startup process cannot be completed as a result of a true short-circuit fault, it will transition to the OFF state. Other state shifts from ON to OFF or from OFF to CL can be facilitated by a remote or manual user command.

The DSP continuously monitors the currents and voltages in the *iBreaker* circuit as shown in Fig. 2 with a sampling cycle time of 72 μs. When operating in the CL state, the DSP examines the difference between the dc-bus voltage and the output voltage. If the error is less than a preset threshold (e.g., 5 V), the DSP sends the *iBreaker* to the ON state. Otherwise, the DSP will check next if the soft start process exceeds a preset time limit (e.g., 2 ms), and send the *iBreaker* to the OFF state if that is the case. Otherwise, the DSP will check next if the output current exceeds the preset overcurrent threshold (e.g. 2$\times$ rated current, 40 A), and continue the PWM operation at the same PWM frequency if that is the case. Otherwise, the buck converter will operate at a reduced PWM frequency as will be discussed as follows. The PWM period can be chosen as 4 μs, 6 μs, 8 μs, 12 μs, 18 μs, 24 μs, 36 μs, and 72 μs. For a true soft start, the *iBreaker* will eventually operate at a PWM frequency of 13.9 kHz (1/72 μs) before exiting to the ON state.

A. Variable Frequency PWM Algorithm

Most ICT equipment has an input capacitor filter in a range of tens of μF [34]. The input capacitance can be as large as thousands of μF in aircrafts [35]. When such a load with an input capacitor is powered up by a dc bus, there will be a very large initial inrush current to charge the capacitor. The proposed *iBreaker* will shift to the PWM-CL state to limit the inrush current and gradually charge the capacitor up to the dc-bus voltage. A variable frequency PWM control algorithm is proposed to optimize the soft startup process. If the PWM frequency is too low at a certain duty cycle, the energy transferred from the dc source will be completely dissipated on the load resistor without actively charging the parallel capacitor within one PWM cycle. This requirement sets the lower limit for the PWM frequency. On the other hand, if the PWM frequency is too high or the PWM cycle time too small, the dc source cannot transfer sufficient amount of energy to the load side within one PWM cycle under the constraint of a finite OFF time for the GaN FETs. This requirement sets the upper limit for the PWM frequency. Note that the upper and lower frequency limits vary with the increasing load voltage (i.e., the buck converter duty cycle).

To successfully charge the input capacitor of an electronic load during the soft start process, the energy transferred from the dc source to the load must be more than the energy dissipated by

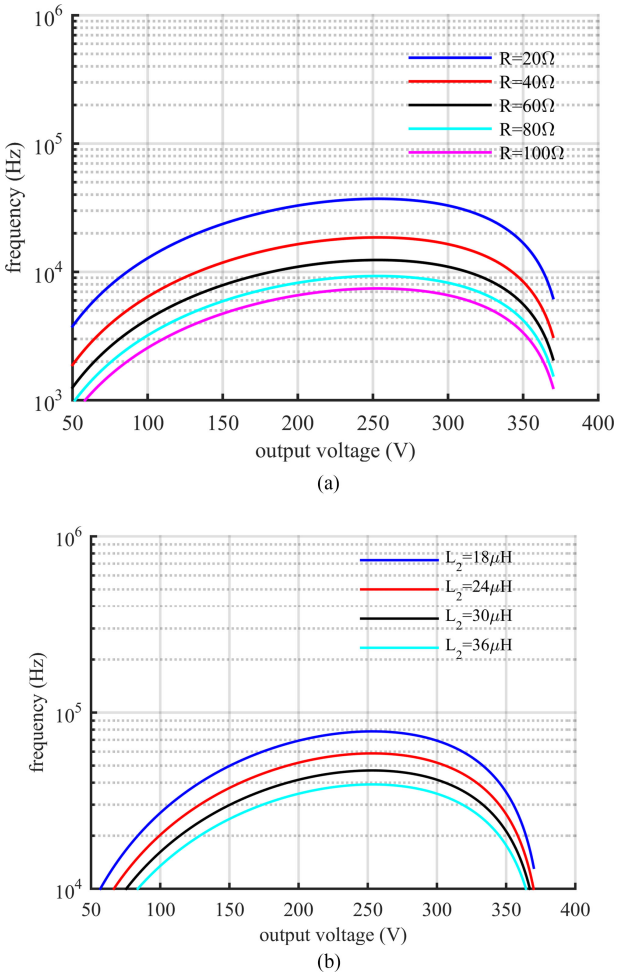


Fig. 5. Relationship between the load voltage and minimum PWM frequency for a set of different load resistor (a) with a fixed L_2 of 36 μH and a set of different load inductor L_2 with a fixed load of 19 Ω.

the load within one PWM cycle. This requirement determines the lower limit for the PWM frequency as [31]

$$f_{\text{pwm}} > \frac{2v_o^2(V_{\text{bus}} - v_o)}{V_{\text{bus}} L_2 I_p^2 R} \tag{1}$$

where V_{bus} is the input bus voltage, v_o is the output voltage, I_p is the overcurrent threshold, and L_2 is the internal inductor, and R is the load resistance.

Fig. 5 shows the relationship between the minimum PWM frequency and the output (load) voltage for a set of different load resistor R and a fixed inductor L_2 of 36 μH. For a load resistor of 100 Ω and 20 Ω, the PWM frequency should be higher than 7.5 kHz and 40 kHz, respectively. When the load resistor is 20 Ω, the PWM frequency should be larger than 40 kHz. A higher PWM frequency is required for a successful soft start if we want to allow a smaller load resistor.

On the other hand, a reasonably long PWM cycle time is required for the dc source to transfer sufficient amount of energy to the load side within one PWM cycle considering a finite OFF time for the GaN FETs. A reasonable PWM OFF time T_{off} sets

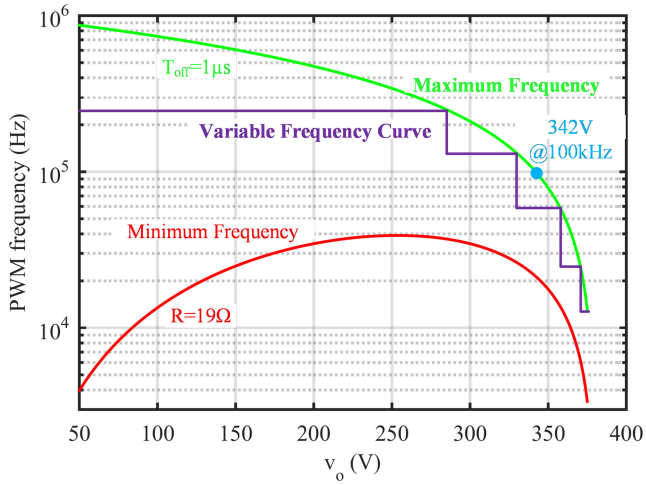


Fig. 6. Variable PWM frequency algorithm between the upper and lower limits set by (1) and (2) for a fixed PWM OFF time of 1 μs.

an upper limit for the PWM frequency

$$T_{\text{off}} = \frac{L_2 I_p^2 R_{\text{rated}}}{2V_{\text{bus}}^2}. \tag{2}$$

For a rated load resistor of 19 Ω, I_p of 40 A, L_2 of 36 μH, and V_{bus} of 380 V, the maximum T_{off} is roughly 4 μs. To guarantee enough margin for a successful soft start, it is better to choose a T_{off} as small as practically possible. WBG devices offer a high switching speed, and allow T_{off} in the range of 1 μs or less. In this work, a fixed T_{off} of 1 μs is selected. Note that the actual PWM OFF time can be longer than T_{off} because the overcurrent detection and register circuit constantly adjusts the PWM signal from the DSP.

To choose an optimal PWM frequency for the buck converter, (1) and (2) are plotted in the f_{pwm}–v_o plane in Fig. 5. The red curve is the minimum PWM frequency required to charge up the input capacitor according to (1). The green curve is the maximum PWM frequency according to (2). A PWM frequency between the lower and upper limits needs to be selected for the buck converter. If a fixed PWM frequency of 100 kHz is used, the output voltage would be charged to around 342 V (the blue dot in Fig. 6), leaving a large difference of 38 V below V_{bus}. If the GaN FET turns ON at this moment, there would be a large inrush current because of this large voltage difference. It is far more optimal to use a variable PWM frequency algorithm, which gradually reduces the PWM frequency as the output voltage v_o increases to approach the dc-bus voltage, as indicated by the multistep purple line in Fig. 6. When the voltage difference is less than 5 V, the PWM operation can be stopped and the GaN FET shifts to the ON state. In practice, the last PWM frequency is usually selected first, which is also the sampling frequency for voltage and current sensing (13. 9 kHz or 1/72 μs in this design case, as shown in Fig. 6). Other PWM frequencies are selected to be multiples of the last PWM frequency to ensure a smooth and easy frequency change. For example, the initial PWM frequency is 18× of the last PWM frequency or 250 kHz in this design case.

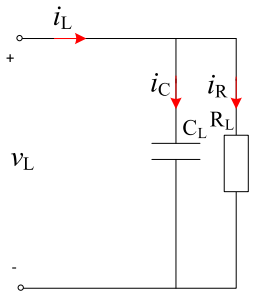


Fig. 7. *RC* load model for startup analysis.

B. Fault Authentication Methods

After an overcurrent is detected and the *iBreaker* shifts into the PWM-CL state, the DSP needs to use a fault authentication method to judge whether it is a true short-circuit fault or just an inrush current for normal equipment startup. The first fault authentication program monitors the output voltage of the *iBreaker* (same as the load voltage V_L) within a preset time window. The time window should be long enough to allow the completion of a soft startup process but short enough to ensure a quick response to a true fault current.

Fig. 7 shows an *RC* load model used for startup analysis. The load current I_L is assumed to be constant (e.g., 40 A in the case study) in the current limiting mode. The soft-start time is simply given as

$$t = R_L C_L \ln \frac{R_L I_L}{R_L I_L - V_{\text{bus}}}. \tag{3}$$

If the output voltage approaches the bus voltage V_{bus} (within a margin of a few volts) within the predetermined time window, it is deemed to be a normal startup process, and the *iBreaker* next shifts to the ON state. If the output voltage of the *iBreaker* does not reaches the bus voltage within the predetermined time window, it is deemed to be a short-circuit fault, and the *iBreaker* shifts to the OFF state. This is a simple fault authentication method that is easy to implement, but requires prior knowledge on the load resistance and capacitance. Nevertheless, a typical time window of 1–5 ms can cover a wide range of loads with various *R* and *C* values.

The second fault authentication method directly measures the rate of change of the load voltage dv_L/dt, as shown in Fig. 2. If $dv_L/dt > 0$, it is deemed to be an inrush current scenario. Otherwise, it is a short-circuit fault. The output or load voltage can be sampled periodically (e.g., every 72 μs) and dv_L/dt can be calculated. The dv_L/dt increment between two consecutive voltage samples is given by

$$\Delta v_L = \frac{I_L}{C_L} e^{-t/(R_L C_L)} \times \Delta t \tag{4}$$

where Δt is the sampling time of 72 μs and I_L at 40 A.

Fig. 8 shows the calculated load voltage change between two consecutive sampling periods as a function of the actual load voltage for different load capacitances and a fixed resistance of 19.5 Ω for startup scenarios. It is evident that the voltage

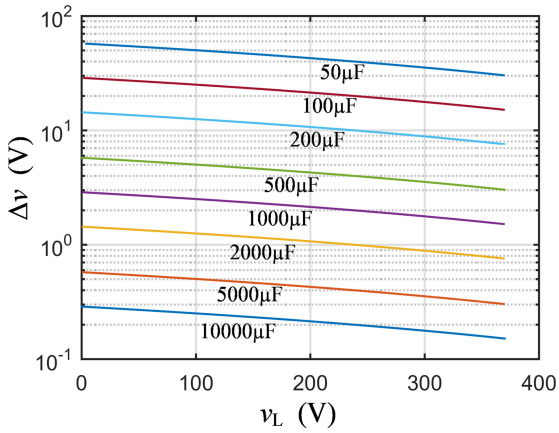


Fig. 8. Load voltage increment as a function of the actual load voltage for different load capacitances for startup scenarios with a fixed *R* of 19.5 Ω.

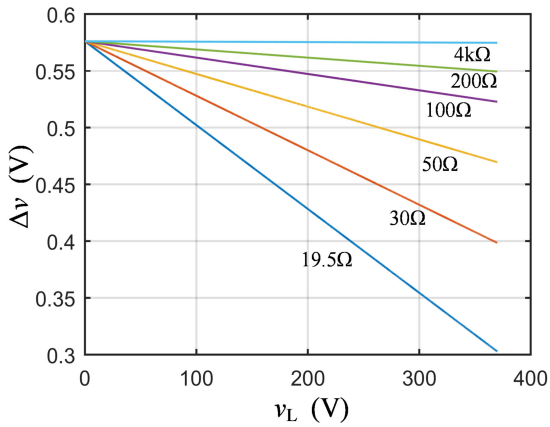


Fig. 9. Load voltage increment as a function of the actual load voltage for different load resistances for startup scenarios with a fixed *C* of 5 mF.

increment between two consecutive sampling periods increases with decreasing load capacitance. For example, for a load capacitance *C* of 10 000 μF and load resistance *R* of 19.5 Ω, Δv_L is between 0.1 V and 0.3 V. Fig. 9 shows the calculated load voltage change between two consecutive sampling periods as a function of the actual load voltage for different load resistances and a fixed capacitance of 5 mF for startup scenarios. Δv_L decreases quickly with increasing load voltage for smaller load resistances. The resolution of ADC in the *iBreaker* design is 12 b, so the theoretical voltage sampling resolution for a voltage range of 0–500 V is 120 mV. Because of the noise and nonlinearity of the ADC, the actual voltage sampling resolution is usually 2–3 times of the theoretical value, roughly 0.3 V. It is also possible to monitor the load voltage change over more than two sampling cycles. Comparing to the first method, the second fault authentication method does not require prior knowledge on the load capacitance and resistance.

C. Fault Locating Algorithms

It is highly desirable to find the fault location on the power line in the event of a fault shutdown so that it can be cleared by the

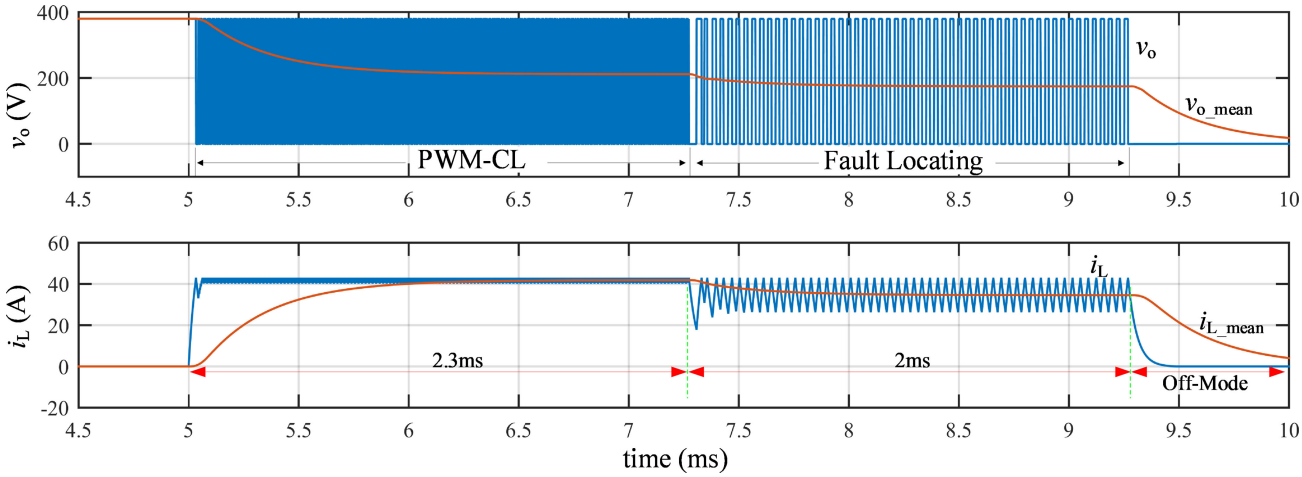


Fig. 10. Simulated current and voltage waveforms of the *iBreaker* responding to a short-circuit fault at t=5 ms. It initially operates in a PWM-CL state with an output current limited to 40 A for 2.3 ms. After the fault condition is authenticated at t=7.3 ms, it switches ON a fault locating algorithm for about 2 ms. The PWM period for these two current limiting modes is 4 μs and 36 μs, respectively.

maintenance personnel as quickly as possible. A method based on travelling-wave was reported to identify short-circuit location in transmission lines in [36]. Other fault location techniques based on power line impedance measurement by injecting small signals were also reported [37], [38]. However, these methods require additional hardware and inevitably increase system cost and complexity. The PWM-CL state of the *iBreaker* provides an opportunity to locate a fault without any additional hardware and greatly simplifies the troubleshoot process after the fault shutdown [31]. After a fault is authenticated in a PWM-CL mode, a fault locating algorithm can be performed and a special PWM gate control pulses will be sent to the buck converter for a short period (a few ms). Since the power line inductance L_{line} between the *iBreaker* and the short location can be considered as part of the output inductance of the buck converter, it can, therefore, be extracted from the converter voltage and current information as

$$L_{\text{line}} = [(V_{\text{in\_mean}} - V_{o\_\text{mean}}) \times t_1/(2I_p - 2I_{L\_\text{mean}})] - L_2 \quad (5)$$

where V_{in_mean} is the input bus voltage, V_{o_mean} is the averaged output voltage, t_1 is the on time of the PWM pulse, I_p is the overcurrent threshold, I_{L_mean} is the averaged output or inductor current, and L_2 is the internal inductor in Fig. 2. The voltages and currents are measured values after the LPFs.

The distance between the *iBreaker* and the fault location can then be calculated based on the per-unit-length inductance value of the power line. The fault locating algorithm is verified by simulation and experiments. Fig. 10 shows the simulated current and voltage waveforms of the *iBreaker* responding to a short-circuit fault at $t = 5$ ms. It initially operates in a PWM-CL state with a PWM period of 4 μs and an output current limited to 40 A. After the fault condition is authenticated at t = 7.3 ms, it switches to a fault locating algorithm with a PWM period of 36 μs for about 2 ms. During this short-time period, it extracts the power line inductance and the distance between the fault and the *iBreaker*. Fig. 11 shows the measured instantaneous and averaged output voltages and currents for an actual power line inductance of 163.8 μH. The extracted power line inductance using the proposed approach is 161.3 μH, within an error of 1.5%.

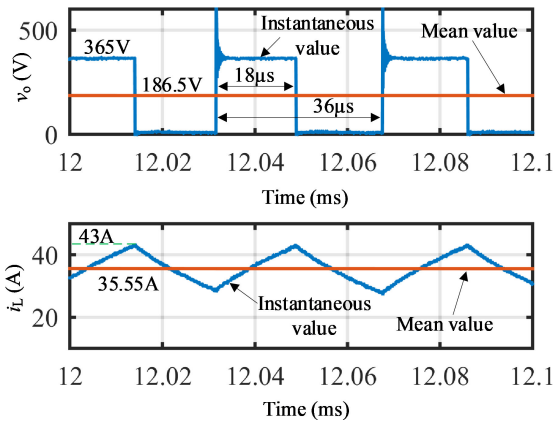


Fig. 11. Measured output voltage and current (instantaneous and average) waveforms under short-circuit fault with an actual line inductance of 163.8 μH.

V. Experimental Results

Two *iBreaker* prototypes, rated at 380 V dc/20 A for dc data center and office building applications and 1000 V/10 A for PV farms and EV charging stations, respectively, are built and tested to validate the proposed design methodology. Fig. 12 shows the *iBreaker* prototype and the capacitor discharge circuit used to characterize its functions. The capacitor bank of 2 $\times$ 5600 μF is first charged by a dc power supply, and then discharges to an *RC* load through the *iBreaker*. In the experiment, two types of *RC* loads are used. Type 1 is a 40 μF capacitor in series with a 2.5 Ω resistor to emulate a normal inrush startup condition. Type 2 is a 2.5 resistor to emulate a short-circuit fault condition. In both cases, four-layer 2-ounce Cu PCBs are used with the main

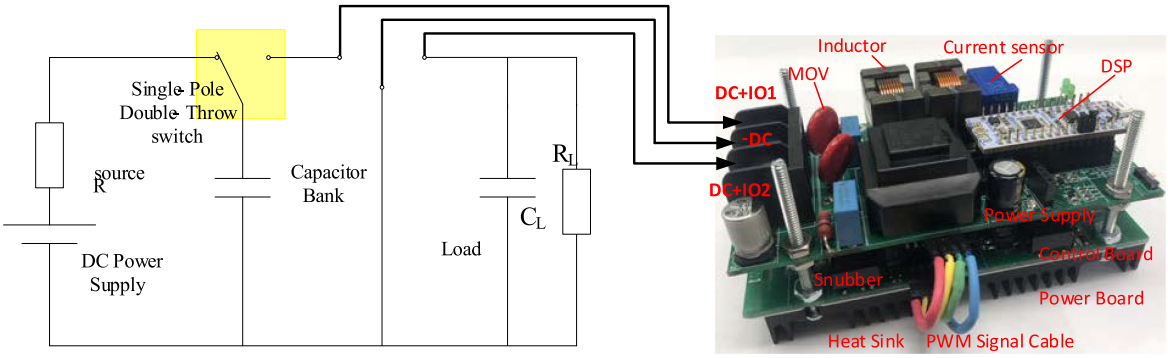


Fig. 12. 380 V/20 A GaN-based *iBreaker* prototype in a capacitor discharge testing circuit.

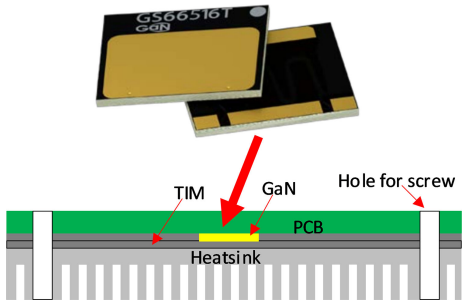


Fig. 13. GaN FET (GS66516T) on the 380 V/20 A *iBreaker* PCB with a heatsink mounted with a TIM pad.

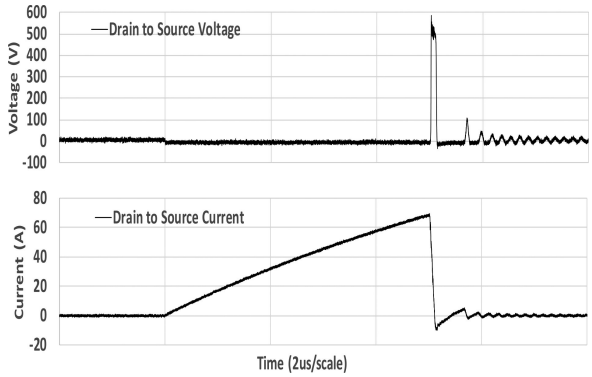


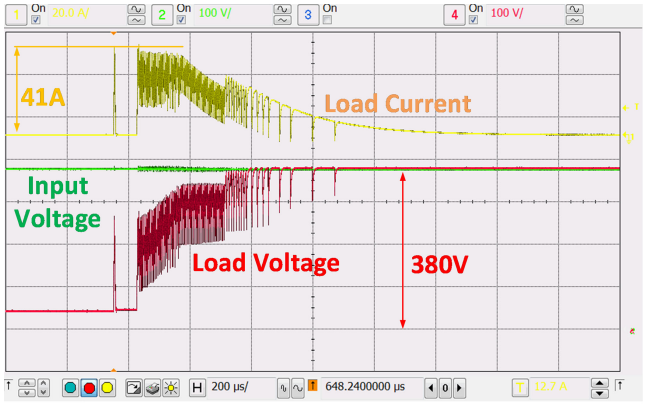
Fig. 14. RBSOA characterization of a single 650 V/60 A GaN FET (GS66516T) using a clamped inductive switching circuit. The device safely turns OFF a current of 68 A with a flyback voltage up to 580 V.

current being conducted mostly by all the four copper layers in parallel except for using 2 or 3 copper layers for the occasional crossovers on the PCB.

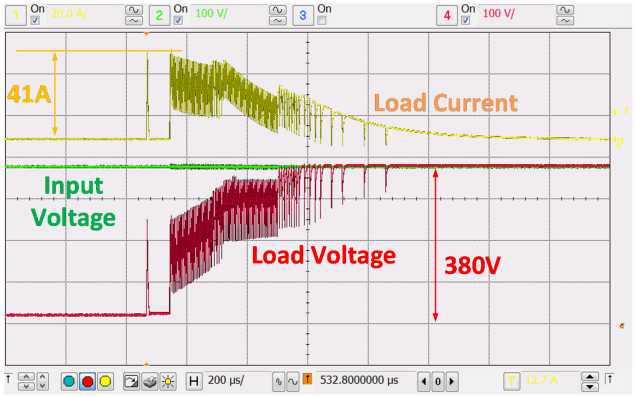
In the 380 V dc/20 A *iBreaker* prototype, each of Q_1 and Q_2 shown in Fig. 2 is made of five paralleled commercial 650 V/60 A/25 mΩ GaN FETs (GaN Systems GS66516T) to offer a total *iBreaker* ON-state resistance of 10 mΩ, which exhibits a total power loss of 4 W and a transmission efficiency of 99.95%. The heatsink pad is on the topside of GS66516T FETs, allowing excellent heat transfer to the heat sink through a thermal interface material (TIM), as shown in Fig. 13. The heat generated by the GaN FETs will flow from the junction to case, then PCB board, TIM, heatsink, and finally to ambient. The thermal resistance $R_{\theta\mathrm{TIM}}$ of the TIM is estimated as 1.3 °C/W. The total junction to case thermal resistance $R_{\theta\mathrm{JC}}$ of all ten GaN FETs is 0.027 °C/W. The heatsink to ambient thermal resistance $R_{\theta\mathrm{HSA}}$ is 4 °C/W. The total ON-state power loss of the *iBreaker* is 4 W at the rated current of 20 A and a total on-resistance of 10 mΩ. The junction temperature rise is estimated to be 21.2 °C at room temperature, offering a fairly large margin for the safe and reliable operation of the 380 V/20 A *iBreaker*.

One concern with using GaN FETs in SSCB applications is whether or not they have sufficient RBSOA to survive a stressful inductive turn-OFF with simultaneously occurring high current and high voltage on the device. These GaN FETs are comprehensively characterized to address this concern. Fig. 14 shows the measured drain voltage and current waveforms of a single GS66516T under a clamped inductive switching RBSOA characterization testing. The single GaN FET can safely turn-OFF a current up to 68 A under a flyback voltage of 580 V, indicating a large safety margin for the intended 380 V dc applications since each of the five parallel GaN FETs only needs to handle 1/5 of the total current (4 A nominal).

Fig. 15(a) and (b) shows the input voltage (green), load voltage (red), and load current (yellow) waveforms of the bidirectional 380 V/20 A *iBreaker* with the 40 μF capacitive load to emulate a soft startup process for a left to right and right to left current flow, respectively. It is observed that the *iBreaker* operates in the PWM-CL state with a gradually decreasing load current as the load voltage increases. The load capacitor is fully charged to the input voltage of 380 V with a peak charging current of 41 A after 500 μs. The behaviors of the bidirectional *iBreaker* are fairly symmetrical between the two current flow directions. Fig. 16(a) and (b) shows the input voltage (green), load voltage (red), and load current (yellow) waveforms of the 380 V/20 A *iBreaker* with a load resistor of 2.5 Ω to emulate a short-circuit fault, and 15 Ω to emulate the turn-ON of a nominal current, respectively. It is observed in the short-circuit fault case in Fig. 16(a) that the *iBreaker* initially senses an overcurrent of 41 A, and quickly turns it OFF within a few μs by the analog control circuit. The *iBreaker*, however, enters into the PWM-CL state after approximately 100 μs, and maintains at an average current of 40 A (2× of the nominal), now controlled by the

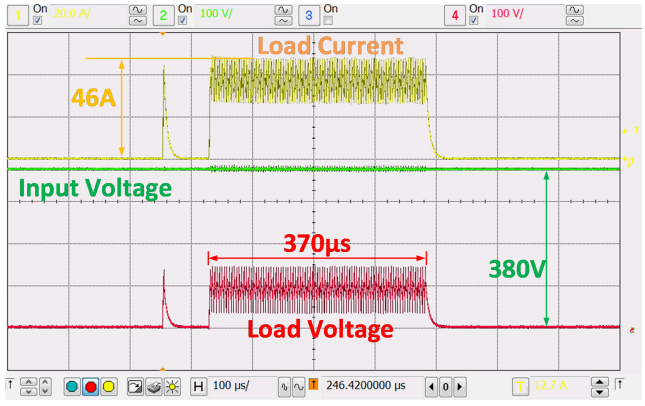


(a)

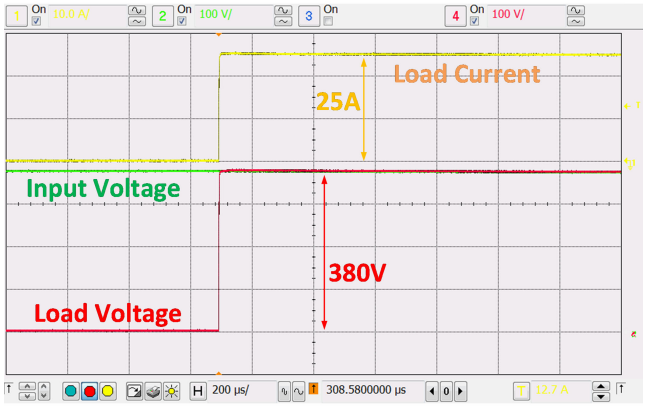


(b)

Fig. 15. Input voltage (green), load voltage (red), and load current (yellow) waveforms of the bidirectional 380 V/20 A *iBreaker* with a 40 μF capacitive load to emulate a soft startup process. (a) Left to right current flow. (b) Right to left current flow.



(a)



(b)

Fig. 16. Input voltage (green), load voltage (red), and load current (yellow) waveforms of the 380 V/20 A *iBreaker* with a load resistor of (a) 2.5 Ω to emulate a short-circuit fault, and (b) 15 Ω to emulate a nominal turn-ON.

combined digital and analog circuits. The *iBreaker* stays in the PWM-CL state for a preset window of 370 μs until the fault authentication algorithm confirms that this is a true fault condition, and shut-OFF at the end. For the case of the turn-ON of a nominal current in Fig. 16(b), the *iBreaker* simply turns ON and conducts a current of 25 A and provide the full input voltage of 380 V to the load side.

Unlike the fixed I^2t profiles in the conventional thermal-magnetic circuit breakers, the *iBreaker* can offer any current-time profile to meet complex application requirement as long as they are within the thermal boundary. Fig. 17 shows a measured current-time profile of the 380 V/20 A *iBreaker* with two thermal boundaries marked for an ambient temperature of 23 °C and 85 °C, respectively. The measurement data curve in the figure is for illustration purpose, and by no means restricts other operation profile of the *iBreaker*.

In the 1000 V/10 A *iBreaker* prototype, Q_1 and Q_2 in Fig. 2 is replaced by stacking four parallel 900 V GaN switches (Transphorm TP90H050WS) to support a bus voltage of 1000 V. A total of 16 GaN switches are used in the 1000 V/10 A *iBreaker* design with a total ON-state resistance of 50 mΩ. The total power loss is 5 W and the transmission efficiency is 99.95%. Fig. 18 shows the input voltage (blue), load current (purple), device v_{ds}

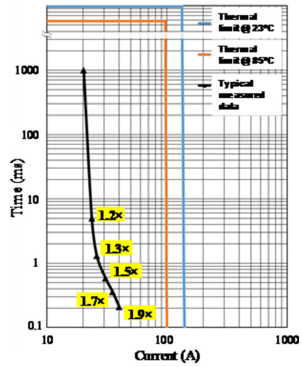


Fig. 17. Flexible and programmable current/time profile offered by the 380 V/20 A bidirectional *iBreaker*.

voltage (red), and device v_{gs} voltage (black) waveforms of the 1000 V/10 A *iBreaker* in response to a short-circuit fault emulated by a load resistor of 2.5 Ω. It is observed that the *iBreaker* initially senses an overcurrent of 20 A, and quickly turns OFF within a few μs by the analog control circuit. The *iBreaker*, however, enters into the PWM-CL state after approximately 100 μs, and maintains an average current of 20 A (2× of the nominal) for roughly 343 μs before final turns OFF. The voltage overshoot

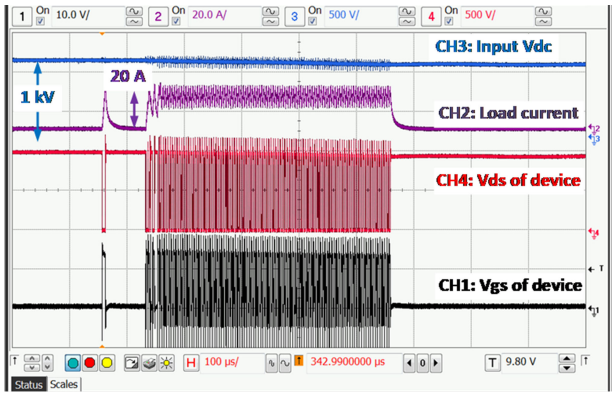


Fig. 18. Short-circuit response of the 1000 V/10 A *iBreaker* with a load resistor of 2.5 Ω.

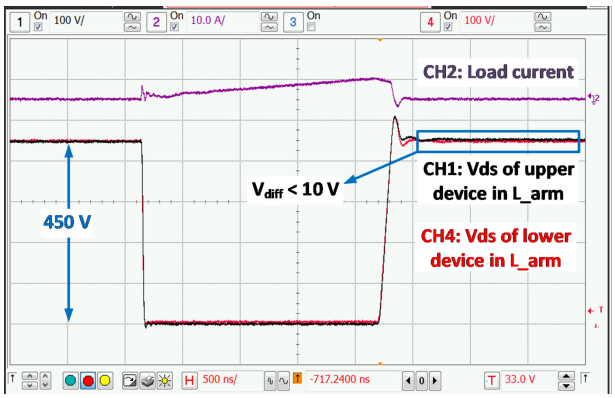


Fig. 19. v_{ds} voltage waveforms of the stacked GaN FETs of the 1000 V/10 A *iBreaker* exhibiting an excellent voltage balancing.

at the GaN FET turn-OFF reaches approximately 1200 V due to the inductance in the circuit. Fig. 19 shows the drain-source v_{ds} voltage waveforms of the two stacked 900 V GaN FETs during the *iBreaker* action at a bus voltage of 900 V. Excellent steady state and dynamic voltage balance between the two GaN FETs with a steady-state voltage difference less than 10 V are observed.

In brief, both *iBreaker* prototypes fully demonstrate the targeted SSCB functions, and validate the design methodology described in Section II.

VI. Conclusion

Protection against short-circuit faults and enabling safe startup of electronic loads present technical challenges in low-voltage dc microgrids. This article provides a comprehensive and integrated discussion on the basic concept and general design methodology of a GaN-based, tri-mode, intelligent SSCB (*iBreaker*). The *iBreaker* concept mainly explores the use of GaN devices in the low-voltage (<1000 V), mΩ-resistance SSCB designs and new SSCB topology and control techniques beyond the commonly used ON/OFF switch configuration in order to integrate more intelligent functions without increasing component count. The *iBreaker* uses a distinct PWM-CL state in addition to the conventional ON and OFF states to facilitate soft startup, fault authentication, and fault location functions. Key design elements, such as use of WBG (particularly GaN) switches, tri-mode operation, combined digital and analog control, and universal hardware/software architecture, are discussed in detail. In particular, the bidirectional buck topology, changes among the three distinct states, variable PWM frequency control, fault locating techniques, GaN FET hardware, and thermal design are discussed. Two *iBreaker* prototypes, rated at 380 V/20 A, and 1000 V/10 A, respectively, are built and tested to validate the proposed SSCB design concept. 99.95% transmission efficiency, passive cooling, and μs-scale response time are demonstrated by both prototypes. While these prototypes are specifically designed for 380 V dc data center and 1000 V EV charging infrastructure applications, the *iBreaker* design principle can be extended to other dc voltage and current ranges.

Acknowledgment

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References

[1] T. Dragicevic, J. C. Vasquez, J. M. Guerrero, and D. Skrlec, "Advanced LVDC electrical power architectures and microgrids: A step toward a new generation of power distribution networks," *IEEE Electrific. Mag.*, vol. 2, no. 1, pp. 54–65, Mar. 2014.

[2] D. E. Geary, D. P. Mohr, D. Owen, M. Salato, and B. J. Sonnenberg, "380V DC eco-system development: Present status and future challenges," in *Proc. 35th IEEE Int. Telecommun. Energy Conf.*, 2013, pp. 1–6.

[3] G. Allee and W. Tschudi, "Edison redux: 380 V DC brings reliability and efficiency to sustainable data centers," *IEEE Power Energy Mag.*, vol. 10, no. 6, pp. 50–59, Nov./Dec. 2012.

[4] D. J. Becker and B. J. Sonnenberg, "DC microgrids in buildings and data centers," in *Proc. 33rd IEEE Int. Telecommun. Energy Conf.*, 2011, pp. 1–7.

[5] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400V DC distribution in telco and data centers to improve energy efficiency," in *Proc. 29th IEEE Int. Telecommun. Energy Conf.*, 2007, pp. 32–39.

[6] H. Pugliese and K. Michael Von, "Discovering DC: A primer on DC circuit breakers, their advantages, and design," *IEEE Ind. Appl. Mag.*, Sep./Oct. 2013 pp. 22–28.

[7] D. Salomonsson, L. Soeder, and A. Sannino, "Protection of low-voltage DC microgrids," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045–1053, Jul. 2009.

[8] R. M. Cuzner and V. Singh, "Future shipboard MVdc system protection requirements and solid-state protective device topological tradeoffs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 244–259, Mar. 2017.

[9] K. Tan, X. Song, C. Peng, P. Liu, and A Q. Huang, "Hierarchical protection architecture for 380V DC data center application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[10] K. Tan, P. Liu, X. Ni, C. Peng, X. Song, and A. Q. Huang, "Performance evaluation of multiple Si and SiC solid-state devices for circuit breaker application in 380VDC delivery system," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 983–989.

[11] A. Abramovitz and K. M. Smedley, "Survey of solid-state fault current limiters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2770–2782, Jun. 2012.

[12] D. Urciuoli and V. Veliadis, "Demonstration of a 600-V, 60-A, bidirectional silicon carbide solid-state circuit breaker," in *Proc. Asia-Pac. Econ. Cooperation*, Mar. 6, 2011, pp. 354–358.

[13] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2597–2605, May 2013.

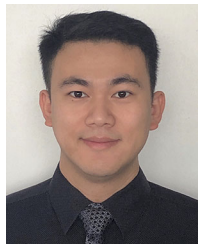
[14] Z. J. Shen, G. Sabui, Z. Miao, and Z. Shuai, "Wide-bandgap solid-state circuit breakers for DC power system: device and circuit considerations," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 294–300, Jan. 2015.
[15] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. Shen, "Design and analysis of DC solid-state circuit breakers using SiC JFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 863–873, Apr. 2016.
[16] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of solid state circuit breaker-based protection for DC shipboard power systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 260–268, Mar. 2017.
[17] F. Liu, W. Liu, and X. Zha, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage DC microgrid," *IEEE Trans. Power Electron.*, vol. 32, no. 4, 3007–3021, Apr. 2017.
[18] O. Vodyakho, M. Steurer, D. Neumayr, C. S. Edrington, G. Karady, and S. Bhattacharya, "Solid-state fault isolation devices: Application to future power electronics-based distribution systems," *IET Elect. Power Appl.*, vol. 5, no. 6, pp. 521–528, Jul. 2011.
[19] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid DC circuit breaker, Part I: Solid-state main breaker based on 15 kV SiC emitter turn off thyristor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 278–288, Mar. 2017.
[20] Y. Wang, W. Li, X. Wu, and X. Wu, "A novel bidirectional solid-state circuit breaker for DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5707–5714, Jul. 2019.
[21] Ji Shu, S. Wang, J. Ma, T. Liu, and Z. He, "An active Z-source DC circuit breaker combined with SCR and IGBT," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10003–10007, Oct. 2020.
[22] K. A. Corzine and R. W. Ashton, "A new Z-source DC circuit breaker," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2796–2804, Jun. 2012.
[23] K. A. Corzine, "A new-coupled-inductor circuit breaker for DC applications," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1411–1418, Feb. 2017.
[24] R. Rodrigues, Yu Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.
[25] Z. J. Shen *et al.*, "First experimental demonstration of solid state circuit breaker (SSCB) using 650V GaN-based monolithic bidirectional switch," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, Jun. 2016, pp. 79–82.
[26] B. Davies, "Analysis of inrush currents for DC powered IT equipment," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf.*, 2011, pp. 1–4.
[27] C. Jin, R. A. Dougal, and S. Liu, "Solid-state Over-current protection for industrial DC distribution systems," in *Proc. 4th Int. Energy Convers. Eng. Conf. Exhibit.*, 2006, pp. 26–29.
[28] S. Munasib and J. C. Balda, "Short-circuit protection for low-voltage DC microgrids based on solid-state circuit breakers," in *Proc. IEEE 7th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2016, pp. 1–7.
[29] F. Luo, J. Chen, X. Lin, Y. Kang, and S. Duan, "A novel solid state fault current limiter for DC power distribution network," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 1284–1289.
[30] Z. J. Shen and Y. Zhou, "Intelligent Tri-Mode Solid State Circuit Breakers," U.S. Patent 20200203943, Jun. 25, 2020.
[31] Y. Zhou, Y. Feng, T. Liu, and Z. J. Shen, "Short circuit fault location in DC power network using intelligent SiC solid-state circuit breaker," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 485–491.
[32] Y. Zhou, Y. Feng, and Z. J. Shen, "*iBreaker*: Intelligent tri-mode solid state circuit breaker technology," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6.
[33] Y. Zhou, Y. Feng, and Z. J. Shen, "Design considerations of tri-mode intelligent solid state circuit breaker using GaN transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2439–2444.
[34] B. Davies, "Analysis of inrush currents for DC powered IT equipment," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf. (Intelec)*, 2011, pp. 1–4.
[35] L. Song, L. Wang, L. Ruan, Z. Dai, and S. Yang, "A switching-on control strategy of the DC-SSPC for the capacitive loads," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–7.
[36] O. M. K. Kasun Nanayakkara, A D. Rajapakse, and R. Wachal, "Location of DC line faults in conventional HVDC system with segments of cables and overhead lines using terminal measurements," *IEEE Trans. Power Del.*, vol. 27, no. 1, pp. 279–288, Jan. 2012.
[37] E. Christopher, M. Sumner, D W.P. Thomas, X. Wang, and F. de Wildt, "Fault location in a zonal DC marine power system using active impedance estimation," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 860–865, Mar. 2013.
[38] R. Mohanty, U. Sri Mukha Balaji, and A. K. Pradhan, "An accurate noniterative fault-location technique for low-voltage DC microgrid," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 475–481, Apr. 2016.

Yuanfeng Zhou (Student Member, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2009, and the M.S. degree from the Huazhong University of Science and technology, Wuhan, China, in 2012. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA.

From 2012 to 2015, he was with the Emerson Network Power, Shenzhen, China, as a Design Engineer. He has authored or coauthored more than ten papers on these topics. His research interests include dc solid-state circuit breakers, hybrid circuit breakers, and wide bandgap power electronics.

Risha Na (Member, IEEE) received the Ph.D. degree in electrical engineering from the Harbin University of Science and Technology, Harbin, China, in 2013.

From 2013 to 2016, he was an Assistant Professor with the Department of Electrical and Electronic Engineering, Harbin University of Science and Technology. He was a Postdoctoral Research Associate with the Ohio State University, Columbus, OH, USA, from 2016 to 2019. He is currently a Senior Research Associate with the Illinois Institute of Technology, Chicago, IL, USA. His research interests include power electronics and applications of WBG devices in medium-voltage drive systems. He has authored or coauthored 25 papers on these topics.



Yanjun Feng (Member, IEEE) received the B.S. degree from the Donghua University, Shanghai, China, in 2013, the M.S. and Ph.D. degrees from the Illinois Institute of Technology, Chicago, IL, USA, in 2015 and 2019, respectively, all in electrical engineering.

He is currently with Canoo EV, Torrance, CA, USA. He has authored or coathored several papers on these topics. His research interests include hybrid circuit breakers and EV drivetrain power electronics.

Zheng John Shen (Fellow, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 1987, and the M.S. and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy, NY, USA, in 1991 and 1994, respectively, all in electrical engineering.

Between 1994 and 1999, he held a variety of positions including Senior Principal Staff Scientist with Motorola. He was on the Faculty of the University of Michigan-Dearborn, from 1999 to 2004, and the University of Central Florida, from 2004 to 2012. He also served as a Board Member and Chief Scientist of GWS Semiconductor, Tempe, AZ, USA, (now a division of Renesas Electronics) from 2002 to 2012, responsible for developing megahertz-frequency lateral power MOSFET technology for supercomputer and server applications. In 2013, he joined the Illinois Institute of Technology, as Grainger Chair Professor in electrical and power engineering. His research interests include power electronics, power semiconductor devices and ICs, automotive electronics, renewable, and alternative energy systems. He has authored or coauthored 300 journal and conference articles, and holds 18 issued and several pending U.S. patents in these areas.

Dr. Shen is the recipient of the 2012 IEEE Region 3 Outstanding Engineer Award, the 2003 NSF CAREER Award, and two IEEE Transactions Paper Awards. He has been an active volunteer in the IEEE Power Electronics Society (PELS), and has served as VP of Products, AdCom Member, General Chair or Technical Program Chair of several major IEEE conferences including ECCE and ISPSD. He is a fellow of the U.S. National Academy of Inventors.