Digital V^2 Constant ON-Time Control Buck Converter With Adaptive Voltage Positioning and Automatic Calibration Mechanism

Kai-Yu Hu, *Member, IEEE*, Chien-Hung Tsai, *Member, IEEE*, and Chien-Wu Tsai

***Abstract*—This article presents a digital V^2 constant ON-time control buck converter with adaptive voltage positioning (AVP) and automatic closed-loop output impedance (Z_{oc}) calibration for advanced system-on-a-chip processors. To ensure that the output voltage deviation remains within the desired range, the system is equipped with AVP. For an optimal AVP design, the system includes a second-order digital inductor current sensor for deriving a constant Z_{oc} within a wide bandwidth. A detailed system-level analysis was performed to design the proposed control architecture. Considering the inevitable variation and aging of power stage components, the system is equipped with an online real-time Z_{oc} calibration mechanism established to ensure the performance of AVP control. A prototype chip was fabricated using a 90-nm complementary metal–oxide–semiconductor (CMOS) process. The digital controller was fully realized using a standard cell library. Under a 0.9-A load transient, the measured output voltage could be adequately constrained within a specified 1.1-V and 110-mV AVP window.**

***Index Terms*—Digital control, dc–dc power converters, power integrated circuit.**

I. Introduction

THE output voltage deviation of dc–dc converters should be within the application tolerance range. Adaptive voltage positioning (AVP) is widely used in voltage regulator modules (VRMs) for personal computers and server processors to reduce dynamic output voltage derivation through the variation of the output voltage of converters such that it is inversely proportional to the output current or inductor current. When a constant and controllable closed-loop output impedance (Z_{oc}) model is designed, both the steady-state and transient output voltages of converters can be adequately defined within a specified AVP window [1]. With the rapid growth of power and current slew-rate demands of future embedded system-on-a-chip (SoC) processors [2], AVP can improve the performance of power management modules.

Recently, analog ripple-based constant ON-time (COT), constant OFF-time, and other derivative control schemes have received considerable research attention because of their superior fast-transient characteristics [3], [4]. Applying AVP in a ripple-based control (RBC) scheme can further improve the transient performance of RBC [5]–[11]. For COT and an adaptive ON-time control, AVP can be implemented to yield an optimal inductor current sensing gain [5]–[8] and time constant for differentially enhanced duty ripple control [9]. For hysteretic control, AVP can be implemented to derive an optimal inductor current sensing filter [10], [11].

A digital RBC scheme [12]–[16], [22] and [23] combines the fast-transient characteristics of an analog RBC scheme and the advantage of digital power management [17]. Moreover, the transient performance of a digital RBC scheme is considerably higher than that of a traditional digital voltage-mode control scheme. However, among digital control schemes, AVP is mostly implemented in digital voltage-mode control schemes. Only the authors in [15] implemented AVP in a digital COT control scheme. The system architecture in [15] is digital hybrid ripple-based COT control with high-level digitalization, in which both current loop and voltage loop are implemented in a digital way. In current loop, an inductor current estimator is used to reduce the sampling rate of inductor current sensing ADC. Detail system analysis is provided in [15] and the AVP was implemented by choosing a proper inductor current sensing gain, as performed in [8].

In terms of design, AVP is based on Z_{oc}, and the desired load-line (R_{LL}) requirement can be adapted accordingly. To optimize AVP performance, Z_{oc} should be a constant within the control bandwidth. If Z_{oc} is not a constant, the output voltage would exhibit extra undershoot or overshoot during load transient operation. Moreover, a higher constant Z_{oc} bandwidth results in faster load transient recovery [10], [11]. However, Z_{oc} may vary with component aging and fabrication mismatch. Considering practical applications, a calibration mechanism for maintaining a constant Z_{oc} is necessary [8], [18], [19]. In general, a Z_{oc} calibration mechanism detects output voltage deviation

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Kai-Yu Hu and Chien-Hung Tsai are with the Department of Electrical Engineering, National Cheng Kung University, Tainan City 701, Taiwan (e-mail: s972882@gmail.com; chtsai@ee.ncku.edu.tw).

Chien-Wu Tsai is with the Information and Telecommunication Engineering Department, Ming Chuan University, Taiwan 333, R.O.C. (e-mail: cwtsai@mcu.edu.tw).

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during transient operation and then calibrates the component that affects $Z_{\rm oc}$. In [18], matching between the current sensing gain and equivalent series resistor of the output capacitor on a power stage affected Z_{oc}. So, the autotuning is done by detecting the output voltage settling after load transient and then tuning the current sensing gain accordingly. In [8] and [19], time constant matching between a current sensing filter and inductor on a power stage affected Z_{oc}; accordingly, these studies have proposed a Z_{oc} calibration mechanism that tunes the time constant of the current sensing filter to achieve constant Z_{oc} in COT control. However, the control loops of the system in [8] and [19] are analog control loop, the autotuning algorithm requires extra discrete components, which induce more hardware cost than fully digital implementation.

This article developed a digital V^2 COT control buck converter equipped with AVP and automatic $Z_{\rm oc}$ calibration for future SoC processors. To optimize AVP performance, a second-order digital inductor current sensor (DICS) was implemented to extend the constant $Z_{\rm oc}$ bandwidth. The $Z_{\rm oc}$ calibration mechanism was designed on the basis of a derived small-signal model. Considering all possible uncertainties of $Z_{\rm oc}$, this article established an online automatic calibration mechanism. A prototype chip was fabricated using a 90-nm complementary metal–oxide–semiconductor (CMOS) process. The digital controller is fully equipped with a standard cell library. Compared with analog controllers, the digital controller does not require external passive compensation components and has unique robustness against ambient interference.

The remainder of this article is organized as follows. Section II introduces the architecture and operational principle of the proposed system. Section III presents the design methodology of the AVP control scheme in the proposed system. Section IV describes the proposed automatic $Z_{\rm oc}$ calibration mechanism. Session V presents the measurement results. Finally, Section VI concludes this article.

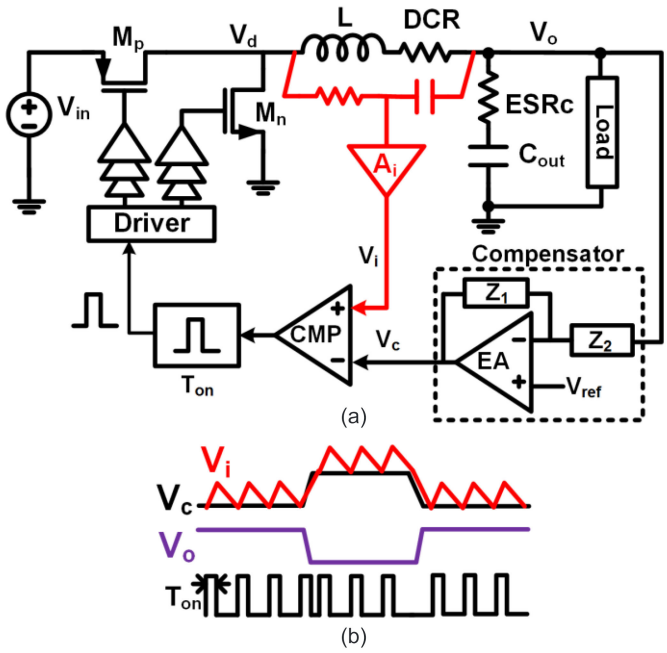

Fig. 1. (a) Block diagram and (b) operational waveform of the analog V^2 COT buck converter equipped with the AVP mechanism.

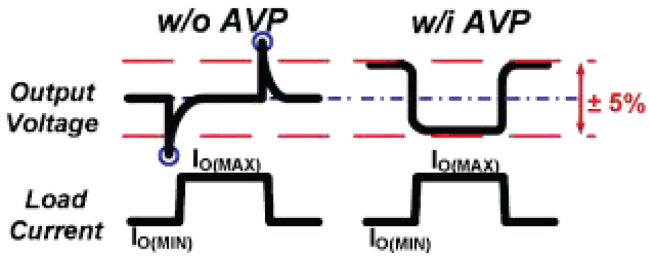

Fig. 2. Output voltage transient waveform with and without the AVP mechanism.

II. Proposed Digital V^2 COT Control Buck Converter With AVP

A. Review of Analog V^2 COT Buck Converter With AVP

Fig. 1(a) illustrates a conventional analog V^2 COT control buck converter equipped with AVP. The controller of the V^2 COT control buck converter comprises an inductor current sensor, a voltage compensator, a comparator, and a COT modulator. During steady-state operation, the output voltage of the compensator is equal to the valley of the sensed inductor current V_i [see Fig. 1(b)]. Consequently, the output voltage is regulated to a particular level, as expressed in (1), where A_i is the inductor current sensor gain and $G_{\rm comp}$ is the dc gain of the compensator. For regulation accuracy, a high gain compensator is required to minimize the output voltage offset caused by the inductor current. For AVP, the desired output voltage level under different load current conditions can be achieved by deriving appropriate A_i and $G_{\rm comp}$ levels.

$$V_o = V_{\rm ref} - I_L \frac{A_i}{G_{\rm comp}} = V_{\rm ref} - I_L R_{\rm LL}. \qquad (1)$$

When AVP is implemented, the output voltage under maximum and minimum load current conditions is set to the upper and lower boundaries of the output voltage window, respectively. Under load current transient conditions, the output voltage deviation occurring when AVP is implemented can be smaller than that observed when AVP is not implemented; this can be attributed to the relatively low target voltage (see Fig. 2). Therefore, AVP can improve transient performance.

B. Proposed Digital V^2 COT Control Buck Converter With AVP

Fig. 3 presents a block diagram of the proposed digital V^2 COT control buck converter. An analog-to-digital converter (ADC) is used for output voltage sampling, and the sampling rate is four times the switching frequency of the buck converter. The digital controller comprises a DICS, digital compensator, comparator, digital COT modulator, and $Z_{\rm oc}$ calibration block. The digital controller is fully equipped with standard cells and a 50-MHz clock. Instead of using a conventional analog inductor current sensor, the controller applies a modified DICS

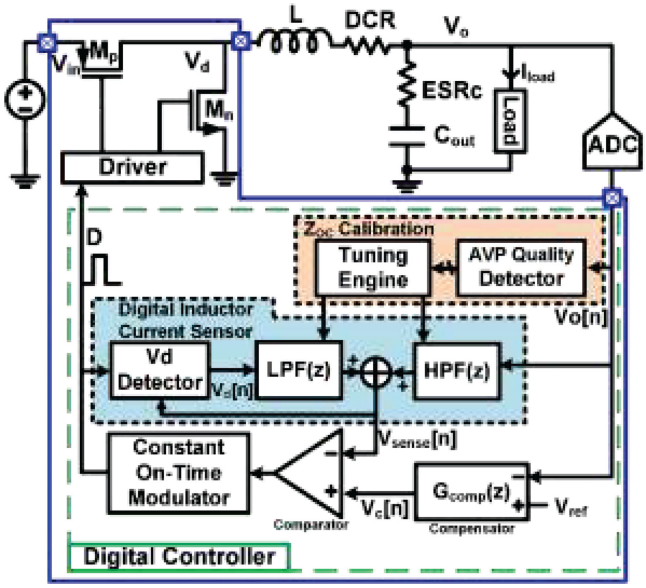

Fig. 3. Block diagram of the proposed digital V^2 COT buck converter.

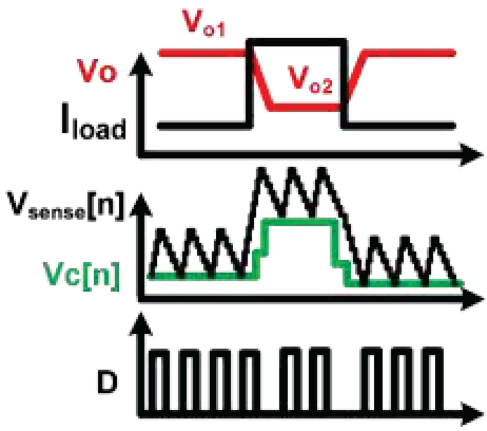

Fig. 4. Key operation waveform.

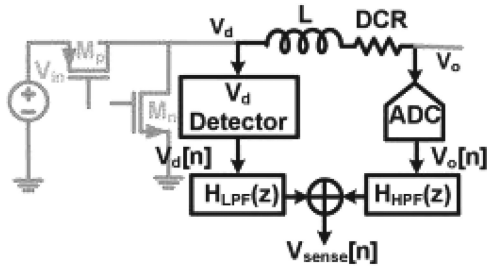

Fig. 5. DICS.

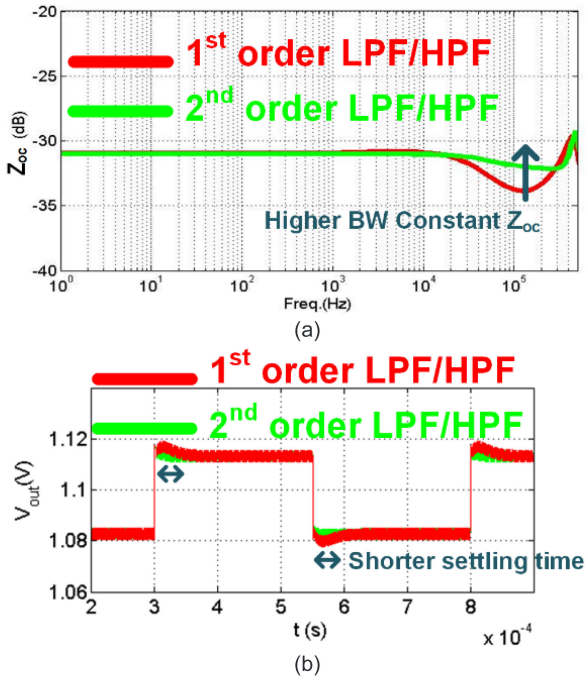

Fig. 6. (a) Z_{oc} simulation and (b) load transient simulation with different ordered LPF/HPF in the DICS.

that comprises a V_d detector, a second-order low-pass filter (LPF), and a second-order high-pass filter (HPF) to support the wide-bandwidth AVP design. Because AVP performance depends on Z_{oc}, the Z_{oc} calibration block calibrates Z_{oc} when this impedance is not a constant due to aging or variations in power stage components. Section IV presents the detailed operating mechanism and implementation of Z_{oc} calibration states.

Fig. 4 displays the key operating waveforms of the proposed digital V^2 COT control buck converter when Z_{oc} calibration is disabled. AVP for COT control is achieved by comparing the output of the digital compensator ($V_c[n]$) with the output of the DICS ($V_{sense}[n]$); a COT control pulse (D) appears whenever $V_c[n]$ is equal to the $V_{sense}[n]$ valley. $V_{sense}[n]$ changes according to the load current (I_{load}). Moreover, $V_c[n]$ tends to be inversely proportional to the output voltage because of the negative feedback topology. For $V_c[n]$ to follow $V_{sense}[n]$, the output voltage (V_O) should change inversely to I_{load}. Accordingly, the output voltage changes inversely and is eventually regulated at the corresponding output levels (V_{O1} and V_{O2}), which are located in the intended AVP design window. Section III provides a detailed analysis of system stability and the control loop design of the proposed AVP states.

1) Modified DICS: A typical DICS is composed of an LPF, an HPF, and a V_d detector (see Fig. 5). The LPF and HPF are used to formulate the inductor current from the V_o and V_d sampling results. The V_d detector replaces the ADC for V_d sampling. For a general RBC scheme, first-order filters are adequate for inductor current sensing [12]. Comparing with the first-order filter, the second-order filter has extra filter coefficients a_1, b_0, and b_1. Based on the derived Z_{oc}, a_1, b_0, and b_1 can dominate the second-order term of Z_{oc}. Therefore, the Z_{oc} in the high-frequency range can be designed with a_1, b_0, and b_1, which cannot be realized with the first-order filter, and wide constant Z_{oc} bandwidth can be achieved. Fig. 6 presents Z_{oc} and load transient simulation results obtained through SIMPLIS using LPFs and HPFs with different orders. In the simulated DICS,

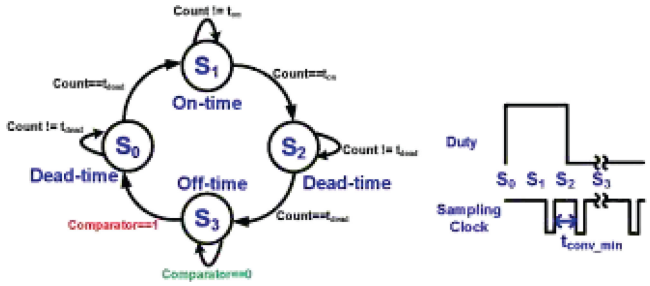

Fig. 7. Digital COT modulator.

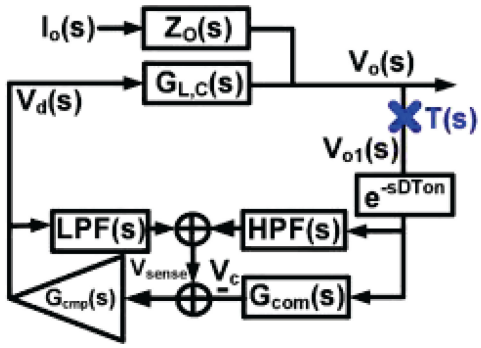

Fig. 8. Control block diagram of the proposed system.

the figure indicates that the application of a second-order LPF and HPF can yield a relatively high constant $Z_{\rm oc}$ bandwidth and faster load transient response compared with the application of a first-order LPF and HPF. Since the output voltage settling can be thought as a current step input to the Z_{oc}, wider constant Z_{oc} bandwidth leads to faster voltage settling based on control theory. Accordingly, the benefit of the DICS with second-order LPF and HPF proposed in this article applies is the ability to extend the constant $Z_{\rm oc}$ bandwidth and further improve transient performance.

On the other hands, considering inductor current sensing, inductor current sensing circuit with the second-order filter can get the signal proportional to inductor current as the conventional inductor current sensing circuit. The derivation of the sensing signal V_s is shown in (2). The sensed signal V_s is the summation of inductor current passes through LPF and the DCR zero and output voltage.

$$V_s(s) \approx i_L(s) \cdot \mathrm{DCR}\left(1 + s\frac{L}{\mathrm{DCR}}\right) \cdot \mathrm{LPF}(s) + V_o(s). \tag{2}$$

2) Digital COT Modulator: The digital COT modulator is a finite-state machine comprising four states (S_0–S_3). Considering a complete switching period, S_0 is the first state, and S_1–S_3 are sequential states. S_0 represents the turn-ON dead time and is triggered when the comparator transmits "1" to the COT modulator. S_1 and S_2 represent the ON-time period and turn-OFF dead time, respectively. S_3 represents the OFF-time period and is terminated when the comparator transmits "1" to the COT modulator. The period of S_0–S_2 is counted by a 50-MHz counter according to the designed value. Moreover, the state machine involves an ADC sampling clock. The first sampling clock is sent at the instant when the state machine reaches three-fourth period of state S_1; subsequently, a fixed sampling interval is established (see Fig. 7).

III. Design of AVP Control

The design of AVP control is based on $Z_{\rm oc}$ derived from the small-signal model. The desired output voltage under different load current conditions, namely "load-line" in VRM specifications, can be designed according to $Z_{\rm oc}$. This section introduces the derivation of the small-signal model and the design of the load line and constant $Z_{\rm oc}$.

A. Small-Signal Model

The small-signal model is derived on the basis of an averaged model [20]. Although the average model cannot well model the small signal behavior in the high-frequency range, it can still well model the small signal in the low-frequency range. And the average model does not need complex mathematic computation such as Fourier transform, the result can be easily simplified for system design. Since the load line design of AVP is based on the low-frequency characteristic of closed-loop output impedance and requires to design many parameters according to the derived model; in this article, the average model is used. Fig. 8 presents the control block diagram of the proposed system; this diagram is based on the system block diagram illustrated in Fig. 3. The V_d-to-output and output impedance transfer functions of the power stage are modeled as $G_{L,C}(s)$ and $Z_o(s)$, in the following equations, respectively:

$$G_{L,C}(s) = \frac{(\mathrm{ESR}_C \cdot Cs + 1)}{L \cdot Cs^2 + (\mathrm{DCR} + \mathrm{ESR}_C) \cdot Cs + 1} \tag{3}$$

$$Z_o(s) = \frac{(Ls + \mathrm{DCR}) \cdot (\mathrm{ESR}_C Cs + 1)}{LCs^2 + (\mathrm{DCR} + \mathrm{ESR}_C)\, Cs + 1} \tag{4}$$

where L, C, DCR, and ESR_C are the inductor, capacitor, dc resistance (DCR) of the inductor, and equivalent series resistance (ESR) of the capacitor on the buck power stage, respectively.

A DICS senses the inductor current by filtering the switch node signal V_d through the LPF and filtering the output voltage V_o through the HPF. The sensing result is the summation of the outputs of the LPF and HPF. Therefore, a DICS can be modeled to include the LPF(s), HPF(s), and summation block. The DICS in the proposed system adopts second-order filters, and the transfer functions for the LPF and HPF are presented in the following equations, respectively:

$$\mathrm{LPF}(s) = \frac{b_0 \cdot s + 1}{a_1 \cdot s^2 + a_2 \cdot s + a_3} \tag{5}$$

$$\mathrm{HPF}(s) = \frac{b_1 \cdot s^2 + b_2 \cdot s}{a_1 \cdot s^2 + a_2 \cdot s + a_3}. \tag{6}$$

A COT modulator and comparator can be modeled to have an infinite gain [21], and the corresponding transfer function is expressed in (7). The proposed system includes a proportional-type compensator, and (8) presents the corresponding transfer

function.

$$\mathrm{G_{cmp}\,(s)} = A|_{A\to\infty} \tag{7}$$

$$\mathrm{G_{comp}\,(s)} = k. \tag{8}$$

Considering the operating principle of digital COT modulators, output voltage variations can be neglected during the ON-time period and hold phase of the ADC. The sampling process of the ADC is designed as described in Section II-B, and the sampling interval is shorter than the ON-time period. Thus, the ON-time period should be considered in the determination of the delay of a digital COT modulator. The delay of a digital COT modulator can be modeled as indicated in the following:

$$T_D\,(s) = e^{-\mathrm{DT_{on}}s}. \tag{9}$$

According to the control block diagram, control loop transfer functions *T(s)* and Z_{oc} can be derived as (10) and (11), respectively. To design the desired load line of AVP control, Z_{oc} can be further simplified as (12)

$$T\,(s) = \frac{V_o\,(s)}{V_{o1}\,(s)} = G_{L,C}\;(s)\cdot\frac{\mathrm{HPF}\,(s) - G_{\mathrm{com}}\,(s)}{\mathrm{LPF}\,(s)}e^{-s\mathrm{DT_{on}}} \tag{10}$$

$$Z_{oc}\,(s) = \frac{V_o\,(s)}{I_o\,(s)} = \frac{Z_o\,(S)}{1+T\,(s)} \tag{11}$$

$$Z_{oc}\,(s) \approx \frac{Lb_0s^2 + Ls + \mathrm{DCR}}{(ka_1+b_1)s^2 + (b_2+ka_2)s + (1+ka_3)}. \tag{12}$$

B. Load Line

Generally, load-line analysis for AVP control is based on the dc condition ($s = 0$) of the applied small-signal model. The output voltage and DICS results can be expressed as the following equations, respectively:

$$v_o\,(s) = G_{L,C}\;(s)\cdot v_d\,(s) - Z_{oc}\,(s)\cdot i_o\,(s) \tag{13}$$

$$v_{\mathrm{sense}}\,(s) = \mathrm{LPF}\,(s)\cdot v_d\,(s) + \mathrm{HPF}\,(s)\cdot v_o\,(s). \tag{14}$$

Under a steady-state condition, V_{sense} should be equal to the reference voltage V_{ref} when the ripple on V_{sense} is neglected. The output voltage under different load conditions can be derived as (15) by substituting (13) into (14) under a dc condition; this voltage can also be further simplified as (16).

$$v_{\mathrm{sense}}\,(0) = V_{\mathrm{ref}} \Rightarrow \left(\frac{\mathrm{LPF}\,(0)}{G_{L,C}\,(0)} + \mathrm{HPF}\,(0)\right)V_o\,(0) + \left(\frac{\mathrm{LPF}\,(0)\cdot Z_{oc}\,(0)}{G_{L,C}\,(0)}\right)I_o\;(0) = V_{\mathrm{ref}} \tag{15}$$

$$V_o = a_3\,V_{\mathrm{ref}} - \frac{\mathrm{DCR}}{1+ka_3}I_o. \tag{16}$$

According to (15), the load line can be designed by selecting an appropriate compensator gain k, filter coefficient a_3, and DCR. With k and a_3, the load-line specification is not limited by the value of DCR. Therefore, flexible load-line design can be achieved in this article. Take 0.1 Ω load line with 0.5 Ω inductor DCR, for example, the compensator gain can be 4 and the a_3 can be 1. Furthermore, the filter coefficient a_3 can be used to determine the output voltage under no-load conditions, and the output voltage can be changed by tuning a_3 without modifying the reference voltage. The compensator gain k and DCR can be used to determine the AVP window.

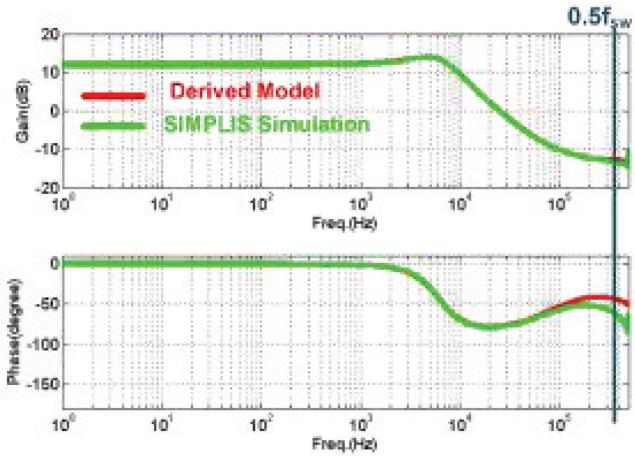

Fig. 9. Bode plot of the derived control loop transfer function and SIMPLIS simulation results.

C. Constant Z_{oc} Design

To achieve optimal AVP control performance, designing a constant Z_{oc} within the specified control bandwidth is necessary. Mathematically, the constant Z_{oc} can be designed by choosing the numerator coefficient and denominator coefficient of (12), which meets (17). According to (17), in the proposed system, Z_{oc} can be derived by selecting a filter coefficient and compensator dc gain as follows. a_3 and k relate to load line and the no-load output voltage as (16). And k also relates to the control loop stability. So, a_3 is chosen with target no-load output voltage (1.01 V in this article), k is chosen via control-loop stability analysis (4 in this article). a_1, a_2, b_0, b_1, and b_2 can be designed with a simple design guideline $a_1 = b_1 = a_2 \times 10^{-5}$ to meet (17) by assigning a_2. And the design of R_{LL} should take a particle DCR value, which includes DCR of inductor and parasitic resistance of PCB trace, wire bonding, IC package and socket into consideration among different implementation platform. Consequently, Z_{oc} becomes constant as R_{LL} in the frequency range of the small-signal model.

$$\frac{Lb_0}{ka_1+b_1} = \frac{L}{b_2+ka_2} = \frac{\mathrm{DCR}}{1+ka_3} = R_{\mathrm{LL}}. \tag{17}$$

To verify the derived functions, Fig. 9 displays bode plots for the derived control-loop transfer function and SIMPLIS simulation results, and Fig. 10 displays bode plots for the derived Z_{oc} transfer function simulation and SIMPLIS simulation results; the simulation parameters are presented in Table I. Considering particle implementation, the DCR in Table I includes DCR of inductor and parasitic resistance of PCB trace, wire bonding, IC package and socket. The ESR_C in Table I includes ESR_C of capacitor and parasitic resistance of PCB trace. The derived transfer function matches the SIMPLIS simulation results. The results for the control-loop transfer function (see Fig. 9) indicate

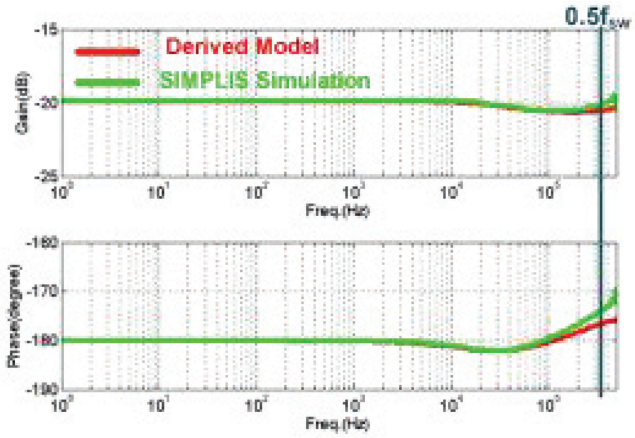

Fig. 10. Bode plot of the derived Z_{oc} transfer function and SIMPLIS simulation results.

TABLE I
SPECIFICATION AND DESIGN PARAMETER OF PROPOSED SYSTEM

Parameter	Value	Parameter	Value
V_{in}	3.3V	f_{sw}	500 kHz
V_{ref}	1.1V	T_{on}	660 ns
C	66 µF	I_o	0-1A
ESR_C	0.03 Ω	k	4
L	10 µH	a_3	1.01
DCR	0.5 Ω	R_{LL}	0.1Ω

a stable control loop exhibiting a 90° phase margin and obviating extra compensation. The results for the Z_{oc} transfer function (see Fig. 10) indicate that when (17) is applied, a constant Z_{oc} can be derived in the control bandwidth; additionally, the derived transfer function matches the SIMPLIS simulation results.

IV. AUTOMATIC CLOSED-LOOP OUTPUT IMPEDANCE CALIBRATION

Deriving a constant Z_{oc} becomes particularly difficult when the variation and aging of power stage components, including inductance, are considered. According to (12), the inductance and parasitic DCR of an inductor influence the characteristics of Z_{oc}. Hence, in practical applications that involve inductor uncertainty and variations, achieving a constant Z_{oc} and optimal AVP is not possible. A nonoptimal AVP design can degrade load transient performance, thereby resulting in extra voltage undershoot/overshoot and a long settling time. Accordingly, the proposed system includes a Z_{oc} calibration block to achieve online and real-time Z_{oc} calibration automatically and, thus, accomplish optimal AVP.

Fig. 11(a) illustrates bode plots of possible Z_{oc} uncertainty conditions induced by inductance and DCR variations in the proposed system. In practical implementation, the possible variation on inductance is about +/–20% and is only component dependent, which can well estimate in the design phase. The possible variation on DCR is about +/–50% and depends on several factors such as PCB trace, IC package, and so on. Fig. 11(b) presents the corresponding load transient simulation results

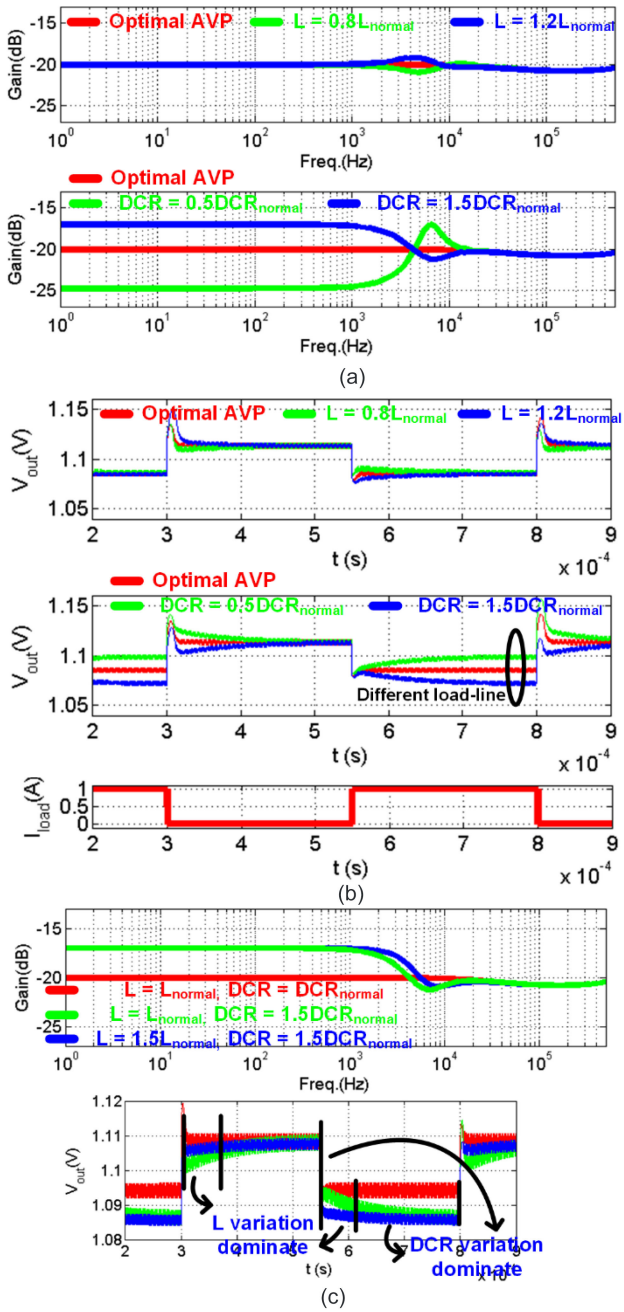

Fig. 11. (a) Z_{oc} bode plot and (b) load transient simulation results under different inductance and DCR variation conditions. (c) Comparison between different variation conditions.

for each Z_{oc} uncertainty condition. The inductance variation reduces the constant Z_{oc} bandwidth, and during load transient operation, the output voltage settling time increases and exceeds the original time. However, the load-line characteristic is not influenced, and the output voltage remains within the desired AVP window. Therefore, inductance variation is not a critical problem for Z_{oc} calibration. By contrast, the DCR variation not only reduces the constant Z_{oc} bandwidth but also changes the Z_{oc} value in the low-frequency range. During load transient operation, the output voltage settling time increases and exceeds

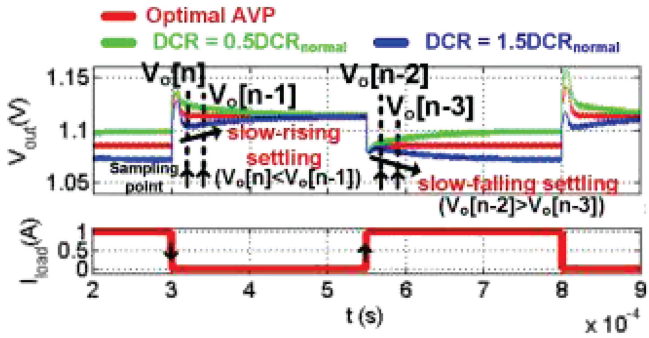

Fig. 12. Output voltage transient simulation results under different DCR variation conditions.

TABLE II
SUMMARY TABLE OF CALIBRATION MECHANISM

Condition	Vo settling @step-down load	Vo settling @step-up load	Calibration
DCR ↑	increasingly	decreasingly	T > 0
DCR ↓	decreasingly	increasingly	T < 0

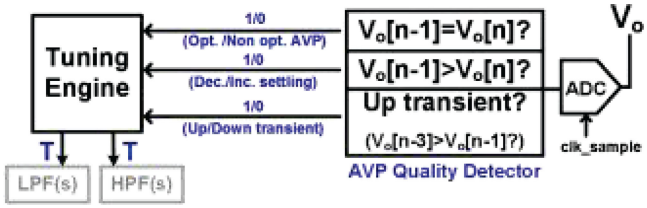

Fig. 13. Hardware implemented inside the Z_{oc} calibration block.

the original time, and the load-line characteristic changes. The output voltage can no longer remain within the desired range. Therefore, Z_{oc} calibration should be implemented to resolve the DCR variation. When both the inductance variation and DCR variation occur at the same time, the influence of each variation occurs simultaneously. According to the simulation results under all possible variation conditions, the inductor variation affects the bode plot mainly in the high-frequency range and affects output voltage right after the load transient only. On the other hand, the DCR variation affects the bode plot mainly in the low-frequency range and also affects the output voltage in the interval which output voltage gradually settles to target voltage. Since inductance variation and DCR variation affect different parts of the bode plot and output voltage, as shown in Fig. 11(c), the output voltage settling after load transient still approximates to the DCR variation condition. Therefore, the DCR variation is still the main issue that should be dealt with.

The output voltage settling tendency after load transient operation clearly reflects Z_{oc} variation (see Fig. 12). Two possible cases can explain this phenomenon: DCR decreases and becomes smaller than the original value, and DCR increases and becomes larger than the original value. When DCR decreases, the output voltage settles to the target voltage and tends to decrease slowly after step-down load transient operation and increase slowly after step-up load transient operation. When DCR increases and becomes larger than the original value, the output voltage settles to the target voltage and tends to increase slowly after step-down load transient operation and decrease slowly after step-up load transient operation. When both the inductance variation and DCR variation occur at the same time, the output voltage settling tendency after load transient operation still reflects DCR variation because the inductor variation affects output voltage right after the load transient only.

Considering the design methodology for constant Z_{oc} (16), when DCR changes, the proportion of DCR to $(1 + ka_3)$ varies simultaneously. Because a_3 is a constant in the denominator polynomial of the LPF and HPF in the DICS, calibration can be performed by modifying this constant as $(a_3 + T)$, where T is the tuning coefficient obtained from the calibration block according to the DCR condition. Furthermore, the DCR condition can be obtained according to the tendency of the output voltage to settle after load transient operation. Therefore, calibration can be executed by first detecting the output voltage after load transient operation and then selecting the tuning coefficient. Table II presents the output voltage settling tendency and tuning coefficient of the corresponding DCR variation condition. The Z_{oc} transfer function with the calibration mechanism is expressed as follows:

$$Z_{oc}(s) \approx \frac{Lb_0 s^2 + Ls + \mathrm{DCR}}{(ka_1 + b_1)s^2 + (b_2 + ka_2)s + [1 + k(a_3 + T)]}. \tag{18}$$

Fig. 13 illustrates the hardware implemented inside the Z_{oc} calibration block. Z_{oc} calibration is executed whenever a load transient status occurs, and the calibration process can be divided into detection step performed by an AVP quality detector and a tuning step performed by a tuning engine. The AVP quality detector detects the load transient status and monitors subsequent neighboring $V_o[n]$ data pairs to identify the type of Z_{oc} variation. In practice, two sampling points are sent after the confirmation of a load transient status to derive $V_o[n]$ (see Fig. 12). For example, if the first sampling result is lower than the second sampling result after step-down transient operation, as indicated by the blue line in Fig. 12, the output voltage settles to the target voltage and tends to increase slowly and corresponds to the case in which DCR increases beyond its original value. The AVP quality detector then sends the required tuning signals to control the tuning engine according to the information provided in Table II. For a preset T value, the tuning engine can be easily implemented using a lookup table. Depending on the T value, Z_{oc} is continually tuned until the optimal AVP condition is met; this online real-time calibration procedure may last several load transient periods.

V. EXPERIMENTAL RESULTS

A prototype of the proposed converter was fabricated using a 90-nm 1-V/3.3-V CMOS logic process. Fig. 14 illustrates the die micrograph. The chip area was measured to be 1.85 mm^2, including the pads. The power metal–oxide–semiconductor (MOS) and its drivers were integrated on the chip. The digital controller

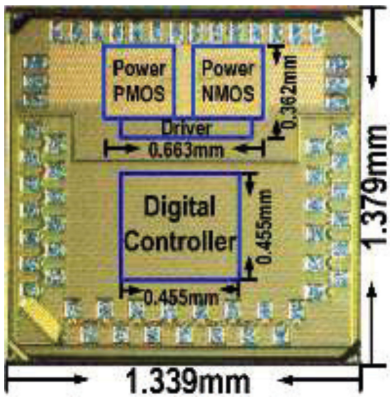

Fig. 14. Die micrograph.

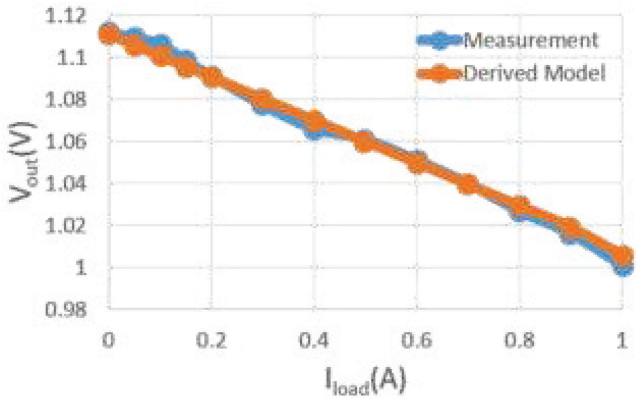

Fig. 15. Measured load-line result at a $V_{\rm in}$ of 3.3 V and $I_{\rm load}$ of 0 to 1 A.

was fully implemented with standard cells. The OFF-chip inductor and capacitor were determined to be 10 μH and 66 μF (22 μF $\times$ 3), respectively. The equivalent ESR of the inductor, including bonding, ceramic quad flat package, socket, and printed circuit board parasitic resistor, was 0.5 Ω. Moreover, an 8-bit 2-MSPS ADC AD7822 [24] was used to sample the output voltage. Table I lists the $T_{\rm on}$, a_3, $V_{\rm ref}$, and k design specifications.

A. Steady-State Measurement

Fig. 15 presents the measured load-line result of the proposed AVP control system. For the 0.5-Ω equivalent DCR, the $R_{\rm LL}$ value was approximately 0.1 Ω. The derived output voltage (16) was consistent with the measured result, and the maximum error was 4 mV, which was determined to be less than the ADC resolution of 7.8125 mV. Figs. 16 and 17 illustrate the steady-state measurement results obtained when $V_{\rm in}$ was 3.3 V and $I_{\rm load}$ was 0 and 900 mA, respectively. V_{gp} represents the gate signal of the high-side power MOS transistor M_p, V_o represents the output voltage of the buck converter, and I_L represents the inductor current of the power stage. With COT modulation, the turn-ON time of M_p was 660 ns. When the load current was 0 A, the output voltage was 1.11 V, with a 1.5 mV ripple, and the switching frequency was 500 kHz. When the load current was

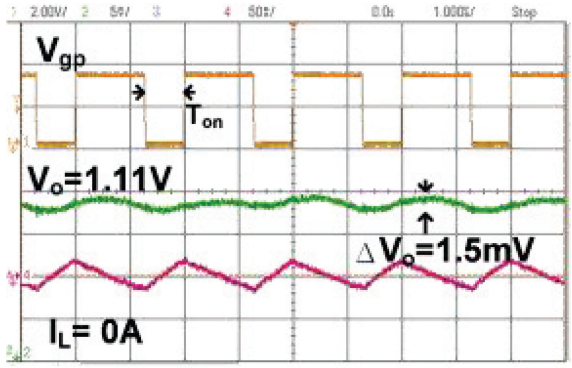

Fig. 16. Steady-state measurement result at a $V_{\rm in}$ of 3.3 V and $I_{\rm load}$ of 0 A.

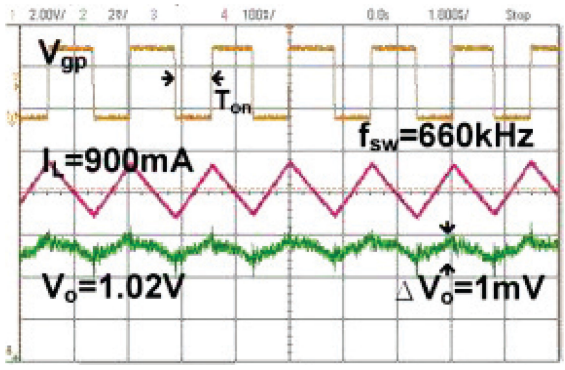

Fig. 17. Steady-state measurement result at a $V_{\rm in}$ of 3.3 V and $I_{\rm load}$ of 900 mA.

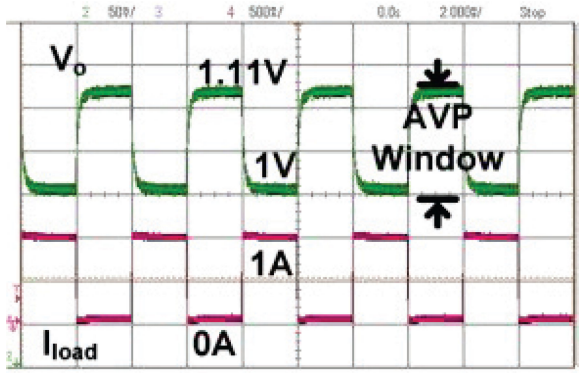

Fig. 18. Load transient measurement result at a $V_{\rm in}$ of 3.3 V and $I_{\rm load}$ of 0 and 1 A.

900 mA, the output voltage was 1.02 V, with a 1 mV ripple, and the switching frequency was 660 kHz.

B. Load Transient Measurement

Fig. 18 shows the load transient measurement results. The input voltage was 3.3 V, and the load current $I_{\rm load}$ changed between minimum (0 A) and maximum (1 A) load conditions. Under the maximum load current transition condition, the output voltage V_o was regulated within the designed 110-mV AVP window.

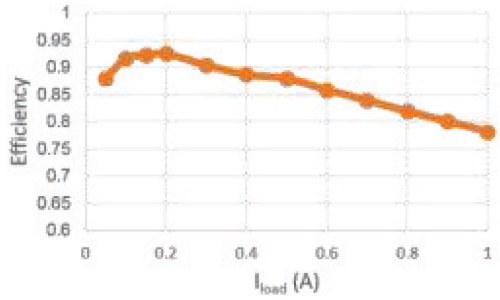

Fig. 19. Efficiency measurement result at a V_{in} of 3.3 V and I_{load} of 0–1 A.

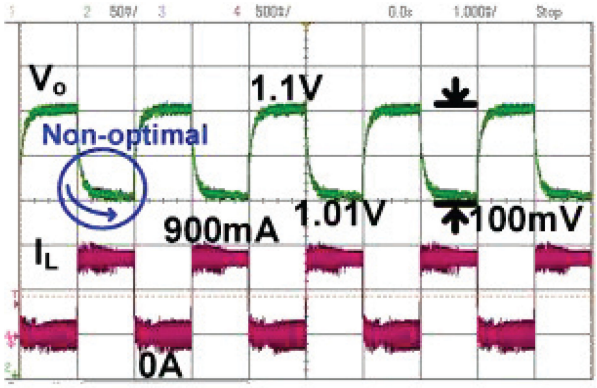

Fig. 20. Load transient measurement result under the nonoptimal AVP condition (DCR is larger than the designed value) and Z_{oc} calibration is not active.

C. Efficiency Measurement

Fig. 19 presents the measured conversion efficiency when the input voltage was 3.3 V and the load current ranged from 0 to 1 A. The maximum efficiency was 92% over the load range. The efficiency curve is measured including the power consumption of the digital controller, driver and power stage loss which includes the loss on inductor, power MOS conduction loss, and switching loss. The power consumption of ADC is not included since the ADC is not integrated on chip. The power consumption of the ADC is 24 mW according to the datasheet of AD7822 [24].

D. Automatic Closed-Loop Output Impedance Calibration Measurement

The first test condition set in the experiment-entailed DCR increasing beyond the specified value. Fig. 20 illustrates that the transient measurement results obtained before the calibration mechanism were active. Corresponding to the simulation results displayed in Fig. 12, when DCR was higher than the specified value, the output voltage after the step-up load transient settled and exhibited a tendency to decrease slowly. Furthermore, the AVP window was larger than the target value.

Fig. 21 displays the results obtained after complete calibration. The proposed calibration mechanism continuously detected the output voltage after load transient occurrence and classified the detected variation into different categories. The constant Z_{oc} preset to test the autotuning process was lower than that set

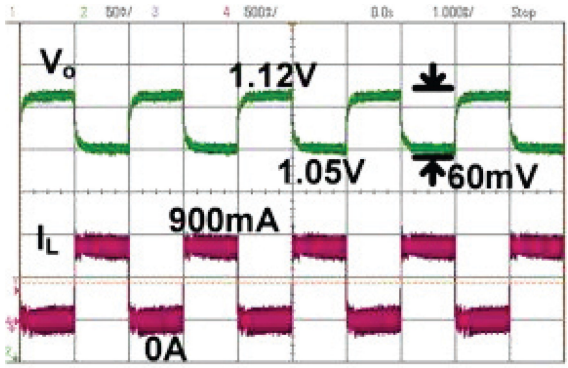

Fig. 21. Load transient measurement result after complete Z_{oc} calibration.

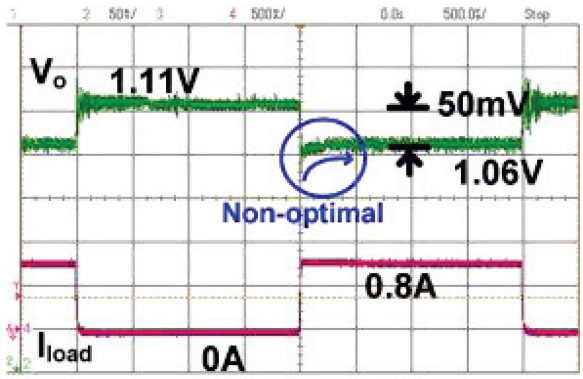

Fig. 22. Load transient measurement result under the nonoptimal AVP condition (DCR is smaller than the designed value) and Z_{oc} calibration is not active.

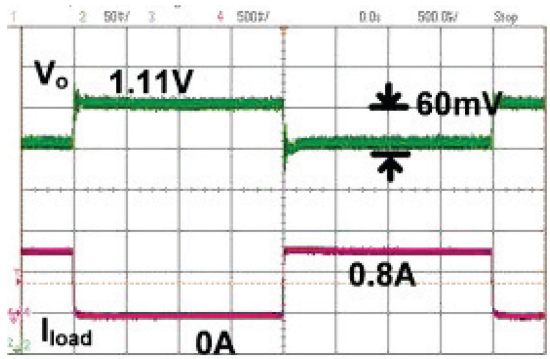

Fig. 23. Load transient measurement result after complete Z_{oc} calibration.

for the actual operating condition (see Fig. 20); therefore, a positive tuning coefficient T was passed to the DICS, and the AVP window shrunk as expected.

The second test condition set in the experiment-entailed DCR decreasing below the specified value. Fig. 22 illustrates that the transient measurement results obtained before the calibration mechanism were active. Corresponding to the simulation results displayed in Fig. 12, when DCR was lower than the specified value, the output voltage after the step-up load transient settled and exhibited a tendency to increase slowly. Furthermore, the AVP window was smaller than the target value.

TABLE III
COMPARISON OF THE PROPOSED AND OTHER MODELS

	TPE 2008 [19]	APEC 2014 [8]	JSSC 2014 [12]	TPE 2014 [15]	IET PE 2016 [18]	This work
Technology	Discrete (STM. L6711)	Discrete (TI TPS59650)	0.13μm CMOS	FPGA	0.18μm CMOS	90nm 1V/3.3V CMOS
Control Methodology	Analog Current mode	Analog COT	Digital Adaptive off-time	Digital COT	Digital Voltage Mode	Digital COT
Inductor Current Sensor	Discrete (R-C filter)	Discrete (R-C filter)	Integrated (1st order DICS)	Integrated (Digital inductor current estimator)	Discrete (LA55-P)	Integrated (2nd order DICS)
AVP	YES	YES	No	YES	YES	YES
Z_{oc} Calibration	YES	YES	-	NO	YES	YES
V_{IN} (V)	12	12	2.0	12	12	3.3
V_O (V)	1.35	1	0.7-1.3	0.85	1.2	1.1
Max I_{load} (A)	N/A	N/A	0.4	N/A	10	1
Switching Freq. (kHz)	300	800	2000	300	300	500
L_O (μH)	0.7	0.36	4.7	0.6	1.5	10
C_O (μF)	15000	792	4.7	660	900	66
Number of ADC	-	-	1	3	2	1

Fig. 23 displays the results obtained after complete calibration. The constant Z_{oc} preset to test the autotuning process was higher than that set for the actual operating condition (see Fig. 22); therefore, a negative tuning coefficient T was passed to the DICS, and the AVP window enlarged as expected.

VI. CONCLUSION

This article presents a digital V^2 COT control buck converter equipped with AVP and automatic Z_{oc} calibration for advanced SoC processors. To confine the output voltage deviation within a desired range, the system executes AVP. A detailed system-level analysis was conducted to design the proposed control architecture. Considering the inevitable variation and aging of power stage components, the proposed system includes an online real-time Z_{oc} calibration mechanism to ensure performance of AVP control. The technical highlights of this article are summarized as follows. Moreover, Table III presents a comparison of the proposed work with state-of-the-art works. First, the proposed system includes an AVP and Z_{oc} calibration mechanism implemented on a chip-level digital COT control buck converter. Additionally, the system includes a second-order DICS for sensing the inductor current without a discrete passive component and for concurrently achieving a constant Z_{oc} within a wide bandwidth.

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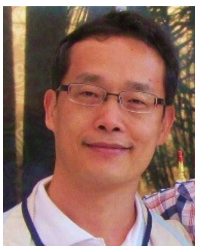
Kai-Yu Hu (Member, IEEE) received the B.S. degree in 2015 from the National Cheng Kung University, Tainan, Taiwan, where he is currently working toward the Ph.D. degree with the Department of Electronic Engineering.

His research interests include fast transient dc–dc converters and digital power management IC design.



Chien-Hung Tsai (Member, IEEE) received the B.S.E.E. degree from the Tatung Institute of Technology, Taipei, Taiwan, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, in 1989 and 1996, respectively.

In 1989, he joined the Design Automation Department of Electronic Research and Service Organization, Industrial Technology and Research Institute, Hsinchu, Taiwan, where he was involved in providing CAD services for mixed-signal design teams. From 1996 to 2001, he served as an Associated Professor and Chairperson with the Department of Electronic Engineering, Lung-Hua University of Science and Technology, Taoyuan, Taiwan. From 2001 to 2004, he served as the Deputy Manager and Director with ALi Inc., Taipei, Taiwan, where he was in charge of designing mixed-signal ICs for optical-drive systems (CD and DVD). Since 2005, he has been with the Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, where he is currently a Professor. His main research interests include mixed-signal and digitally controlled system-on-chip design for power-management applications.

Chien-Wu Tsai received the B.S. degree in computer science and information engineering from the Tatung Institute of Technology, Taipei, Taiwan, in 1987, the M.S.c. degree from the University of Southern California in computer science and information engineering, Los Angeles, CA, USA, in 1992, and the Ph.D. degree in computer science and information engineering from National Taiwan University, Taipei, Taiwan, in 2001.

From 1995 to 2004, he held several teaching positions with the Electronic Engineering Department, Lunghwa University of Science and Technology, Taoyuan, Taiwan. He is currently an Associate Professor with the Department of Information and Telecommunications Engineering, Ming Chuan University, Taoyuan, Taiwan. His current research interests include are as of computer vision, robot control, and video signal processing.