Coupled Three-Phase Converter Concept and an Example: A Coupled Ten-Switch Three-Phase Three-Level Inverter

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***Abstract*—The bridge arms of traditional three-phase multilevel converters are independent of each other; thus, more active switches and passive diodes are required. In order to reduce the number of devices, a coupled three-phase converter architecture, which is suitable for both dc–ac and ac–dc converters, is presented. Based on this architecture, a ten-switch three-phase three-level (10S-3P-3L) inverter is proposed in this article. The proposed topology employs only ten active switches and no additional diodes, which helps to cut size, weight, and costs of system. The proposed space vector modulation enables 10S-3P-3L inverter to operate full modulation indexes. A comparison between the proposed inverter with some existing topologies in terms of device voltage and current stresses, conduction loss, switching loss, and other parameters is made to highlight its excellent performance. Moreover, the experimental results from a 3-kW experimental prototype reveal that the proposed inverter offers superior power quality.**

***Index Terms*—Multilevel inverter, space vector modulation (SVM), three-phase system.**

I. Introduction

In ORDER to meet the requirements for voltage levels and system capacity, three-phase multilevel converters have been adopted in many applications, such as motor drives, photovoltaic power generation, battery energy storage systems, and uninterrupted power supplies [1]. Generally, conventional three-phase converters usually consist of three independent single-phase multilevel converters. These single-phase multilevel converters are independent of each other, and they can output different voltage levels independently [2].

Manuscript received July 12, 2020; revised October 9, 2020; accepted November 2, 2020. Date of publication November 6, 2020; date of current version February 5, 2021. This work was supported in part by the National Natural Science Foundation of China Under Grant 51977069, in part by the Innovative Talents of "High-Level Talent Gathering Project" of Hunan Province, China, Under Grant 2018RS3048, in part by the Natural Science Foundation for Distinguished Young Scholars of Hunan Province, China Under Grant 2020JJ2007, and in part by the First Key Research and Talents Preprogram of Changsha, Hunan Province, China, under Grant kq2004020. Recommended for publication by Associate Editor J. He. *(Corresponding author: Hongliang Wang.)*

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Digital Object Identifier 10.1109/TPEL.2020.3036391

There are three types of classic multilevel converter topologies: neutral point clamped (NPC) [3], flying capacitor (FC) [4], and cascaded H-bridge (CHB) [5]. NPC converters are very popular solutions in the industry because of its excellent performance, such as improved output quality and lower total harmonic distortion (THD) [6]. FC converter using floating capacitor instead of clamping diode is another famous multilevel topology. Different from NPC converters, the regulation of FC voltages is independent, which contributes to simplify balance control strategies of capacitors. CHB converters do not require clamping diodes or FCs, and attain lower component count compared to NPC or FC topologies [5]. They are also the common topologies for high voltage and power applications.

In addition to conventional multilevel topologies, a lot of improved topologies have been proposed in the literature. Derived from NPC topologies, active-clamp NPC (ANPC) [7] and stacked NPC (SNPC) [8] structures are proposed to balance the total losses in power switches under all specified operating conditions (low or high modulation index). The active SNPC converter (ASNPC) [9], which is a derivative of the SNPC structure, is presented to reduce the average switching frequency for the power devices. Furthermore, an improved SNPC is proposed in [10] for solar applications in order to improve the efficiency. The purpose of these topologies is to optimize the system efficiency; however, due to the adoption of additional active switches, the system cost is increased at the same time. In order to overcome the drawback that the conventional inverter can only provide a buck operation, the Z-source inverter has been proposed and become the research hotspot [11], [12]. There are many kinds of Z-source inverter structures, such as three-level Z-source NPC inverter (NPC-ZSI) [13], [14], three-level quasi-Z-source NPC inverter (NPC-qZSI) [15], [16], and three-level modified Z-source NPC (MZS-NPC) inverter [17]. However, due to the existence of the Z-source network, the number of passive components increases greatly, the volume and cost of the system also increase greatly.

As the voltage levels increase, the number of components increases in the multiple of three, and the cost of the system increases at the same time. In order to achieve a balance between system performance and component cost, some reduced component topologies have been proposed successively by experts and scholars over the past few years. Hybrid three-phase cascaded

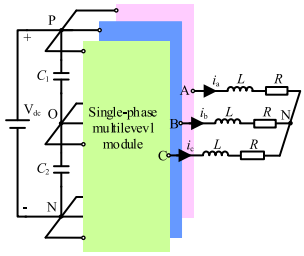

Fig. 1. Independent three-phase converter architecture.

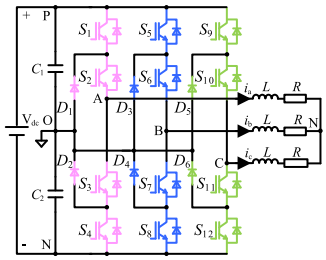

Fig. 2. Type-I: I-type NPC converter.

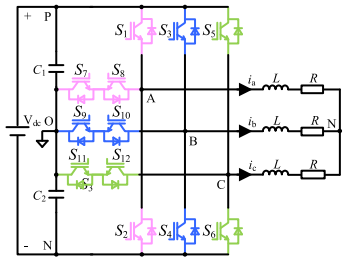

Fig. 3. Type-II: T-type NPC converter.

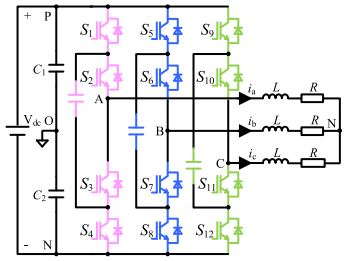

Fig. 4. Type-III: FC-type converter.

multilevel converters are reported in [18] and [19], where the cascaded half-bridge cells are connected with a three-phase voltage source inverter. This has reduced the number of the devices as well as the dc supplies. Unfortunately, a lot of capacitors are still required. A three-phase symmetrical dc-link multilevel converter is proposed in [20], and the number of input dc supplies is found to be nearly 67% less than the similar symmetric half-bridge topologies. At the same time, a three-phase transformer with an operating frequency of 50/60 Hz is still required. A reduced component count three-phase five-level stacked inverter topology is proposed in [21]. Although the number of switches is reduced, complex control algorithms, which require information on load currents and duty cycles, are needed to balance the FC voltages. A 17-level converter is proposed in [22], the drawback is that it is difficult to balance the capacitors. In [23], a three-phase five-level current source inverter that employs only eight active switches is proposed. To enable the high-power operation, a modular multilevel converter is proposed in [24]. Other reduced component count converters have been proposed in [25]–[27].

By analyzing the topologies of three-phase converters with independent bridge arm, this article proposes a coupled three-phase converter architecture concept to reduce the number of components. The proposed architecture is suitable for both dc–ac and ac–dc converters. Based on this architecture, a ten-switch three-phase three-level (10S-3P-3L) topology is proposed, and the same performance as traditional three-phase inverters is obtained with the proposed space vector modulation (SVM) method. The rest of this article is organized as follows. Section II provides the concept of coupled three-phase converter. Section III gives the topology and modulation strategy of 10S-3P-3L inverter. Section IV makes a comparison between some conventional topologies and 10S-3P-3L topology in terms of device stress, losses, and other parameters. Section V gives the experimental results. Finally, Section VI provides the conclusion.

II. Concept of Coupled Three-Phase Converter

Fig. 1 shows the architecture of conventional three-phase multilevel converters, such as I-type NPC, as shown in Fig. 2, T-type NPC, as shown in Fig. 3, and FC-type, as shown in Fig. 4. The dc-link voltage is defined as $V_{\rm dc}$, the dc-link consists of two capacitors (C_1, C_2), whose voltages are rated at a half of dc-link voltage ($V_{\rm dc}/2$). L and R are the loads. $i_{\rm a}$, $i_{\rm b}$, and $i_{\rm c}$ are three-phase current. Three phases, which are represented by blocks of different colors, are independent of each other. In other words, they are composed of three single-phase modules. Thus, the total number of components used in three-phase converter is three times that of a single-phase converter. As the number of levels increases, for example, in the case of five- and seven-level applications, the number of components will increase rapidly, which will increase the cost, volume, and control complexity of the system.

By analyzing the architecture of traditional three-phase converters, the coupled converter concept is proposed for the purpose of reducing the number of components. Coupled converter means that there is a coupling relationship between three bridge arms. The output voltage level state of one bridge arm is related to the other two bridge arms. This relationship is coupled through a common module. The detail architecture of the coupled three-phase multilevel converter is shown in Fig. 5. First, a dc source and two split capacitors are required in the input stage. The power stage is divided into two parts. The first part (common module) includes the common switches. These switches are shared by three bridge arms. The second part (independent module) includes the additional switches, which are owned by each phase. The number of switches in the independent module is far less than that of the traditional independent system after

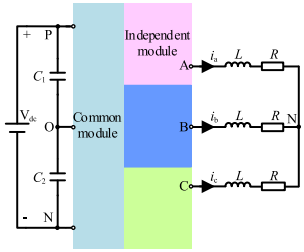

Fig. 5. Coupled three-phase converter architecture.

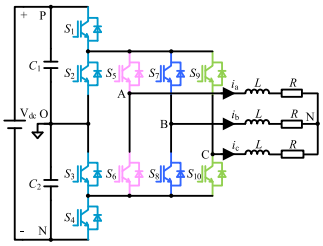

Fig. 6. Proposed 10S-3P-3L inverter.

adding the common module into the power stage. Finally, the total number of the switches is reduced.

III. Operation Principles and Modulation Strategy of 10S-3P-3L Inverter

A. Introduction of the 10S-3P-3L Inverter

According to the coupled three-phase converter architecture, a novel 10S-3P-3L inverter is deduced, as shown in Fig. 6. Clearly, an important feature of the 10S-3P-3L inverter is that it utilizes only ten switches compared to conventional three-phase three-level inverters. Four switches (S_1-S_4) make up the common module and six switches (S_5-S_{10}) make up the independent module. Among the six switches, phase A consists of S_5 and S_6, phase B consists of S_7 and S_8, and phase C consists of S_9 and S_{10}.

Each phase has a three-level voltage $+V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$, which are defined as 2, 1, and 0, respectively. The switching states are represented here with "xyz," where the numbers of "x," "y," and "z" refer to the corresponding output voltage level of phases A, B, and C, respectively. A total of 21 switching states are obtained by the different switch combinations. All the switching states can be divided into 13 space vectors, including 1 zero vector, 6 small vectors, and 6 large vectors. The switch combinations are represented here with {x, …, y}, where the numbers of "x" and "y" refer to the corresponding ON-switch in different switching states. For instance, switch combination {4, 6, 8, 10} means that the switches S_4, S_6, S_8, and S_{10} are ON, and other switches are all turned OFF. All the space vectors with the corresponding output voltages are categorized in Table I.

Seen from Table I, zero vector has three redundant switching states and they have no influence on the dc-link capacitor voltages. It should be noted that there are six different combinations of switch states 111, which are distinguished by a, b, c, d, e, and f. The output voltage of these six combinations is the same, but the ON-switch is different. There are six small vectors, and each of them has redundant switching states. These redundant switching states have an opposite effect on the capacitor voltages, which leads to the possibility of regulating the dc-link capacitor voltages to a constant value ($V_{\rm dc}/2$). Six large vectors have no redundant switching states, and they also have no influence on the dc-link capacitor voltages.

Fig. 7 further shows 4 equivalent circuits in all the 21 switching states. When S_4, S_6, S_8, and S_{10} are turned ON, all the points A, B, and C are connected with the negative of the dc-link, then switching state 000 is obtained, as shown in Fig. 7(a). Similarly, the equivalent circuits of states 100, 211, and 200 are shown

TABLE I
Switching Combinations for 10S-3P-3L Inverter

Space vectors		Switching states	Switch combinations	dc capacitors C_1	dc capacitors C_2
Zero vector	V_0	000	{4, 6, 8, 10}	-	-
		111a, 111b 111c, 111d 111e, 111f	{2, 3, 5, 8, 10}, {2, 3, 5, 7, 10} { 2, 3, 6, 7, 10}, {2, 3, 6, 7, 9} {2, 3, 6, 8, 9}, {2, 3, 5, 8, 9}	-	-
		222	{1, 5, 7, 9}	-	-
Small vector	V_1	100, 211	{2, 4, 5, 8, 10}, {1, 3, 5, 8, 10}	↑,↓	↓,↑
	V_2	110, 221	{2, 4, 5, 7, 10}, {1, 3, 5, 7, 10}	↑,↓	↓,↑
	V_3	010, 121	{2, 4, 6, 7, 10}, {1, 3, 6, 7, 10}	↑,↓	↓,↑
	V_4	011, 122	{2, 4, 6, 7, 9}, {1, 3, 6, 7, 9}	↑,↓	↓,↑
	V_5	001, 112	{2, 4, 6, 8, 9}, {1, 3, 6, 8, 9}	↑,↓	↓,↑
	V_6	101, 212	{2, 4, 5, 8, 9}, {1, 3, 5, 8, 9}	↑,↓	↓,↑
Large vector	V_7	200	{1, 4, 5, 8, 10}	-	-
	V_8	220	{1, 4, 5, 7, 10}	-	-
	V_9	020	{1, 4, 6, 7, 10}	-	-
	V_{10}	022	{1, 4, 6, 7, 9}	-	-
	V_{11}	002	{1, 4, 6, 8, 9}	-	-
	V_{12}	202	{1, 4, 5, 8, 9}	-	-

Note: "↓" represents capacitor discharging, "↑" represents capacitor charging, and "-" represents no influence on capacitors.

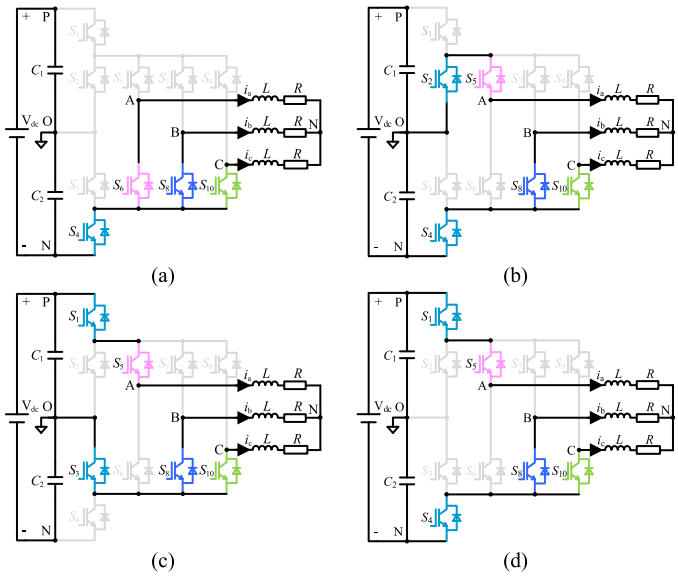

Fig. 7. Example equivalent circuits of different switching states. (a) State: 000. (b) State: 100. (c) State: 211. (d) State: 200.

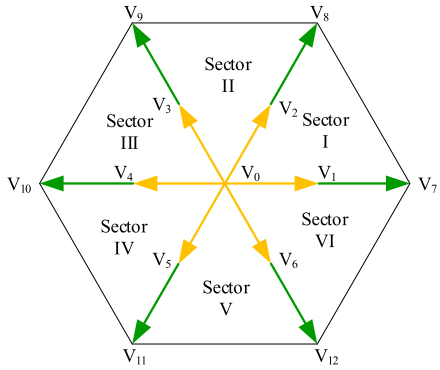

Fig. 8. Space vector diagram of the proposed SVM.

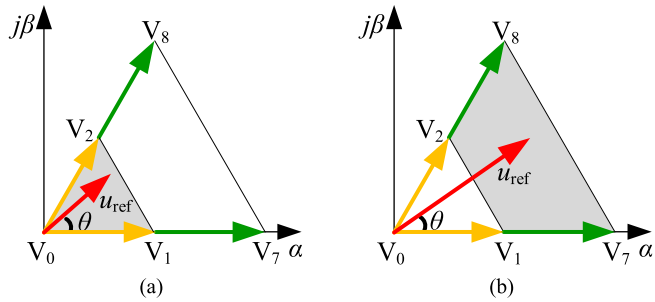

Fig. 9. Synthesis of the reference vector in different regions. (a) Region A. (b) Region B.

in Fig. 7(b), (c) and (d), respectively. It can be seen that all these four switching states have the ability to operate reactive power because all current paths are bidirectional. In addition, the current flowing through the common switch is phase current. For example, the current flowing through S_4 is 0 in Fig. 7(a) when the load is symmetrical. In Fig. 7(b)–(d), the current flowing through S_1, S_2, S_3, and S_4 is i_a. Therefore, the current stress of the common switch will not increase. Other switching states also have the same characteristics, which will not be described in detail here. It should be noted that similar to I-type, T-type, and FC-type, it only works in buck mode and cannot realize soft switching.

B. Modulation Strategy

Since there is a coupling relationship among three bridge arms, it is better to use SVM strategy to operate the proposed inverter. The overall space vector diagram of the proposed inverter is shown in Fig. 8. The whole vector space is divided into six large sectors, each of which occupies 60°.

In order to generate a proper switching signal for each switch, the modulation strategy mainly follows these principles.

1) Always using the nearest voltage vectors to generate the reference vector to reduce the output harmonic.

In order to select the nearest vectors to synthesize the reference vector, each large sector in Fig. 8 is further divided into two small regions. So, the overall space vector diagram is divided into 12 regions.

Sector I in Fig. 8 is considered as a representative example to explain the sector division principle and switching sequence design, as shown in Fig. 9. Three vectors V_0, V_1, and V_2 form the first triangular region, which is defined as Region A in the α-β plane, as shown in Fig. 9(a). u_{ref} is the reference vector, and θ is the phase angle. If u_{ref} locates in this region, then it can be synthesized by these three vectors. The second region, which is defined as Region B, is formed by four vectors V_1, V_2, V_7, and V_8, as shown in Fig. 9(b). If u_{ref} locates in the trapezoidal region, then it can be synthesized by these four vectors simultaneously.

2) Carefully selecting the vector sequence to ensure that the switch is only turned ON or OFF once in each switching cycle to reduce switching losses.

TABLE II
SWITCHING SEQUENCE IN ALL THE 12 REGIONS

Sector	Region	Vector Order						
I	A	110	100	111a	211	111a	100	110
	B	200	100	110	220	221	211	200
II	A	110	111b	221	121	221	111b	110
	B	220	110	010	020	121	221	220
III	A	011	010	111c	121	111c	010	011
	B	020	010	011	022	122	121	020
IV	A	011	111d	122	112	122	111d	011
	B	022	011	001	002	112	122	022
V	A	101	001	111e	112	111e	001	101
	B	002	001	101	202	212	112	002
VI	A	101	111f	212	211	212	111f	101
	B	202	101	100	200	211	212	202

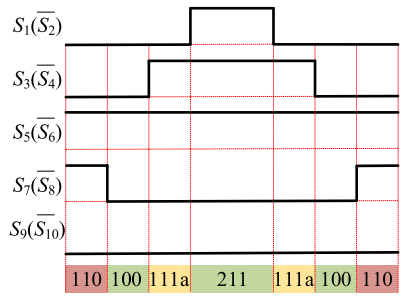

Fig. 10. Switching interval operation in Region A of Sector I.

The vector sequences in all the 12 regions are given in Table II. Seen from Table II, the output voltage of each phase is always switched between two adjacent levels (0 and 1) or (1 and 2) during each large sector. When u_{ref} enters from one large sector to another, the output voltage switched between two nonadjacent voltage levels (0 and 2). However, this situation is only six times in a power frequency cycle, and its contribution to switching loss is very small. Based on Table II, the switching interval operations in Regions A and B of Sector I are shown in Figs. 10 and 11, respectively. It can be seen that switches S_1, S_3, and S_7 are only turned ON and OFF once within one switching cycle in both Regions A and B, and S_5 and S_9 are always ON or OFF. The signals of other switches are complementary to those of the five switches. In other large sectors, only six switches are turned ON and OFF in a switching cycle, so the number of switching actions is similar with the traditional topologies.

TABLE III
VOLTAGE, CURRENT STRESSES, AND AVERAGE SWITCHING FREQUENCY OF FOUR TYPES OF INVERTER

Device	I-type			T-type			FC-type			10S-3P-3L		
	Voltage stress	Current stress	Switching frequency	Voltage stress	Current stress	Switching frequency	Voltage stress	Current stress	Switching frequency	Voltage stress	Current stress	Switching frequency
S_1	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	V_{dc}	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	$I_A/I_B/I_C$	f_S
S_2	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	V_{dc}	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	$I_A/I_B/I_C$	f_S
S_3	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	V_{dc}	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	$I_A/I_B/I_C$	f_S
S_4	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	V_{dc}	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	$I_A/I_B/I_C$	f_S
S_5	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_A	$f_S/3+f_L$
S_6	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_A	$f_S/3+f_L$
S_7	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_B	$f_S/3+f_L$
S_8	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	V_{dc}	I_B	$f_S/3+f_L$
S_9	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	V_{dc}	I_C	$f_S/3+f_L$
S_{10}	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	V_{dc}	I_C	$f_S/3+f_L$
S_{11}	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	-	-	-
S_{12}	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	-	-	-
D_1	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-
D_2	$V_{dc}/2$	I_A	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-
D_3	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-
D_4	$V_{dc}/2$	I_B	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-
D_5	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-
D_6	$V_{dc}/2$	I_C	$f_S/2+f_L/2$	-	-	-	-	-	-	-	-	-

Note: "-" represents not needed.

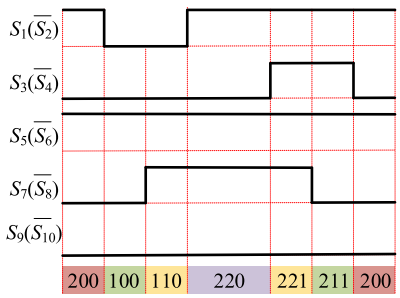

Fig. 11. Switching interval operation in Region B of Sector I.

3) The redundant vectors need to be evenly arranged in each switching cycle to ensure the voltage balance at the midpoint of the dc-link.

The neutral point voltage of the dc-link is balanced by selection proper redundant vectors. In Region A of Sector I, switching states 110 and 100 charge C_1 and discharge C_2, so the neutral point voltage drops. The redundant vector 211 has an opposite effect on the dc-link capacitors that is C_1 is discharged and C_2 is charged. As a result, the neutral point voltage is balanced at a switching frequency. Similarly, in Region B of Sector I, two pair of redundant switching states (100, 211) and (110, 221) are selected, and their effect on the neutral point voltage is also opposite to each other. Therefore, it is possible to regulate the neutral point voltage to a constant value under the full range of modulation indexes.

IV. COMPARISON BETWEEN 10S-3P-3L AND CONVENTIONAL THREE-PHASE THREE-LEVEL TOPOLOGIES

To better illustrate the performance of the proposed topology, it is important to make a comparison between 10S-3P-3L inverter and conventional topologies in terms of device stress, losses, and investment cost.

A. Device Stress and Average Switching Frequency [28]

Table III lists the device stress and average switching frequency for I-type, T-type, FC-type, and 10S-3P-3L topologies. f_S and f_L indicate switching frequency and power line frequency, respectively. Compared to I-type inverter, the voltage stress of S_5-S_{10} for 10S-3P-3L inverter is increased to V_{dc}, which means higher voltage rating devices should be selected for these switches. However, in practical applications, switches S_2, S_3, S_6, S_7, S_{10}, and S_{11} in I-type inverter are generally configured as V_{dc} because the voltage stress on them may be larger than $V_{dc}/2$. Compared to T-type inverter, the number of switches that withstand V_{dc} for 10S-3P-3L inverter is the same as that of T-type. However, the number of switches whose voltage stress is $V_{dc}/2$ is decreased to four. Compared to FC-type inverter, 10S-3P-3L inverter requires more devices, which withstand the voltage stress of V_{dc}. Finally, 10S-3P-3L inverter is better than I-type and T-type inverters and worse than FC-type inverter in terms of device voltage stress.

The current stress of each device for I-type, T-type, and FC-type inverters is phase current I_A, I_B, and I_C (where I_A, I_B, and I_C are the maximum value of i_a, i_b, and i_c, respectively). For 10S-3P-3L inverter, the current flowing through S_1-S_4 may be the phase current, or the sum of two-phase current (such as 100 and 200), or the sum of three-phase current (such as 000 and 222). When the three-phase system is symmetrical, the sum of two-phase current is the negative value of the third phase, and the sum of three-phase current is 0. Thus, the current stress for these four switches is still phase current I_A, I_B, or I_C. The current stress for S_5 and S_6 is I_A, for S_7 and S_8 is I_B, and for S_9 and S_{10} is I_C. Therefore, device current stress of all switches in the four topologies is the same.

The average switching frequency of S_1-S_4 in 10S-3P-3L inverter increases to f_S, thus the switching loss of each of them is larger than that of other types. However, S_1-S_4 can be replaced by high-performance device, such as silicon carbide (SiC)

TABLE IV
TOTAL VAR COMPARISON OF FOUR INVERTERS

	I-type	T-type	FC-type	10S-3P-3L
Total VAR	$9V_{dc}I$	$9V_{dc}I$	$6V_{dc}I$	$8V_{dc}I$

TABLE V
NUMBER OF SWITCHES WITH INCREASED CURRENT STRESS UNDER THREE CASES FOR FOUR TOPOLOGIES

Topologies	I-type	T-type	FC-type	10S-3P-3L
Case I	6	4	4	6
Case II	12	8	8	8
Case III	18	12	12	10

switches to reduce the switching loss. The average switching frequency of S_5-S_8 reduces to $f_S/3+2f_L$, it means the switching loss of each of them is lower than that of other types.

The power electronics topology for a specific application can be evaluated by the total volt-ampere rating (VAR) and power device utilization (PDU) [29]. A good candidate topology for a specific application should have minimized voltages and currents imposed on the semiconductor devices while the transferred power is maximized. The total VAR and the PDU can be defined as follows:

$$\mathrm{VAR} = \sum_{j=1}^{k} V_j I_j \tag{1}$$

$$\mathrm{PDU} = \frac{P_{\max}}{\mathrm{VAR}} \tag{2}$$

where V_j and I_j are the peak voltage and current applied to semiconductor device j, respectively. $P_{\max}$ is the power rating of the inverter.

According to (1), the total VAR of four topologies is obtained in Table IV. It can be seen that the total VAR of 10S-3P-3L topology is lower than that of I-type and T-type topologies, whereas higher than that of FC-type topology

$$\frac{\mathrm{PDU}_{10\mathrm{S}-3\mathrm{P}-3\mathrm{L}}}{\mathrm{PDU}_{\mathrm{I}-\mathrm{type}}} = 112.5\%. \tag{3}$$

Combining (2) and Table IV, the PDU ratio between the 10S-3P-3L topology and the I-type or T-type topology can be calculated as (3). This equation indicates that the PDU of the 10S-3P-3L topology is improved 12.5% compared to the I-type or T-type topology

$$\frac{\mathrm{PDU}_{10\mathrm{S}-3\mathrm{P}-3\mathrm{L}}}{\mathrm{PDU}_{\mathrm{PC}-\mathrm{type}}} = 25\%. \tag{4}$$

Similarly, the PDU ratio between the 10S-3P-3L topology and the FC-type topology can be calculated as (4). It can be seen that the PDU of the 10S-3P-3L topology is lower than that of FC-type topology.

Finally, the total VAR and the PDU performances of the 10S-3P-3L topology are better than that of I-type or T-type topologies and worse than that of FC-type topology.

When the load is unbalanced, the current stresses of some devices may increase. Table V lists the number of switches with increased current stress under different cases for these four topologies. Case I represents that only one output phase current increases, Case II represents that two phase currents increase, and Case III represents that all the three phase currents increase. It is observed that the number of devices of the 10S-3P-3L topology is the same as that of I-type and more than that of T-type and FC-type topologies in Case I. However, in Cases II and III, the number of devices of 10S-3P-3L topology is less than or equal to other topologies. In summary, under unbalance load condition, the current stresses of some devices in all these four topologies will increase. However, the current stress of each device is the same in all these four topologies, and the total number of increased devices is almost the same as well.

B. Conduction and Switching Loss Analysis

Estimation of power losses is critical for predicting the maximum efficiency of power electronic circuits. This section gives a description of conduction and switching losses in the power devices.

During the conduction mode, the insulated gate bipolar transistor (IGBT) collector-emitter voltage drop v_{ce} is approximated as [30]

$$v_{\mathrm{ce}}(t) = v_{\mathrm{ceo}} + R_{\mathrm{c}} i_{\mathrm{c}}(t) \tag{5}$$

where v_{ceo} is the on-state collector-emitter forward voltage-drop and R_{c} is the collector-emitter on-state resistance.

For antiparallel diodes, the voltage drop is calculated as

$$v_{\mathrm{F}}(t) = v_{\mathrm{Fo}} + R_{\mathrm{F}} i_{\mathrm{F}}(t) \tag{6}$$

where v_{Fo} is the on-state forward voltage drop and R_{F} is on-state resistance

$$P_{\mathrm{con\_IGBT}}(t)\frac{1}{2\pi}\int_0^{2\pi} \left[v_{\mathrm{ce}}(t) i_{\mathrm{c}}(t) d_{\mathrm{sw}}(t)\right] d_{\omega t} \tag{7}$$

$$P_{\mathrm{con\_Diode}}(t)\frac{1}{2\pi}\int_0^{2\pi} \left[v_{\mathrm{F}}(t) i_{\mathrm{F}}(t) d_{\mathrm{F}}(t)\right] d_{\omega t}. \tag{8}$$

The average conduction losses of IGBT ($P_{\mathrm{con\_IGBT}}$) and diode ($P_{\mathrm{con\_Diode}}$) are given as (7) and (8), respectively. i_{c} and i_{F} are the current flowing through switch and diode, respectively, and d_{sw} and d_{F} are the duty cycle of switch and diode, respectively.

The conduction loss calculation method of 10S-3P-3L inverter under the proposed SVM scheme is illustrated by taking switch S_1 as an example. Fig. 12 shows the current flowing through S_1 during a foundation period when the reference locates in Region B. The phase current lags behind phase voltage and a phase angle of φ ($0 < \varphi < \pi/2$). i_{S1} is the current flowing through S_1, and roman numerals represent sectors. According to the switching sequence listed in Table II, the dwell time of each vector and the instantaneous current flowing through S_1 can be obtained. For example, in Region B of Sector I, the switching sequence 200-100-110-220-221-211-200 is selected, as shown in Fig. 12, where t_{x}, t_{y}, t_{z}, and t_{w} are dwell times of the selected vectors. In switching states 200 and 211, the current flowing through S_1 is i_{a}, and the dwell times are t_{x} and $t_{\mathrm{y}}/2$, respectively. In switching states 220 and 221, the current flowing through S_1 is $-i_{\mathrm{c}}$, and the dwell times are t_{w} and $t_{\mathrm{z}}/2$, respectively.

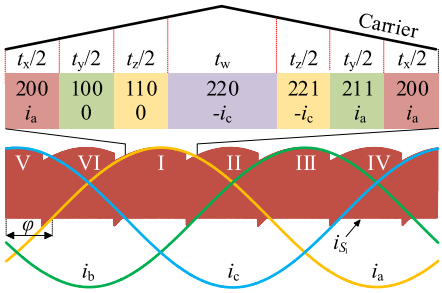

Fig. 12. Scheme diagram of conduction loss calculation for S_1.

When $\varphi \leq \pi/6$, both i_a and $-i_c$ are positive, they flow through S_1, and the conduction loss in Region B of Sector I can be written as follows, according to (7):

$$P_{\text{con\_}S_1\_I} = \frac{3}{\pi}\int_{\frac{\pi}{2}}^{\frac{5\pi}{6}} \begin{bmatrix} v_{\text{ce}}(t) i_a(t)\left(d_x + \frac{d_y}{2}\right) \\ +v_{\text{ce}}(t)(-i_c(t))(d_w + \frac{d_z}{2}) \end{bmatrix} d(\omega t) \quad (9)$$

where $d_x = t_x/T_s$, $d_y = t_y/T_s$, $d_z = t_z/T_s$, $d_w = t_w/T_s$, and T_s is the switching period.

When $\varphi > \pi/6$, i_a flows through S_1, $-i_c$ flow through S_1 during $[\pi/3+\varphi, 5\pi/6]$ while through the antiparallel-diode of S_1 during $[\pi/2, \pi/3+\varphi]$. Thus, the conduction loss is divided into two parts as written as follows, according to (7) and (8):

$$P_{\text{con\_}S_1\_I} = \frac{3}{\pi}\int_{\frac{\pi}{2}}^{\frac{\pi+\varphi}{3}} \begin{bmatrix} v_{\text{ce}}(t) i_a(t)\left(d_x + \frac{d_y}{2}\right) \\ +v_F(t)\left|-i_c(t)\right|(d_w + \frac{d_z}{2}) \end{bmatrix} d(\omega t) + \frac{3}{\pi}\int_{\frac{\pi+\varphi}{3}}^{\frac{5\pi}{6}} \begin{bmatrix} v_{\text{ce}}(t) i_a(t)\left(d_x + \frac{d_y}{2}\right) \\ +v_{\text{ce}}(t)\left|-i_c(t)\right|(d_w + \frac{d_z}{2}) \end{bmatrix}. \quad (10)$$

The conduction loss in other sectors can be obtained in the same way, and the total conduction loss of S_1 during a fundamental period can be expressed as the average value of the conduction loss in six sectors, as shown as follows. The conduction loss for other switches is derived in a similar way

$$P_{\text{con\_}S_1} = \frac{1}{6}\sum P_{\text{con\_}S_{i\_}i}, (i = \text{I}, \text{II}, \ldots, \text{VI}). \quad (11)$$

The switching loss comparison can be obtained by using the switching loss function under the same peak value of phase current, switching frequency, and different switching sequences of same seven segment [31]. Assuming that the OFF-state voltage (V_{off}) of switches would maintain constant during the current transition, the average switching loss ($P_{\text{sw·IGBT}}$) of switches over the fundamental cycle T_s of any phase can be calculated as

$$P_{\text{con\_IGBT}} = \frac{1}{2\pi}\frac{V_{\text{off}}(t_{\text{on}} + t_{\text{off}})}{2T_s}\int_0^{2\pi} f_i(\theta) d\theta \quad (12)$$

where t_{on} and t_{off} are turn ON and OFF time of IGBTs. $f_i(\theta)$ can be written as follows and it equals 0 when the switch has no action in one switching cycle, i is the phase current, and S denotes the switch is switched or not:

$$f_i(\theta) = \begin{cases} |i|, & S = 1 \\ 0, & S = 0. \end{cases} \quad (13)$$

TABLE VI
KEY PARAMETERS OF SWITCHES

Devices	v_{ceo}/V	R_c/mΩ	V_{Fo}/V	R_F/mΩ	t_{on}/ns	t_{off}/ns	Q_{rr}/uC
IKW40N60	0.8	24.33	0.895	23.26	48	249	1.7
IKW40N120	1	25.75	1.165	23.26	78	414	4.3

TABLE VII
COMPARISON WITH EXISTING TOPOLOGIES

	a		b	c	d	e	f
	V_{dc}	$V_{\text{dc}}/2$					
I-type NPC	0	12	6	1	0	0	2
T-type NPC	6	6	0	1	0	0	2
FC-type	0	12	0	1	3	0	2
3L-CHB [33]	12	0	0	3	0	0	3
3L-ANPC [8]	0	18	0	1	0	0	2
3L-SNPC [9]	0	18	6	1	0	0	2
3L-ASNPC [10]	0	24	0	1	0	0	2
Improved SNPC [11]	0	24	18	1	0	0	2
NPC-ZSI [14]	0	12	8	1	0	2	4
MZS-NPC [18]	0	12	9	1	0	2	4
10S-3P-3L	6	4	0	1	0	0	2

Note: a: No. of switches. b: No. of diodes. c: No. of dc sources. d: No. of FCs. e: No. of dc inductors. f: No. of dc capacitors.

TABLE VIII
PARAMETERS OF 10S-3P-3L INVERTER

Parameters	Symbols	Values
Power rating	P	3 kW
Input voltage	V_{dc}	400 V
Filter inductor	L_F	6 mH
Filter capacitor	C_F	4.7 uF
Switching frequency	f_s	6 kHz
Devices	S_1–S_4	IKW40N60
	S_5–S_{10}	IKW40N120

For diodes, only the reverse recovery loss is taking into consideration, which is expressed by

$$P_{\text{sw\_Diode}} = \frac{1}{2\pi}\frac{Q_n V_R}{\sqrt{2 I_F T_S}}\int_0^{2\pi} i_F d\theta \quad (14)$$

where Q_{rr} and V_{R} are diode reverse recovery charge and reverse voltage, respectively.

To analyze the loss of 10S-3P-3L inverter and modulation scheme, two commercially available IGBTs are considered. Their voltage ratings are 600 and 1200 V, respectively, and current ratings are 40 A. The key parameters of the selected IGBTs are list in Table VI.

Based on these, a comparison between I-type, T-type, FC-type, and 10S-3P-3L topologies is conducted in terms of losses. In order to show the relationship of losses for different topologies, the loss ratio functions P_{10S}/P_I, P_{10S}/P_T, and P_{10S}/P_{FC} are defined, where P_{10S}, P_I, P_T, and P_{FC} are the total loss of 10S-3P-3L, I-type, T-type, and FC-type topologies.

Fig. 13 shows the total losses comparison of four topologies under the uniform parameters listed in Table VIII at different modulation index (m) and power factor (PF) angle (φ). Fig. 13(a)–(c) shows the results of P_{10S}/P_I, P_{10S}/P_T, and P_{10S}/P_{FC}, respectively. As can be seen from Fig. 13(a) that the ratio P_{10S}/P_I changes little with m, and it changes sinusoidal

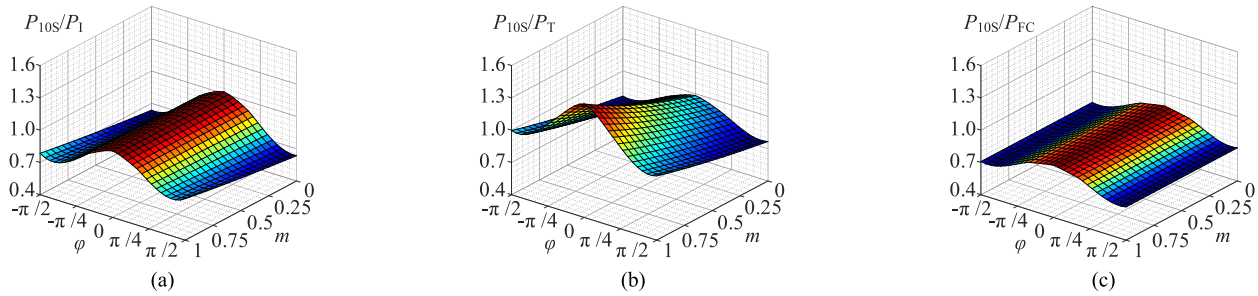

Fig. 13. Losses comparison. (a) P_{10S}/P_I. (b) P_{10S}/P_T. (c) P_{10S}/P_{FC}.

roughly with φ. The maximum value of the ratio is 1.017, which appears when $\varphi = 0$ and $m = 1$. As $|\varphi|$ increases, the ratio decreases, and the minimum value of 0.65 appears at $\varphi = \pm\pi/2$ and $m = 0$. In most ranges of φ, the ratio is less than 1, so the loss of the 10S-3P-3L is less than I-type inverter in most ranges of φ. For the ratio of P_{10S}/P_T, it is greater than 1 at high modulation index and less than 1 at low modulation index. This is because the conduction loss of the T-type inverter is smaller than the other topologies. The maximum value of the ratio is 1.4 when $\varphi = 0$ and $m = 1$ and the minimum value is 0.77 when $\varphi = \pm\pi/2$ and $m = 0$. For the ratio P_{10S}/P_{FC}, it is smaller than 1 at all φ and m. Finally, it can be concluded that in most cases, the loss of 10S-3P-3L inverter is less than that of I-type and FC-type inverters but greater than that of T-type inverters.

C. Comparison With Other Existing Topologies

Table VII presents a comparison of 10S-3P-3L inverter with several existing topologies in terms of component count, supply configuration.

Compared with conventional NPC topologies, the total number of switches and diodes for 10S-3P-3L inverter is reduced. The capacitors in the FC-type topology are three in number, storing high amounts of energy, translating to increased size, weight, and cost with reduced reliability. The three-level CHB (3L-CHB) requires three independent dc power supplies, suitable for battery energy storage and photovoltaic power generation applications. The improved three-level NPC topologies exhibit significant advantages in terms of device loss distribution and system efficiency improvement. However, these performance improvements are achieved at the cost of increased system cost. For example, the topologies 3L-ANPC, 3L-SNPC, and 3L-ASNPC construct redundant switching states by adding additional switches and diodes, and then the total loss is distributed to each device evenly. The improved SNPC topology adopts a hybrid parallel connection of IGBT and CoolMosfet to provide additional current paths for alleviating the power losses. However, this also resulted in twice the active switches investment compared with conventional topologies. Although Z-source inverters, such as NPC-ZSI and MZS-NPC, have the ability to step up the output voltage, they introduce more passive components in the input stage, which will lead to a sharp increase in system size and cost. Therefore, the proposed topology has excellent advantages in terms of system cost.

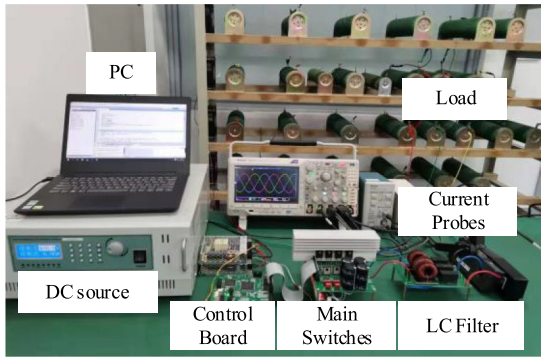

Fig. 14. Experimental prototype of 10S-3P-3L inverter.

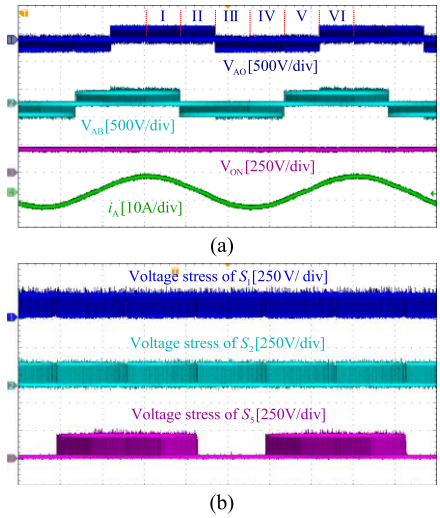

Fig. 15. Experimental waveforms when $m = 0.4$ and $\varphi = 0$. (a) Output voltages and current. (b) Voltage stresses of S_1, S_2, and S_5.

V. Experiment Verification

In order to verify the feasibility of 10S-3P-3L inverter, the experimental prototype, which is shown in Fig. 14, is built and the static and dynamic tests are carried out. The parameters are reported in Table VIII. The control system is implemented in a digital signal processor (TMS320F28335) plus a field programmable gate array (Altera EP2C8Q208) platform.

Figs. 15 and 16 show the experimental waveforms when $m = 0.4$ and $m = 0.95$ under unite power condition, the load resistor

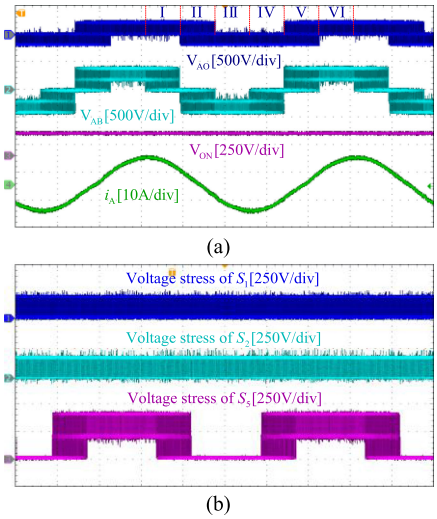

Fig. 16. Experimental waveforms when $m = 0.95$ and $\varphi = 0$. (a) Output voltages and current. (b) Voltage stresses of S_1, S_2, and S_5.

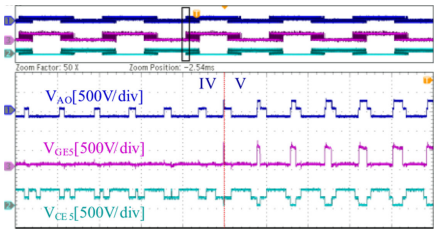

Fig. 17. Detailed waveforms in Sectors IV and V.

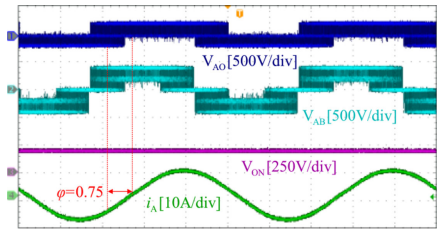

Fig. 18. Experimental waveforms under resistance–inductance condition $m = 0.95$ and $\varphi = 0.66$ (PF = 0.79).

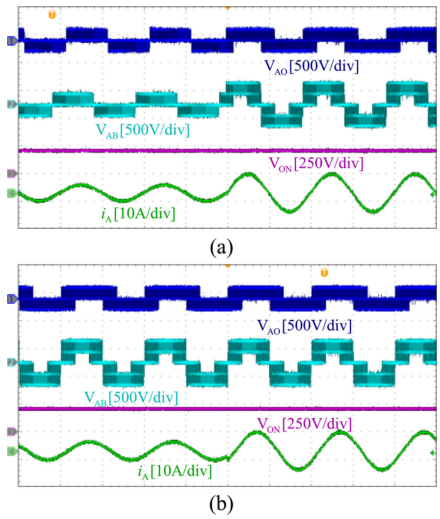

Fig. 19. Transient response of 10S-3P-3L inverter. (a) Sudden changes in m (0.4 to 0.95). (b) Sudden changes in load resistance (60 to 30 Ω).

R is 18 Ω. The phase voltage V_{AO}, line-line voltage V_{AB}, the midpoint voltage of dc-link V_{ON}, and phase current i_A are shown from top to bottom. The roman numerals represent different sectors. It can be observed from Fig. 15(a) that the phase voltage V_{AO} and line-line voltage V_{AB} have three voltage levels, which are −200 V, 0, and 200 V because the reference vector locates in Region A of each large sector. The measured rms value of midpoint voltage V_{ON} is 197 V, so the unbalance is within 2% (3 / 200 = 1.5%). The rms values of phase current i_A is 3.42 A and the THD is about 3.68%. Fig. 15(b) shows the voltage stresses of S_1, S_2, and S_5. Obviously, the maximum voltages on all switches are $V_{dc}/2$. Seen from Fig. 16(a), the phase voltage V_{AO} is switched between 200 V and 0 during large Sectors I and II, between −200 V and 0 during large Sectors IV and V, whereas it is switched between −200 V, 0, and 200 V during Sectors III and VI. The experiment waveforms are consistent with the switching sequence, as shown in Table II. The line-line voltage V_{AB} has five voltage levels, which are −400, −200, 0, +200, and +400 V. The midpoint voltage is well balanced at about 200 V, and the phase current i_A is about 7.83 A with the THD of 2.6%. As seen in Fig. 16(b), the maximum voltages on S_1 and S_2 are $V_{dc}/2$ and the maximum voltage on S_5 is V_{dc}, which is consistent with the theoretical analysis.

Fig. 17 shows the detailed waveforms in Sectors IV and V. Channel 1 is the phase voltage V_{AO}. It is observed that V_{AO} is always switched from 0 to +200 V or 0 to −200 V during Sector IV or V. Channel 2 is the voltage across S_5 (V_{CE5}) and Channel 3 is the gating signal of S_5 (V_{GE5}). In Sector IV, S_5 is always OFF, the voltage across S_5 depends on the potential difference between point A and the emitter potential of S_1. In Sector V, S_5 is switched at the switching frequency. When S_5 is ON, the voltage across S_5 is 0. When S_5 is OFF, the voltage across S_5 also depends on the potential difference between point A and the emitter potential of S_1. Thus, S_5 should withstand the whole dc-link voltage while the dv/dt is still the same as that of conventional three-level topologies. The same is true for switch S_6−S_{10}.

Fig. 18 shows the experimental waveforms under resistance–inductance load. The resistance is 18 Ω and the inductance is 45 mH, so the PF is about 0.79 ($\varphi = 0.66$). As can be observed, the phase voltage V_{AO} and line-line voltage V_{AB} are the same as that under resistive load. The phase current i_A is about 6.55 A with a THD of 2.14% and the midpoint voltage is well balanced. Thus, 10S-3P-3L inverter can also be used in motor drive applications.

Fig. 19 show the experimental results of the dynamic tests. It can be seen from Fig. 19(a) that phase current i_A is smoothly generated along with the increase of m. Simultaneously, phase voltage V_{AO} is always three level, and line-line voltage V_{AB} changes from three level to five level. Fig. 19(b) shows the experimental waveforms when the load changes from 60 to 30 Ω. The voltage levels of phase voltage V_{AO} and line-line voltage

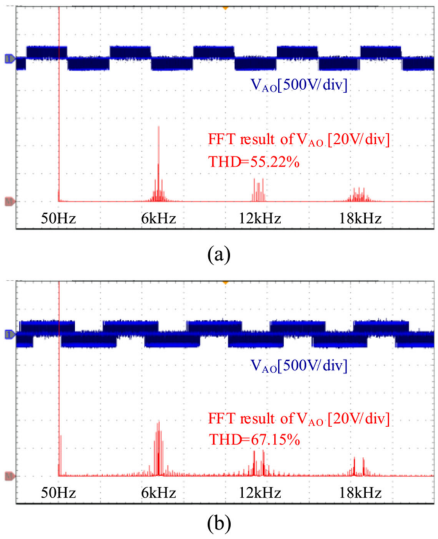

Fig. 20. FFT results of the bridge voltages for different topologies. (a) I-type NPC topology. (b) 10S-3P-3L topology.

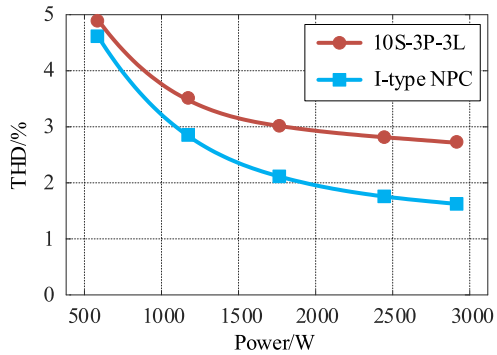

Fig. 21. Measured THD various with load.

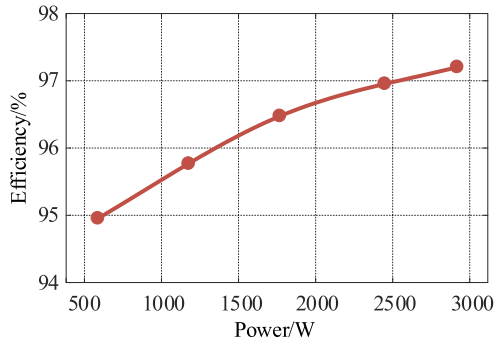

Fig. 22. Measured efficiency various with load.

V_{AB} remain unchanged under dynamic loads. The amplitude of phase current varies from 2.47 to 4.98 A. In all, the experimental tests have validated the effectiveness of the proposed 10S-3P-3L inverter.

Fig. 20 shows the fast Fourier transform (FFT) results of the bridge voltages for I-type and 10S-3P-3L topologies. It can be seen that the carrier harmonics of I-type inverter are higher than that of the 10S-3P-3L inverter, whereas the sideband harmonics of I-type inverter are lower than that of the 10S-3P-3L inverter. Because of the lack of medium vector, the measured THD of 10S-3P-3L topology is higher than that of I-type topology.

Fig. 21 shows the measured THD for both 10S-3P-3L and I-type NPC when $m = 0.95$ and $\varphi = 0$ under the same switching frequency and filter inductor parameters. As the power increases, the THD for two topologies decrease. It can be also seen that the THD of 10S-3P-3L topology is higher than that of type-I inverter. When the load reaches about 3000 W, the THD of 10S-3P-3L topology is about 2.6%, and the THD of type-I topology is about 1.62%. Therefore, the experimental results and theoretical analysis are consistent. Fig. 22 shows the efficiency curves of experimental result. It is concluded that the efficiency of 10S-3P-3L topology is higher than 95% when the load power is from 500 to 3000 W, and the maximum efficiency is about 97.2% at about 3000 W.

VI. Conclusion

A reduced component count three-phase three-level inverter topology named 10S-3P-3L inverter is proposed in this article. It couples three independent bridge arms together, then two active switches and six diodes are reduced compared with I-type NPC. A total of 13 space vectors, including 21 switching states, are achieved from the proposed inverter. Two large and two small vectors are used to synthesize the reference in Region B of each large sector, so that the voltage utilization of 10S-3P-3L inverter under the proposed SVM method is the same as conventional three-phase three-level inverters. The detailed comparison of 10S-3P-3L inverter with other existing topologies shows its obvious advantages in terms of the number of devices, stresses, and losses. Finally, practical results obtained using an experimental prototype were given, so as to verify the feasibility of the proposed topology.

Compared with other topologies, the performance demonstrated by 10S-3P-3L inverter is highly competitive, potentially making it an appropriate topology choice for a wide range of power conversion applications, such as motor drives, electric vehicles, and grid-connected renewable energy systems.

References

[1] M. Bragard, N. Soltau, S. Thomas, and R. De Doncker, "The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3049–3056, Dec. 2010.

[2] A. Usmani, M. Shahrukh, and A. Mustafa, "Comparison of different three phase inverter topologies: A review," in *Proc. Int. Conf. Innov. Elect. Electron. Instrum. Media Technol.*, 2017, pp. 19–24.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, May 1981.

[4] L. He and C. Cheng, "A flying-capacitor-clamped five-level inverter based on bridge modular switched-capacitor topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, Dec. 2016.

[5] Y. Yu, G. Konstantinou, B. Hredzak, and V. Agelidis, "Power balance of cascaded H-bridge multilevel converters for large-scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 292–303, Jan. 2016.

[6] H. Wang, L. Kou, Y. Liu, and P. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5146–5161, Jul. 2017.

[7] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.
[8] D. Floricau, G. Gateau, M. Dumitrescu, and R. Teodorescu, "A new stacked NPC converter: 3l-topology and control," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
[9] D. Floricau, G. Gateau, and A. Leredde, "New active stacked NPC multilevel converter: Operation and features," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2272–2278, Jul. 2010.
[10] Y. Wang and F. Wang, "Novel three-phase three-level-stacked neutral point clamped grid-tied solar inverter with a split phase controller," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2856–2866, Jun. 2013.
[11] O. Husev *et al.*, "Comparison of impedance-source networks for two and multilevel buck-boost inverter applications," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7564–7579, Nov. 2016.
[12] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.
[13] D. Panfilov, O. Husev, F. Blaabjerg, J. Zakis, and K. Khandakji, "Comparison of three-phase three-level voltage source inverter with intermediate dc–dc boost converter and quasi-Z-source inverter," *IET Power Electron.*, vol. 9, no. 6, pp. 1238–1248, May 2016.
[14] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, "Three-level Z-source inverters using a single LC impedance network," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 706–711, Mar. 2007.
[15] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electron.*, vol. 8, no. 1, pp. 1–10, Jan. 2015.
[16] S. Prasanth, M. H. M. Sathik, A. A. Ayu, T. C. Seng, and K. S. S. Kumar, "Maximum boost space vector modulated three-phase three-level neutral point-clamped quasi-Z-source inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.
[17] A. Ho and T. Chun, "Topology and modulation scheme for three-phase three-level modified Z-source neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11014–11025, Nov. 2019.
[18] A. Batschauer, S. Mussa, and M. Heldwein, "Three-phase hybrid multilevel inverter based on half-bridge modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 668–678, Feb. 2012.
[19] A. Hota, S. Jain, and V. Agarwal, "An improved three-phase five-level inverter topology with reduced number of switching power devices," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3296–3305, Apr. 2018.
[20] M. Hasan, A. Abu-Siada, and M. Dahidah, "A three-phase symmetrical DC-link multilevel inverter with reduced number of DC sources," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8331–8340, Oct. 2018.
[21] A. Karthik and U. Loganathan, "A reduced component count five-level inverter topology for high reliability electric drives," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 725–732, Jan. 2020.
[22] P. Kumar, R. Kaarthik, K. Gopakumar, J. Leon, and L. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3471–3478, Jul. 2015.
[23] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "An eight-switch five-level current source inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8389–8404, Sep. 2019.
[24] A. Nami, J. Liang, F. Dijkhuizen, and G. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.
[25] M. Aleenejad, S. Jafarishiadeh, H. Mahmoudi, and R. Ahmadi, "Reduced number of auxiliary H-bridge power cells for post-fault operation of three phase cascaded H-bridge inverter," *IET Power Electron.*, vol. 12, no. 11, pp. 2923–2931, Aug. 2019.
[26] F. Khosravi, N. A. Azli, and A. Kaykhosravi, "Design of a reduced component count single-phase to three-phase quasi-Z-source converter," *IET Power Electron.*, vol. 7, no. 3, pp. 489–495, Mar. 2014.
[27] A. Masaoud, H. W. Ping, S. Mekhilef, and A. S. Taallah, "New three-phase multilevel inverter with reduced number of power electronic components," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6018–6029, Nov. 2014.
[28] D. G. Holmes and T. A. Lipo, in *Pulse Width Modulation For Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.
[29] B. Gu, J. Dominic, B. Chen, L. Zhang, and J. Lai, "Hybrid transformer ZVS/ZCS DC–DC converter with optimized magnetics and improved power devices utilization for photovoltaic module applications," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2127–2136, Apr. 2015.
[30] M. R. Islam, A. M. Mahfuz-Ur-Rahman, M. M. Islam, Y. G. Guo, and J. G. Zhu, "Modular medium-voltage grid-connected converter with improved switching techniques for solar photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 64, no. 11, pp. 8887–8896, Nov. 2017.
[31] N. Nguyen, B. Nguyen, and H. Lee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 58, no. 9, pp. 3958–3966, Sep. 2011.
[32] S. B. Veeranna, A. R. Beig, and U. R. Yaragatti, "Performance analysis of PWM strategies for cascaded H-bridge three-level inverter," in *Proc. IEEE GCC Conf. Exhib.*, 2011, pp. 81–84.

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