Control and Experimental Verification of a Bidirectional Nonisolated DC–DC Converter Based on Switched-Capacitor Converters

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***Abstract*—This article presents a bidirectional nonisolated dc–dc converter based on switched-capacitor converters intended for electric railway system applications. It consists of plural main converters with two power devices per converter, plural auxiliary converters each of which is formed by cascaded chopper cells, and small-sized inductors for current control. The dc–dc converter can achieve zero-current switching (ZCS) for all power devices used in the main converters under arbitrary load conditions and an arbitrary voltage ratio of high-voltage-side voltage and low-voltage-side voltage. Consequently, square-wave currents can be removed from both the high- and low-voltage sides of the converter. The validity of the operating principles as well as the control methods proposed in this article is verified by experiments using a 200-V, 2-kW downscaled model.**

***Index Terms*—Battery energy storage systems, dc–dc converters, switched-capacitor converters, zero-current switching.**

I. Introduction

ELECTRIC railway systems with reduced greenhouse-gas emissions have attracted attention as they can help create a low-carbon society. To achieve this aim, in recent years, Japanese dc electric railway systems with nominal dc catenary voltages of 600, 750, 1000, and 1500 V have installed battery energy storage systems to improve the utilization of electric power [1]–[4]. It is strongly required to reduce the mass and volume of the power converter used in battery energy storage systems because it is placed in a moving train car [5]–[10].

Since a dc catenary voltage is different from a battery voltage in terms of amplitude, a bidirectional chopper (i.e., a nonisolated dc–dc converter) should be used for voltage conversion [11]–[14]. Fig. 1 shows the circuit configuration of a conventional bidirectional chopper for battery energy storage systems, where V_{H} corresponds to the catenary voltage, V_{L} corresponds to the battery voltage, and i is the high-voltage-side current. The conventional bidirectional chopper suffers from the disadvantage of a large mass and volume because of an inductor used. It is possible to reduce the size and weight of an inductor by increasing the switching frequency, whereas it is typically set less than 1 kHz for a power converter applied to a dc catenary voltage of 1500 V. The reason for this is that 3.3-kV Si-IGBTs with relatively poor switching characteristics compared with 600-V or 1.2-kV Si-IGBTs are applied when a dc centenary voltage is 1500 V [4]. In addition, an amount of square-wave current flows in i which may cause an undesirable surge voltage in power devices as well as increase EMI (electromagnetic interference) emissions, resulting in reduced reliability.

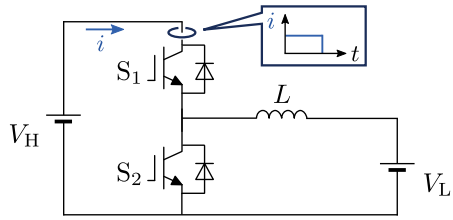

Fig. 1. Circuit configuration of a conventional bidirectional chopper for battery energy storage systems.

Numerous dc–dc converter topologies have been studied for reducing the size and weight of an inductor. The authors of [4], [15], [16] have shown that the switching-ripple components included in the low-voltage-side current can be reduced by applying interleaved bidirectional choppers with appropriate phase shift. A bidirectional chopper with an auxiliary converter presented in [17], [18] is characterized by applying an auxiliary converter to the conventional bidirectional chopper, which is formed by the cascade connection of multiple single-phase full-bridge converter cells working as an active power filter. It is reported in [17] that the size and weight of an inductor can be 1/50 that of the conventional bidirectional chopper. However, a square-wave current still flows in the high-voltage side of the chopper even if these choppers are applied. Switched-capacitor-based resonant converters (SCRCs) [19]–[22] are characterized by achieving zero-current switching (ZCS) in power devices by forming a resonant circuit with an inductor and a capacitor connected in series. However, the ZCS can be achieved only when the low-voltage-side voltage is half of the high-voltage-side voltage, and the ZCS cannot be achieved under arbitrary load conditions [21]. In addition, the SCRCs are not suitable for a large-capacity

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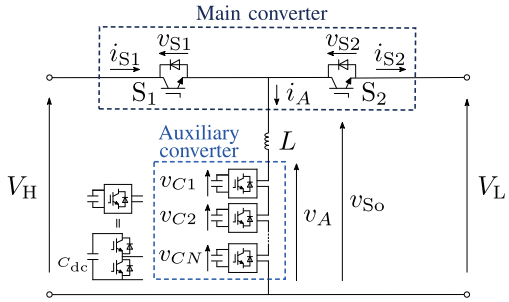


Fig. 2. Circuit configuration of a bidirectional nonisolated dc–dc converter based on a switched-capacitor converter.

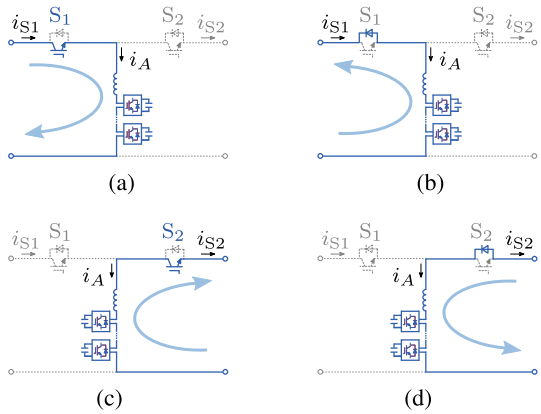


Fig. 3. Four operating modes of the circuit shown in Fig. 2 according to the switching states, where the power is sent from the high-voltage side to the low-voltage side. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

converter with a power rating higher than 100 kW because of the limitations on the current rating of the capacitor.

This article proposes a new bidirectional nonisolated dc–dc converter based on switched-capacitor converters intended for electric railway system applications. It consists of plural main converters, plural auxiliary converters, and small-sized inductors, where the auxiliary converter is formed by the cascade connection of multiple chopper cells (i.e., a bidirectional chopper). The dc–dc converter can achieve the ZCS for all power devices used in the main converters under arbitrary load conditions, including a sudden load change and the arbitrary voltage ratio of high-voltage-side voltage and low-voltage-side voltage. Consequently, square-wave currents can be removed from both the high- and low-voltage sides of the converter. The current control method based on the $dq0$ transformation and the voltage control method of the floating dc capacitors used in the auxiliary converters are presented.

The rest of the article is organized as follows. Section II provides explanations on circuit configuration and principles of operation of the proposed dc–dc converter. Sections III and IV present a current control method based on the $dq0$ transformation, and the control method of the main and auxiliary converters. Section V carries out experimental verification of the dc–dc converter using a down-scaled model rated at 200 V and 2 kW. Section VI presents the loss analysis of an actual dc–dc converter system. Finally, Section VII concludes the work.

II. Circuit Configuration and Principles of Operation

A. Circuit Configuration

Fig. 2 shows the circuit configuration of a bidirectional nonisolated dc–dc converter based on a switched-capacitor converter (SCC) presented in this article. Fig. 2 consists of a main converter, an auxiliary converter, and an inductor, where $V_{\rm H}$ is the high-voltage-side voltage and $V_{\rm L}$ is the low-voltage-side voltage ($V_{\rm H} > V_{\rm L}$). The main converter is formed by two power devices, $\rm S_1$ and $\rm S_2$, where $v_{\rm S1}$ and $v_{\rm S2}$ are the device voltages of $\rm S_1$ and $\rm S_2$, $i_{\rm S1}$ and $i_{\rm S2}$ are the device currents flowing to $\rm S_1$ and $\rm S_2$, and $v_{\rm So}$ is the output voltage of the main converter. It is noteworthy that the closed loop formed by $V_{\rm H}$, $V_{\rm L}$, $\rm S_1$, and $\rm S_2$ should be wired and assembled within the shortest distance for protecting the power devices from overvoltage. The main converter acts as a voltage source, producing $v_{\rm So} = V_{\rm H}$ or $v_{\rm So} = V_{\rm L}$ according to the switching states. The voltage rating of the power devices is $V_{\rm H} - V_{\rm L}$, which is smaller than power devices used in Fig. 1 with a voltage rating of $V_{\rm H}$. The auxiliary converter consists of a cascade connection of multiple chopper cells (i.e., a bidirectional chopper), and it is connected to the main converter via an inductor L. v_{C1}, v_{C2}, and v_{CN} are the dc-capacitor voltages, v_A is the output voltage of the auxiliary converter, and i_A is the inductor current, where the chopper-cell count is N.

B. Principles of Operation

Fig. 3 shows the four operating modes of the circuit shown in Fig. 2 according to the switching states of the main converter, where the power is sent from the high-voltage side to the low-voltage side. In mode 1 where $\rm S_1$ is ON and $\rm S_2$ is OFF, the current flows to the IGBT of $\rm S_1$ and the power is sent from $V_{\rm H}$ to the auxiliary converter as shown in Fig. 3(a). In mode 3 where $\rm S_1$ is OFF and $\rm S_2$ is ON, the current flows to the IGBT of $\rm S_2$ and the power is sent from the auxiliary converter to $V_{\rm L}$ as shown in Fig. 3(c). During the dead-time period where $\rm S_1$ and $\rm S_2$ are OFF simultaneously, the operating modes are different according to the polarity of i_A. In mode 2 where $\rm S_1$ and $\rm S_2$ are OFF, and $i_A < 0$, the current flows to the diode of $\rm S_1$ and the power is sent from the auxiliary converter to $V_{\rm H}$ as shown in Fig. 3(b). In mode 4 where $\rm S_1$ and $\rm S_2$ are OFF, and $i_A > 0$, the current flows to the diode of $\rm S_2$ and the power is sent from $V_{\rm L}$ to the auxiliary converter as shown in Fig. 3(d). It is obvious from Fig. 3 that the operation of the Fig. 2 circuit is similar to that of a traditional SCC, where the power is sent and received via a capacitor. Meanwhile, the Fig. 2 circuit is different from the SCC in that i_A can be controlled actively and the ZCS can be achieved in $\rm S_1$ and $\rm S_2$ not only under steady states but also under transient states, including a sudden change in $V_{\rm H}$ and/or $V_{\rm L}$. Consequently, square-wave currents can be removed from both the high- and low-voltage sides of the main converter. It should be noted that the power devices used in the auxiliary converters are always in hard-switching operation with a blocking voltage of $\frac{V_{\rm H}}{N}$.

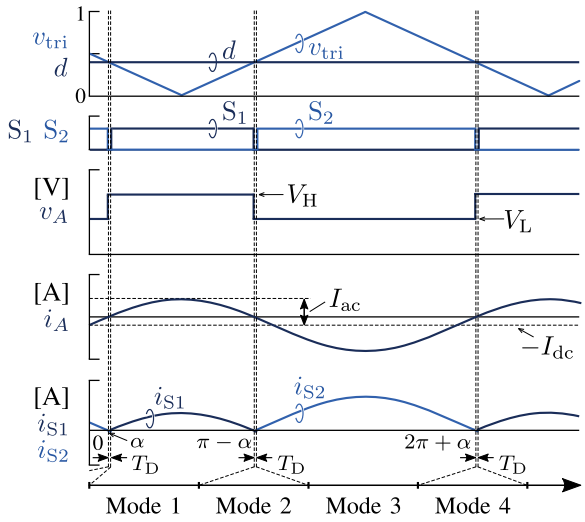


Fig. 4. Ideal voltage and current waveforms of the circuit shown in Fig. 2, where the power is sent from the high-voltage side to the low-voltage side.

Fig. 4 shows the ideal voltage and current waveforms of Fig. 2, where the power is sent from the high-voltage side to the low-voltage side. $v_{\rm tri}$ is the carrier wave and d is the instantaneous duty ratio of S_1. The following simplifications (i.e., assumptions) have been made in Fig. 4.

1) The switching-ripple components included in v_A and i_A are set to zero.
2) The voltage components used for current control and dc-capacitor voltage control are set to zero in v_A.
3) The ON-state voltages of S_1 and S_2 are set to zero.

The first simplification is valid because the switching-ripple components have little effect on the power flow between $V_{\rm H}$ and $V_{\rm L}$. In fact, the power is determined by the fundamental-frequency component included in i_A as will be shown in (4)–(10) later. The second assumption is reasonable because the power is determined by $V_{\rm H}$, $V_{\rm L}$, and i_A as will be shown in (4)–(10) later, and therefore the voltage components for current control and dc-capacitor voltage control included in v_A do not contribute to the power transfer between $V_{\rm H}$ and $V_{\rm L}$. The third assumption is valid because the ON-state voltages are less than 1% of $V_{\rm H}$ or $V_{\rm L}$ and they are negligible. In summary, the above simplifications have been introduced because they have little effect on the power flow between $V_{\rm H}$ and $V_{\rm L}$. Consequently, a simple and easy circuit analysis can be carried out. According to the above simplifications, v_A in Fig. 2 is given by

$$v_{\rm A} = \begin{cases} V_{\rm H} & \text{when } v_{\rm tri} < d \\ V_{\rm L} & \text{when } v_{\rm tri} > d. \end{cases} \tag{1}$$

However, the voltage over inductor L is not zero because v_A contains the voltage components for current control and dc-capacitor voltage control, and the switching-ripple components, the waveform of which will be shown experimentally later in Figs. 17–20. Equation (1) and Fig. 4 imply that v_A can be divided into a dc component and a square-wave ac component with a frequency $f_{\rm CM}$, which is the carrier frequency of the main converter. The following equation regarding the instantaneous power is obtained from Fig. 2 as

$$p_A = v_A i_A \tag{2}$$

where p_A is the instantaneous active power flowing into the auxiliary converter. The one-period average value of p_A, P_A, should be zero for regulating the dc-capacitor voltages of the floating capacitors. For achieving the ZCS of S_1 and S_2, and the relation $P_A = 0$ simultaneously, i_A is given by

$$i_A = I_{\rm ac}\sin\theta - I_{\rm dc} = I_{\rm ac}\sin 2\pi f_{\rm CM} t - I_{\rm dc}. \tag{3}$$

i_A contains a sinusoidal-wave ac component with a frequency $f_{\rm CM}$ and a dc component, where $I_{\rm ac}$ is the amplitude of the ac component and $I_{\rm dc}$ is that of the dc component ($I_{\rm dc} > 0$). The auxiliary converters play the role of generating (i.e., controlling) i_A by working as controlled voltage sources. The detail of the generation process will be provided in Section IV-B. Equation (3) implies that the relation $P_A = 0$ can be realized by controlling $I_{\rm dc}$ appropriately. Let the phase angle when the polarity of i_A changes from negative to positive be $\alpha(0 < \alpha < \frac{\pi}{2})$ as shown in Fig. 4. The following relation holds between $I_{\rm dc}$ and $I_{\rm ac}$:

$$I_{\rm dc} = I_{\rm ac}\sin\alpha. \tag{4}$$

Assuming the dead-time period is zero, i_{S1} and i_{S2} are expressed as follows:

$$i_{S1} = \begin{cases} i_A & \text{when } v_{\rm tri} < d \\ 0 & \text{when } v_{\rm tri} > d \end{cases} \tag{5}$$

$$i_{S2} = \begin{cases} 0 & \text{when } v_{\rm tri} < d \\ -i_A & \text{when } v_{\rm tri} > d. \end{cases} \tag{6}$$

S_1 and S_2 can achieve the ZCS if they can turn ON/OFF at α, $\pi-\alpha$, and $2\pi+\alpha$ in Fig. 4.

C. Derivation of α

The converter loss and dead-time period T_D are assumed to be zero in the following analysis. In addition, it is assumed that the ZCS of S_1 and S_2 is realized as shown in Fig. 4. The one-period average power of the high- and low-voltage sides, $P_{\rm H}$ and $P_{\rm L}$, is given by

$$P_{\rm H} = V_{\rm H} I_{S1} \tag{7}$$

$$P_{\rm L} = V_{\rm L} I_{S2} \tag{8}$$

where I_{S1} and I_{S2} are the one-period average values of i_{S1} and i_{S2}, which can be calculated from (3)–(6) as

$$\begin{aligned} I_{S1} &= \frac{1}{2\pi}\int_0^{2\pi} i_{S1}\,d\theta \\ &= \frac{I_{\rm ac}}{2\pi}\left(2\cos\alpha - \pi\sin\alpha + 2\alpha\sin\alpha\right) \end{aligned} \tag{9}$$

$$\begin{aligned} I_{S2} &= \frac{1}{2\pi}\int_0^{2\pi} i_{S2}\,d\theta \\ &= \frac{I_{\rm ac}}{2\pi}\left(2\cos\alpha + \pi\sin\alpha + 2\alpha\sin\alpha\right). \end{aligned} \tag{10}$$

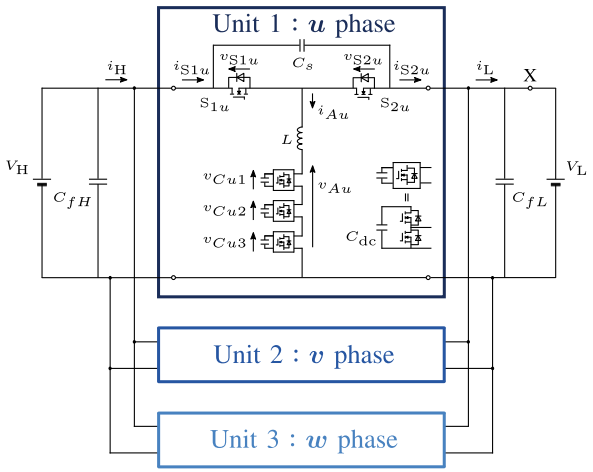


Fig. 5. Circuit configuration of an interleaved dc–dc converter system with three units.

The relationship $P_{\rm H} = P_{\rm L}$ holds under steady states. Based on (7)–(10), α is derived with the help of $P_{\rm H} = P_{\rm L}$ as

$$\alpha^2 - \pi\frac{V_{\rm H}+V_{\rm L}}{V_{\rm H}-V_{\rm L}}\alpha + 2 = 0 \tag{11}$$

where the reasonable approximations, $\sin\alpha \approx \alpha$ and $\cos\alpha \approx 1-\frac{\alpha^2}{2}$, are applied. The relation $\frac{\sin\alpha}{\alpha} = 0.95$ holds when $\alpha = \frac{\pi}{6}$. In other words, the approximation is reasonable when $0 < \alpha < \frac{\pi}{6}$ if an acceptable error is less than 5%. Considering that $0 < \alpha < \frac{\pi}{2}$, α is obtained as

$$\alpha = \frac{1}{2}\left(\pi\frac{1+\frac{V_{\rm L}}{V_{\rm H}}}{1-\frac{V_{\rm L}}{V_{\rm H}}} - \sqrt{\left(\pi\frac{1+\frac{V_{\rm L}}{V_{\rm H}}}{1-\frac{V_{\rm L}}{V_{\rm H}}}\right)^2 - 8}\right). \tag{12}$$

Substituting the relation $0 < \alpha < \frac{\pi}{6}$ into (12) produces the exact range of ZCS as $0.15 \le V_{\rm L}/V_{\rm H} < 1$. Equation (12) means that the ZCS of $\rm S_1$ and $\rm S_2$ can be achieved if α is given by (12), and α does not depend on i_A, whereas it depends on $V_{\rm H}$ and $V_{\rm L}$. This implies that the ZCS can be achieved at arbitrary load conditions in both steady and transient states. Moreover, it is possible to achieve the ZCS even when $V_{\rm H}$ or $V_{\rm L}$ varies with time using the detected instantaneous dc voltages. Although the converter can work under the arbitrary voltage ratio of $0 < V_{\rm L}/V_{\rm H} < 1$, the ZCS cannot be achieved when the approximations mentioned above are not reasonable, and this can happen when the voltage ratio $V_{\rm L}/V_{\rm H}$ is close to zero.

D. Interleaved dc–dc Converter

Fig. 5 shows the circuit configuration of an interleaved dc–dc converter for high-power conversion, where the circuit shown in Fig. 2 is used as a unit dc–dc converter. The high- and low-voltage sides of each unit converter are connected in parallel, where $i_{\rm H}$ and $i_{\rm L}$ are the total high- and low-voltage-side currents, respectively. $i_{\rm H}$ and $i_{\rm L}$ approach to pure dc currents with less ac components by increasing the number of unit converters with appropriate phase shifts. In Fig. 5, the unit count and chopper-cell count are set to $M = 3$ and $N = 3$, which is the same configuration as an experimental system developed in the laboratory. However, they can be set to an arbitrary number. The initial phases of the triangular carriers applied to each main converter are shifted by $120°(= 360°/3)$, and those applied to chopper cells in each unit are shifted by $120°(= 360°/3)$.

In Fig. 5, units 1, 2, and 3 are referred to as u-, v-, and w-phase converters, respectively, for convenience sake, because the operation of Fig. 5 with three units is similar to that of a three-phase four-wire grid-connected converter as mentioned later. Meanwhile, the control method can be easily changed and expanded even when the unit count is increased to four or more. A snubber capacitor C_s is connected in parallel with the main converter for protecting $\rm S_{1u}$ and $\rm S_{2u}$ from overvoltage, which is also applied to a conventional dc–dc converter as shown in Fig. 1. The dc-link capacitors (C_{fH} and C_{fL}) and the three main converters should be wired and assembled within the shortest distance for protecting the power devices from overvoltage.

E. Difference Between Fig. 2 and SCC

Although the operation of a traditional SCC and Fig. 2 is similar as shown in Fig. 3, the transfer functions of both converters are entirely different because the combination of inductor L and the auxiliary converter in Fig. 2 works as a robust controlled current source, whereas a capacitor used in the SCC simply works as a passive component. The term "passive component" in this article means a capacitor or an inductor itself without any active switch. Further, the power-flow operation of Fig. 2 does not rely on the resonance between inductor and dc capacitor because the inductor current is actively controlled by the auxiliary converter, whereas the SCC relies on the resonance between inductor and capacitor. Consequently, Fig. 2 is more robust against the tolerance of inductance or capacitance compared with the SCC, and the problem of right-half-plane (RHP) zero which occurs in the traditional SCC does not occur in Fig. 2. Further, Fig. 2 is strong against the variation of voltage ratio, which will be shown experimentally in Fig. 20. However, the detailed stability analysis of Fig. 2 is left for the future work.

F. Downsizing the Passive Components

1) DC Capacitor: Each dc-capacitor voltage in Fig. 2 consists of a dc component V_C and a dominant ac component of $f_{\rm CM}$. The following relation holds regarding instantaneous power in the cell numbered 1 shown in Fig. 2 as

$$v_{A1}i_A = \frac{v_A}{N}i_A = C_{\rm dc}v_{C1}\frac{dv_{C1}}{dt} \approx C_{\rm dc}V_C\frac{dv_{C1}}{dt}. \tag{13}$$

The relation $v_A \ge 0$ holds in (13); hence, v_{C1} increases when $i_A > 0$ and decreases when $i_A \le 0$. Based on (3), the relation $\alpha < \theta < \pi - \alpha$ ($\frac{\alpha}{2\pi f_{\rm CM}} < t < \frac{\pi-\alpha}{2\pi f_{\rm CM}}$) holds when $i_A > 0$. The ac-voltage fluctuation of the dc-capacitor voltage Δv_{C1} is given from (1), (3), (4), and (13) as

$$\begin{aligned}\Delta v_{C1} &= \int_{\frac{\alpha}{2\pi f_{\rm CM}}}^{\frac{\pi-\alpha}{2\pi f_{\rm CM}}} \frac{V_{\rm H}I_{\rm ac}}{N}(\sin 2\pi f_{\rm CM}t - \sin\alpha)dt \\ &= \frac{V_{\rm H}I_{\rm ac}}{2\pi f_{\rm CM}C_{\rm dc}V_C N}\left(2\cos\alpha - \pi\sin\alpha + 2\alpha\sin\alpha\right).\end{aligned} \tag{14}$$

Equation (14) means that $C_{\rm dc}$ can be reduced by increasing the chopper-cell count N and/or increasing $f_{\rm CM}$ when Δv_{C1} is set to a constant value.

2) AC Inductor: L can be reduced by applying the phase-shift PWM to the auxiliary converters. This technique is also applied to modular multilevel cascade converters (MMCC) [23]–[26]. According to [27], the maximum ripple current Δi_A is given by

$$\Delta i_A = \frac{V_C}{8N f_{\rm CA} L} \tag{15}$$

where $f_{\rm CA}$ is the carrier frequency of the auxiliary converter. Equation (15) means that the mass and volume can be reduced by increasing the chopper-cell count N and/or increasing $f_{\rm CA}$ when Δi_A is set to a constant value.

III. Current Control Based on $dq0$ Transformation

A. Equivalent Circuit of Fig. 5

The power devices used in the main converters are assumed to behave as ideal switches, which can turn ON/OFF instantaneously with no time delay and produce no loss. In addition, the parasitic resistance/inductance in the Fig. 5 circuit is set to zero for a simple and easy circuit analysis. The following equation holds in the u-phase converter when $\rm S_{1u}$ is ON and $\rm S_{2u}$ is OFF:

$$V_{\rm H} = L\frac{di_{Au}}{dt} + v_{Au}. \tag{16}$$

Meanwhile, the following equation holds when $\rm S_{1u}$ is OFF and $\rm S_{2u}$ is ON:

$$V_{\rm L} = L\frac{di_{Au}}{dt} + v_{Au}. \tag{17}$$

The output voltage of the u-phase main converter, $v_{{\rm So}u}$, is given by

$$v_{{\rm So}u} = \begin{cases} V_{\rm H} & \text{when } v_{{\rm tri}u} < d \\ V_{\rm L} & \text{when } v_{{\rm tri}u} > d \end{cases} \tag{18}$$

where $v_{{\rm tri}u}$ is the carrier wave of the u-phase main converter, and d is the instantaneous duty ratio common to the three main converters. Based on (16)–(18), the following equation holds in the u-phase converter:

$$v_{{\rm So}u} = L\frac{di_{Au}}{dt} + v_{Au}. \tag{19}$$

Similar equations hold in the v- and w-phase converters, where the initial phases of the triangular carriers are shifted by 120° each other.

Fig. 6 shows the voltage waveforms of $v_{{\rm So}u}$, $v_{{\rm So}v}$, and $v_{{\rm So}w}$, where they include a common positive dc component and a square-wave ac component with a phase difference of 120°. Meanwhile, the inductor currents include a common dc component (i.e., the zero-sequence current) and a sinusoidal ac component with a frequency $f_{\rm CM}$ and a phase difference of 120° (i.e., the positive-sequence current) as shown in (3). Since the inductor currents can be controlled independently, Fig. 6 can be transformed into Fig. 7, which is equivalent to a three-phase four-wire power system with a grid-connected converter. This

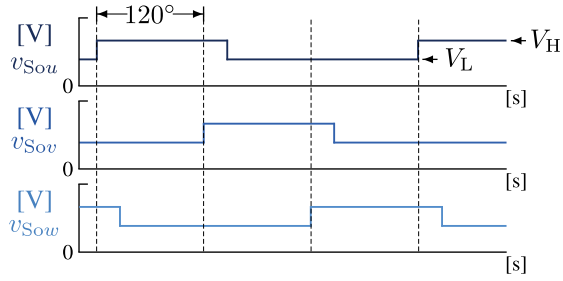


Fig. 6. Voltage waveforms of $v_{{\rm So}u}$, $v_{{\rm So}v}$, and $v_{{\rm So}w}$.

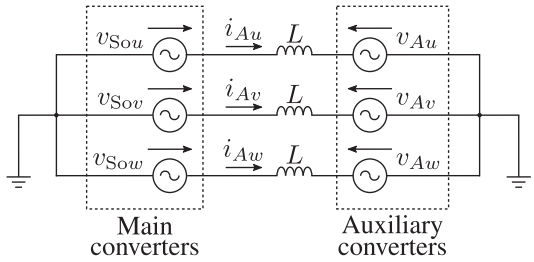


Fig. 7. Equivalent circuit of Fig. 5.

implies that a similar current control method based on the $dq0$ transformation can be applied to Fig. 5.

B. Current Control Based on $dq0$ Transformation

The current controllability can be improved by applying the $dq0$ transformation because ac currents can be transformed into dc currents. Meanwhile, Fig. 5 is different from a conventional power system with a fundamental frequency of 50 or 60 Hz in that the frequency of the ac currents is high (e.g., 450 Hz). This means that the advantage of applying the $dq0$ transformation is more remarkable in Fig. 5 than a conventional power system owing to its medium-frequency operation. The d- and q-axes currents, i_d and i_q, are defined as follows.

- i_d : The ac components of the inductor currents that are in phase or out of phase by 180° with those of $v_{{\rm So}u}$, $v_{{\rm So}v}$, and $v_{{\rm So}w}$.
- i_q : The ac components of the inductor currents that lead or lag the ac components of $v_{{\rm So}u}$, $v_{{\rm So}v}$, and $v_{{\rm So}w}$ by 90°.

It is noteworthy that only i_d contributes to power transmission between $V_{\rm H}$ and $V_{\rm L}$, and i_q should be set to zero for efficient power transmission. When $i_d \geq 0$, the power is transmitted from $V_{\rm H}$ to $V_{\rm L}$, and vice versa when $i_d < 0$.

The zero-sequence current i_0 which is common to all phases is given by the following equation:

$$i_0 = \frac{1}{\sqrt{3}}(i_{Au} + i_{Av} + i_{Aw}). \tag{20}$$

It consists of a dc component and an ac component with a frequency $f_{\rm CM}$. The dc component in i_0 forms an active power with a common positive dc voltage included in v_{Au}, v_{Av}, and v_{Aw}. When $i_0 \geq 0$, a positive power flows into the auxiliary converters from $v_{{\rm So}u}$, $v_{{\rm So}v}$, and $v_{{\rm So}w}$, and the individual dc-capacitor voltages increase. Meanwhile, a negative power flows when

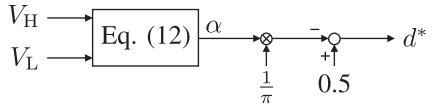


Fig. 8. Block diagram for the main converters.

$i_0 < 0$ and the dc-capacitor voltages decrease. This interesting feature can be used for overall voltage control. Further, the ac component with a frequency $f_{\rm CM}$ in i_0 has the function of producing power exchanges between phases, and this feature can be used for cluster-balancing control. The definitions of zero-sequence current and its references are listed below:

- i_0: It is calculated from (20), and included dc and ac components.
- $i^*_{0\rm dc1}$: It is a dc reference for i_0, generated by the overall voltage control.
- $i^*_{0\rm dc2}$: It is a dc reference for i_0 calculated from (4), (12), and (25).
- $i^*_{0\rm ac}$: It is the ac reference for i_0, generated by the cluster-balancing control.
- i^*_0: It is the total reference for i_0, which is given as $i^*_0 = i^*_{0\rm dc1} + i^*_{0\rm dc2} + i^*_{0\rm ac}$.

C. Relation Between Unit Count and Current Control

The current control method based on the $dq0$ transformation can be easily expanded when the unit count is more than three. Specifically, the multiphase inductor currents can be transformed into i_d, i_q, and i_0 by applying the multiphase to the $dq0$ transformation, where each inductor current is phase-shifted by $360^\circ/N$. However, the $dq0$ transformation cannot be applied when the unit count is one or two, where the inductor currents should be controlled individually, which may result in the deterioration of current controllability. For this reason, this article focuses on the control system of Fig. 5, where the unit count is equal to or more than three.

IV. Control Method

The following focuses on the control method of Fig. 5 where the unit- and chopper-cell counts are $M = N = 3$. However, it can be easily redesigned when M is more than three and N is different from three.

A. Main Converter Control

Fig. 8 shows the control block diagram for the main converter, where the command value for the instantaneous duty ratio common to the three main converters, d^*, is calculated from α given by (12) and Fig. 4 as

$$d^* = 0.5 - \frac{\alpha}{\pi}. \tag{21}$$

The switching states of the main converters are determined by comparing d^* and the triangular carriers as shown in Fig. 4, where the initial phase of each carrier is shifted by 120°.

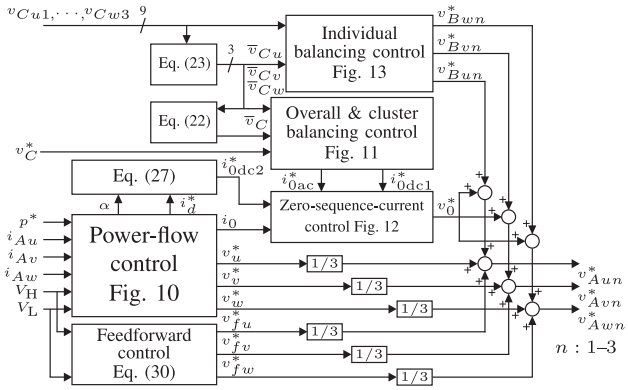


Fig. 9. Block diagram for the auxiliary converters.

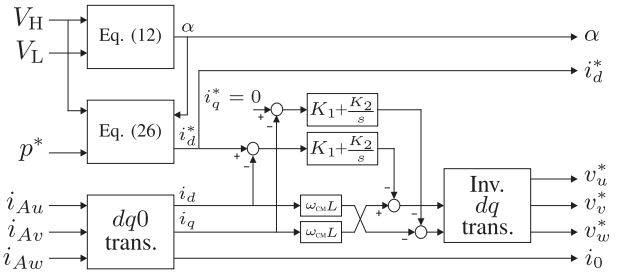


Fig. 10. Block diagram for power-flow control.

B. Auxiliary Converter Control

Fig. 9 shows the control block diagram for the auxiliary converters, where it is divided into the following three controls:

1) power-flow control;
2) dc-capacitor voltage control; and
3) feedforward control.

Further, the dc-capacitor voltage control can be classified into the following three sub-controls:

1) overall voltage control;
2) cluster-balancing control; and
3) individual-balancing control.

It is noteworthy that this hierarchical control method is basically the same as the one presented in [24], which was intended for regulating multiple floating capacitors of a MMCC. Consequently, the voltage equalization of multiple series-connected floating capacitors can be achieved. In Fig. 9, $\overline{v}_C$ is the arithmetic average voltage for all the floating dc capacitors used in Fig. 5, which is given by

$$\overline{v}_C = \frac{1}{3}(\overline{v}_{Cu} + \overline{v}_{Cv} + \overline{v}_{Cw}) \tag{22}$$

where $\overline{v}_{Cu}$, $\overline{v}_{Cv}$, and $\overline{v}_{Cw}$ are the voltages of the three phases. For example, $\overline{v}_{Cu}$ can be calculated as

$$\overline{v}_{Cu} = \frac{1}{3}(v_{Cu1} + v_{Cu2} + v_{Cu3}). \tag{23}$$

where it is the arithmetic average voltage of dc-capacitor voltages of u-phase converter. A factor of 1/3 exists in (23) because the number of converter cells per phase is three.

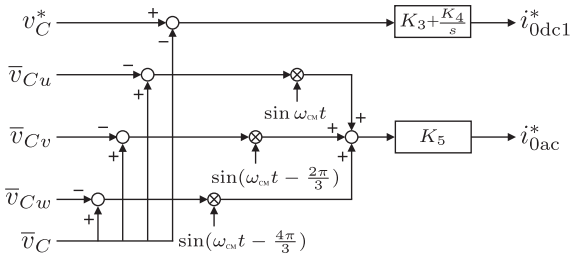


Fig. 11. Block diagram for overall voltage control and cluster-balancing control.

1) Power-Flow Control: Fig. 10 shows the block diagram for the power-flow control, where i_d, i_q, and i_0 are calculated by applying the $dq0$ transformation to the inductor currents i_{Au}, i_{Av}, and i_{Aw}. As mentioned in the previous section, the power flow between V_{H} and V_{L} can be controlled by adjusting i_d, whereas i_q should be zero for efficient power transmission. Hence, the command value for i_q, i_q^* is always set to zero. i_d and i_q can be controlled independently by applying the conventional decoupled current control which is widely applied to power systems with grid-connected converters. The relation $\omega_{\mathrm{CM}} = 2\pi f_{\mathrm{CM}}$ holds in Fig. 10.

Based on (7) and (9), the one-period average power of the high-voltage side in Fig. 5, $P_{\mathrm{H}}(= P_{\mathrm{L}})$, is given by

$$\begin{aligned} P_{\mathrm{H}} &= 3V_{\mathrm{H}}I_{\mathrm{S1}} \\ &= 3\frac{V_{\mathrm{H}}I_{\mathrm{ac}}}{2\pi}\left(2\cos\alpha - \pi\sin\alpha + 2\alpha\sin\alpha\right) \end{aligned} \tag{24}$$

where the coefficient "3" represents the unit count, and the average power of each phase is assumed to be the same. The following relation holds between I_{ac} and i_d:

$$i_d = \sqrt{\frac{3}{2}}I_{\mathrm{ac}}. \tag{25}$$

Let the command value for the one-period average power be p^*. The following equation holds between p^* and i_d^* from (24) and (25) as

$$p^* = \sqrt{\frac{3}{2}}\frac{V_{\mathrm{H}}i_d^*}{\pi}\left(2\cos\alpha - \pi\sin\alpha + 2\alpha\sin\alpha\right) \tag{26}$$

where i_d^* is the command value for i_d. Hence, i_d^* can be calculated from p^*, V_{H}, and α. Finally, the command values for power-flow control, v_u^*, v_v^*, and v_w^* are generated by applying the inverse dq transformation. In Fig. 9, they are further divided by three, which is the chopper-cell count, and given to each cell.

2) DC-Capacitor Voltage Control: Fig. 11 shows the control block diagram for the overall voltage control and the cluster-balancing control. The overall voltage control takes the responsibility for regulating $\overline{v}_C$ given by (22) to its command value, v_C^*. This is achieved by adjusting the dc component included in i_0, $i_{0\mathrm{dc1}}$. In Fig. 11, $i_{0\mathrm{dc1}}^*$ is the reference for $i_{0\mathrm{dc1}}$. The cluster-balancing control is responsible for balancing $\overline{v}_{Cu}$, $\overline{v}_{Cv}$, and $\overline{v}_{Cw}$, given by (23) to $\overline{v}_C$ by adjusting the ac component included in i_0, $i_{0\mathrm{ac}}$. In Fig. 11, $i_{0\mathrm{ac}}^*$ is the reference for $i_{0\mathrm{ac}}$. It is noteworthy that $\sin\omega_{\mathrm{CM}}t$, $\sin(\omega_{\mathrm{CM}}t - 2\pi/3)$, and $\sin(\omega_{\mathrm{CM}}t - 4\pi/3)$ in Fig. 11 are in phase with the fundamental ac components with a frequency f_{CM} included in $v_{\mathrm{So}u}$, $v_{\mathrm{So}v}$, and $v_{\mathrm{So}w}$ as shown in Fig. 6. When $\overline{v}_C > \overline{v}_{Cu}$, the product of $v_{\mathrm{A}u}$ and $i_{0\mathrm{ac}}$ forms a positive active power because $i_{0\mathrm{ac}}$ contains the same frequency component as $v_{\mathrm{A}u}$ (i.e., $v_{\mathrm{So}u}$). Consequently, an amount of active power flows into the u-phase converter, thus leading to increasing $\overline{v}_{Cu}$. Meanwhile, the product of v_{Au} and $i_{0\mathrm{ac}}$ forms a negative active power when $\overline{v}_C < \overline{v}_{Cu}$, thus leading to decreasing $\overline{v}_{Cu}$.

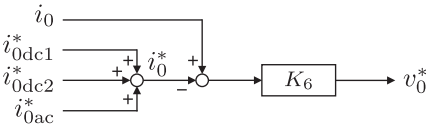


Fig. 12. Block diagram for zero-sequence current control.

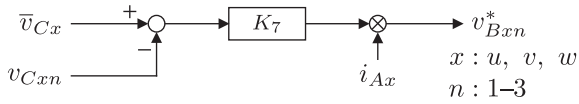


Fig. 13. Block diagram for individual-balancing control.

Fig. 12 shows the control block diagram for the zero-sequence-current control. It forces i_0 to follow its command $i_0^*(= i_{0\mathrm{dc1}}^* + i_{0\mathrm{dc2}}^* + i_{0\mathrm{ac}}^*)$, producing the voltage command for the zero-sequence voltage common to all phases, v_0^*. Next, we focus on the role of $i_{0\mathrm{dc2}}^*$. As mentioned before, the relation of (4) holds under the steady state and each dc-capacitor voltage can be regulated to a constant value. Meanwhile, an amount of active power may flow into or out from the dc capacitors during the transient state where p^* (i.e., i_d^*) changes rapidly, resulting in the deterioration of the transient performance of the dc-capacitor voltage control. For achieving the relation of (4) under the rapid change in p^*, $i_{0\mathrm{dc2}}^*$ is given with the help of (4) and (25) as

$$i_{0\mathrm{dc2}}^* = -\sqrt{\frac{2}{3}}i_d^*\sin\alpha \approx -\sqrt{\frac{2}{3}}\,i_d^*\,\alpha. \tag{27}$$

Consequently, the relation of (4) holds even during the transient state, and the transient performance can be improved. It is noteworthy that a similar technique is applied to grid-connected converters such as back-to-back converters.

Fig. 13 shows the control block diagram for the individual-balancing control. It forms an active power between the low-voltage-side voltage of each chopper cell and the corresponding inductor current. The voltage commands v_{Bun}^*, v_{Bvn}^*, and v_{Bwn}^* are given by

$$\begin{aligned} v_{Bun}^* &= K_7(\overline{v}_{Cu} - v_{Cun})i_{Au} \\ v_{Bvn}^* &= K_7(\overline{v}_{Cv} - v_{Cvn})i_{Av} \\ v_{Bwn}^* &= K_7(\overline{v}_{Cw} - v_{Cwn})i_{Aw}. \end{aligned} \tag{28}$$

The following equation holds according to (23) and (28):

$$\sum_{n=1}^{3} v_{Bun}^* = 0, \sum_{n=1}^{3} v_{Bvn}^* = 0, \sum_{n=1}^{3} v_{Bwn}^* = 0. \tag{29}$$

Consequently, the total sum of the voltage commands is equal to zero. This means that no interference occurs between the individual-balancing control and the other controls.

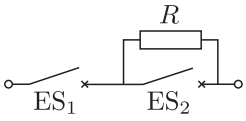


Fig. 14. Configuration of an auxiliary circuit used for initial charge.

3) Feedforward Control: The aim of the feedforward control is to improve the current controllability by producing the voltage commands v^*_{fu}, v^*_{fv}, and v^*_{fw}, which are identical to $v_{\mathrm{So}u}$, $v_{\mathrm{So}v}$, and $v_{\mathrm{So}w}$ shown in Fig. 6. Specifically, v^*_{fu} is given by

$$v^*_{fu} = \begin{cases} V_{\mathrm{H}} & \text{when } v_{\mathrm{tri}u} < d \\ V_{\mathrm{L}} & \text{when } v_{\mathrm{tri}u} > d. \end{cases} \tag{30}$$

It is noteworthy that a similar technique is widely used in grid-connected converters where the supply voltage is detected and used for feedforward control. In Fig. 9, v^*_{fu}, v^*_{fv}, and v^*_{fw} are further divided by three, which is the chopper-cell count, and given to each cell.

Finally, the command values for the low-voltage-side voltages of each cell, v^*_{Aun}, v^*_{Avn}, and v^*_{Awn}, are generated. Subsequently, they are normalized by each dc-capacitor voltage and compared with the triangular carriers (maximum value: 1, minimum value: 0) with a frequency f_{CA} and an initial-phase difference of 120° $(= 360^\circ/3)$.

C. Startup

The initial charge of dc capacitors used in each cell should be achieved for the startup of Fig. 5, and it can be achieved by the following two steps.

1) The first step is based on an auxiliary circuit.
2) The second step is based on control.

During the first step, all the power devices used in the main and auxiliary converters are OFF, except for those in S_{2u}, S_{2v}, and S_{2w}, which are in ON states. The auxiliary converters start the switching operation when the second step starts, whereas S_{1u}, S_{1v}, and S_{1w} are OFF, and S_{2u}, S_{2v}, and S_{2w} are ON.

Fig. 14 shows the configuration of the auxiliary circuit consisting of two electromagnetic switches, ES_1 and ES_2, and a resistor R. The circuit is inserted in terminal "X" as shown in Fig. 5; hence, the initial charge is achieved using V_{L}. ES_1 and ES_2 are OFF initially, and the charge starts by turning ES_1 ON. Each dc-capacitor voltage is charged to $V_{\mathrm{L}}/3$ via the diodes of S_{2u}, S_{2v}, and S_{2w} in the main converters and the upper diodes of each chopper cell. Then, ES_2 turns ON, and the first step is completed.

Subsequently, a control method is applied to increase each voltage more than $V_{\mathrm{L}}/3$, whose control block diagram is shown in Fig. 15. It consists of the feedback control and feedforward control, and the former control consists of a voltage major loop for making each dc-capacitor voltage, $\overline{v}_{Cx}$, to follow its command, v^*_C, producing a current command for initial charge. Then, a current minor loop for making each inductor current, $i_{Ax}(x : u, v, w)$, is to follow its command produced by the voltage major loop. Subsequently, a voltage $V_{\mathrm{L}}/3$ which is given by the feedforward control is added, producing the voltage reference for each cell, v^*_{Axn}. After $\overline{v}_{Cx}$ reaches the rated value, the second step finishes and the converter starts the normal operation described in Section II.

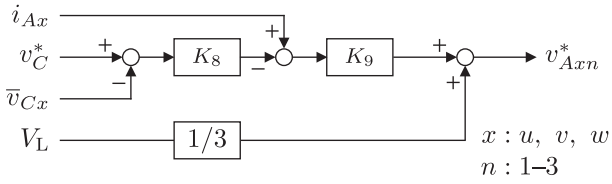
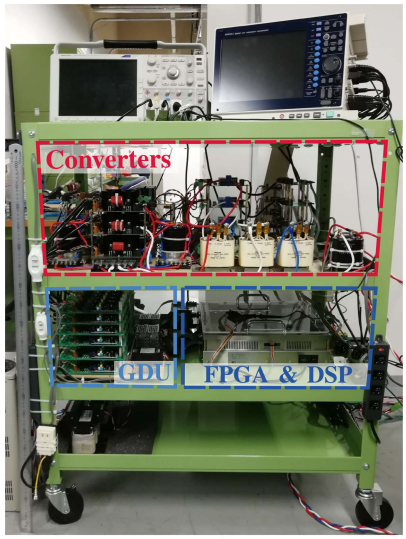


Fig. 15. Block diagram for the initial charge.



GDU: Gate Driver Units

Fig. 16. Photo of an experimental system.

TABLE I
CIRCUIT PARAMETERS OF FIG. 5 USED IN EXPERIMENTS

Rated power	P	2 kW
High-voltage-side voltage	V_{H}	200 V
Low-voltage-side voltage	V_{L}	120 V
DC-capacitor voltage	V_C	80 V
Chopper-cell count	N	3
Unit count	M	3
Carrier freq. (Main)	f_{CM}	450 Hz
Carrier freq. (Aux.)	f_{CA}	7.2 kHz
Equivalent carrier freq.	Nf_{CA}	21.6 kHz
Dead time	T_{D}	3 μs
AC inductor	L	0.5 mH (7.1%)
Snubber capacitor	C_s	3.0 μF
DC capacitor	C_{dc}	4.4 mF
DC-link capacitor	C_{fH}, C_{fL}	3.3 mF

Value in () is on a 200-V, 2-kW, and 450-Hz base.

V. EXPERIMENT

A. Experimental Conditions

Fig. 16 shows a photo of an experimental system rated at 200 V and 2 kW, which is used for the verification of Fig. 5. Table I summarizes the circuit parameters used in the experiments. Si-MOSFETs are used as power devices in the main and auxiliary converters. The carrier frequency of the main converters is set

to $f_{\rm CM} = 450$ Hz, and that of the auxiliary converters is set to $f_{\rm CA} = 7.2$ kHz, so that the equivalent switching frequency of each auxiliary converter is 21.6 kHz($= 7.2$ kHz $\times$ 3). The dead time of both converters is set to $T_D = 3\mu$s. In Fig. 5, the high- and low-voltage-side dc voltages are $V_{\rm H} = 200$ V and $V_{\rm L} = 120$ V, where they are realized using the Myway-Plus pCUBEs capable of regenerative operation. A battery energy storage system shown in Fig. 1, which is applied to the Japanese dc electric railway systems, has a dc catenary voltage $V_{\rm H}$ ranging from 0.95 to 2 kV and has a battery voltage $V_{\rm L}$ ranging from 0.5 to 0.713 kV, according to [4]. It corresponds to a voltage ratio $\frac{V_{\rm L}}{V_{\rm H}}$ ranging from 0.25 to 0.79. Considering the above, a voltage ratio was set to $\frac{V_{\rm L}}{V_{\rm H}} = 0.6$ in the experimental system. The relation $p \geq 0$ holds when the power is sent from the high-voltage side to the low-voltage side, and vice versa when $p < 0$, where p is the one-period average power. The snubber capacitance of the main converter is set to $C_s = 3.0\mu$F. The capacitance of each chopper cell is set to $C_{\rm dc} = 4.4$ mF, and the dc-capacitor voltage is set to $V_C = 80$ V. Here, $C_{\rm dc}$ is designed by setting $\Delta v_{Cu1} = 1.4$ V in (14). The capacitance of dc capacitors used in the high- and the low-voltage sides are set to $C_{fH} = C_{fL} = 3.3$ mF. The ac inductance is set to $L = 0.5$ mH, where L is designed by setting $\Delta i_A = 0.9$ A in (15) and the percent impedance is 7.1% based on P, $V_{\rm H}$, and $f_{\rm CM}$.

The control system consists of a digital signal processor (DSP) unit using the Texas Instruments TMS320C6678 and a field-programmable gate array (FPGA) unit using the Altera Cyclone IV. The FPGA unit including A/D converters detects the nine dc-capacitor voltages of each chopper cell, the three inductor currents, and the high- and the low-voltage-side dc voltages. The FPGA unit produces 24-bit gate signals in total.

The experimental "voltage" waveforms were captured using the Hioki Memory HiCorder 8861-50. The experimental "current" waveforms were captured using the Tektronix TCP0030A with a frequency band of 120 MHz, the Tektronix TCP0150 with a frequency band of 20 MHz, and the Tektronix TCP303 with a frequency band of 15 MHz.

B. Steady-State Performance

Fig. 17 shows experimental waveforms when $V_{\rm H} = 200$ V, $V_{\rm L} = 120$ V, and $p^* = 2$ kW, where the power is sent from the high-voltage side to the low-voltage side. p^* is the reference for p given by (26). The voltage and current waveforms correspond to those shown in Fig. 5. v_{Cu1}, v_{Cv1}, and v_{Cw1} are the dc-capacitor voltages of chopper cell 1 in each auxiliary converter, where a digital low-pass filter of 5 kHz is applied to them for reducing the measurement noise.

The device voltages $v_{{\rm S}1u}$ and $v_{{\rm S}2u}$ are 80 V ($= V_{\rm H} - V_{\rm L}$) or zero according to the switching states of the main converters. Further, a voltage drop that is proportional to the device current is superimposed on $v_{{\rm S}1u}$ and $v_{{\rm S}2u}$ as shown in Fig. 17 owing to the on resistance of the MOSFETs.

The inductor currents i_{Au}, i_{Av}, and i_{Aw} contain a 450-Hz ac component and a negative dc component. The dc current should flow for regulating the average value of p_A given by (2) to zero. Carefully looking into Fig. 17 reveals that the amplitudes

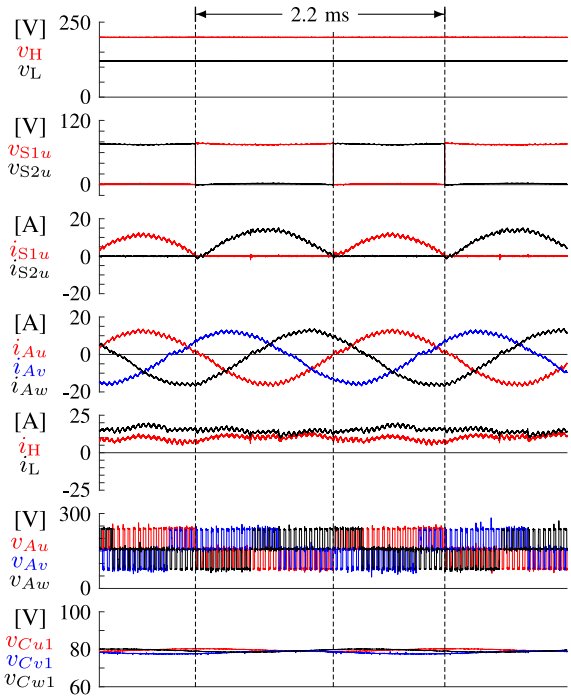


Fig. 17. Experimental waveforms of Fig. 5 when $v_{\rm H} = 200$ V, $v_{\rm L} = 120$ V, and $p^* = 2$ kW, where the power is sent from the high-voltage side to the low-voltage side.

of the 450-Hz ac component in i_{Au}, i_{Av}, and i_{Aw} are slightly different. The reason for this interesting phenomenon results from the cluster-balancing control compensating uneven loss distribution between phases. However, this imbalance gives little effect on the circuit operation, because it is much smaller than the converter capacity.

It was confirmed from the waveforms of $v_{{\rm S}1u}$, $v_{{\rm S}2u}$, $i_{{\rm S}1u}$, and $i_{{\rm S}2u}$ that the ZCS was achieved in ${\rm S}_{1u}$ and ${\rm S}_{2u}$ by giving d^* as shown in Fig. 8. Moreover, no surge voltage occurred in ${\rm S}_{1u}$ and ${\rm S}_{2u}$ owing to the beneficial effect of the ZCS. Meanwhile, $i_{{\rm S}1u}$ and $i_{{\rm S}2u}$ contain a slight ringing current which is not included in i_{Au}. This current corresponds to the current flowing in the snubber capacitor C_s at every switching transition, and it does not flow in the power devices. It can be suppressed by connecting an appropriately designed resistor in series with C_s.

The waveforms of $i_{\rm H}$ and $i_{\rm L}$ are regarded as dc currents with less ac components by applying the interleaved configuration. The output voltages of the auxiliary converters v_{Au}, v_{Av}, and v_{Aw} are three-level waveforms with a voltage step of 80 V ($= V_C$) owing to the phase-shifted PWM. Each output voltage is the sum of voltage components produced by feedforward control, power-flow control, and dc-capacitor voltage control. In addition, 21.6-kHz switching-ripple voltages are included.

The dc-capacitor voltages v_{Cu1}, v_{Cv1}, and v_{Cw1} show that their dc components are well regulated to the command value of 80 V. Meanwhile, the ac components included is small in amplitude, because it is inversely proportional to $f_{\rm CM}$.

Fig. 18 shows the experimental waveforms when $V_{\rm H} = 200$ V, $V_{\rm L} = 120$ V, and $p^* = -2$ kW, where the power is sent

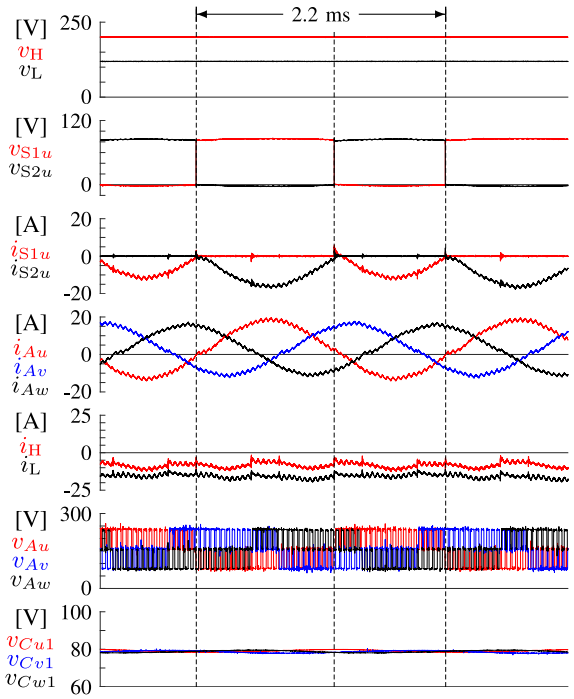


Fig. 18. Experimental waveforms of Fig. 5 when $v_{\rm H} = 200$ V, $v_{\rm L} = 120$ V, and $p^* = -2$ kW, where the power is sent from the low-voltage side to the high-voltage side.

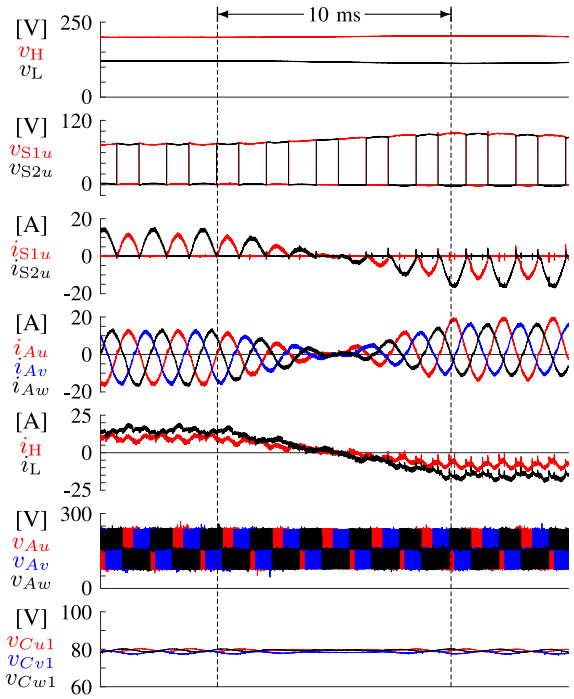


Fig. 19. Experimental waveforms of Fig. 5 when $v_{\rm H} = 200$ V and $v_{\rm L} = 120$ V, where p^* was changed from 2 kW to -2 kW in 10 ms.

from the low-voltage side to the high-voltage side. A comparison of Figs. 17 and 18 shows that both waveforms are similar except for the following three differences.

1) The polarity of the dc current included in each inductor current was changed from negative to positive.
2) That of $i_{\rm H}$ and $i_{\rm L}$ was changed from positive to negative owing to the reverse of power flow.
3) That of i_{S1u} and i_{S2u} was changed from positive to negative.

Similar to Fig. 17, a ringing current is included in i_{S1u} and i_{S2u} flowing in the snubber capacitor. It was confirmed that the ZCS was achieved in $\rm S_{1u}$ and $\rm S_{2u}$ regardless of the power-flow direction. The dc-capacitor voltages v_{Cu1}, v_{Cv1}, and v_{Cw1} show that their dc components are well regulated to the command value of 80 V.

C. Transient-State Performance

Fig. 19 shows experimental waveforms of Fig. 5 when $v_{\rm H} = 200$ V and $v_{\rm L} = 120$ V, where p^* was changed from 2 kW to -2 kW in 10 ms. During the transition, $v_{\rm H}$ increased and $v_{\rm L}$ decreased as shown in Fig. 19. As a result, the device voltages v_{S1u} and v_{S2u} increased transiently. It was confirmed that i_{S1u} and i_{S2u} realized the ZCS even in transient-state conditions where a steep change in current occurred. Moreover, no overcurrent occurred in i_{Au}, i_{Av}, and i_{Aw} as well as in $i_{\rm H}$ and $i_{\rm L}$. The dc-capacitor voltages v_{Cu1}, v_{Cv1}, and v_{Cw1} show that their dc components are well regulated to a command value of 80 V.

Fig. 20 shows the experimental waveforms of Fig. 5 when $p^* = 2$ kW and $v_{\rm L} = 120$ V, where $v_{\rm H}$ was changed from 200 to 150 V under a ramp change in 10 ms. The envelope curve formed

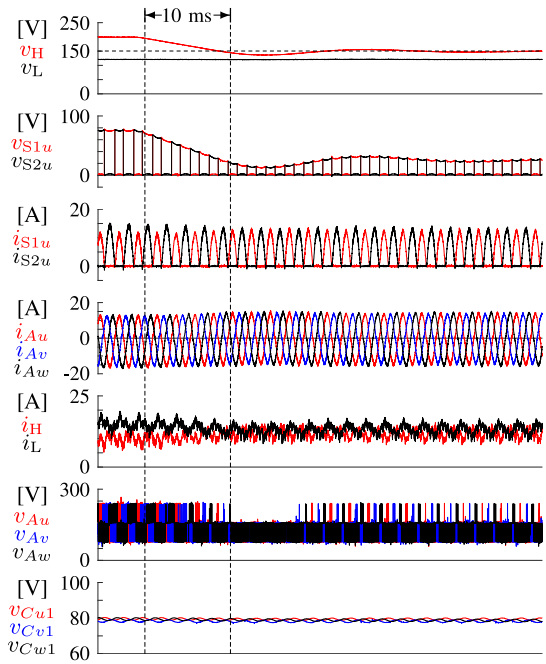


Fig. 20. Experimental waveforms of Fig. 5 when $p^* = 2$ kW and $v_{\rm L} = 120$ V, where $v_{\rm H}$ was changed from 200 to 150 V under a ramp change in 10 ms.

by v_{S1u} and v_{S2u} is similar to the waveform of $v_{\rm H}$, because the device voltages under OFF states are given by $v_{\rm H} - v_{\rm L}$, where $v_{\rm L}$ is constant. It was confirmed that i_{S1u} and i_{S2u} realized the ZCS even in transient-state conditions where a steep change in voltage occurred. Moreover, no overcurrent occurred in i_{Au}, i_{Av}, and i_{Aw} as well as in $i_{\rm H}$ and $i_{\rm L}$. The dc-capacitor voltages

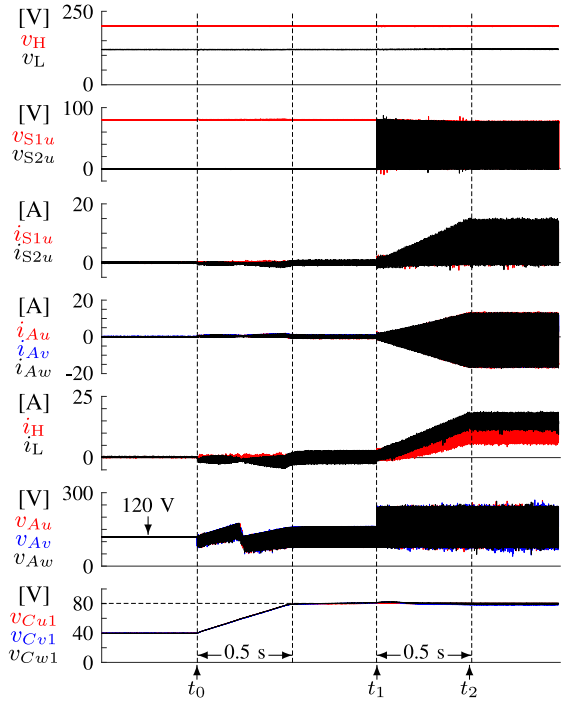


Fig. 21. Experimental waveforms during the start-up when $v_{\rm H} = 200$ V, $v_{\rm L} = 120$ V.

v_{Cu1}, v_{Cv1}, and v_{Cw1} show that their dc components are well regulated to a command value of 80 V. It can be concluded from Figs. 19 and 20 that Fig. 5 shows superior transient performance without any overvoltage/overcurrent, and the ZCS of the device currents is always achievable under an arbitrary voltage/current.

Fig. 21 shows the experimental waveforms of Fig. 5 during the startup, where $v_{\rm H} = 200$ V and $v_{\rm L} = 120$ V. The startup procedure can be divided into the following four periods.

1) $t < t_0$: During this period, all the power devices used in the main and auxiliary converters are OFF, except of those in S_{2u}, S_{2v}, and S_{2w} which are in the ON states. Hence, the relations $v_{S1u} = 80$ V$(= v_{\rm H} - v_{\rm L})$ and $v_{S2u} = 0$ always hold in Fig. 21. Further, the relation of $v_{Au} = v_{Av} = v_{Aw} = v_{\rm L}$ holds. In the experiment, each dc-capacitor voltage was charged from zero to 40 V $(= v_{\rm L}/3)$ by increasing $v_{\rm L}$ from zero to 120 V gradually for convenience, although an actual system uses the auxiliary circuit shown in Fig. 14 along with a fixed voltage of $v_{\rm L}$ represented by a battery voltage.
2) $t_0 \le t < t_1$: The control method shown in Fig. 15 was applied during this period, and the command value of the dc-capacitor voltage, v_C^*, was increased in a ramp change from 40 to 80 V in 0.5 s. A negative dc current was included in $i_{\rm L}$ for charging each dc-capacitor voltage. Meanwhile, the relations $v_{S1u} = 80$ V$(= v_{\rm H} - v_{\rm L})$ and $v_{S2u} = 0$ still hold in this period, and no current was contained in $i_{\rm H}$. After v_C^* reached 80 V, each dc-capacitor voltage was kept at 80 V.
3) $t_1 \le t < t_2$: Fig. 5 started power-flow control at t_1 by applying the control methods shown in Figs. 8–13, where p^* was increased in a ramp change from 0 to 2 kW in 0.5 s.
4) $t_2 \le t$: After p^* reached 2 kW, the startup procedure was completed and the converter continued steady-state operation.

It was confirmed that a seamless startup was achieved from the initial charge to the steady-state operation.

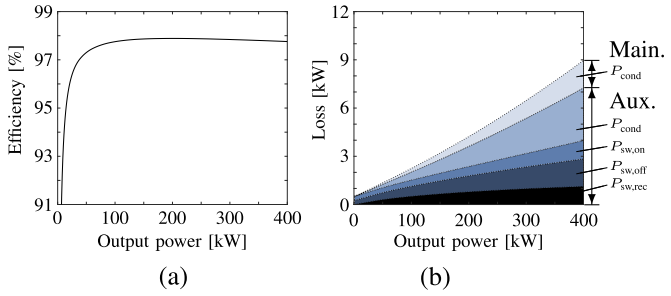


Fig. 22. Estimated efficiency and loss breakdown of Fig. 5 where $V_{\rm H} = 1.5$ kV, $V_{\rm L} = 0.75$ kV, and $V_{\rm C} = 0.6$ kV. (a) Efficiency. (b) Loss breakdown.

VI. Loss Analysis of an Actual System

The loss analysis of an actual dc-dc converter system is conducted on the basis of specification data supplied by manufacturers. The assumed circuit configuration is the same as in Fig. 5, where the switching frequencies are set to $f_{\rm CM} = 450$ Hz and $f_{\rm CA} = 7.2$ kHz, respectively. The assumed rated power is $P = 400$ kW, the assumed high-voltage-side voltage is $V_{\rm H} = 1.5$ kV, the assumed low-voltage-side voltage is $V_{\rm L} = 0.75$ kV, and the assumed dc-capacitor voltage is $V_C = 0.6$ kV. In addition, the following conditions are considered.

1) The conduction loss $P_{\rm cond}$ and turn-ON/OFF switching loss $P_{\rm sw,on}/P_{\rm sw,off}$ are considered in IGBTs, and the conduction loss $P_{\rm cond}$ and turn-OFF switching loss $P_{\rm sw,rec}$ are considered in diodes.
2) The switching loss of the main converter is assumed to be zero.
3) The conduction loss and switching loss are calculated based on the voltage, current, and loss characteristics when the junction temperature is 125°C, which are described in the specification sheets provided by manufacturers.
4) The ac components included in each dc-capacitor voltage are set to zero for a simple and easy analysis.
5) The losses of passive components are assumed to be zero.

Fig. 22(a) shows the relationship between the output power and efficiency. The power devices 2MBI550VN-170-50 (Si-IGBT, 2-in-1, 1.7 kV) manufactured by Fuji Electric is assumed to be used in the main converters, where the device characteristics are provided in [28]. The power devices 2MBI600XDE120-50 (Si-IGBT, 2-in-1, 1.2 kV) manufactured by Fuji Electric is assumed to be used in the auxiliary converter, where the device characteristics are provided in [29]. The maximum efficiency can be obtained as 97.9% when the power is 200 kW. Fig. 22(b) shows the relationship between the output power and loss including the loss breakdown. It is obvious that the loss of the auxiliary converter is dominant over that of the main converter. Hence, it is required to apply low-loss power devices to the auxiliary converters to improve the converter efficiency.

VII. Conclusion

This article has presented a bidirectional nonisolated dc–dc converter based on switched-capacitor converters. It is characterized by achieving the ZCS of power devices used in the main converter under arbitrary load conditions and arbitrary voltage ratio of high-voltage-side voltage and low-voltage-side voltage. The validity of the converter has been confirmed by experiments using a 200-V, 2-kW downscaled model. In addition, the loss analysis of an actual dc–dc converter system rated at 400 kW has been conducted, and it has been shown that the converter can achieve high-efficiency operation over wide operating areas.

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