Comprehensive Analysis, Design, and Experiment of Shoot-Through Faults in MMC Based on IGCT for VSC-HVDC

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***Abstract*—Modular multilevel converter (MMC) based on integrated gate commutated thyristor (IGCT) with high reliability, low cost, and voltage drop is a promising choice for high-voltage dc transmission based on the voltage-source converter. This article gives a comprehensive analysis, design, and experiment of shoot-through faults in IGCT-MMC. First, the designed structure of the submodule based on the IGCT (IGCT-SM) is introduced and an equivalent circuit is established with the accurate estimation of the stray inductances. Then, the failure processes of devices and the behavior of the clamping diode are discussed in detail. Meanwhile, the mechanical stress of the connecting copper bar is analyzed during shoot-through faults. After that, an experimental platform is built for performing the shoot-through faults. Both tests with switching action and without switching action are carried out under the dc-link capacitor and voltage with 10 mF and 2.5 kV. The results show that although IGCT cannot turn OFF the fault current, it can withstand the fault current. The whole structure maintains stable without any cracked housing package or copper bars under the surge current of 266 kA/0.40 ms. The 24-h short-circuit test under 3.15 kA shows that failed IGCT has an extremely low ON-state voltage of not more than 1.2 V and is suitable for bypassing the faulty submodule when a destroyed shoot-through fault occurs.**

***Index Terms*—Failure process, integrated gate commutated thyristor (IGCT), modular multilevel converter (MMC), shoot-through fault, short-circuit characteristics.**

I. Introduction

IN RECENT years, high-voltage dc transmission based on the voltage-source converter (VSC-HVdc) has become one of the best solutions for connecting different ac grids with the back-to-back configuration as well as ac grids and renewable energy sources, such as onshore and offshore wind farms [1]–[4]. And modular multilevel converter (MMC) becomes the main technology of VSC-HVdc for advantages, including large capacity, low-voltage harmonics, and flexible switching frequency [5], [6]. In China, the latest projects of VSC-HVdc include China state grid's four-terminal Zhangbei HVdc system (up to ±500 kV/3000 MW) [7] and China Southern power grid's three-terminal Wudongde HVdc system (up to ±800 kV/5000 MW) [8]. Power semiconductors, such as insulated gate bipolar transistor (IGBTs) and injection enhanced gate transistor (IEGTs), have been applied in these projects of MMC [9]–[11]. However, the conducting loss and the manufacturing costs of IGBTs in MMC are very high [12], [13].

To decrease the loss and costs of MMC, the integrated gate commutated thyristor (IGCT) has been discussed a lot in recent years [12]–[14]. IGCT is a kind of high-power semiconductors with extremely low conducting loss [15] and the price of an IGCT is about a third or half of an IGBT. This is because IGCT inherits most of the structures and manufacture processes of thyristors. Besides, the reliability of IGCTs is higher than that of IGBTs [16]–[19]. Although IGCT has higher turn-OFF losses than IGBTs, the low frequencies in MMC help IGCT overcome this [20]. And the problem of power supply of IGCTs can be solved with a kind of special self-powered supply source [14]. Besides, a designed compact structure of the submodule based on IGCT (IGCT-SM) can save lots of volumes for series connection [14]. These make IGCT a very promising choice for MMC with high voltage and large capacity.

Different from IGBTs, the maximum controllable current of commercial 4-in IGCT is 5 kA and there is no desaturation process in IGCT. Therefore, the MMC cannot turn OFF the IGCT successfully when a shoot-through fault occurs in IGCT-SM; it is needed to employ IGCT's characteristics of high surge current and package with rupture resistance to withstand the fault current. However, there are no analysis and experiments about the shoot-through faults of MMC based on IGCT in the pieces of literature.

Consider the situation above, this article gives a comprehensive analysis, design, and experiment of shoot-through faults in IGCT-SM. Section II compares the differences of the

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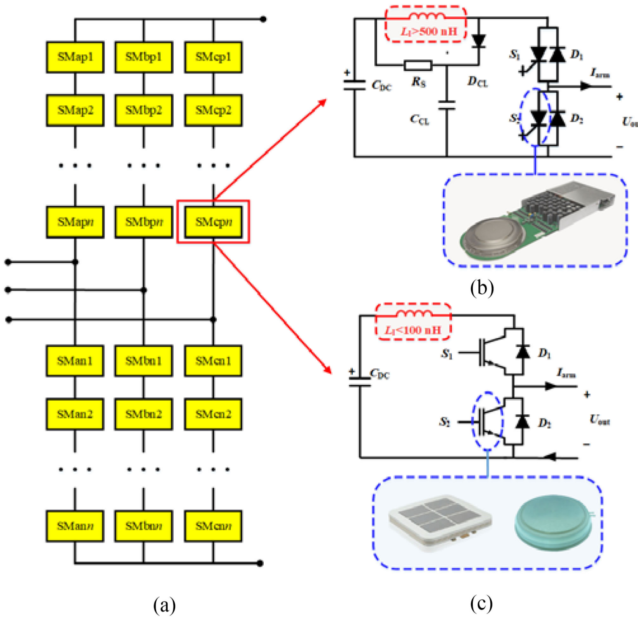

Fig. 1. Comparison of the topologies and anode inductances in different SMs for MMC. (a) Typical MMC system. (b) IGCT-SM. (c) IGBT-SM.

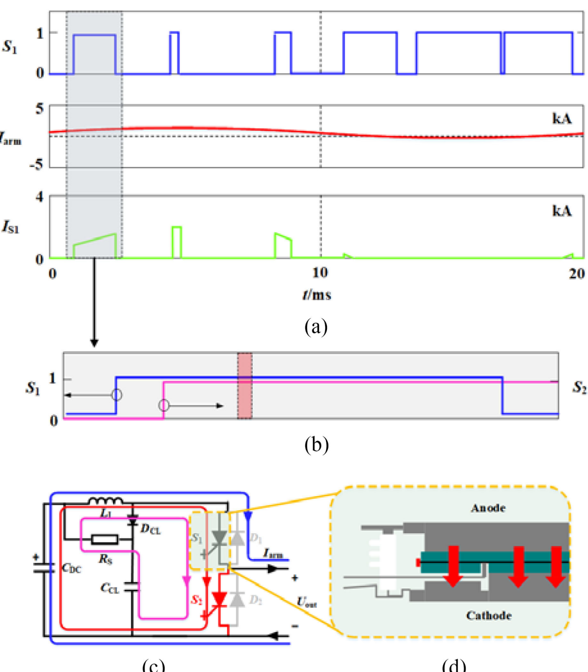

Fig. 2. Analysis of the shoot-through fault without switching action. (a) Typical waves of S1'current. (b) Triggering signals of S1 and S2. (c) Current loops of the shoot-through fault. (d) Current paths in IGCT without switching action.

shoot-through faults in the submodule based on IGBT (IGBT-SM) and IGCT-SM. And different shoot-through faults in IGCT-SM are analyzed according to the triggering signals. Section III gives the designed structure of IGCT-SM and the equivalent circuit based on the extracted stray inductances is introduced. Then, the failure processes of devices and the behavior of the clamping diode are discussed in detail using the equivalent circuit. Meanwhile, the mechanical stress and deformation of the connecting copper bar under the shoot-through fault current in IGCT-SM is simulated. In Section IV, an experimental platform is built for performing the shoot-through faults. Then, both shoot-through tests with and without IGCT's switching action are carried out. Finally, a continuous short-circuit test of the failed IGCT is taken without decompression of IGCT-SM.

II. Analysis of Shoot-Through Faults of IGCT-MMC

A. IGCT-SM for MMC

The topology of IGCT-MMC is shown in Fig. 1(b). For IGCT-SM, S_1 and S_2 are IGCTs, meanwhile D_1 and D_2 are freewheeling diodes matched with S_1 and S_2. L_{I} is the anode inductance. D_{CL}, R_S, and C_{CL} make up the clamping circuit. I_{arm} represents the output current of IGCT-SM and U_{out} represents the output voltage of IGCT-SM. The directions, as shown in Fig. 1(b), are set to positive direction. Compared with the topology of IGBT-SM for MMC, as shown in Fig. 1(c), IGCT-SM for MMC has a larger anode inductance L_I and an extra clamping circuit. The larger anode inductance is used to protect the freewheeling diode from being destroyed by the high *di/dt* rate during the diode's reverse recovery period; this is because the positive feedback effects existing in the turn-ON process of IGCT make the *di/dt* uncontrollable. The extra clamping circuit is used to limit the overvoltage caused by the anode inductance when IGCT turns OFF.

When a shoot-through fault occurs, there are significant differences between the behaviors in IGCT-SM and IGBT-SM. First, in the early stage of the fault current in IGBT, the devices are not destroyed and the fault current will be limited to a certain value for not more than 10 μs due to the desaturation characteristics of IGBT. During this time, IGBT can turn OFF the fault current but the rise rate of fault current is almost unlimited in IGCT-SM. So, it is almost impossible for IGCT to turn OFF the fault current successfully and the destruction of IGCTs is almost inevitable. Second, the protection mentioned is complex and challenging for IGBTs and once IGBT gets destroyed due to the heat accumulation in the desaturation period, then a destructive fault current occurs due to the extremely low stray inductance in IGBT-SM. Under the same discharge energy, the anode inductance in IGCT-SM will help limit the fault current when the shoot-through fault occurs.

B. Shoot-Through Fault of IGCT-SM Without Switching Action

According to the directions of I_{arm} and U_{out}, there are four operation states of IGCT-SM in MMC, matching with the arm current flowing in S_1, D_1, S_2, and D_2. When the arm current is flowing in S_1 and S_2 is triggered by mistake or a symmetrical situation occurs, then a shoot-through fault happens.

Take the shoot-through fault in the former situation as an example. Fig. 2(a) gives a typical situation of S_1's working stage, including the pulsewidth modulation signals and currents of S_1. Then, when S_2 is triggered by mistake, as shown in Fig. 2(b), S_1 and S_2 are conducting for a long period without any switching action. Finally, they will be destroyed by high surge currents.

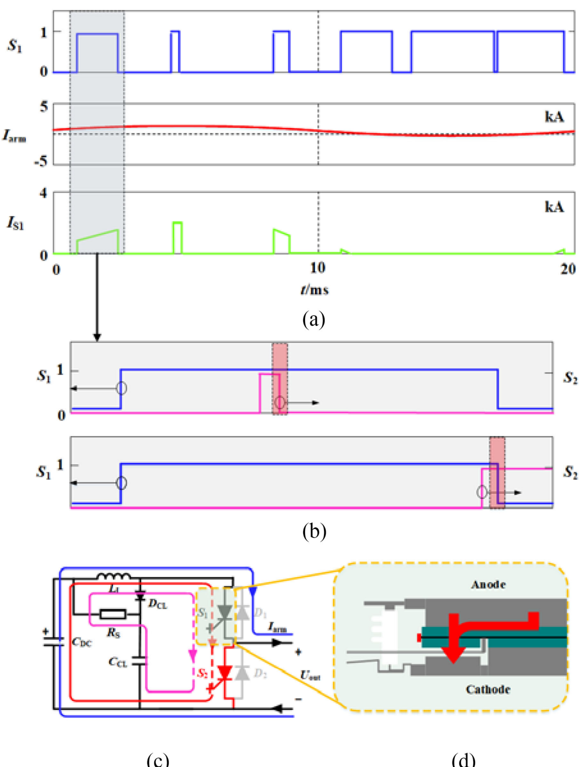

Fig. 3. Analysis of the shoot-through fault with switching action. (a) Typical waves of S_1'current. (b) Triggering signals of S_1 and S_2. (c) Current loops of the shoot-through fault. (d) Current paths in IGCT with switching action.

Before S_2 is triggered, S_1 is conducting the arm current and the SM's output voltage is decided by the capacitor C_{DC}. When the mistaken triggering occurs, the capacitor C_{DC} is discharged through the anode inductance L_{I} and the four devices. And the clamping capacitor C_{CL} is discharged through the clamping resistance, the anode inductance, and the four devices, which contributes little current to the total fault current. The SM's output voltage is decided by the states of S_2 and D_2, as shown in Fig. 2(c). Due to the full turn-ON of the devices, the surge current will flow in both the inner and outer regions of the chip, as shown in Fig. 2(d).

C. Shoot-Through Fault of IGCT-SM With Switching Action

However, in the typical situation of S_1's working stage in Fig. 3(a), when S_2 is triggered by mistake, there may be other situations, as shown in Fig. 3(b).

1) S_2 is triggered by a narrow pulse and will perform a turn-OFF action, as shown in the first situation in Fig. 3(b). Because the fault current will rise to tens of kiloampere in such short time, S_2 will get failed first in the turn-OFF process.
2) S_2 is triggered just before S_1 begins to turn OFF, as shown in the second situation in Fig. 3(b). At this time, S_1 will get failed in the turn-OFF process.

In both two kinds of situations, the failed IGCTs will suffer the fault current in the following period, as shown in Fig. 3(c), and the current loops are same to those in Section II-B. But these situations include the failure of turn-OFF process of IGCT. And this is different from the failure, which is caused by the surge current. In the turn-OFF process of IGCT, the current will usually get concentrated in the outer regions of the chip and the energy is dissipated in fewer areas, causing larger thermal stress in the housing package, as shown in Fig. 3(d).

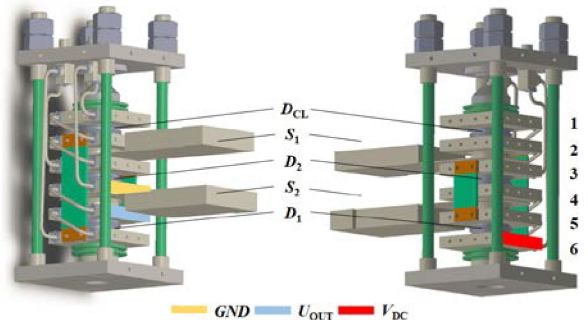

Fig. 4. Design for the IGCT-SM valve series.

III. Design and Characterization of IGCT-SM Under Shoot-Through Faults

A. Design and Equivalent Circuit of IGCT-SM Based on Practical Valve Series

To minimize the volume of IGCT-SM, the connection of S_1, D_1, S_2, and D_2 in a series is proper. Considering the position of D_{CL} and the insulation distance of IGCTs, the final designed IGCT-SM valve series is shown in Fig. 4. The terminal of *GND*, U_{OUT}, and V_{DC} is connected at the fourth, fifth, and sixth heat sink, independently. The anode of S_1 (the second heat sink) and the cathode of D_1 (the sixth heat sink) are connected by a long copper bar. And the cathode of S_1 (the third heat sink) and the anode of D_1 (the fifth heat sink) are connected by a short copper bar.

Because the positions of IGCTs and diodes in the submodule are not spatially symmetric. There exist different stray inductances between them. Fig. 5(a) and (b) shows the current loops of V_{DC}-S_1-S_2-*GND* and *GND*-D_2-D_1-V_{DC} in the real IGCT-SM. Then, the equivalent stray inductances can be extracted from the current loops between the terminals of the devices. For example, L_{stray3} stands for the stray inductance between the cathode of S_2 and *GND*, meanwhile L_{stray2} stands for the stray inductance between the cathode of S_1 and the anode of S_2, which also stands for that between the cathode of D_2 and the anode of D_1. Based on the extracted equivalent stray inductances, a detailed equivalent circuit of IGCT-SM for MMC is shown in Fig. 5(c).

B. Stray Inductance Extraction of IGCT-SM

According to the analysis above, the stray inductances are estimated in the AnsysQ3D extractor considering the equivalent resistivity of the devices. Then, the curves of the inductances following frequencies are shown in Fig. 6. It is found that the long copper bar on the side of the structure contributes to L_{stray1} greatly and makes L_{stray1} than the stray inductances else. Then,

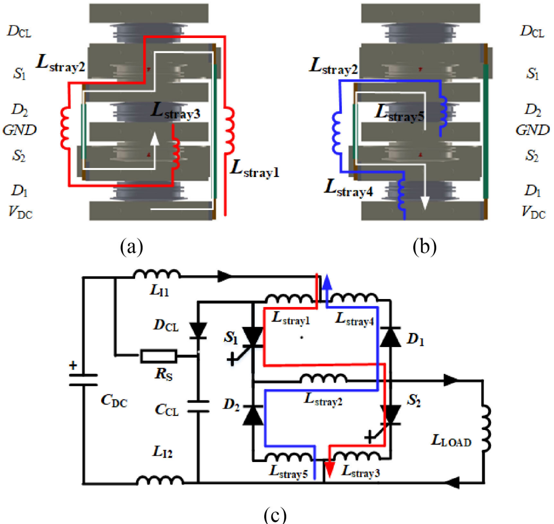

Fig. 5. Analysis of the stray inductances in IGCT-SM. (a) Current loop of V_{DC}-S_1-S_2-*GND*. (b) Current loop of *GND*-D_2-D_1-V_{DC}. (c) Equivalent circuit of IGCT-SM for MMC.

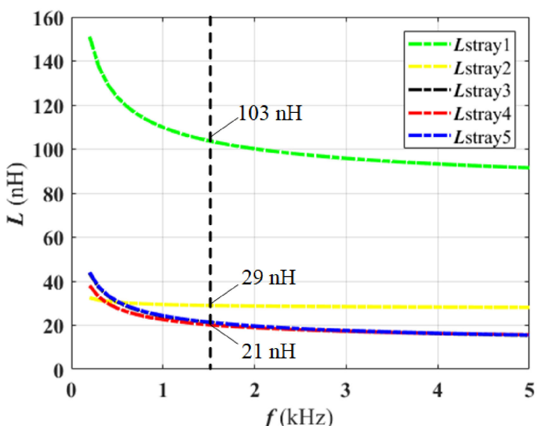

Fig. 6. Stray inductances following frequencies extracted in AnsysQ3D.

the inductances at the frequency of 1.5 kHz are used to simulate the process of the shoot-through fault in MATLAB Simulink. The circuit simulation assumes that the dc-link capacitor/voltage is 10 mF/2800 V and the total loop inductance is 0.75 μH.

C. Failure Processes of IGCT-SM Under Shoot-Through Fault

First, it is assumed that all devices are not destroyed in the shoot-through fault. Because the inductance of L_{stray1} is much larger than those else, the decreasing rate of the current in S_1 is slower than that in S_2, which also means the delay of crossing the zero point. Due to Kirchhoff's current law, the current difference between S_1 and S_2 is compensated by the difference between D_1 and D_2, so the current in D_1 increases faster than that in D_2 and the maximum difference is nearly 100 kA. As a result, D_1 will reach the thermal breakdown limitation in advance, as shown in Fig. 7. The positive directions of the currents in D_1, D_2, S_1, and S_2 are all from the anode to the cathode.

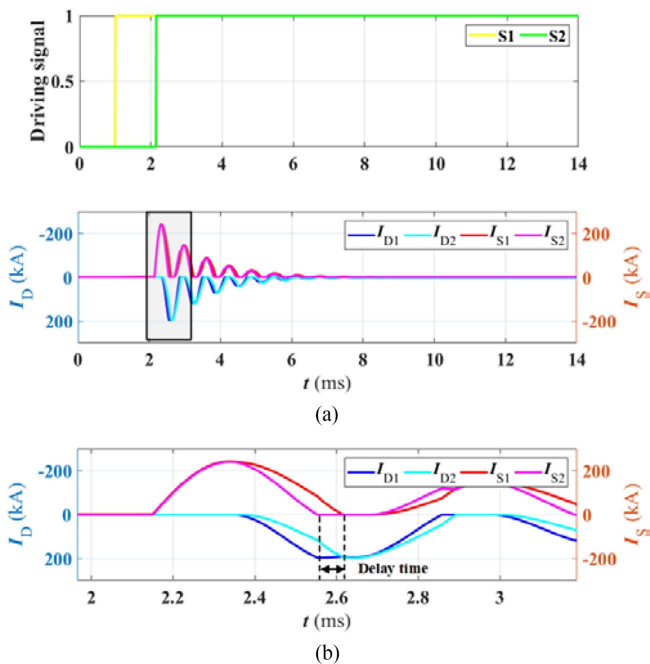

Fig. 7. Simulated current waves assuming no device is undamaged. (a) Total discharge wave with the driving signals. (b) Magnified waveform of the shaded area in (a) showing the delay time of zero-point crossing.

In Fig. 8, S_1 and S_2 break down thermally at t_1. After the current of S_2 passes the zero point at t_2, it shares the current with D_2, then the risk of D_2's failure is reduced. Then, at t_3, D_1 breaks down thermally due to the high surge current. The reduced equivalent resistance of failed D_1 will further decrease the risk of D_2's failure. As a result, D_2 is protected by failed S_2 and D_1 together. The current paths during the following subsequent periods are shown in Fig. 8(c) and (d) in which the red and blue arrows show the positive and negative direction, respectively.

D. Behavior of the Clamping Diode Under Shoot-Through Fault

During the shoot-through fault in IGCT-SM, there are actually two capacitors discharging. One is the dc capacitor C_{DC} and another is the clamping capacitor D_{CL}. D_{CL}'s cathode is connected to the clamping capacitor C_{CL}, while the anode is connected to S_1. Based on this, simulation without D_{CL} is shown in Fig. 9(a). It is found that the anode potential of D_{CL} oscillates in a small range because the sum of the destroyed devices' voltage drops and the stray inductances' voltages are low. However, the cathode potential oscillates in a large range because C_{CL} has a large initial voltage (over 2 kV). As a result, D_{CL} will turn ON when the voltage between D_{CL}'s anode and cathode is over the turn-ON threshold voltage (usually less than 3 V). Fig. 9(b) illustrates D_{CL}'s current and voltage in the simulation with D_{CL}. The result shows that D_{CL}'s maximum peak current is less than 1 kA and will not be destroyed because C_{CL} is much smaller than C_{DC} and stores little energy.

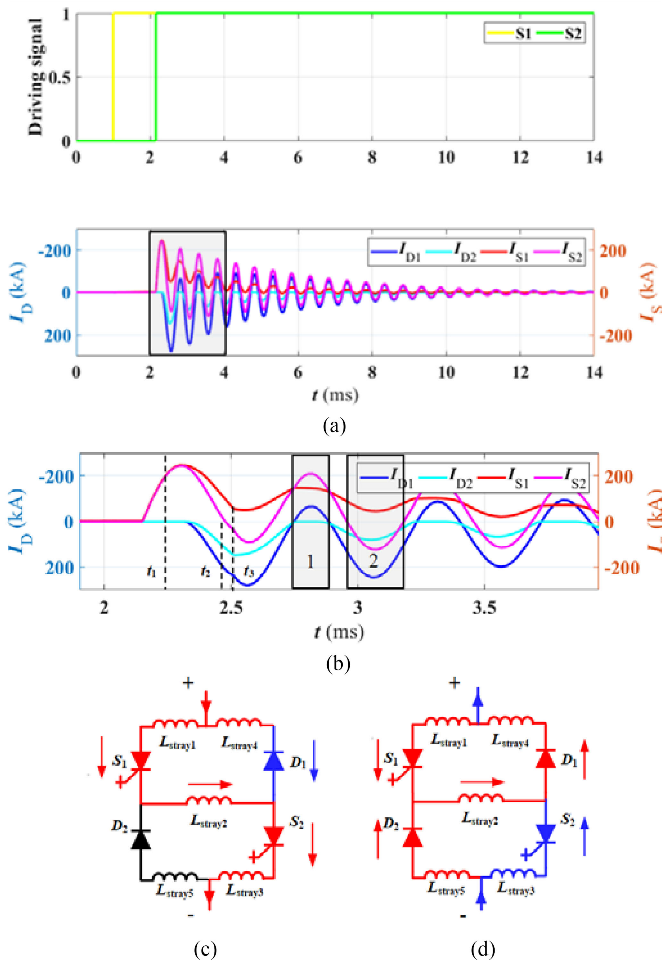

Fig. 8. Simulated current waves and analyzed current paths considering the failure processes of the devices. (a) Total discharge wave with the driving signals. (b) Magnified waveform of the shaded area in (a). (c) Current path of the shaded area 1 in (b). (d) Current path of the shaded area 2 in (b).

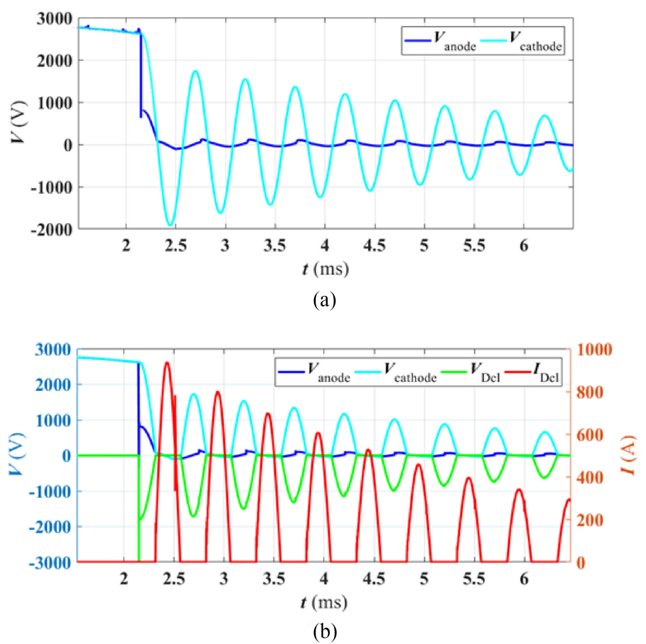

Fig. 9. Behavior of D_{CL} during the short-circuit fault. (a) Simulation without D_{CL}. (b) Simulation with D_{CL}.

E. Mechanical Stress Characterization of IGCT-SM Under Shoot-Through Fault

Due to the high transient current in the shoot-through fault, the long copper bar that causes L_{stray1} may suffer a huge mechanical force in short time. To evaluate the reliability of this copper bar, the mechanical stress is simulated in Comsol Multiphysics. The structure of the submodule is simplified, as shown in Fig. 10(a), including $S_1, S_2, D_1, D2$, and the heat sinks between them. The size of the heat sink is 155 mm × 155 mm × 25 mm and the size of the long copper bar is 5 mm × 65 mm × 231 mm. The two sides of the copper bar are set to fixed displacement before simulation. And the current loop of V_{DC}-S_1-S_2-*GND* is set with the fitted current, as shown in Fig. 10(b); the expression of the current is as follows:

$$I_{S_1}=100\left(e^{-t}-e^{-25t}\right)\left(2+\sin\left(\frac{2\pi t}{0.5}\right)\right)[kA]. \quad (1)$$

Then, the load applied to the copper bar is provided by the ampere force caused by the transient surge current and flux densities around. Fig. 11(a) shows the distribution of flux density in the y–z cut plane ($x = 0$) at $t = 0.13$ ms, which is the first peak of the fault current. It shows that the flux densities are rather high with average transient flux densities above 2 T near the copper bars. Fig. 11(b) shows the directions of the force on the copper bar's surfaces and the displacement at $t = 1.00$ ms. The force on the surface outside is much larger than that on the surface inside, so the copper bar bends outward. Because of the continuous effects of the ampere force, the copper will continue moving until the completion of the final shaping after the largest several surge current wave heads. The final maximum displacement in the middle is more than 3 mm. Fig. 11(c) shows the distribution of the mechanical stress at $t = 1.00$ ms and the maximum stress in the middle of the copper bar is more than 400 MPa.

IV. Experiment of Shoot-Through Faults for IGCT-SM in MMC Submodule

A. Experimental Platform and Test Sequences

The topology of the test circuit of shoot-through faults is shown in Fig. 12 and the parameters are listed in Table I. The dc-link capacitor C_{DC} of IGCT-SM is connected to the dc source with a 5 kV isolation switch K_1. Meanwhile, the capacitor C_{DC} is connected to the discharge resistor R with another isolation switch K_2. The output and *GND* terminal of IGCT-SM are connected to the load inductor L_{LOAD}.

The tested IGCTs and diodes are 4.5 kV/5 kA IGCT-plus and 4.5 kV/2.6 kA fast recovery diode, as shown in Fig. 12. The picture of the real test circuit is illustrated in Fig. 13, and the positions of the dc-link capacitor, the discharge circuit, the load inductor, and the devices are marked. To ensure the safety of the experiment, the circuit is surrounded by explosion proof boards.

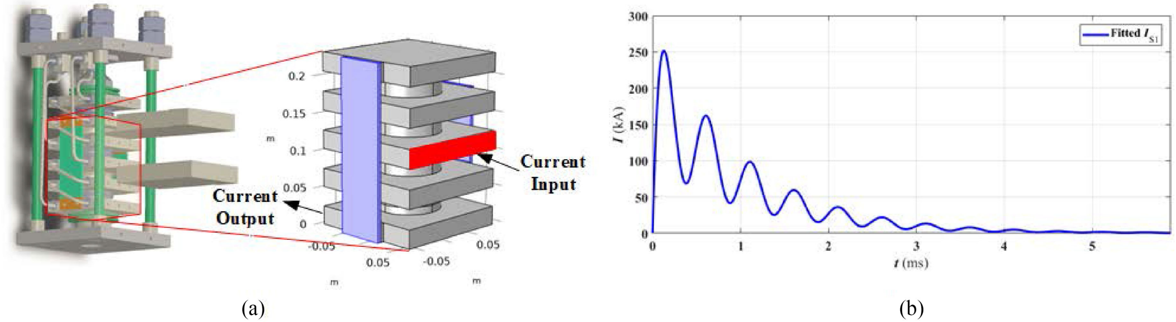

Fig. 10. Model for the mechanical stress simulation. (a) Simplified MMC submodule. (b) Simplified input surge current.

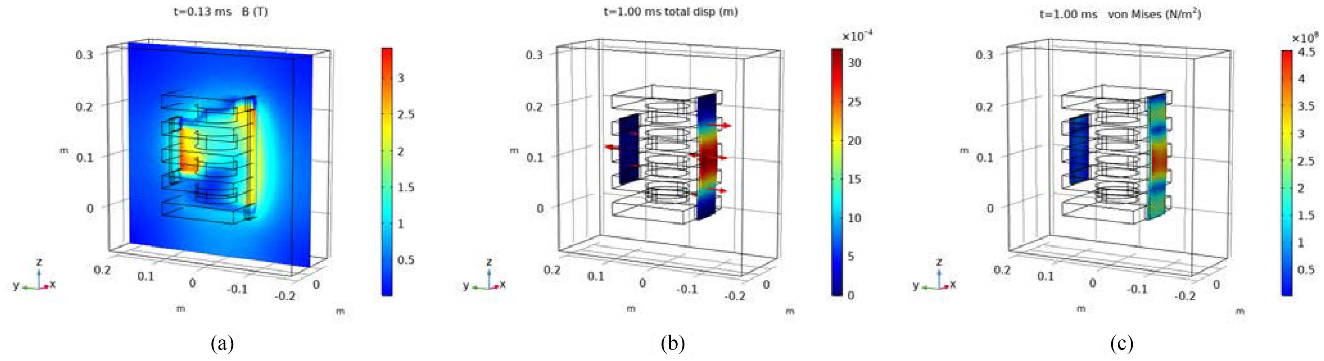

Fig. 11. Analysis of the electromechanical effects under the assumed input surge current. (a) Maximum magnetic flux density at $t = 0.13$ ms. (b) Maximum displacement at $t = 1.00$ ms. (c) Maximum stress at $t = 1.00$ ms.

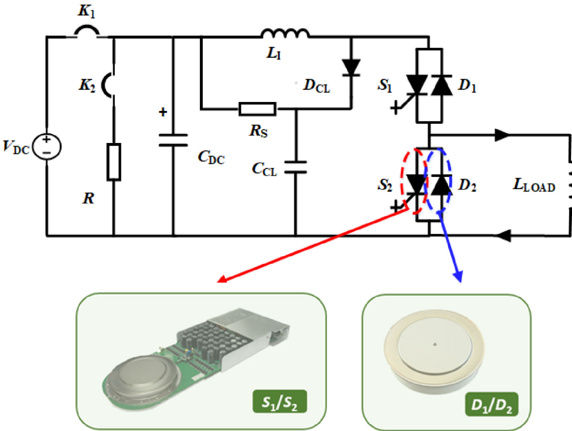

Fig. 12. Topology of the shoot-through test platform.

TABLE I
PARAMETERS OF THE TEST CIRCUIT

Component	Symbol	Unit	Value
DC source	V_{DC}	V	3000
Isolation switch	K_1, K_2	V	5000
Discharge resistor	R	kΩ	1
DC-Link capacitor	C_{DC}	mF	10
Anode inductor	L_I	uH	0.6
Clamping resistor	R_S	Ω	2
Clamping capacitor	C_{CL}	uF	4
Clamping diode	D_{CL}	kV/kA	4.5/1.1
IGCT	S_1, S_2	kV/kA	4.5/5.0
Fast recovery diode	D_1, D_2	kV/kA	4.5/2.6
Load inductor	L_{LOAD}	mH	1

And three monitors are arranged from different directions to record the process of the shoot-through test.

The test sequences are as follows. First, K_1 is closed and the dc-link capacitor is charged to 2800 V through the dc source. Then, K_1 is opened to isolate the dc source. After that, S_1 is triggered to build the load current. Through calculation, after 1.15 ms, the load current will last more than the rated current for about 100 ms. Finally, there are two kinds of shoot-through faults to be carried out. The first one is that S_2 is triggered and the devices are destroyed by the surge current. The second one is that S_1 will perform a turn OFF action 20 μs after S_2's triggering.

B. Anode and Stray Inductance Measurement

As the anode inductance has an important impact on the *di/dt* and peak current of the shoot through, so it needs to be evaluated before the formal shoot-through fault test. When the shoot through occurs, considering the first half current wave, the voltage of the dc-link capacitor V_C can be written as follows. The former part is the voltage drops of the IGCTs and the latter part is the voltage drops of the total loop inductance, which is composed of the anode inductances and the stray inductances,

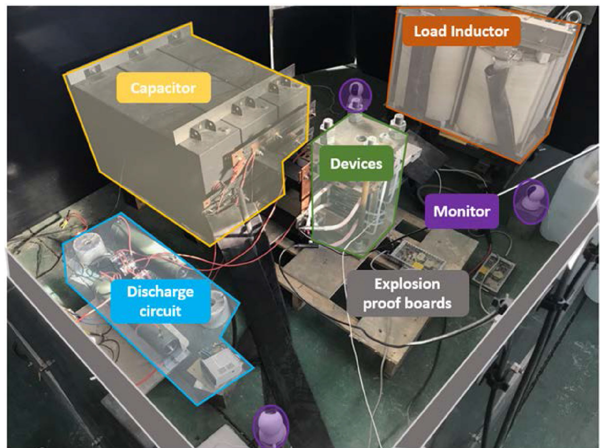

Fig. 13. Photograph of the real test platform.

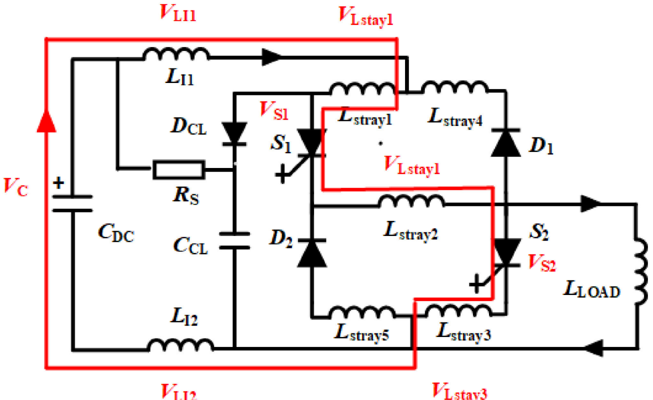

Fig. 14. Voltage drops along the current loop of the first half surge current wave.

as shown in Fig. 14.

$$V_C = \underbrace{2(V_{\text{th}} + I_{\text{igct}} r_t)}_{V_{S1}+V_{S2}} + \underbrace{\frac{dI_{\text{igct}}}{dt} L_{\text{I}}}_{V_{LI1}+V_{LI2}} + \underbrace{\frac{dI_{\text{igct}}}{dt} L_{\text{stray}}}_{V_{L\text{stray1}}+V_{L\text{stray2}}+V_{L\text{stray3}}}. \tag{2}$$

The 10 mF dc-link capacitor is charged to 50 V by the dc source and perform the shoot-through test. According to the test results, the voltage of the capacitor is discharged to 47 V before shoot through begins. Finally, a peak current of about 6 kA is measured, as shown in Fig. 15. Using the current results in the rise phase of the first wave, the fitted result of total loop inductance is around 750 nH. And the differences between the times of S_1 and S_2's zero points confirm the higher L_{stray1}, as mentioned before.

C. Experiments of Shoot-Through Fault Without Switching Action

Then, the dc-link capacitor is charged to 2.8 kV for the formal shoot-through test without any switching action. Finally, the peak surge current in S_1 is about 240 kA/0.47 ms under the discharge of 10 mF/2.55 kV. The discharging total energy is

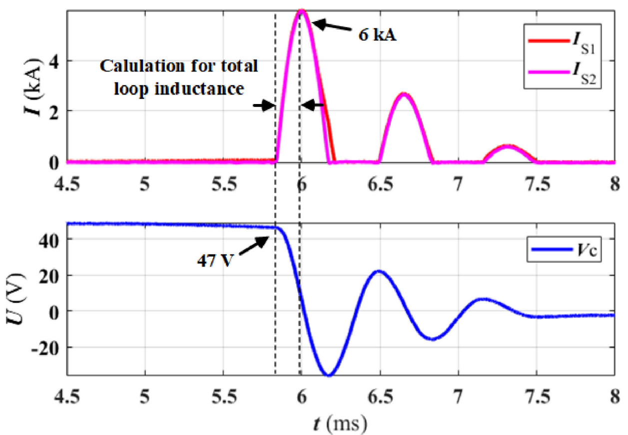

Fig. 15. Experimental results of 10 mF/47 V without switching action.

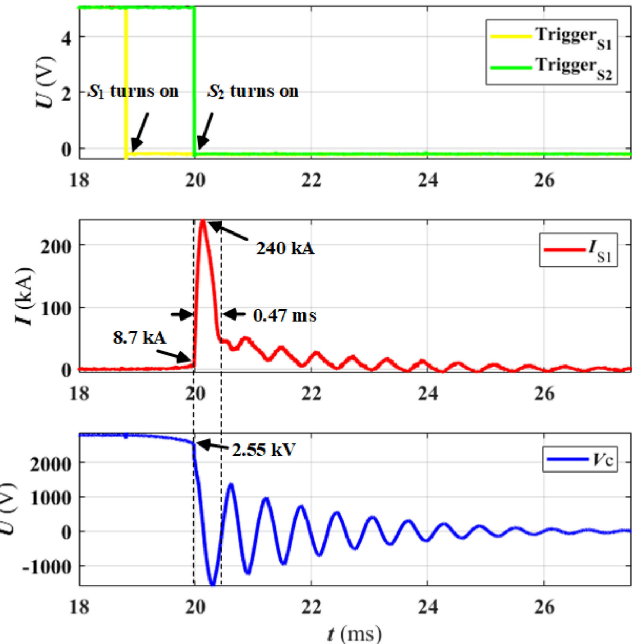

Fig. 16. Experimental results of 10 mF/2.55 kV without switching action.

about 32.5 kJ, and the maximum I^2t is about 14.2 MA^{2}s. The results are shown in Fig. 16.

Fig. 17 gives the comparison of S_2's gate voltages and S_1's surge currents of the tests under 10 mF/47 V and 10 mF/2.55 kV. The red dotted line is the expected gate voltage of undestroyed S_2, and the sudden falling of S_2's real gate voltage can be observed at 0.08 ms after the shoot-through fault begins. This can be determined as the signal of IGCT's local thermal failure caused by the surge current. Because the rising surge current of the first wave of S_1 and S_2 during the shoot-through process is same; as a result, S_2's surge current under 10 mF/2.55 kV is about 194 kA and the I^2t is 1.46 MA^{2}s at the failure time.

D. Experiments of Shoot-Through Fault With Switching Action

In another test, after S_2 is triggered, S_1 is set to turn OFF 20 μs later. Finally, the peak current reaches 266 kA/0.4 ms under the

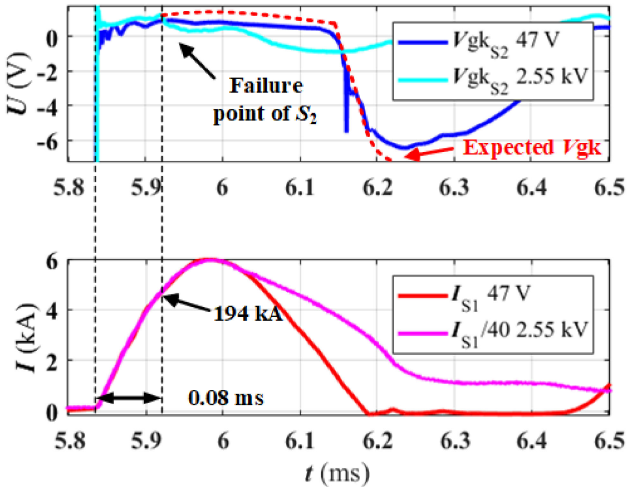

Fig. 17. Confirmation of S_2's failure point according to S_2's gate voltages and S_1's surge currents of the tests under 10 mF/47 V and 10 mF/2.55 kV (the current of the test under 10 mF/2.55 kV is reduced by 40×).

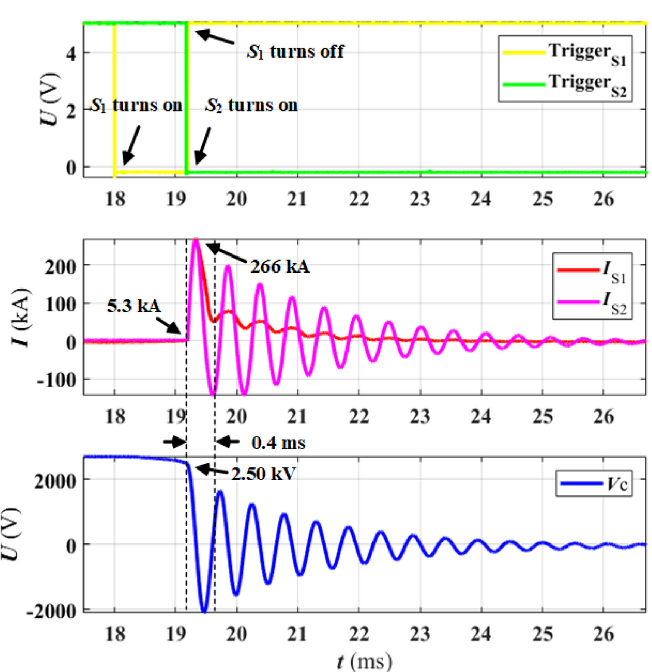

Fig. 18. Experimental results of 10 mF/2.5 kV with switching action.

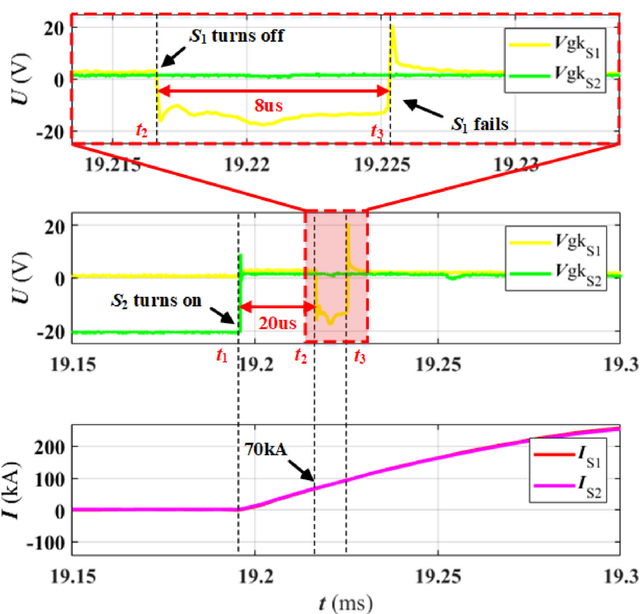

Fig. 19. Illustration of the switching action in shoot-through fault test.

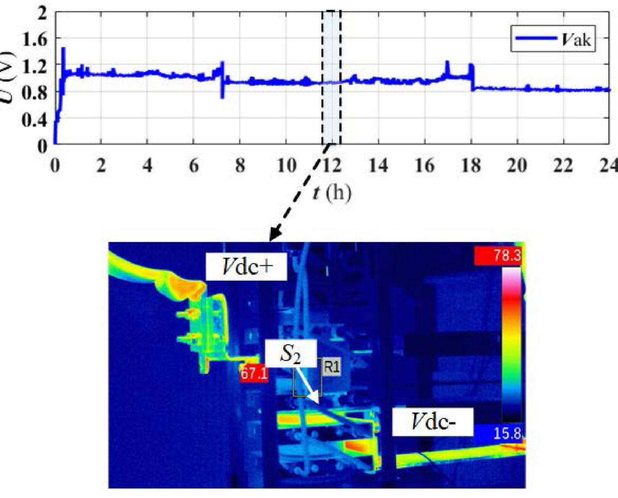

Fig. 20. Measured voltage of the 24-h short-circuit test (above) and the infrared picture of S_2 at $t = 12$ h (below).

test of 10 mF/2.50 kV, as shown in Fig. 18, and the maximum I^2t is about 17 MA^{2}s.

The results in Fig. 19 show that S_2 is triggered at t_1, and S_1 begins to turn OFF at t_2 after 20 μs. It proves that S_1 still work well at t_2 and the following 8 μs shows the commutating period of S_1 during which the gate driver keeps trying to transfer the current from cathode to gate. However, the current of 70 kA is too large for S_1 to turn OFF. Finally, the gate cathode voltage of S_1 rushes to 20 V and it means S_1 has broken down.

E. Long-Term Short-Circuit Experiment Without Decompression

The measured resistances of the devices show that D_1, S_1, and S_2 are both destroyed, but D_2 still works well. This is consistent with the analysis in Section III. But this is not helpful when the submodule needs to be bypassed.

Based on this, the failed S_2 is connected to the current source individually for the long-term short-circuit test. The ON-state voltage of failed S_2 is kept rather low (not more than 1.2 V) under dc 3.15 kA during the continuous 24-h test, as shown in Fig. 20. The picture of the infrared camera shows that maximum of S_2 is kept below 80 ° under the set cooling condition. This

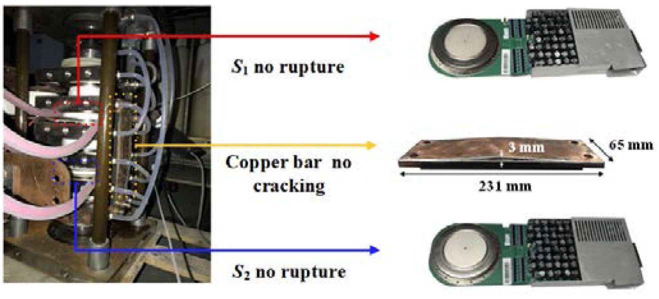

Fig. 21. Pictures of the failed IGCTs and the copper bar after the test.

proves that S_2 could bypass the faulty submodule independently without the help of D_2.

F. Shaping Performance With the Large Mechanical Stress in Shoot-Through Fault

Fig. 21 shows the block after the test. The housing packages of the devices were kept pressed, and no rupture case occurs. The stability of the submodule under the shoot-through fault is verified. The deformation of the copper bar's middle part is about 3 mm without cracking, which is similar with the simulation results in Fig. 11(b). And the copper bar is able to withstand the mechanical stress without cracking. Besides, because the long copper bar is not in the bypassing loop, it would not cause problems on the long-term bypassing of the submodule.

V. Conclusion

This article gives a comprehensive analysis, design, and experiment of shoot-through faults for IGCT-MMC and proves that the IGCT can withstand the fault current when a shoot-through fault in IGCT-SM occurs and the failed IGCT is suitable for bypassing the faulty submodule.

The analysis shows that due to a higher anode inductance, the fault current of shoot through in the IGCT-SM could be decreased a lot compared with IGBT-SM. The measured peak current achieves 266 kA and the maximum I^2t is about 17 MA^{2}s under the dc-link capacitor and the voltage of 10 mF and 2.5 kV. Then, although IGCT cannot turn OFF the fault current, the housing package can keep stable and no rupture occurs. And there are no cracked copper bars, although some deformation cannot be avoided due to the transient ampere force.

In addition, there is a large stray inductance in S_1's current branch, and this leads to a higher increasing rate of current in D_1 than that in D_2. Then, D_1 achieves the thermal failure limitation earlier than D_2, and D_2 is protected by the current sharing of destroyed D_1 and S_2. Although D_2 is not destroyed, the failed S_2 has good long-term short-circuit characteristics and can be used for bypassing the faulty submodule. The results show that the failed IGCT's ON-state voltage is not more than 1.2 V in the continuous 24-h test under 3.15 kA.

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