Common-Mode EMI Mathematical Modeling Based on Inductive Coupling Theory in a Power Module With Parallel-Connected SiC MOSFETs

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***Abstract*—Parallelization of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) could significantly improve the current capability and power rating of power converters. However, the inductive coupling effect of parasitic inductance between the paralleled branches is a critical challenge for the mathematical modeling of electromagnetic interference (EMI) in a power module with parallel-connected SiC MOSFETs (PMPSM). In this article, first, an EMI source generation mathematical modeling method for PMPSM is proposed. The quantitative analysis of EMI interference source caused by inductive coupling of PMPSM is introduced. Second, a common mode (CM) interference propagation mathematical modeling method for PMPSM is proposed. Through the equivalent CM interference source and equivalent impedance model, the strong and weak inductive coupling theory of CM interference equivalent circuit based on parallel-connected SiC MOSFETs is proposed. Third the effect of different decoupling capacitance values on EMI source is compared and analyzed and the influence of changing the ratio of coupling inductance inside and outside the decoupling branch on EMI source of parallel-connected switches is analyzed. Finally, a self-made 1.2-kV 160-A PMPSM based on EMI optimized layout is proposed and tested via an experimental platform of synchronous buck converter, which can verify the feasibility and validity of the proposed power module and the theoretical analysis.**

***Index Terms*—Common-mode interference, decoupling capacitors, electromagnetic interference (EMI), inductive coupling, mathematical modeling, parallel-connected, SiC MOSFET.**

I. Introduction

IN RECENT years, the demand of high-frequency and high-capacity power converters for industrial applications, such as electric vehicles (EVs), renewable energy, aircraft and solid-state switch, is steadily growing [1]–[4]. Because of the wider bandgap, higher dielectric breakdown field strength and larger thermal conductivity compared to silicon (Si), silicon carbide (SiC) metal-oxide-semi-conductor field-effect transistor (MOSFET) becomes more and more attractive in high-capacity power converters [5], [6]. However, the size of single-die SiC MOSFET is usually limited to tens of square millimeters because of the high thermal-mechanical stress and low yield rate in wafer. The current capability of single bare die is generally within 100 A [7], which makes them incompatible with those applications where high-power levels are required. Thus, there is a great interest in paralleling two or more SiC MOSFETs to elevate the current rating and improve the high capacity of the power converter. Whether using the paralleled connection of discrete SiC MOSFETs [8]–[10] or using multichip SiC MOSFETs power module [11]–[14], some challenges have to be taken into account during the implementation, such as problem of dynamic current balance [15]–[19], problem of device and circuit mismatches [20]–[22], robustness and reliability issues [23], [24], and electromagnetic interference and compatibility (EMI/EMC) issues [25]–[34].

The parasitic inductances and capacitances in circuit will cause large oscillations in voltage and current transitions [35]. Due to the high-frequency characteristics of wide band gap semiconductor, the operation of the SiC MOSFETs in high switching speed will lead to severe EMI problem caused by high *dv/dt* and *di/dt* [36], which can be conducted by the wire-connection of circuit, or radiated into the surrounding environment. Moreover, in high current rating applications with parallel-connected switches, the EMI issue will be more serious.

Substantial works have been done to analyze and reduce the EMI issue of a power module with parallel-connected SiC MOSFETs (PMPSM). Some literatures focus on changing the physical structure or using new materials of PMPSM. The literature [25] presents a 10-kV SiC MOSFET power module with an integrated screen, which reduces the common-mode current by ten times. A vertically integrated design method of power module for better common-mode (CM) noise and thermal performance is presented in [26]. A layout of a low-permittivity material is designed in a power semiconductor module to reduce parasitic CM capacitance and attenuate the CM current [27]. A shielding method to suppress the parasitic capacitance caused EMI a SiC MOSFET integrated power module is presented in [28]. These

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methods provide the EMI suppression strategies for PMPSM, but lack of comprehensive mathematical modeling and analysis, which is not beneficial to understand the EMI generation and propagation processes fundamentally. Besides, these methods make the circuit structure complex, and increase the cost and volume, which is difficult for industrialization.

Some literatures use more in-depth simulation modeling analysis of PMPSM. In [29], a simulation scheme based on the S-parameters for simultaneously predicting the circuit operation of a power module and its consequent magnetic near-field strength. A simulation methodology that incorporates cosimulation techniques using ANSYS EM tools is studied to predict radiated and conducted EMI from power electronic modules [30]. However, there is still a lack of comprehensive mathematical modeling and analysis of PMPSM, which is hard to understand the EMI mechanism inside the power module.

Some literatures have studied the modeling method of PMPSM. The work in [31] derives a quantitative model of the leakage current through the baseplate of an MCPM-based half-bridge inverter in a custom-designed EMI characterization testbed. The near magnetic field characterization of power electronic modules has been studied based on an integrated antenna measurement [32]. In [33], a CM noise model is developed for an ac–dc–ac system with paralleled power modules. The work in [34] has investigated the conducted EMI in SiC-based high power density electronic systems from packaging structures and modulation methods. However, the published EMI modeling studies merely take the multiple parasitic inductances between the paralleled switches into consideration or just treat the parallel-connection of SiC MOSFETs in power module as single switch in EMI modeling. There are few modeling and analysis for the EMI mechanism of parallel-connected switches. Due to the high integration of a PMPSM, the parasitic inductance caused by aluminum wire bonding will make the process of EMI modeling and analysis more complex.

In this article, a new CM EMI mathematical modeling method of PMPSM is proposed based on the inductive coupling theory. The main contributions of this article can be listed as follows.

1) An EMI source generation mathematical modeling method of PMPSM is proposed based on the inductive coupling theory. The proposed model found the coupling difference in condition of multiswitch in parallel. Then, the interference quantity can be calculated according to the inductive coupling of parallel-connected switches.
2) A CM propagation mathematical modeling method of PMPSM is proposed based on the inductive coupling theory. Then, the strong and weak inductive coupling theory of CM interference equivalent circuit is proposed. The proposed model found the suppressed effect to high-frequency CM interference by parasitic inductances between the switches in parallel. In this respect, the parasitic inductance caused by aluminum wire bonding in power module is beneficial to suppress CM interference in high frequency range.
3) The influence of different location and values of decoupling capacitance on EMI are analyzed in detail, which can guide the EMI optimized design of the self-made power module. A self-made 1.2-kV 160-A power module with SiC MOSFETs in parallel based on EMI optimized layout is proposed and tested, which has significant suppressed effect to high-frequency CM interference compared to the traditional power module.

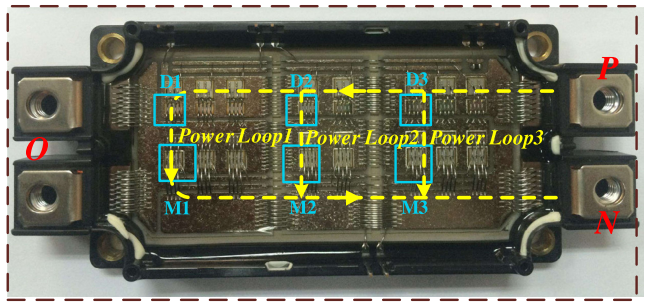

Fig. 1. Photograph of a commercial ROHM 1.2-kV 300-A PMPSM.

The rest of this article is organized as follows. Section II proposes EMI source generation mathematical modeling method for phase-leg power module with parallel-connected SiC MOSFETs. In Section III, the common-mode interference propagation mathematical modeling method for phase-leg power module with parallel-connected SiC MOSFETs is proposed. Combining the EMI source generation and CM interference coupling propagation together, further analysis of equivalent CM interference is discussed in Section IV. In Section V, effect of decoupling capacitor on EMI analysis of phase-leg power module based on parallel-connected SiC MOSFETs is analyzed. In Section VI, experimental platform based on a ROHM commercial power module and a self-made power module is designed and tested. Finally, Section VII concludes the article.

II. EMI Source Generation Mathematical Model of PMPSM Based on Inductive Coupling Theory

A. Double Pulse Circuit Modeling of PMPSM

As a widely used packaging structure of wire-bonded power module in industrial applications, a commercial 1.2-kV, and 300-A phase-leg full-SiC MOSFET power module is chosen in this study as shown in Fig. 1. It can be seen that the upper and lower devices in the phase leg module are all composed of multiple paralleled SiC MOSFETs and multiple antiparalleled diodes, in order to realize the high-power application of power module. P and N nodes are the incoming and outgoing terminals of dc bus, and O node is the ac output terminal. From Fig. 1, the farther away from the dc bus terminals P and N is, the larger power loop will be.

The double pulse test (DPT) equivalent circuit of PMPSM with parasitic parameters can be established, as shown in Fig. 2. The related parasitic parameters are defined in Table I. According to the working principle of DPT, when the lower SiC MOSFETs are in turn-ON state, the upper SiC MOSFETs are turned OFF, and the current flows directly through the output inductor L and the lower leg of power module. At this time, the diodes of upper-leg do not work. The parasitic inductances of upper leg and dc bus (several nanohenry) are much smaller than output inductance

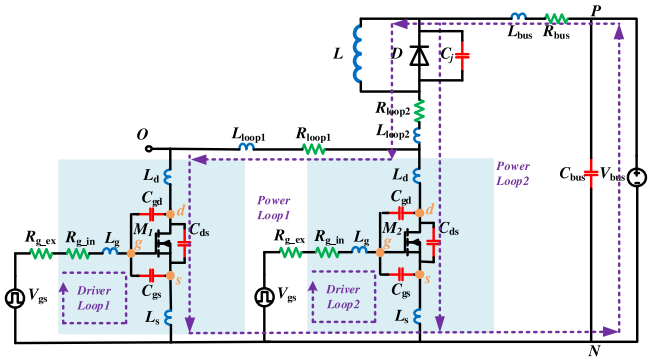

Fig. 2. Double pulse equivalent circuit of PMPSM with parasitic parameters.

TABLE I
PARASITIC PARAMETERS OF PMPSM IN DOUBLE PULSE EQUIVALENT CIRCUIT

Parameters	Descriptions
L_d	drain inductance
L_s	source inductance
L_g	gate inductance
C_{gd}	gate-drain capacitance
C_{ds}	drain-source capacitance
C_{gs}	gate- source capacitance
R_{g_in}	internal gate resistance
R_{g_ex}	external gate resistance
L_{loop}	parasitic inductance between two branches
R_{loop}	parasitic resistance between two branches
L_{bus}	DC bus inductance
R_{bus}	DC bus resistance
C_{bus}	DC bus capacitance
C_j	junction capacitor of Schottky diode

L (several hundred μH). When the lower SiC MOSFETs are on turn-OFF state, the current of output inductance L flows through the diodes of upper-leg, and the lower-leg has no current at this time. The parasitic inductance of the upper leg at this moment has no effect on the lower leg. Therefore, when studying the parasitic inductances coupling effect on lower leg paralleled SiC MOSFETs of power module, the parallel connection of the upper leg diodes is ignored and regarded as a single diode. The junction capacitance and dc bus parasitic parameters of upper leg are ignored. Due to the analytical process of parasitic inductances of negative bus is similar to that of positive bus, for the sake of simplicity, this article only considers the parasitic inductances of positive bus between parallel branches of lower-leg SiC MOSFETs and the mutual inductances are not marked for simplicity.

B. Inductive Coupling Theory Between Parallel Branches of Power Modules

In order to study the coupling effect of parasitic inductances between multiple SiC MOSFETs in parallel, the small signal model of the lower-leg with parasitic inductance coupling is established as Fig. 3. When the SiC MOSFETs of lower-leg

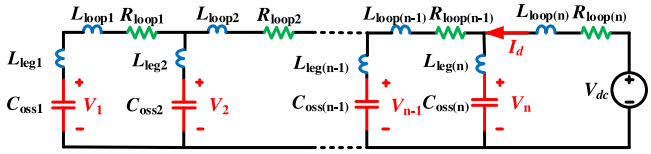

Fig. 3. Small signal model of the PMPSM with parasitic inductance coupling.

operating at the switching transition, the input current of L can be seen as a constant current I_d. $L_{Leg(i)}$ and $C_{oss(i)}$ represent the total parasitic inductances and output capacitance of the branch i separately. Because the impedance of $L_{Leg(i)}$ (several to tens of nanohenry) is much smaller than the impedance of $C_{oss(i)}$ (several to tens of nanofarad) when the frequency is below hundreds of megahertz (within the frequency range of conducted EMI and near field radiated EMI analysis), $L_{Leg(i)}$ can be ignored. The parasitic resistance R_{Loop} is also omitted in the high frequency analysis compared to L_{Loop}. Thus, the drain–source voltage of the MOSFET in branch i can be represented as V_i and calculated as follows, where $i = 1, 2, \ldots, n$:

$$\begin{aligned} V_i &= (I_1 + I_2 + \cdots + I_i)\, Z_{\mathrm{loop}(i)} + V_{i+1} \\ &= \sum_{j=1}^{i} I_j Z_{\mathrm{loop}(i)} + V_{i+1}. \end{aligned} \tag{1}$$

The impedances of the parasitic elements and the current of each parallel branch can be defined as

$$\begin{aligned} Z_{\mathrm{Coss}(i)} &= \frac{1}{\omega C_{\mathrm{Coss}(i)}}, \frac{V_i}{Z_{\mathrm{Coss}(i)}} = I_i, Z_{\mathrm{Loop}(i)} \\ &= \omega L_{\mathrm{Loop}(i)} + R_{\mathrm{Loop}(i)}. \end{aligned} \tag{2}$$

Through iterative summation of parallel voltage sources, the voltage expression of each paralleled branch can be obtained as

$$\begin{aligned} V_i &= \sum_{j=1}^{i} I_j Z_{\mathrm{loop}} + \cdots + \sum_{j=1}^{n-1} I_j Z_{\mathrm{loop}} + \sum_{j=1}^{n} I_j Z_{\mathrm{loop}} + V_{\mathrm{dc}} \\ &= V_{\mathrm{dc}} + Z_{\mathrm{loop}} \sum_{m=i}^{n} \left(\sum_{j=1}^{m} I_j \right). \end{aligned} \tag{3}$$

C. Effect of Inductive Coupling Between Parallel Branches on EMI Sources

Assuming that the parasitic inductance of each branch loop is the same as L_{Loop}, then the voltage differences of adjacent branches are deduced as

$$\Delta V_i = V_i - V_{i+1} = (I_1 + I_2 + \cdots + I_i)\, Z_{\mathrm{loop}} = \sum_{j=1}^{i} I_j Z_{\mathrm{loop}}. \tag{4}$$

In this case, the ratio of voltage difference between adjacent paralleled branches is

$$\begin{aligned} &\Delta V_1 : \Delta V_2 : \cdots : \Delta V_i : \cdots : \Delta V_{n-2} : \Delta V_{n-1} \\ &= I_1 : \sum_{j=1}^{2} I_j : \cdots : \sum_{j=1}^{i} I_j : \cdots : \sum_{j=1}^{n-2} I_j : \sum_{j=1}^{n-1} I_j. \end{aligned} \tag{5}$$

TABLE II
PARAMETERS IN LTSPICE SIMULATION OF PARALLEL-CONNECTED SiC MOSFETS IN DOUBLE PULSE CIRCUIT

Parameters	Values	Parameters	Values
Input voltage	100V	Schottky diode	CPW4-1200-S020B
Input capacitance	100μF	SiC MOSFET	CPM2-1200-0080B
Output inductance	1mH	L_{loop}	10nH
Switching frequency	10kHz	L_d、L_s、L_g	10nH
Driving resistance	10Ω	Duty cycle	0.5

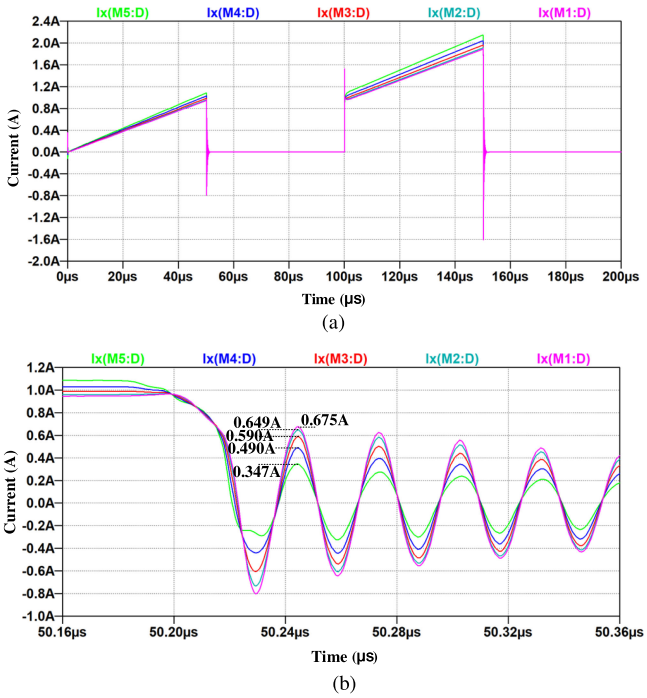

Fig. 4. Time-domain simulated drain currents of paralleled SiC MOSFETs when the parallel number $N = 5$. (a) Drain current waveforms during whole simulation process of double pulse circuit. (b) Turn-OFF transition of drain current waveforms.

In the high-frequency oscillation parts of the SiC MOSFETs, due to the coupling effect of parasitic inductances between the power circuits of each SiC MOSFET, the farther away from the dc bus terminals, the larger parasitic loop inductance, and the higher amplitude of high-frequency oscillation voltage, which means the greater amplitude of high-frequency EMI interference source. This fully reflects the influence of inductive coupling theory on EMI interference sources.

When the number of parallel branches is five and the currents of different branches are not equal, the simulation analysis with parameters in Table II can be carried out based on the software LTSpice. The parasitic inductance $L_{\rm loop}$ between the two branches can be extracted from 3-D model of the ROHM SiC power module in Fig. 1 by ANSYS Q3D software. By applying ac value current source at 50 MHz, the parasitic inductance $L_{\rm loop}$ is extracted as 10.481 nH in positive bus and 10.072 nH in negative bus. Therefore, the value of parasitic inductance $L_{\rm loop}$ is selected as 10 nH in the simulation analysis. The simulation

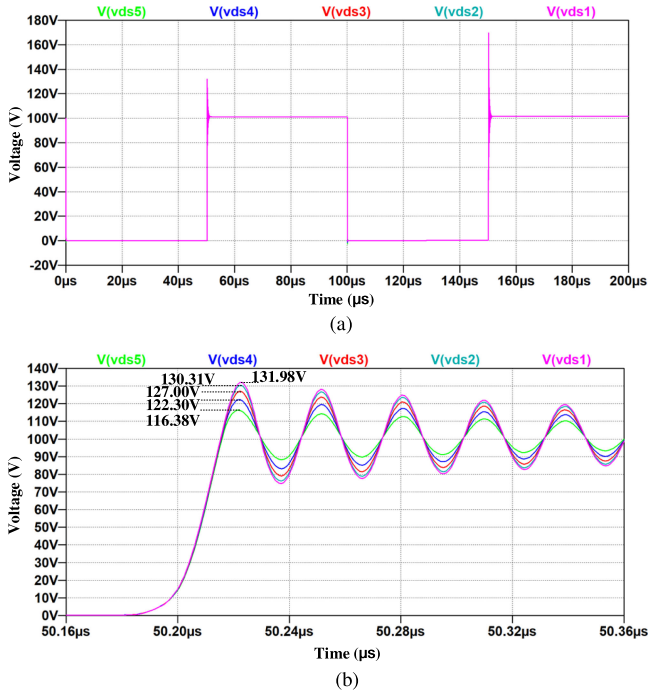

Fig. 5. Time-domain simulated $V_{\rm ds}$ voltages of paralleled SiC MOSFETs when the parallel number $N = 5$. (a) $V_{\rm ds}$ voltage waveforms during whole simulation process of double pulse circuit. (b) Turn-OFF transition of $V_{\rm ds}$ voltage waveforms.

results of drain currents, $V_{\rm ds}$ voltages, and EMI spectrums of SiC MOSFETs in parallel are shown in Figs. 4, 5, and 6. The related simulated and calculated results are shown in Table III, where k represents the branch number (from 1 to 5 is the direction close to the dc bus terminals). I_{k_s} and V_{k_s} represent the simulated drain current and $V_{\rm ds}$ voltage of each SiC MOSFET, respectively, which can be obtained from Figs. 4 and 5 directly. ΔV_{k_c} is defined as the calculated voltage difference values of adjacent branches and can be calculated as follows, according to the voltage differences of adjacent branches in (4) and simulated currents I_{k_s}in Table III:

$$\Delta V_{k\_c} = \sum_{j=1}^{k} I_{j\_s} Z_{\rm loop}. \tag{6}$$

ΔV_{k_s} is defined as the simulated voltage difference values of adjacent branches, which can be obtained as formula (7) according to the simulated values of V_{k_s} in Table III

$$\Delta V_{k\_s} = V_{k\_s} - V_{k+1\_s}. \tag{7}$$

Therefore, ΔV_{k_c} and ΔV_{k_s} ratios of adjacent branches are obtained, and the error between the calculated ratio and the simulated ratio is obtained as error of ratios in Table III. It can be seen that the error of ratios is about 1%, which proves the accuracy of the proposed inductive coupling model of parallel-connected SiC MOSFETs.

The amplitude $\mathrm{Mag}(V_k)$ and amplitude difference $\Delta\mathrm{Mag}(V_k)$ of each SiC MOSFET during turn-OFF transition in the simulated spectrums of EMI interference source are

TABLE III
SIMULATED AND CALCULATED RESULTS OF CURRENT AND VOLTAGE OF EACH BRANCH BY LTSPICE SOFTWARE

Parameters	k=1	k=2	k=3	k=4	k=5
I_{k_s} / A	0.675	0.649	0.590	0.490	0.347
ΔV_{k_c} / V	0.675*Z_{loop}	1.324*Z_{loop}	1.914*Z_{loop}	2.404*Z_{loop}	
V_{k_s} / V	131.98	130.31	127.00	122.30	116.38
ΔV_{k_s} / V	1.67	3.31	4.7	5.92	
$\Delta V_{1\_c} : \Delta V_{2\_c} : \Delta V_{3\_c} : \Delta V_{4\_c}$	1 : 1.9615 : 2.8356 : 3.5615				
$\Delta V_{1\_s} : \Delta V_{2\_s} : \Delta V_{3\_s} : \Delta V_{4\_s}$	1 : 1.9820 : 2.8144 : 3.5449				
Error of ratios	0 : 1.05% : 0.75% : 0.47%				
$\mathrm{Mag}(V_k)$ / dBV	-22.45	-22.91	-23.90	-25.56	-28.19
$\Delta\mathrm{Mag}(V_k)$ / dBV	0.46	0.99	1.66	2.63	
$V_{overshoot\_k\_s}$ / V	31.98	30.31	27.00	22.30	16.38
$20\log\left(\frac{V_{overshoot\_k\_s}}{V_{overshoot\_k+1\_s}}\right)$	0.465	1.01	1.66	2.68	
Error of Mag	1% : 2% : 0 : 1.9%				

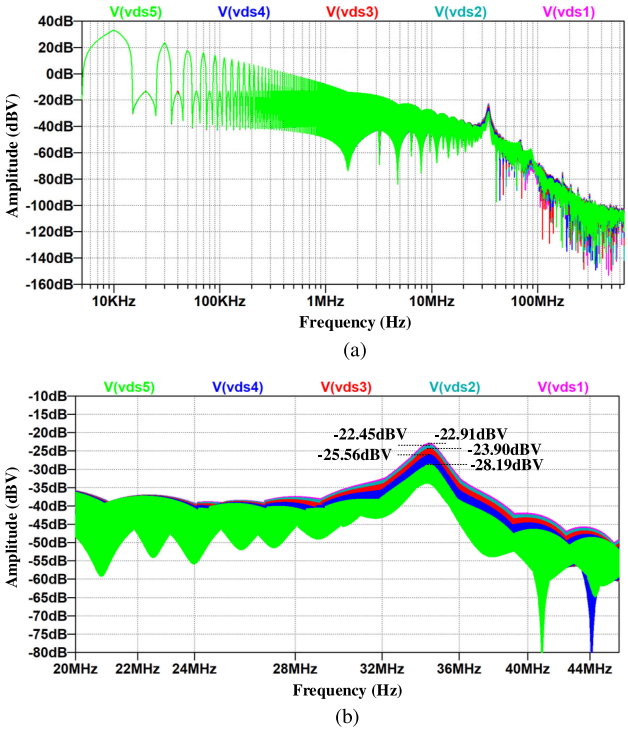

Fig. 6. Frequency-domain simulated EMI spectrums of SiC MOSFETs in parallel when the parallel number $N = 5$. (a) EMI spectrums of SiC MOSFETs during whole frequency-domain. (b) Turn-OFF transition of EMI spectrums.

obtained by Fig. 6 and shown in Table III, and the values of $\Delta\mathrm{Mag}(V_k)$ are calculated by

$$\Delta\mathrm{Mag}\left(V_k\right) = \mathrm{Mag}\left(V_k\right) - \mathrm{Mag}\left(V_{k+1}\right). \tag{8}$$

According to the time-domain V_{ds} voltage waveforms in Fig. 5, the time-domain overshoot voltage $V_{overshoot\_k\_s}$ of each SiC MOSFET and the spectrum amplitude of adjacent branches' overshoot voltage ration $20\log(\frac{V_{overshoot\_k+1\_s}}{V_{overshoot\_k\_s}})$ can be calculated, as shown in Table III. The error between the simulated amplitude difference $\Delta\mathrm{Mag}(V_k)$ and the calculated spectrum amplitude of adjacent branches' overshoot voltage ration is obtained as error of Mag in Table III. It can be seen that the error of Mag is below 2%, so it can be concluded that the EMI spectrum amplitude difference values between adjacent branches at the moment of turn-OFF is proportional to the corresponding time-domain overshoot voltage difference values.

D. Analysis of Inductive Coupling Between Paralleled Branches Under Current Balance State

Assuming that the paralleled branches are all in current balance state and equally sharing the total input current, it can be derived that

$$I_1 = I_2 = \cdots = I_n = \frac{I_d}{n}. \tag{9}$$

Thus, the ratio of voltage difference between adjacent paralleled branches is

$$\begin{aligned}&\Delta V_1 : \Delta V_2 : \cdots : \Delta V_i : \cdots : \Delta V_{n-2} : \Delta V_{n-1}\\ &= 1 : 2 : \cdots : i : \cdots : n-2 : n-1.\end{aligned} \tag{10}$$

According to (4), V_{ds} voltage expression of each paralleled branch can be obtained as follows:

$$\begin{aligned}V_i = V_{\mathrm{dc}} + Z_{\mathrm{loop}} \sum_{m=i}^{n} \left(\sum_{j=1}^{m} I_j \right) = V_{\mathrm{dc}}\\ + \frac{Z_{\mathrm{loop}} I_d}{n} \left(\sum_{j=1}^{n} j - \sum_{k=0}^{i-1} k \right).\end{aligned} \tag{11}$$

It can be calculated that $\sum_{j=1}^{n} j = \frac{(1+n)n}{2}$ and $\sum_{k=0}^{i-1} j = \frac{i(i-1)}{2}$. Therefore, V_{ds} voltage of the ith switch can be expressed

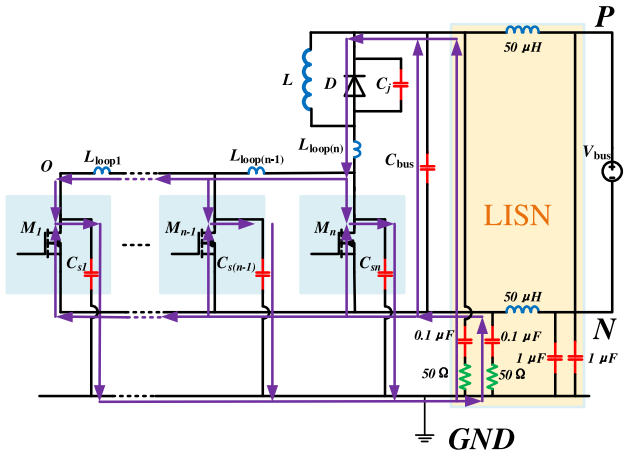

Fig. 7. CM interference's high-frequency coupling paths of PMPSM with inductive coupling between paralleled branches.

as follows, when the total amount of paralleled switches is n:

$$\begin{aligned} V_i &= V_{\mathrm{dc}} + Z_{\mathrm{loop}} \sum_{m=i}^{n} \left(\sum_{j=1}^{m} I_j \right) \\ &= V_{\mathrm{dc}} + \frac{Z_{\mathrm{loop}} I_d}{n} \left(\frac{(1+n)n}{2} - \frac{i(i-1)}{2} \right) \\ &= V_{\mathrm{dc}} + Z_{\mathrm{loop}} I_d \frac{n^2 + n - i^2 + i}{2n}. \end{aligned} \tag{12}$$

III. Common-Mode EMI Propagation Modeling of PMPSM Based on Inductive Coupling Theory

Based on the DPT circuit of phase-leg power module, a high-frequency coupling paths of CM interference with inductive coupling between paralleled branches is established. As shown in Fig. 7, the amount of switches connected in parallel is n, and the parasitic capacitances from drain of each SiC MOSFET to ground are $C_{s1}, C_{s1}, \cdots, C_{sn}$, respectively, and the coupling parasitic inductances between adjacent branches are $L_{\mathrm{loop1}}, L_{\mathrm{loop2}}, \cdots, L_{\mathrm{loop}(n)}$. The CM interference is detected by line impedance stabilization network (LISN). In the process of high-frequency EMI analysis, dc bus capacitance can be regarded as short circuit and load inductance as open circuit. Because the purpose of this part is to study the influence of inductive coupling of lower-leg paralleled SiC MOSFET on CM interference coupling circuit, the junction capacitance of upper-leg diode is not considered here, and the circuit is simplified as Fig. 8.

The CM interference equivalent mathematical model of the simplified circuit in Fig. 8 can be further established as Fig. 9(a) shown, where SiC MOSFET of each branch can be regarded as a current source. The equivalent model of n-switch paralleled CM interference is obtained by Thevenin–Norton equivalent network theorem as Fig. 9(b). Then, by ignoring the active sources in the circuit, the circuit impedance network is shown in Fig. 9(c). Finally, after simplifying the equivalent mathematical model, there is only one equivalent CM interference source and one

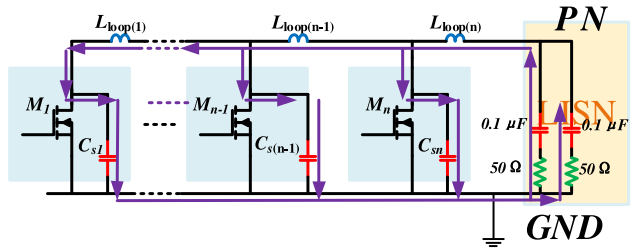

Fig. 8. Simplification of the CM interference equivalent circuit.

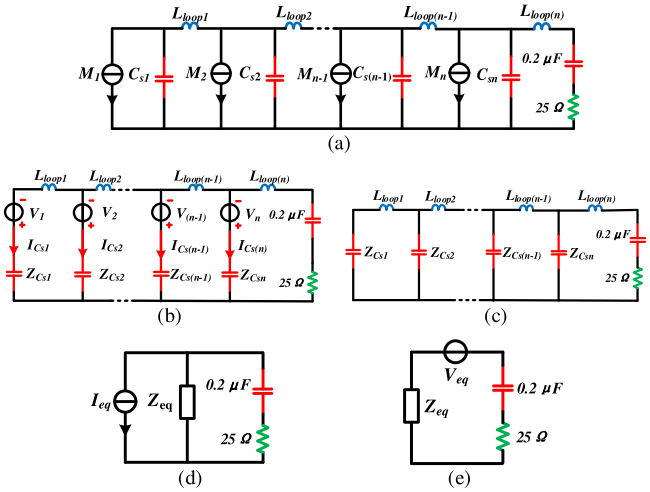

Fig. 9. CM interference equivalent mathematical model of power module with parallel-connected SiC MOSFETs. (a) CM interference equivalent mathematical model. (b) Simplicity circuit by the Thevenin–Norton theorem. (c) Circuit impedance network of the CM interference equivalent circuit. (d) Equivalent CM current source model. (e) Equivalent CM voltage source model.

equivalent impedance of CM interference as shown in Fig. 9(d) and (e).

The CM current flowing through each branch in Fig. 9(b) is defined as (13). There is a new function $Y_i(X)$ defined in (14), where i is a positive integer. A new concept $\bigcup_{i=1}^{n} Y_i(X)$ is defined in (15), which means that the value of the ith function is iterated into the independent variable of the $(i+1)$th function, and then, the final function value is obtained by iterations of n times

$$I_{Cs(i)} = \frac{V_{(i)}}{Z_{Cs(i)}} \quad , \quad 1 \le i \le n \tag{13}$$

$$Y_i(X) = \begin{cases} X, & i = 1 \\ (X) // Z_{Cs(i+1)} + Z_{\mathrm{loop}(i+1)}, & i > 1 \end{cases} \tag{14}$$

$$\bigcup_{i=1}^{n} Y_i(X) = Y_n\left(Y_{n-1}\left(\cdots\left(Y_2\left(Y_1(X)\right)\right)\right)\right). \tag{15}$$

Then, the equivalent CM interference voltage source $V_{eq(n)}$, current source $I_{eq(n)}$, and equivalent CM interference impedance $Z_{eq(n)}$ of n-switch in parallel shown in Fig. 9(d) and (e) can be expressed as (16), (17), and (18), which can be derived

and proved by mathematical induction in the Appendix

$$\begin{aligned} V_{eq(n)} &= \left(I_{eq(n-1)} + I_{Csn}\right)\left(Z_{eq(n)} - Z_{\mathrm{loop}(n)}\right) \\ &= \left(I_{eq(n-1)} + I_{Csn}\right) \\ &\quad \times \left(\bigcup_{i=1}^{n} Y_i(Z_{Cs1} + Z_{\mathrm{loop}1}) - Z_{\mathrm{loop}(n)}\right) \end{aligned} \tag{16}$$

$$\begin{aligned} I_{eq(n)} &= \frac{V_{eq(n)}}{Z_{eq(n)}} = \frac{\left(I_{eq(n-1)} + I_{Csn}\right)\left(Z_{eq(n)} - Z_{\mathrm{loop}(n)}\right)}{Z_{eq(n)}} \\ &= \frac{\left(I_{eq(n-1)} + I_{Csn}\right)\left(\bigcup_{i=1}^{n} Y_i(Z_{Cs1} + Z_{\mathrm{loop}1}) - Z_{\mathrm{loop}(n)}\right)}{\bigcup_{i=1}^{n} Y_i(Z_{Cs1} + Z_{\mathrm{loop}1})} \end{aligned} \tag{17}$$

$$Z_{eq(n)} = \bigcup_{i=1}^{n} Y_i(Z_{Cs1} + Z_{\mathrm{loop}1}). \tag{18}$$

IV. Further Analysis of CM Interference Equivalent Mathematical Model

It is assumed that the parasitic capacitances of each SiC MOSFET's drain to ground are the same as C_s, the coupling parasitic inductances between parallel branches are the same as L_{loop}, and the parallel branches are in current balance state as (9). In this section, the characteristics of the EMI interference sources with inductive coupling in the chapter II are introduced. Combined with the CM interference coupling propagation modeling in chapter III, the equivalent CM interference can be comprehensively analyzed.

A. Analysis of CM Impedance Characteristics in Equivalent Mathematical Model

The equivalent CM interference impedance can be expanded as (19), shown at the bottom of this page, when the amount of paralleled switches *N* is 1, 2, 3 … *n*-1 and *n*, respectively, according to (18) and above assumption. It can be seen that this is an iterative process of expression $(Z_{Cs} + Z_{\mathrm{loop}})//Z_{Cs} + Z_{\mathrm{loop}}$ for *N* times

It can be assumed that when $Z_{Cs} = Z_{\mathrm{loop}} = \frac{1}{\omega C_s} = \omega L_{\mathrm{loop}}$, the corresponding corner frequency can be calculated as $\omega_0 = \frac{1}{\sqrt{L_{\mathrm{loop}} C_s}}$.

1) When $\omega \le \frac{1}{10}\omega_0$, it can be considered that $Z_{Cs} \gg Z_{\mathrm{loop}}(Z_{Cs} \ge 100 Z_{\mathrm{loop}})$, and the coupling effect of Z_{loop} is negligible, which shows the weak coupling effect. The CM equivalent impedance can be expressed as

$$\begin{aligned} &Z_{eq(n)}\Big|_{\omega \le \frac{1}{10}\omega_0} \\ &= \bigcup_{i=1}^{n} Y_i(Z_{Cs} + Z_{\mathrm{loop}}) = Z_{Cs}//Z_{Cs}//\cdots//Z_{Cs} \\ &= \frac{Z_{Cs}}{n} = \frac{1}{n\omega C_s}. \end{aligned} \tag{20}$$

2) When $\omega \ge 10\omega_0$, it can be considered that $Z_{Cs} \ll Z_{\mathrm{loop}}$ $(Z_{\mathrm{loop}} \ge 100 Z_{Cs})$, and $Z_{Cs} + Z_{\mathrm{loop}} \approx Z_{\mathrm{loop}}$, which shows the strong coupling effect. The CM equivalent impedance can be expressed as

$$Z_{eq(n)}\Big|_{\omega \ge \frac{1}{10}\omega_0} = \bigcup_{i=1}^{n} Y_i(Z_{Cs} + Z_{\mathrm{loop}}) = Z_{\mathrm{loop}} = \omega L_{\mathrm{loop}}. \tag{21}$$

To be exact, Z_{loop} in (21) is the parasitic inductance between SiC MOSFET which is the nearest to the dc bus $Z_{\mathrm{loop}(n)}$.

1) When $\frac{1}{10}\omega_0 < \omega < 10\omega_0$, it can be seen that $Z_{\mathrm{loop}} < Z_{eq(n)}|_{\frac{1}{10}\omega_0 < \omega < 10\omega_0} < Z_{Cs} + Z_{\mathrm{loop}}$. Obviously, when the amount of switches in parallel increases, the CM equivalent impedance decreases as

$$Z_{eq1} > Z_{eq2} > Z_{eq3} > \cdots > Z_{eq(n)}. \tag{22}$$

It can be seen that the inductive coupling effect caused by the parasitic inductance between the paralleled branches will enhance with the increasing frequency, and the attenuation of CM interference will enlarge by inductive coupling effect.

B. Analysis of CM Current Characteristics in Equivalent Mathematical Model

The equivalent CM interference current can be simplified as

$$I_{eq(n)} = \frac{V_{eq(n)}}{Z_{eq(n)}} = \frac{\left(I_{eq(n-1)} + I_{Cs(n)}\right)\left(Z_{eq(n)} - Z_{\mathrm{loop}}\right)}{Z_{eq(n)}}. \tag{23}$$

A new function $W_i(X)$ is defined in (24), where i is a positive integer and $\bigcup_{i=1}^{n} W_i(X)$ can be expressed as

$$W_i(X) = \begin{cases} X, & i = 1 \\ \frac{(X + I_{Cs(i)})\left(Z_{eq(i)} - Z_{\mathrm{loop}}\right)}{Z_{eq(i)}}, & i > 1 \end{cases} \tag{24}$$

$$Z_{eq(n)} = \underbrace{\left(\underbrace{\left(\underbrace{\left(\underbrace{(Z_{Cs} + Z_{\mathrm{loop}})}_{N=1}//Z_{Cs} + Z_{\mathrm{loop}}\right)}_{N=2} \cdots\cdots//Z_{Cs} + Z_{\mathrm{loop}}\right)}_{N=n-1}//Z_{Cs} + Z_{\mathrm{loop}}\right)}_{N=n} \tag{19}$$

$$\bigcup_{i=1}^{n} W_i(X) = W_n\left(W_{n-1}\left(\cdots\left(W_2\left(W_1(X)\right)\right)\right)\right). \tag{25}$$

Therefore, the equivalent CM current expression of *N*-switch in parallel can be expressed as follows, and expanded as (27), shown at the bottom of this page:

$$I_{eq(n)} = \bigcup_{i=1}^{n} W_i\left(\frac{V_1}{Z_{Cs}+Z_{\text{loop}}}\right) \tag{26}$$

It can be seen that this is an iterative process of expression (28), shown at the bottom of this page, for *N* times, which can be decomposed into the multiplication of parts A and B. The symbol S_i can be defined as follows for simplicity:

$$S_i = \begin{cases} Z_{Cs}+Z_{\text{loop}}, & i=1 \\ \underbrace{(((((Z_{Cs}+Z_{\text{loop}})\,//Z_{Cs})+Z_{\text{loop}})\cdots)\,//Z_{Cs})}_{i\ times}, & i>1 \end{cases} \tag{29}$$

It can be seen that part A is a superposition accumulation process of current from branch 1 to branch *n*. When the amount of paralleled switches *N* increases, the accretion of part A will cause the enlargement of CM equivalent current. However, with the amount of paralleled switches *N* increasing, the reduction of part B will cause the decrease of CM equivalent current, due to the diminution of S_i according to (29). Therefore, the changing trend of equivalent CM current needs further analysis.

The part B obviously can deduce the expression in (30), which means that the part B is an inductive coupling effect repeatedly applied to the currents of paralleled branches, and the farther away from the dc bus, the more times the inductive coupling effect is applied to EMI source, which is a attenuation for the equivalent CM current. The larger of Z_{loop}, the more obvious the suppressed effect

$$\frac{1}{1+\frac{Z_{\text{loop}}}{S_i}} \le 1. \tag{30}$$

Based on the above analysis of CM impedance characteristics of $Z_{eq(n)}$, the further analysis of CM equivalent current can be deduced.

1) When $\omega \le \frac{1}{10}\omega_0$, it can be considered that $Z_{Cs} \gg Z_{\text{loop}}(Z_{Cs} \ge 100Z_{\text{loop}})$, and the coupling effect of Z_{loop} is negligible. Thus, the value of part B is approximately equal to 1 and the CM equivalent current can be expressed as (31). Then, $I_{eq(n)}$ can be further obtained by (32)

$$I_{eq(i)} = I_{eq(i-1)} + \frac{V_i}{Z_{Cs}} \tag{31}$$

$$I_{eq(n)}\Big|_{\omega\le\frac{1}{10}\omega_0} = \sum_{i=1}^{n}\frac{V_i}{Z_{Cs}} = \frac{1}{Z_{Cs}}\sum_{i=1}^{n}V_i. \tag{32}$$

According to formula (12), the accumulation of V_i can be calculated

$$\begin{aligned}\sum_{i=1}^{n}V_i &= nV_{\text{dc}} + Z_{\text{loop}}I_d\sum_{i=1}^{n}\frac{n^2+n-i^2+i}{2n} \\ &= nV_{\text{dc}} + Z_{\text{loop}}I_d\frac{(n+1)(2n+1)}{6}.\end{aligned} \tag{33}$$

Thus, the CM voltage can be calculated in (34). It can be seen that the CM voltage increases with the amount of parallel switches *n* increasing. With the increasing of frequency, Z_{Cs} decreases. Thus, the CM voltage will increase and the increasing trend will be more and more obvious

$$\begin{aligned}V_{cm(n)}\Big|_{\omega\le\frac{1}{10}\omega_0} &= I_{eq(n)}\Big|_{\omega\le\frac{1}{10}\omega_0}\,Z_{lisn} \\ &= \frac{Z_{lisn}}{Z_{Cs}}\left(nV_{\text{dc}} + Z_{\text{loop}}I_d\frac{(n+1)(2n+1)}{6}\right).\end{aligned} \tag{34}$$

1) When $\omega \ge 10\omega_0$, it can be considered that $Z_{Cs} \ll Z_{\text{loop}}$ $(Z_{\text{loop}} \ge 100Z_{Cs})$. The CM equivalent current can be expressed as (35). Then, $I_{eq(n)}$ can be further obtained

$$I_{eq(n)} = \underbrace{\left(\underbrace{\left(\underbrace{\frac{V_1}{Z_{Cs}+Z_{\text{loop}}}}_{N=1}+\frac{V_2}{Z_{Cs}}\right)((Z_{Cs}+Z_{\text{loop}})\,//Z_{Cs})}_{N=2}\cdots\cdots+\frac{V_n}{Z_{Cs}}\right)(((((Z_{Cs}+Z_{\text{loop}})\,//Z_{Cs})+Z_{\text{loop}})\cdots)\,//Z_{Cs})}_{N=n} \tag{27}$$

$$I_{eq(i)} = \underbrace{\left(I_{eq(i-1)}+\frac{V_i}{Z_{Cs}}\right)}_{A}\underbrace{\frac{(((((Z_{Cs}+Z_{\text{loop}})\,//Z_{Cs})+Z_{\text{loop}})\cdots)\,//Z_{Cs})}{(((((Z_{Cs}+Z_{\text{loop}})\,//Z_{Cs})+Z_{\text{loop}})\cdots)\,//Z_{Cs})+Z_{\text{loop}}}}_{B} = \underbrace{\left(I_{eq(i-1)}+\frac{V_i}{Z_{Cs}}\right)}_{A}\underbrace{\frac{1}{1+\frac{Z_{\text{loop}}}{S_i}}}_{B} \tag{28}$$

as (36), shown at the bottom of this page

$$I_{eq(i)} = \frac{\left(I_{eq(i-1)} + \frac{V_i}{Z_{Cs}}\right)}{1 + \frac{Z_{\text{loop}}}{S_i}} = \frac{I_{eq(i-1)}}{1 + \frac{Z_{\text{loop}}}{S_i}} + \frac{\frac{V_i}{Z_{Cs}}}{1 + \frac{Z_{\text{loop}}}{S_i}} \tag{35}$$

Because the denominator is a multiplication of $(1 + \frac{Z_{\text{loop}}}{S_i})$, which is bigger than 100. Therefore, this strong inductive coupling between the paralleled branches will lead to attenuation of the CM currents for all SiC MOSFETs $M_1 \sim M_{n-1}$ except the switch M_n, which is the closest to the dc bus. Moreover, with the amount of paralleled switches increasing, the farther away from the dc bus, the stronger the attenuation effect of inductive coupling on the CM current.

Thus, the CM voltage can be calculated in (37), shown at the bottom of this page. It can be seen that the CM voltage is independent of the amount of paralleled switches *n*. With the increasing of frequency, Z_{loop} increases, and the CM voltage will decrease.

1) When $\frac{1}{10}\omega_0 < \omega < 10\omega_0$, the trend is from weak inductive coupling to strong inductive coupling. According to (12) and (36), the CM voltage can be calculated in (38), shown at the bottom of this page. It can be seen that the CM voltage increases with the amount of parallel switches *n* increasing. With the increase of frequency, the CM inductive coupling factor $(1 + \frac{Z_{\text{loop}}}{S_i})$ will be larger, and the CM voltage detected by LISN will be smaller. This means that with the increase of frequency, the difference between the CM voltages generated by the paralleled switches becomes smaller and smaller

C. Simulation Analysis

Because the current of the DPT is continuously increasing, the current of the later switching period is greater than that of the previous cycle. According to the equivalent EMI interference source voltage expression deduced above, the EMI in the later switching period will also increase. Therefore, waveforms of only one switching period are selected for the EMI simulation based on the parameters in Table II.

1) Comparative Analysis of Different Amount of Switches N in Parallel: When the amount of paralleled branches *N* is 2, 3, 4, and 5 separately, the zoom-in-view of turn-OFF transition simulated drain currents, V_{ds} voltages of SiC MOSFETs in parallel are shown in Fig. 10. The CM voltages' spectrum of parallel-connected SiC MOSFETs is shown in Fig. 11. When number i switches are in parallel, the expression $V_{lisn(i)+}$ and $V_{lisn(i)-}$ represent the high-frequency voltage detected by positive and negative buses of LISN, respectively. According to the definition of CM voltage, the CM voltage detected by LISN can be calculated as

$$V_{cm(i)} = \left(V_{lisn(i)+} + V_{lisn(i)-}\right)/2. \tag{39}$$

When $\omega \le \frac{1}{10}\omega_0$, It can be seen that $V_{cm(2)} < V_{cm(3)} < V_{cm(4)} < V_{cm(5)}$, and with the increasing of frequency, the CM voltage increases as shown in Fig. 11(b). When $\frac{1}{10}\omega_0 < \omega < 10\omega_0$, it can be seen that $V_{cm(2)} < V_{cm(3)} < V_{cm(4)} < V_{cm(5)}$, and with the increasing of frequency, the CM voltage is smaller, and the difference between the CM voltages generated by the paralleled switches becomes smaller and smaller as shown in Fig. 11(c). When $\omega \le \frac{1}{10}\omega_0$, It can be seen that $V_{cm(2)} = V_{cm(3)} = V_{cm(4)} = V_{cm(5)}$, and with the increasing of frequency, the CM voltage decreases as shown in Fig. 11(d). The simulation results are highly consistent with the theoretical mathematical model analysis in (34), (37), and (38).

2) Comparative Analysis of Different Strength of Inductive Coupling Effect: When the amount of paralleled branches *N* is 5, and the coupling parasitic inductance L_{loop} between the branches is 10, 50, and 100 nH, respectively, the CM voltages in frequency are shown in Fig. 12.

It can be seen that the spectrum amplitude of high-frequency oscillation during turn-OFF transition is increasing and the frequency of peak-point is shifting to the left with increasing L_{loop}. This is because when L_{loop} increases, $\omega_0 = \frac{1}{\sqrt{L_{\text{loop}} C_s}}$ decreases, so the frequency of peak-point shifts to the left.

$$I_{eq(n)}\,|_{\omega \ge 10\omega_0} = \frac{V_1}{S_1 \prod_{i=2}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \frac{V_2}{Z_{Cs} \prod_{i=2}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \frac{V_3}{Z_{Cs} \prod_{i=3}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \cdots + \frac{V_n}{Z_{Cs}\left(1 + \frac{Z_{\text{loop}}}{S_n}\right)}$$
$$\approx \frac{V_n}{Z_{Cs}\left(1 + \frac{Z_{\text{loop}}}{S_n}\right)} \approx \frac{V_n}{Z_{\text{loop}}}. \tag{36}$$

$$V_{cm(n)}\,|_{\omega \ge 10\omega_0} = I_{eq(n)}\,|_{\omega \ge 10\omega_0}\, Z_{lisn} = \frac{V_n}{Z_{\text{loop}}} Z_{lisn} = \frac{V_{\text{dc}} + Z_{\text{loop}} I_d}{Z_{\text{loop}}} Z_{lisn} = \left(\frac{V_{\text{dc}}}{Z_{\text{loop}}} + I_d\right) Z_{lisn} \tag{37}$$

$$V_{cm(n)}\Big|_{\frac{1}{10}\omega_0 < \omega < 10\omega_0}$$
$$= \left(\frac{V_{\text{dc}} + Z_{\text{loop}} I_d \frac{n^2+n}{2n}}{S_1 \prod_{i=2}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \frac{V_{\text{dc}} + Z_{\text{loop}} I_d \frac{n^2+n-2}{2n}}{Z_{Cs} \prod_{i=2}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \frac{V_{\text{dc}} + Z_{\text{loop}} I_d \frac{n^2+n-6}{2n}}{Z_{Cs} \prod_{i=3}^{n}\left(1 + \frac{Z_{\text{loop}}}{S_i}\right)} + \cdots + \frac{V_{\text{dc}} + Z_{\text{loop}} I_d \frac{n^2+n-i^2+i}{2n}}{Z_{Cs}\left(1 + \frac{Z_{\text{loop}}}{S_n}\right)} \right) Z_{lisn} \tag{38}$$

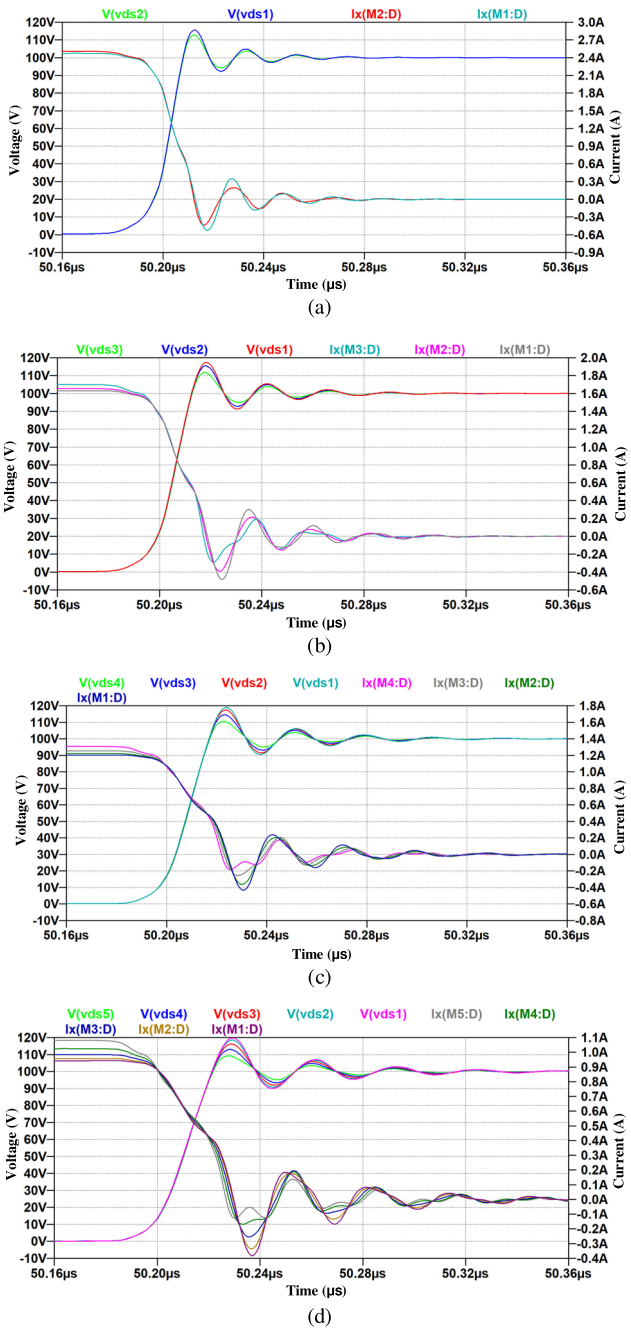

Fig. 10. Zoom-in-view of turn-OFF transition simulated drain currents and V_{ds} voltages of paralleled SiC MOSFETs when the parallel number $N = 2$, 3, 4, and 5 separately. (a) $N = 2$. (b) $N = 3$. (c) $N = 4$. (d) $N = 5$.

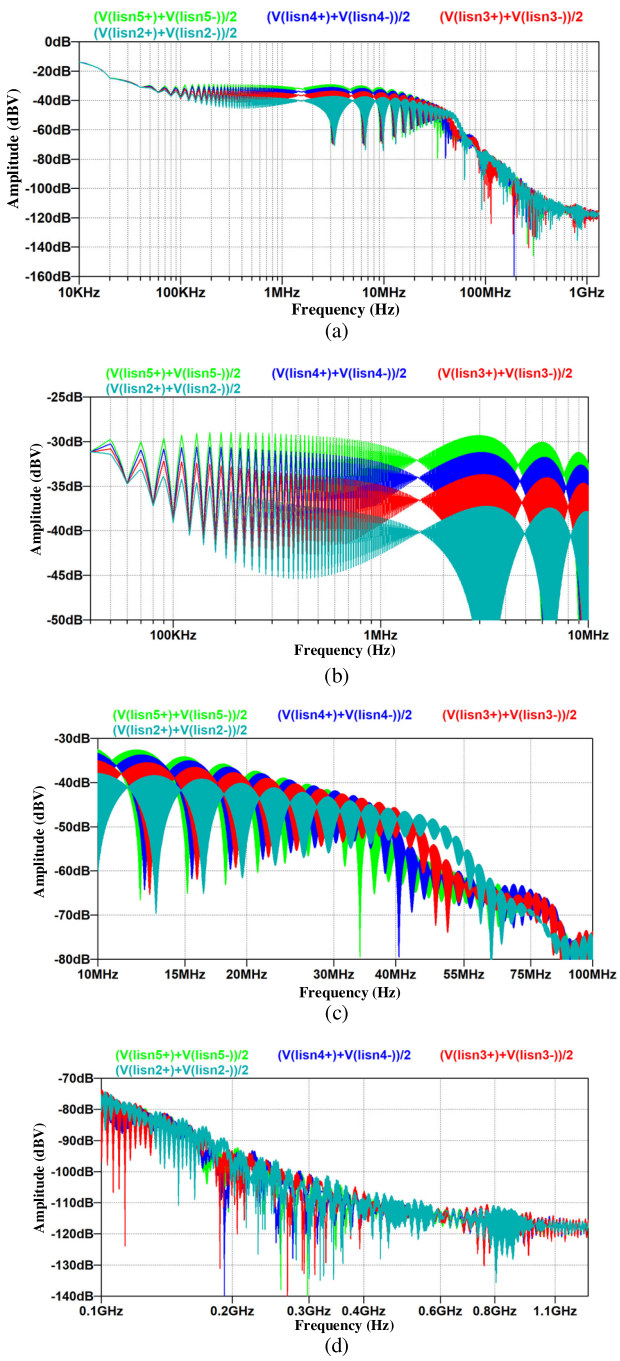

Fig. 11. CM voltages in frequency-domain of paralleled SiC MOSFETs when the parallel number $N = 2$, 3, 4, and 5 separately. (a) CM voltages spectrum during whole frequency domain. (b) Zoom-in when $\omega \leq \frac{1}{10}\omega_0$. (c) Zoom-in when $\frac{1}{10}\omega_0 < \omega < 10\omega_0$. (d) Zoom-in when $\omega \geq 10\omega_0$.

From Fig. 12(b), during the weak inductive coupling range, the amplitude of CM voltage increases slightly with increasing L_{loop}, but not very much, due to the weak effect of L_{loop}. But with the increasing frequency, the enlargement is more and more obvious, according to (34).

From the Fig. 12(c), during the strong inductive coupling range, the larger the coupling inductance L_{loop}, the lower the CM voltage, due to the strong effect of L_{loop}, according to (37).

V. Effect of Decoupling Capacitor on EMI Analysis of PMPSM

A. Modeling of CM Interference of PMPSM With Multiple Decoupling Capacitors

The decoupling capacitors are paralleled between the positive and negative buses of each switch. The small signal model of the PMPSM with parasitic inductance coupling is established in Fig. 13. The paralleled decoupling capacitance $C_{dec(i)}$ of branch

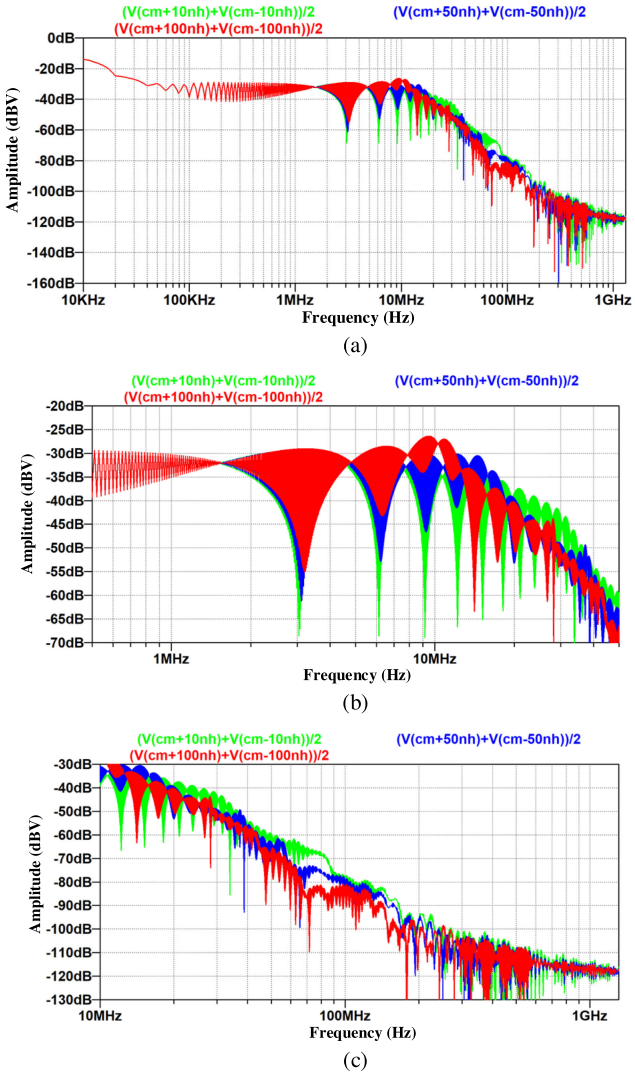

Fig. 12. CM voltages in frequency-domain of paralleled SiC MOSFETs when L_{loop} = 10, 50, and 100 nH separately. (a) CM voltages spectrum during whole frequency domain. (b) Zoom-in during weak inductive coupling range. (c) Zoom-in during strong inductive coupling range.

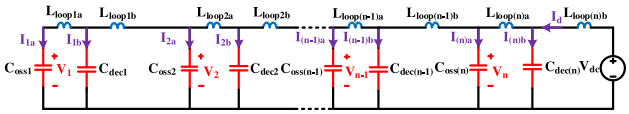

Fig. 13. Small signal model of the PMPSM with multiple decoupling capacitors.

i divides the parasitic inductance $L_{\mathrm{loop}(i)}$ into two parts, the part close to the branch is $L_{\mathrm{loop}(i)a}$ and the part far away from the branch is $L_{\mathrm{loop}(i)b}$. Therefore, the effect of decoupling capacitor on EMI source can be analyzed by simulation.

B. Simulation Analysis

When the amount of paralleled branches N is 5, the values of decoupling capacitors are the same as 10 nF, and the parasitic inductances between paralleled switching branches L_{loop} are the same as 10 nH, the drain currents and V_{ds} voltages in time-domain are shown in Fig. 14. The currents and voltages

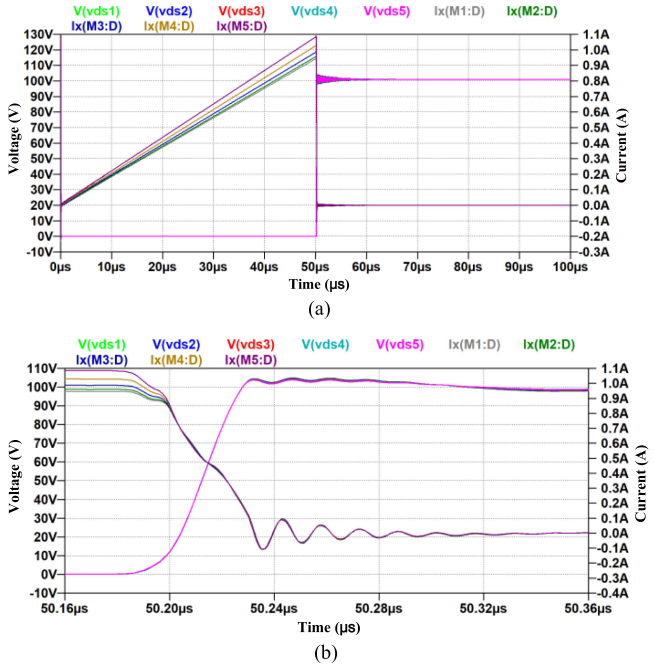

Fig. 14. Time-domain simulated drain currents and V_{ds} voltages of paralleled SiC MOSFETs with decoupling capacitance. (a) Drain currents and V_{ds} voltages waveforms. (b) Zoom-in of turn-OFF transition.

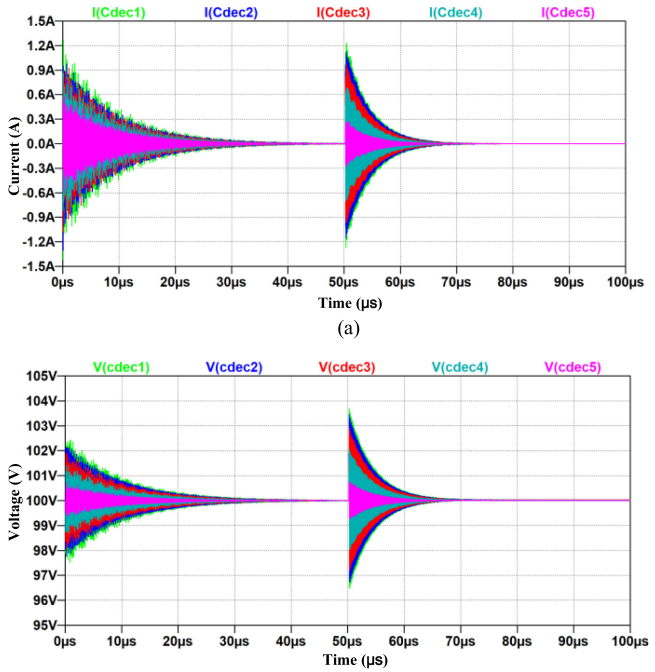

Fig. 15. Time-domain simulated currents and voltages of decoupling capacitances. (a) Currents of decoupling capacitances. (b) Voltages of decoupling capacitances.

of decoupling capacitances are shown in Fig. 15. It can be seen that there are a large number of high frequency components in the process of turn ON and turn OFF, and the farther from the dc bus, the higher the absorption of the corresponding decoupling capacitor. Thus, the decoupling capacitor can significantly suppress the high frequency component of the switching transition.

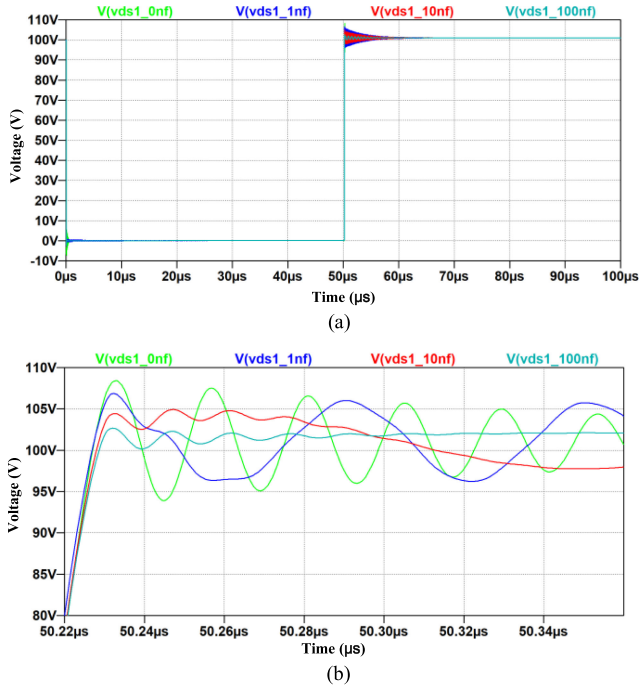

Fig. 16. Time-domain simulated V_{ds1} voltages of SiC MOSFET M1 with different decoupling capacitance values 0, 1, 10, and 100 nF separately. (a) V_{ds1} voltages of SiC MOSFET M1. (b) Zoom-in of turn-OFF transition.

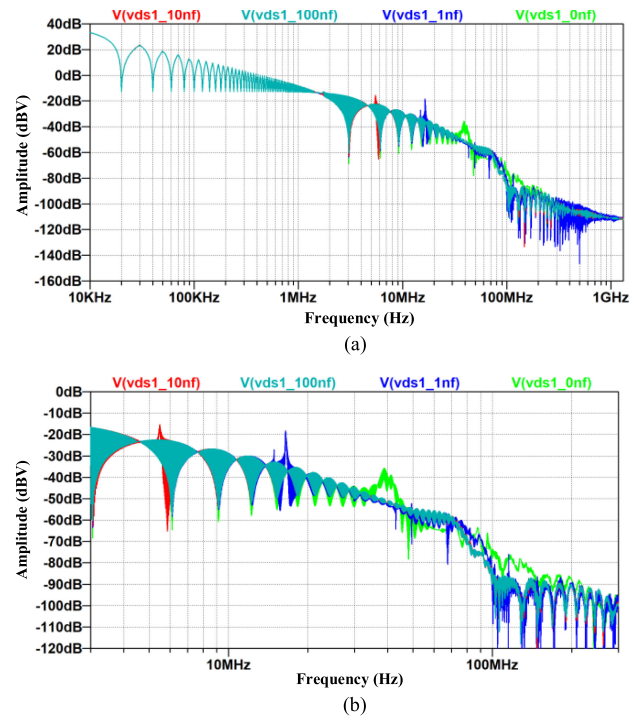

Fig. 17. Frequency-domain simulated EMI spectrums of SiC MOSFET M1 with different decoupling capacitance values 0, 1, 10, and 100 nF separately. (a) EMI spectrums of SiC MOSFET M1. (b) Zoom-in.

1) Comparative Analysis of Different Values of Decoupling Capacitors: When the amount of paralleled branches N *is* 5, the parasitic inductances between branches are 10 nH, and the decoupling capacitances are 0, 1, 10, and 100 nF separately, the simulation results of V_{ds1} voltages of SiC MOSFET M1 in time-domain and frequency-domain are shown in Figs. 16 and 17,

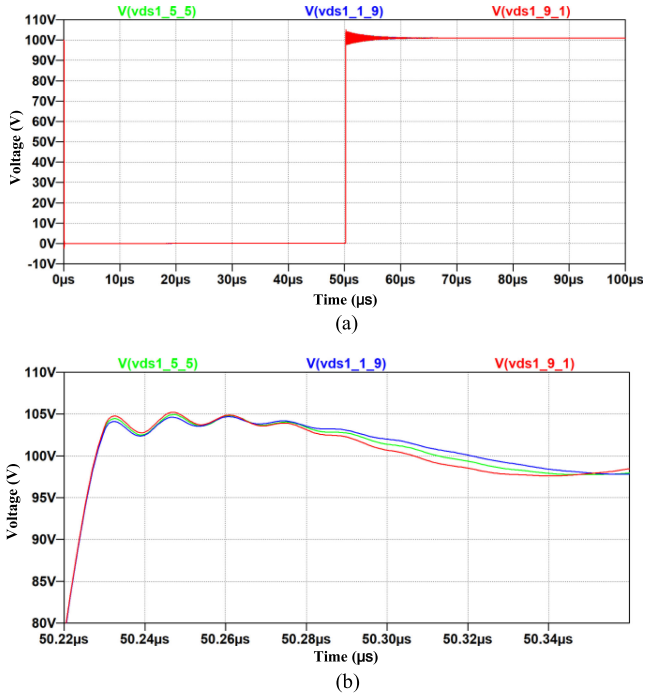

Fig. 18. Time-domain simulated V_{ds1} voltages of SiC MOSFET M1 with different proportion of coupling inductances 5nH:5nH, 1nH:9nH, 9nH:1nH separately. (a) V_{ds1} voltages of SiC MOSFET M1. (b) Zoom-in of turn-OFF transition.

respectively. It can be seen that with the increasing of decoupling capacitance value, the amplitude of high frequency oscillation decreases, and the oscillation frequency decreases. When the decoupling capacitance is 100 nF, the EMI spectrum amplitude caused by high-frequency oscillation is almost eliminated.

2) Comparative Analysis of Different Proportion of Coupling Inductances Between Branches: When the amount of paralleled branches N is 5, the decoupling capacitances are 10 nF, and the ratio of part A to B of parasitic inductance between branches is $Z_{\mathrm{loop}(i)a}/Z_{\mathrm{loop}(i)b} = \frac{5\,\mathrm{nH}}{5\,\mathrm{nH}}, \frac{1\,\mathrm{nH}}{9\,\mathrm{nH}}, \frac{9\,\mathrm{nH}}{1\,\mathrm{nH}}$, respectively, the time-domain waveforms and frequency spectrums of V_{ds1} voltage are shown in Figs. 18 and 19, respectively. It can be seen from Fig. 23 that when the parasitic inductance close to the branch (part A) is smaller than the parasitic inductance far away from the branch (part B), the oscillation of V_{ds} in the switching transition and the frequency are slightly reduced. When the parasitic inductance close to the branch (part A) is larger than the parasitic inductance far away from the branch (part B), there will be an opposite conclusion. When the parasitic inductance increases, this effect will be amplified proportionally. In order to reduce the proportion of parasitic inductance inside the branch (part A), the position of decoupling capacitor can be designed as close as possible to the switch, so as to reduce the high-frequency EMI produced by the switching transition.

VI. Experimental Analysis

A. Experimental Platform

In this article, the experimental platform of synchronous buck converter based on two comparative power modules with parallel-connected SiC MOSFETs are established as shown in

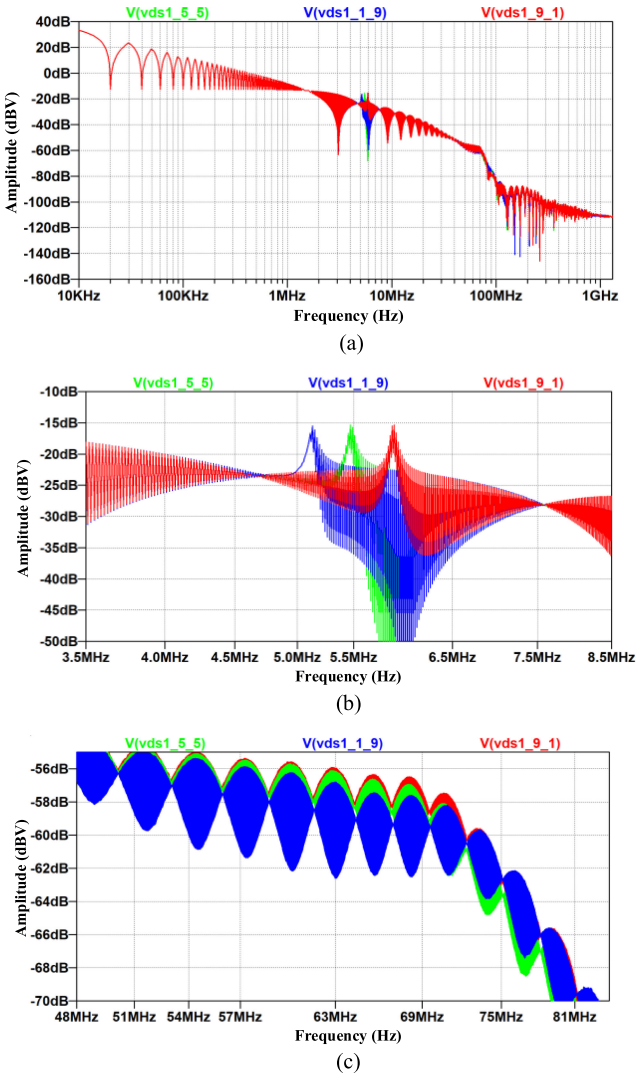

Fig. 19. Frequency-domain simulated EMI spectrums of SiC MOSFET M1 with different proportion of coupling inductances 5nH:5nH, 1nH:9nH, 9nH:1nH separately. (a) EMI spectrums of SiC MOSFET M1. (b) Zoom-in 1. (c) Zoom-in 2.

Fig. 20(a). One is a ROHM commercial 1.2-kV 300-A power module based on traditional layout, as shown in Fig. 1. The other is the self-made 1.2-kV 160-A power module with new layout including decoupling capacitance as shown in Fig. 20(b). According to the CM EMI theoretical mathematical modeling and analysis of PMPSM based on the parasitic inductive coupling theory, the self-made power module retains the ability of parasitic inductances between paralleled branches to suppress high-frequency CM interference. At the same time, decoupling capacitors are added near each SiC MOSFET to further suppress the high-frequency oscillation of the switching transition, so as to achieve the optimal suppression of CM interference, especially in the high-frequency range.

The SiC MOSFET in self-made power module is CPM2-1200-0080B manufactured by CREE, which has maximum voltage for 1200 V and rated current for 27 A when the junction temperature is 100 °C. The SiC Schottky barrier diode (SBD) in self-made power module is CPW4-1200-S020B manufactured by CREE,

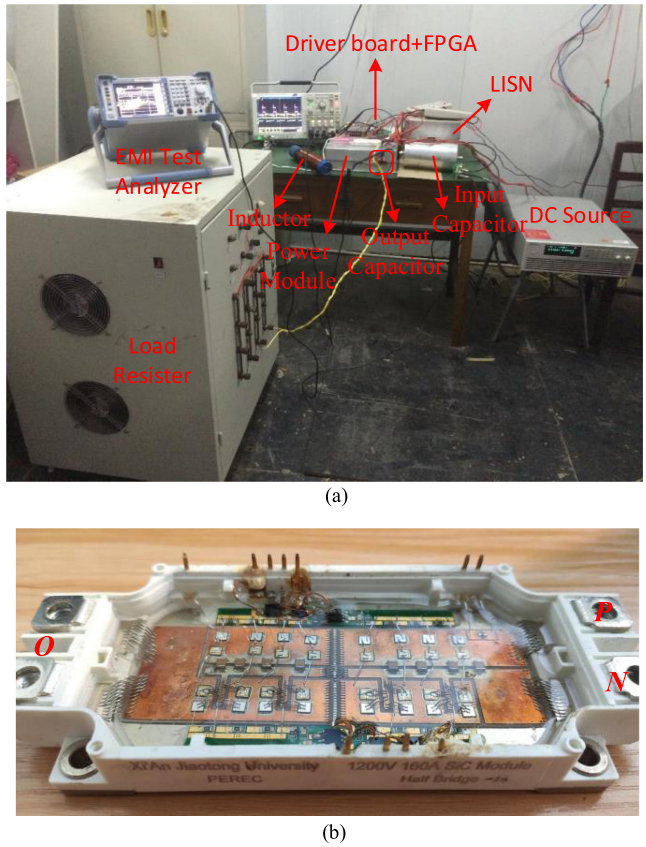

Fig. 20. Photograph of the prototype. (a) Experimental platform. (b) Self-made power module.

which has maximum voltage for 1.2 kV and rated current for 20 A when the junction temperature is 175 °C. Each phase-leg of power module contains eight paralleled SiC MOSFETs and eight antiparalleled SiC SBDs. The decoupling capacitor is C1210C563KDRACTU manufactured by KEMET, which has value for 560 nF and maximum voltage for 1 kV. The bonding wire is made of Al and the DBC substrate is made of Cu/AlN/Cu. The baseplate is made of Cu (2 mm).

Except for the two power modules used in the experimental platform, the other conditions are the same. The experimental platform uses 1200 V/15 A dc input voltage source, adds 400-μF input capacitor to maintain bus voltage, adopts self-winding 212.5-μH air core inductor, and three 3.3-μF/630-V film capacitors are connected in parallel to form a 9.9-μF output capacitance. Because the power of load resistance required in the experiment is very large, the high-power resistance box is selected as the load of the synchronous buck converter. There are twelve 40 Ω resistors in the resistance box, and the rated power of each resistor is 1.5 kW. In this experiment, eight resistors are connected in parallel to form the required 5 Ω resistance load. The driving resistance of self-made SiC power module is 10 Ω, while that of ROHM power module is 1 Ω, because the input capacitance of ROHM power module is much larger than the self-made power module.

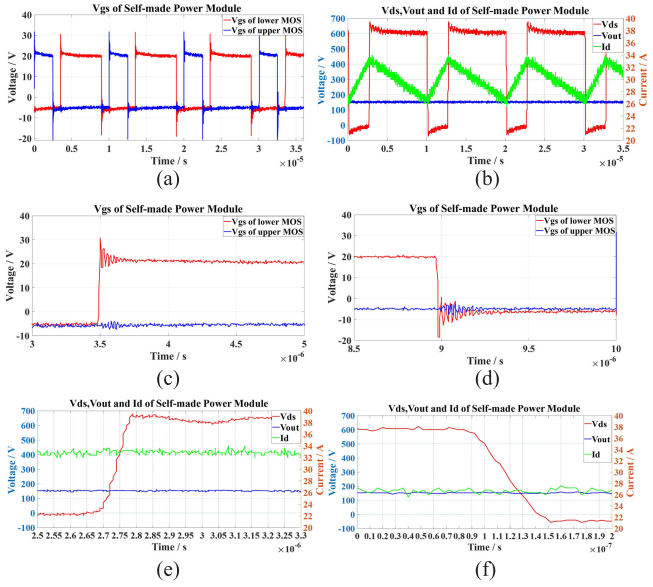

Fig. 21. Experimental results of synchronous buck converter based on self-made power module. (a) V_{gs}. (b) V_{ds}, I_d and V_{out}. (c) Zoom-in-view of V_{gs} during turn-ON period of lower MOS. (d) Zoom-in-view of V_{gs} during turn-OFF period of lower MOS. (e) Zoom-in-view of V_{ds}, $I_{d,}$ and V_{out} during turn-OFF period of upper MOS. (f) Zoom-in-view of V_{ds}, I_d, and V_{out} during turn-ON period of upper MOS.

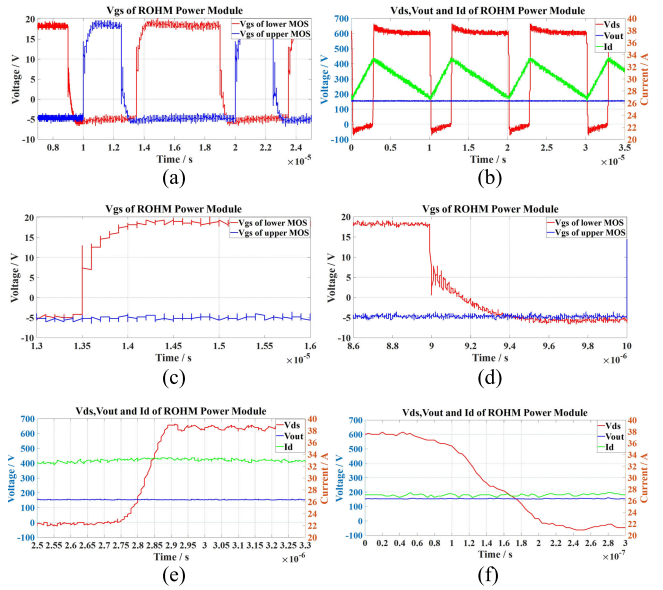

Fig. 22. Experimental results of synchronous buck converter based on ROHM power module. (a) V_{gs}. (b) V_{ds}, I_d and V_{out}. (c) Zoom-in-view of V_{gs} during turn-ON period of lower MOS. (d) Zoom-in-view of V_{gs} during turn-OFF period of lower MOS. (e) Zoom-in-view of V_{ds}, $I_{d,}$ and V_{out} during turn-OFF period of upper MOS. (f) Zoom-in-view of V_{ds}, $I_{d,}$ and V_{out} during turn-ON period of upper MOS.

B. Experimental Results

When the input dc voltage of the synchronous buck converter is 600 V, the driving signal with frequency of 100 kHz and duty cycle of 25% is applied to the upper switch of SiC MOSFET power module. The driving voltage V_{gs} and working waveforms V_{ds}, V_{out}, and I_d of the self-made SiC MOSFET power module and ROHM commercial power module are shown in Figs. 21 and 22, respectively. It can be seen that although the driving resistance of self-made power module is larger than that of ROHM power module, the driving voltage in self-made power module is faster than the ROHM power module. This is because the input parasitic capacitance of SiC MOSFET chip used in ROHM power module is much larger than that of self-made power module, which reduces the switching speed of the device. From Figs. 21 and 22, the rise time and fall time of V_{ds} in self-made power module are 100 and 60 ns, respectively. The rise time and fall time of V_{ds} in the ROHM power module are 120 and 145 ns, respectively. The rise time and fall time of V_{ds} in self-made power module are both smaller than the ROHM power module. According to the dc input voltage 600 V, the *dv/dt* during turn-OFF period of self-made power module and the ROHM power module are 6 and 5 V/ns, respectively. The *dv/dt* during turn-ON period of self-made power module and ROHM power module are 10 and 4.12 V/ns, respectively.

The LISN is installed on the input side of the dc buses to detect the CM voltage. The EMI test analyzer is used to test the CM interference spectrum. The CM conducted interference (150 kHz to 30 MHz) and near-field radiated interference (30 to 300 MHz) of synchronous buck converter based on two comparative power modules are shown in Fig. 23. It can be seen that the CM voltage of self-made power module decreases

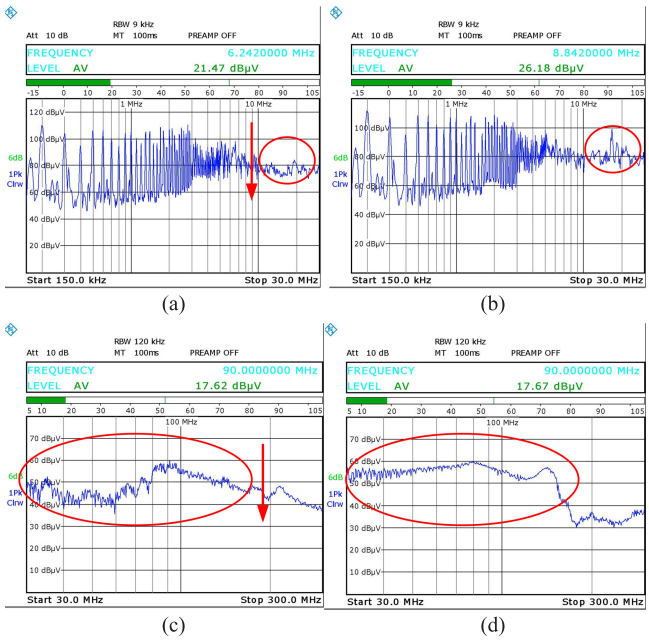

Fig. 23. CM EMI spectrums during of synchronous buck converter based on two comparative power modules. (a) CM EMI of self-made power module during conducted interference range. (b) CM EMI of ROHM power module during conducted interference range. (c) CM EMI of self-made power module during near-field radiated interference range. (d) CM EMI of ROHM power module during near-field radiated interference range.

significantly in high-frequency range of conducted interference (10 to 30 MHz) and low-frequency range of near-field radiated interference range (30 to 150 MHz) compared with the ROHM power module, which shows similar results with simulation in Fig. 17. As for the frequency band of 200–300 MHz, the

influence of other high-frequency parasitic parameters in the experimental circuit will be more and more important in the EMI test, such as the parasitic parameters of magnetic components like output inductor, the wire inductance of synchronous buck circuit, etc.

From Figs. 21 and 22, it can be seen that the *dv/dt* of self-made power module is larger than the ROHM power module, which may lead to more severe EMI noise source. However, the CM EMI of self-made power module tested by experiment is less than the ROHM power module, which proves the effectiveness of theoretical analysis and optimal design of the self-made power module.

VII. Conclusion

In this article, first, an EMI source generation mathematical modeling method for PMPSM is proposed, which found the coupling difference in condition of multiswitch in parallel. And the interference quantity can be calculated according to the inductive coupling of parallel-connected switches. Next, a CM propagation mathematical modeling method for PMPSM is proposed based on the inductive coupling theory, which found the suppressed effect to high-frequency CM interference by parasitic inductances between switches in parallel. In this respect, the parasitic inductance caused by aluminum wire bonding in power module is beneficial to suppress CM interference in high frequency range. Then, the influence of different location and values of decoupling capacitance on EMI are analyzed in detail, which pointed out that the position of decoupling capacitor can be designed as close as possible to the switch, so as to reduce the high-frequency EMI produced by the switching transition. Finally, a self-made 1.2-kV 160-A power module with SiC MOSFETs in parallel based on EMI optimized layout is proposed and tested, which has significant suppressed effect to high-frequency CM interference compared to the traditional power module.

Appendix

The equivalent CM interference source and impedance of (16), (17), and (18) can be deduced and proved by the mathematical induction as follows.

1) If the parallel-connected number $N = 1$ (see Fig. 24).

$$V_{eq1} = V_1 \tag{40}$$

$$Z_{eq1} = Z_{Cs1} + Z_{\text{loop1}} \tag{41}$$

$$I_{eq1} = \frac{V_1}{Z_{Cs1} + Z_{\text{loop1}}}. \tag{42}$$

2) If $N = 2$ (see Fig. 25), the derivation process of intermediate variables are as follows:

$$I_{cm1} = \frac{V_1}{Z_{Cs1} + Z_{\text{loop1}}} \tag{43}$$

$$Z_{\text{loop1}}{}' = Z_{Cs1} + Z_{\text{loop1}} \tag{44}$$

$$I_{cm2} = \frac{V_2}{Z_{Cs2}} \tag{45}$$

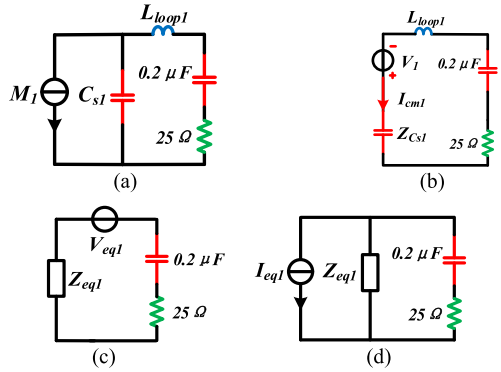

Fig. 24. Equivalent CM interference source and impedance when $N = 1$. (a) Deduction 1. (b) Deduction 2. (c) Deduction 3. (d) Deduction 4.

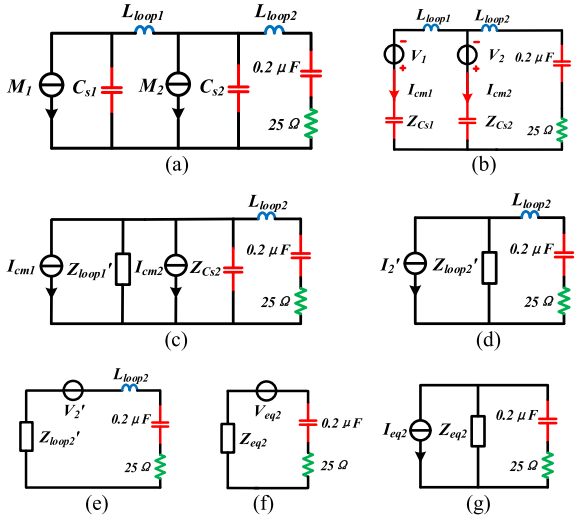

Fig. 25. Equivalent CM interference source and impedance when $N = 2$. (a) Deduction 1. (b) Deduction 2. (c) Deduction 3. (d) Deduction 4. (e) Deduction 5. (f) Deduction 6. (g) Deduction 7.

$$I_2{}' = I_{cm1} + I_{cm2} = \frac{V_1}{Z_{Cs1} + Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}} \tag{46}$$

$$Z_{\text{loop2}}{}' = Z_{\text{loop1}}{}' // Z_{Cs2} = (Z_{Cs1} + Z_{\text{loop1}}) // Z_{Cs2} \tag{47}$$

$$V_2{}' = I_2{}' Z_{\text{loop2}}{}' = \left(\frac{V_1}{Z_{Cs1} + Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right) ((Z_{Cs1} + Z_{\text{loop1}}) // Z_{Cs2}). \tag{48}$$

Thus, the equivalent CM interference source and impedance can be deduced as follows:

$$V_{eq2} = V_2{}' = I_2{}' Z_{\text{loop2}}{}' = \left(\frac{V_1}{Z_{Cs1} + Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right) ((Z_{Cs1} + Z_{\text{loop1}}) // Z_{Cs2}) \tag{49}$$

$$Z_{eq2} = Z_{\text{loop2}}{}' + Z_{\text{loop2}} = (Z_{Cs1} + Z_{\text{loop1}}) // Z_{Cs2} + Z_{\text{loop2}} \tag{50}$$

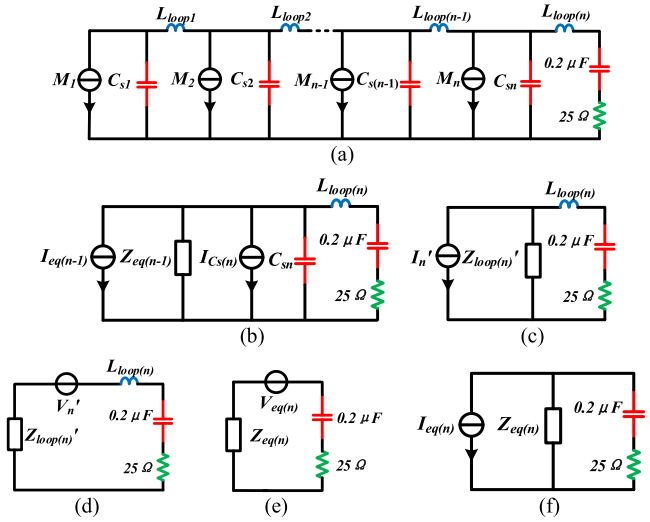

Fig. 26. Equivalent CM interference source and impedance when $N = n$. (a) Deduction 1. (b) Deduction 2. (c) Deduction 3. (d) Deduction 4. (e) Deduction 5. (f) Deduction 6.

$$I_{eq2} = \frac{V_{eq2}}{Z_{eq2}} = \frac{\left(\frac{V_1}{Z_{Cs1}+Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right)\left(\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}\right)}{\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}+Z_{\text{loop2}}}. \tag{51}$$

3) Assuming that $N = n-1$, we have

$$Z_{eq(n-1)} = \bigcup_{i=1}^{n-1} Y_i(Z_{Cs1}+Z_{\text{loop1}}) \tag{52}$$

$$V_{eq(n-1)} = \left(I_{eq(n-2)} + I_{Cs(n-1)}\right) \times \left(Z_{eq(n-1)} - Z_{\text{loop}(n-1)}\right) \tag{53}$$

$$I_{eq(n-1)} = \frac{V_{eq(n-1)}}{Z_{eq(n-1)}} = \frac{\left(I_{eq(n-2)} + I_{Cs(n-1)}\right)\left(Z_{eq(n-1)} - Z_{\text{loop}(n-1)}\right)}{Z_{eq(n-1)}}. \tag{54}$$

4) If $N = n$ (see Fig. 26).

$$I_{Cs(n)} = \frac{V_n}{Z_{Csn}}. \tag{55}$$

From (31) and (33), the intermediate variables can be calculated as

$$Z_{\text{loop}(n)}{}' = Z_{eq(n-1)}//Z_{Csn} = \left(\bigcup_{i=1}^{n-1} Y_i(Z_{Cs1}+Z_{\text{loop1}})\right)//Z_{Csn} \tag{56}$$

$$I_n{}' = I_{eq(n-1)} + I_{Cs(n)} = \frac{\left(I_{eq(n-2)} + I_{Cs(n-1)}\right)\left(Z_{eq(n-1)} - Z_{\text{loop}(n-1)}\right)}{Z_{eq(n-1)}} + \frac{V_n}{Z_{Csn}}. \tag{57}$$

Thus, if $N = n$, then

$$Z_{eq(n)} = Z_{\text{loop}(n)}{}' + Z_{\text{loop}(n)} = \left(\bigcup_{i=1}^{n-1} Y_i(Z_{Cs1}+Z_{\text{loop1}})\right)//Z_{Csn} + Z_{\text{loop}(n)} = \bigcup_{i=1}^{n} Y_i(Z_{Cs1}+Z_{\text{loop1}}) \tag{58}$$

$$V_{eq(n)} = V_n{}' = I_n{}' Z_{\text{loop}(n)}{}' = \left(\frac{\left(I_{eq(n-2)} + I_{cm(n-1)}\right)\left(Z_{eq(n-1)} - Z_{\text{loop}(n-1)}\right)}{Z_{eq(n-1)}} + \frac{V_n}{Z_{Csn}}\right) * \left(Z_{eq(n)} - Z_{\text{loop}(n)}\right) = \left(I_{eq(n-1)} + I_{Cs(n)}\right) \times \left(Z_{eq(n)} - Z_{\text{loop}(n)}\right) \tag{59}$$

$$I_{eq(n)} = \frac{V_{eq(n)}}{Z_{eq(n)}} = \frac{\left(I_{eq(n-1)} + I_{Cs(n)}\right)\left(Z_{eq(n)} - Z_{\text{loop}(n)}\right)}{Z_{eq(n)}}. \tag{60}$$

Next, we verify the initial value. If $n = 1$, we have

$$V_{eq1} = I_{Cs1}\left(Z_{eq1} - Z_{\text{loop1}}\right) = \frac{V_1}{Z_{Cs1}}\left(Z_{Cs1}+Z_{\text{loop1}}-Z_{\text{loop1}}\right) = V_1$$

$$Z_{eq1} = \bigcup_{i=1}^{1} Y_i(Z_{Cs1}+Z_{\text{loop1}}) = Y_1(Z_{Cs1}+Z_{\text{loop1}}) = Z_{Cs1}+Z_{\text{loop1}}$$

$$I_{eq1} = \frac{V_{eq1}}{Z_{eq1}} = \frac{V_1}{Z_{Cs1}+Z_{\text{loop1}}}$$

which are the same as (40), (41), and (42).

If $n = 2$, we have

$$V_{eq2} = \left(I_{eq1} + I_{Cs2}\right)\left(Z_{eq2} - Z_{\text{loop2}}\right) = \left(\frac{V_1}{Z_{Cs1}+Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right) * \left(\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2} + Z_{\text{loop2}} - Z_{\text{loop2}}\right) = \left(\frac{V_1}{Z_{Cs1}+Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right)\left(\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}\right)$$

$$Z_{eq2} = \bigcup_{i=1}^{2} Y_i(Z_{Cs1}+Z_{\text{loop1}}) = Y_2\left(Y_1(Z_{Cs1}+Z_{\text{loop1}})\right) = \left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}+Z_{\text{loop2}}$$

$$I_{eq2} = \frac{V_{eq2}}{Z_{eq2}} = \frac{\left(\frac{V_1}{Z_{Cs1}+Z_{\text{loop1}}} + \frac{V_2}{Z_{Cs2}}\right)\left(\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}\right)}{\left(Z_{Cs1}+Z_{\text{loop1}}\right)//Z_{Cs2}+Z_{\text{loop2}}}$$

which are the same as (49), (50), and (51).

Therefore, that is the end of the proof and the final CM interference equivalent voltage source, current source, and impedance are proposed as (16), (17), and (18).

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