






Circuit Configuration and Modulation of a Seven-Level Switched-Capacitor Inverter

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Abstract—In this article, a step-up seven-level inverter supplied by a single dc source suitable for renewable energy application is presented. Forming the desired output is realized by charging capacitors and synthesizing them based on a switched-capacitor concept. This structure is praised for the ability of sensorless voltage balancing of the capacitors, reducing control complexity to produce a bipolar staircase waveform. It also benefits from regenerative performance, avoiding unwanted capacitors overvoltage. A phase disposition pulsewidth modulation (PD-PWM) technique is utilized to control the circuit operation. Furthermore, a comparison with other recent topologies reveals that losses, number of semiconductor devices, and gate driver circuits are reduced. Theoretical analysis is verified through a laboratory prototype implementation. Experimental results under various types of loads approve the performance of the proposed inverter and validity of the design. Finally, maximum experimental efficiency of 94.3% (115 V, 250 W load) was reached.

Index Terms—Multilevel inverter, self-balancing, single-source, step-up converter, switched-capacitor.

I. INTRODUCTION

NOWADAYS, increasing use of renewable energy sources (RESs) due to the end of fossil energy and the necessity of reducing gas emissions has been influencing energy arena. Mostly these sources generate dc power while the conventional power systems are in the ac form. Hence, for connecting these energy sources to the power grid, various types of dc–ac converters are introduced. Among all, multilevel inverters (MLIs) have significantly drawn the attention of electrical engineers. These structures are praised for their better quality of output waveform, lower voltage stresses (dv/dt), less total harmonic distortion (THD) and their ability to operate in lower switching

frequencies [1]. MLIs have become popular and have some advantages in many applications such as fuel cells [2], solar panels [3], electric vehicles [4], motor drives [5], wind turbines, and grid-connected applications [6], [7]. The most applicable structures among them include cascaded H-Bridges (CHB) [8], neutral point clamped (NPC) [9], flying capacitor (FC) [10], and switched capacitor (SC) [11].

The CHB topology is famous for its modularity and simplicity to expand, leading to an increase in the number of output voltage levels. According to the aforementioned pros, by increasing H-bridge cells, the number of required switches and independent dc voltage sources are raised in CHB structures [12]. In this circumstance, implementation complexity, cost increment, and bulky system caused by low-frequency operation of the CHB structures increase [13]. To alleviate these problems, applying asymmetrical dc voltage sources [14] and a cascaded transformer [15] are proposed. Both NPC and FC structures suffer from voltage balancing complexity of dc-link capacitors. Moreover, high number of semiconductor components decreases the reliability of the circuit and its application. Also, among their active switches, they do not have the ability of equal voltage sharing, both statically and dynamically [16], [17].

Switched-capacitor multilevel inverters (SCMLIs) are, therefore, introduced in order to cover the abovementioned problems. Many new converters were designed to decrease the number of components such as semiconductors, dc sources, and capacitors to lessen costs but they have other drawbacks in their structure [18], [19].

One of the most essential traits for such converters (especially in many renewable energy applications with low-voltage dc source such as solar systems), which standard MLI circuits do not possess, is boosting capability. The voltage boosting is realized by charging capacitors and then summing the capacitors voltages up in a series connection to be applied to the output, eliminating the need for bulky transformers or inductors [20], [21].

Another crucial character for an SCMLI circuit is whether the inverter can be used in application with regenerative load feature or not. For any inverter circuits, every time interval that the polarity of the output voltage and current are the same, the power is supplied to the load and the inverter is in the “inverting” mode. Otherwise, the inverter is in the “rectification or regeneration” mode [22]. Application with regenerative loads requires inverters with a bidirectional power flow preventing the capacitors from over-charging and potential damages. Ergo, the

Manuscript received March 28, 2020; revised August 24, 2020; accepted October 22, 2020. Date of publication November 6, 2020; date of current version February 5, 2021. Recommended for publication by Associate Editor J. Wang. (Corresponding author: Jafar Adabi.)

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Digital Object Identifier 10.1109/TPEL.2020.3036351

excess charge is fed to the input source. In this case, the authors in [23]–[26] introduced new SCMLI structures with a regenerative load feature. Also, they all have the boosting capability except for [26], where the maximum amplitude of the output is equal to the input source. Besides, the capacitors' voltages in [23]–[25] are self-balanced and there is no need for any extra balancing control system. However, the number of components required for these topologies are high. The structures introduced in [20] and [27]–[29] can boost the input voltage, but as they use series diodes in their capacitors' charging paths, they lack the regenerative load feature.

This article presents a seven-level single-source step-up boost inverter with a low number of components. It requires two capacitors to boost the input voltage up to $3V_{in}$. Phase disposition pulsewidth modulation (PD-PWM) control strategy is used to produce the desired output waveform with lower harmonic content. By charging or discharging capacitors in small sequential time intervals, they would face the least possible voltage drop. This structure is suitable for a vast range of low-voltage single-source application using photovoltaic, batteries, and fuel cells (without any need for bulky and sometimes low efficient inductors).

The rest of this article is organized as follows. The working principles of the proposed circuit are brought in Section II, containing capacitors charging pattern, different operation modes, and a brief note on a circuit modulation method. Section III reveals the determination of circuit capacitors, power loss calculation, and a comparative discussion of the presented structure against several recent topologies. Furthermore, design considerations and results of a test setup including both regenerative and nonregenerative load behaviors are added in Section IV. Finally, Section V concludes this article.

II. PRINCIPLE OF OPERATION

Fig. 1 describes the overall structure of the proposed seven-level boost inverter and its operating modes. It consists of a single dc source (V_{dc}), which charges the capacitors C_1 and C_2 one after the other, directly. Also, the inverter supplies the load by a few numbers of switches (maximum number of four) per each level, which will increase the overall efficiency of the converter. However, this converter produces seven-levels of voltage ($\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm 1V_{dc}$, and 0) with only two capacitors, nine switches, and nine driver circuits.

A. Capacitor Charging

The capacitors C_1 and C_2 can be charged up to V_{dc} by the input source at different operation modes when they are not being used to generate the output. Thus, the capacitors' voltages would be kept in an acceptable range and well balanced. This means that there is no need for any voltage feedback from the capacitors to the control system.

It is worth noting that the proposed converter has power regeneration capability, which means that the capacitors can be automatically discharged to the source if overcharged (as an example is brought in Fig. 1). Therefore, the converter can be

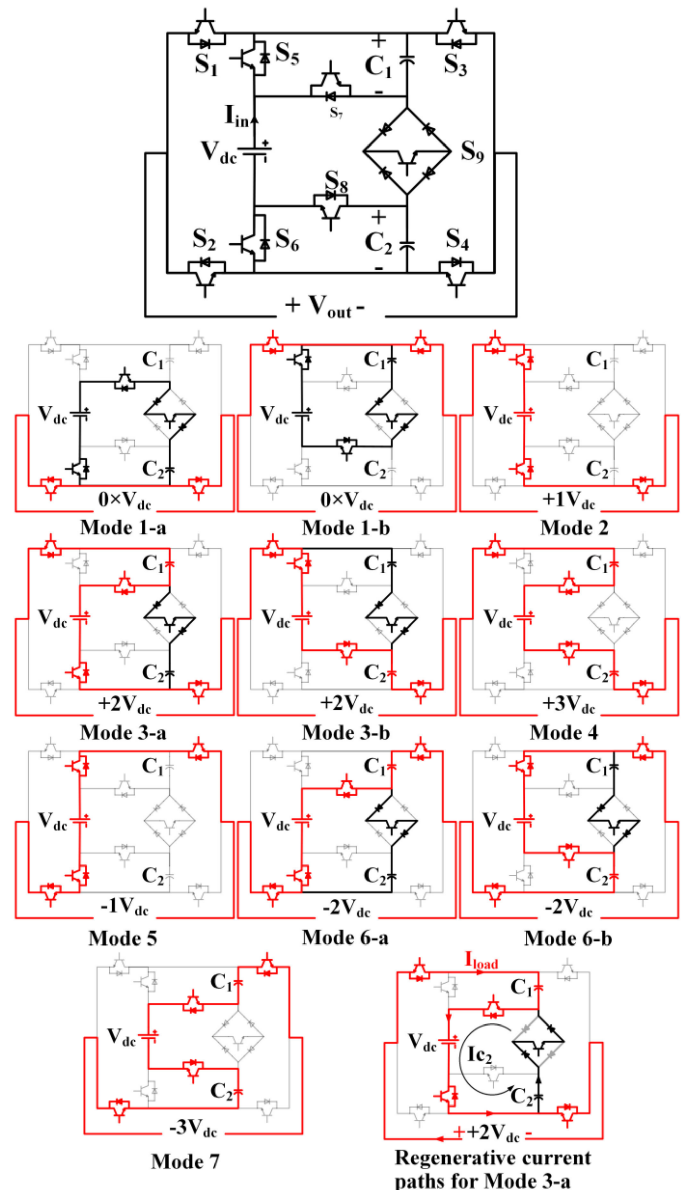


Fig. 1. Overall structure of the proposed seven-level boost inverter and its operating modes.

also used for motor drive purposes. Note that for nonregenerative loads, the structure can operate normally and S_9 could be simplified as a unidirectional switch.

B. Operation Modes

Fig. 1 also shows the different operation modes of the proposed converter and its switching states to generate the output voltage levels. Furthermore, the capacitor charging paths are added. These modes are described below.

1) *Mode 1-a, 1-b: $0V_{dc}$* : This mode of operation which produces zero voltage at the v_{dc} output can be applied by two different switching states; by using either switches S_2 and S_4 or S_1 and S_3 . In each of these states, one of the capacitors can be charged. By applying these states sequentially, both of the capacitors will stay balanced.

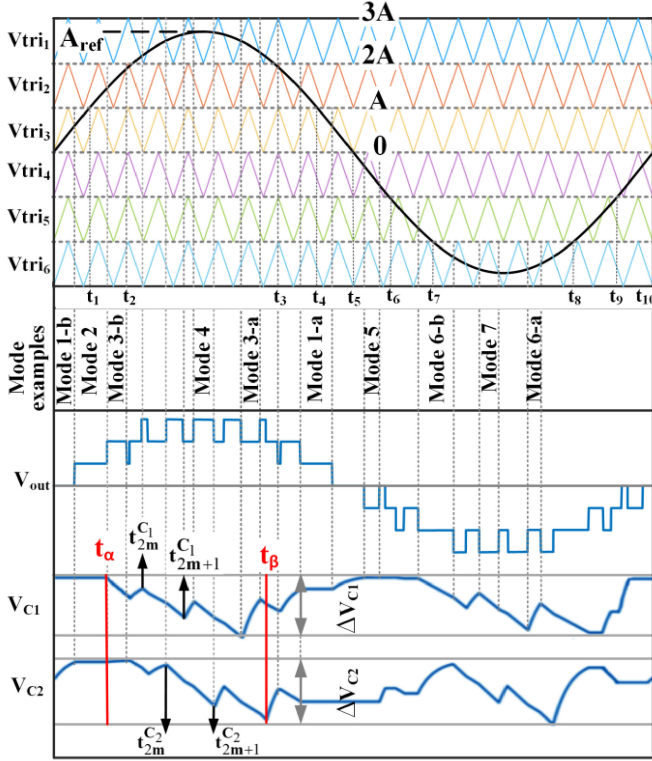


Fig. 2. PD-PWM modulation strategy.

2) *Mode 2*: $+1V_{dc}$: In this mode, input voltage is directly applied to the load through switches S_1 , S_5 , S_6 , and S_4 .

3) *Mode 3-a, 3-b*: $+2V_{dc}$: This mode can be applied by two different switching states. In the first state, a series connection of the supply voltage and C_1 generates the output while C_2 is being charged (mode 3-a). In the second state, C_1 is replaced by C_2 (mode 3-b). Similar to mode 1, both states are applied sequentially to maintain the capacitors voltage balance.

4) *Mode 4*. $+3V_{dc}$: To generate $+3V_{dc}$ across the load, both of the capacitors and the input source are used, meaning that at this stage no capacitor can be charged.

5) *Mode 5-7*. $-1V_{dc}$, $-2V_{dc}$, $-3V_{dc}$: These voltages can be generated in the same way as their positive counterparts. The only difference is that switches S_2 and S_3 must be turned ON instead of S_1 and S_4 .

C. PD-PWM Modulation Method

The PD-PWM technique has been adapted to control the sensorless operation of the proposed converter in the offline mode. As shown in Fig. 2, six level-shifted PWM carriers (with an amplitude of A and frequency of f_{pwm}) are compared to a sine reference signal ($V_{ref} = A_{ref} \sin(2\pi f_{ref} t)$) in the DSP controller. As a result, the appropriate gate signals for the circuit switches are produced in predetermined time intervals. The main benefit of this method is its simplicity in realization, fast response, and a waveform with lower harmonic content [24].

The rules of operation under such technique are revealed in Table I. Where $V_{tri1,2,\dots,6}$ are six carrier (PWM) signals (with shifted levels and identical amplitudes) generated to be

TABLE I
PD-PWM SWITCHING MODES AND RELEVANT STATES OF CHARGE

Amplitude of V_{ref}	mode	Output voltage	C_1	C_2
$V_{ref} > V_{tri1}$	Mode 4	$+3V_{dc}$	▼	▼
$V_{tri2} < V_{ref} < V_{tri1}$	Mode 3-a	$+2V_{dc}$	▲	▼
$V_{tri2} < V_{ref} < V_{tri1}$	Mode 3-b	$+2V_{dc}$	▼	▲
$V_{tri3} < V_{ref} < V_{tri2}$	Mode 2	$+1V_{dc}$	-	-
$V_{tri4} < V_{ref} < V_{tri3}$	Mode 1-a	0	▲	-
$V_{tri4} < V_{ref} < V_{tri3}$	Mode 1-b	0	-	▲
$V_{tri5} < V_{ref} < V_{tri4}$	Mode 5	$-1V_{dc}$	-	-
$V_{tri6} < V_{ref} < V_{tri5}$	Mode 6-a	$-2V_{dc}$	▲	▼
$V_{tri6} < V_{ref} < V_{tri5}$	Mode 6-b	$-2V_{dc}$	▼	▲
$V_{ref} < V_{tri6}$	Mode 7	$-3V_{dc}$	▼	▼

compared with the reference signal. Also, the output waveform and capacitors voltages for different modes of operations are illustrated over one period in Fig. 2.

III. DESIGN CONSIDERATIONS

A. Capacitor Calculations

It is essential to make sure that the voltages of the two capacitors do not drop below a permissible value, as they have the task of generating the output voltage with magnitudes higher than $1V_{dc}$. For this, the amount of energy they store and pump to the output should be measured to calculate the capacitances. The capacitors voltages and their charging and discharging patterns at different modes of operation are shown in Fig. 2. Maximum discharge happens for a resistive load as the maximum current is drawn in mode 4, in which both capacitors are supplying the output.

The capacitors' voltage drop occurs in $[t_\alpha, t_\beta]$. To calculate the required capacitances, the discharge of the capacitors in this time interval must be measured for a permissible voltages drop at the desired output load. The charge and discharge cycle of the capacitors in $[t_\alpha, t_\beta]$ is assumed to happen for n times and $m = (0, 1, 2, \dots, n)$. As can be seen in Fig. 2, discharging cycles of C_1 starts at $t_{2m}^{C_1}$ and ends at $t_{2m+1}^{C_1}$. Similarly, the discharge of C_2 happens between $[t_{2m}^{C_2}, t_{2m+1}^{C_2}]$ cycles. The amount of electrical charge (Q) discharged from t_{2m} to t_{2m+1} of the capacitors C_1 and C_2 are [23] as follows:

$$\Delta Q_m^{C_1} = \int_{t_{2m}^{C_1}}^{t_{2m+1}^{C_1}} I_{out} \cdot \sin(\omega t) \cdot dt \quad (1)$$

$$\Delta Q_m^{C_2} = \int_{t_{2m}^{C_2}}^{t_{2m+1}^{C_2}} I_{out} \cdot \sin(\omega t) \cdot dt \quad (2)$$

where I_{out} represents the amplitude of the output current, $\Delta Q_m^{C_1}$ and $\Delta Q_m^{C_2}$ are the discharge amount of the capacitors during the m th cycle, and $\omega = 2\pi f_{ref}$. The total amount of electrical charge drawn from each capacitor (Q_{total}) can be expressed as follows:

$$Q_{total}^{C_1} = \sum_0^n \Delta Q_m^{C_1} = \sum_0^n \left(\int_{t_{2m}^{C_1}}^{t_{2m+1}^{C_1}} I_{out} \cdot \sin(\omega t) \cdot dt \right) \quad (3)$$

$$Q_{\text{total}}^{C_2} = \sum_0^n \Delta Q_m^{C_2} = \sum_0^n \left(\int_{t_{2m}}^{t_{2m+1}} I_{\text{out}} \cdot \sin(\omega t) \cdot dt \right). \quad (4)$$

Regardless of the increase in capacitors voltages at level ± 2 , assuming the worst case in which no charge is absorbed by the capacitors, the minimum allowable capacitance can be formulated as follows:

$$C_{1\text{min}} = \frac{Q_{\text{total}}^{C_1}}{V_{\text{ripple}}^{C_1}} \quad C_{2\text{min}} = \frac{Q_{\text{total}}^{C_2}}{V_{\text{ripple}}^{C_2}}. \quad (5)$$

By assuming V_{ripple}^C below 10%, recovery of the capacitors voltage at levels 0 and ± 2 will be assured. Also, it is noticeable that no capacitors are charged or discharged at level ± 1 .

B. Power Loss Study

Power loss of the proposed converter can generally be classified into the following three categories:

- 1) switching losses (P_{sw});
- 2) conduction losses (P_{cond});
- 3) capacitor voltage ripple (charging) losses.

In the following, a brief discussion of each category and its impact on efficiency in different load conditions is presented.

1) *Switching Loss*: Switching energy losses of insulated-gate bipolar transistors (IGBTs) (E_{sw}) in each switching cycle consist of turn-ON loss (E_{on}) and turn-OFF loss (E_{off}). Switching losses are inherent characteristics of IGBTs, specified by the manufacturer under predefined conditions. These losses vary under different circumstances, including: junction temperature (T_j), collector current (I_c), blocking voltage (V_b), gate-emitter voltage (V_{GE}), and gate resistance (R_{GE}). Therefore, the E_{sw} can be calculated as follows:

$$E_{\text{sw}} = (E_{\text{on}} + E_{\text{off}}) \cdot \text{adj}_{T_j} \cdot \text{adj}_{I_c} \cdot \text{adj}_{V_b} \cdot \text{adj}_{V_{\text{GE}}}. \quad (6)$$

In which E_{on} and E_{off} are losses presented by the IGBT module datasheet in nominal condition and adj_{T_j} , adj_{I_c} , adj_{V_b} , and $\text{adj}_{V_{\text{GE}}}$ are adjustment factors for the aforementioned variable conditions. Therefore, the total switching power loss for the nine switches (P_{sw}) can be defined as follows:

$$P_{\text{sw}} = \sum_{k=1}^9 P_{\text{sw}_k} = \sum_{k=1}^9 E_{\text{sw}_k} \cdot f_{\text{ref}} \cdot N_k. \quad (7)$$

N_k is the number of times each switch is turned ON and OFF in one cycle of reference waveform. Switches S_1, S_2, S_3 , and S_4 turn ON and OFF once per each PWM cycle while $|A_{\text{ref}} \sin(\omega t)| \leq A$ and stay ON or OFF for the rest of the reference cycle time. S_5, S_6, S_7 , and S_8 turn ON and OFF once per each two PWM cycles. While, S_9 turns ON and OFF once for every PWM cycles. Thus,

$$N_k = \begin{cases} 2f_{\text{PWM}} \frac{\sin^{-1} \sin(\frac{A}{A_{\text{ref}}})}{\pi f_{\text{ref}}} & k = 1, 2, 3, 4 \\ \frac{f_{\text{PWM}}}{2f_{\text{ref}}} & k = 5, 6, 7, 8 \\ \frac{f_{\text{PWM}}}{f_{\text{ref}}} & k = 9. \end{cases} \quad (8)$$

2) *Conduction Loss*: Conduction losses occur due to current passing through circuit components. In the proposed structure, the conduction losses are the result of capacitors' internal resistance (R_{ESR}) losses and IGBTs/diodes losses. IGBT losses can

TABLE II
CIRCUIT CONDUCTIVE LOSS FACTORS

V _{out} Level	Equivalent Circuit	Loss factors	
		V _L	R _L
0 V _{dc}	1 IGBT & 1 Diode	$V_{CE_0} + V_{F_0}$	$R_{CE} + R_D$
± 1 V _{dc}	2 IGBTs & 2 Diodes	$2(V_{CE_0} + V_{F_0})$	$2(R_{CE} + R_D)$
± 2 V _{dc}	3 IGBTs, 1 Diode & 1 Capacitor	$3V_{CE_0} + V_{F_0}$	$3R_{CE} + R_D + R_{ESR}$
± 3 V _{dc}	4 IGBTs & 2 Capacitors	$4V_{CE_0}$	$4R_{CE} + 2R_{ESR}$

be calculated by multiplying the IGBT collector-emitter voltage (V_{CE}) and collector current (I_c). Likewise, diode losses are the result of the forward voltage drop (V_F) while it conducts current (I_F). The output characteristics of IGBT (V_{CE}) and diode (V_F) change at different current and operation conditions. V_{CE} and V_F can be calculated as follows:

$$V_{\text{CE}} = V_{\text{CE}_0} + R_{\text{CE}} \cdot I_c \quad (9)$$

$$V_F = V_{F_0} + R_D \cdot I_F. \quad (10)$$

V_{CE_0} and R_{CE} are the adjusted IGBT parameters, which represent the nonlinear relation between V_{CE} and I_c at circuit operation conditions. Similarly, V_{F_0} and R_D are adjusted diode internal voltage drop and resistance, respectively. Therefore, equivalent circuits of the proposed topology and its conductive loss factors for each output levels are brought in Table II. It is worth mentioning that loss factors R_L and V_L represent the path resistance and internal voltage drop of semiconductor devices for each level of the output, respectively.

According to Fig. 2, while $|A_{\text{ref}} \sin(\omega t)| \leq A$, the output goes back and forth between levels $L = 0$ and 1. Similarly, the output alternate between levels $L = 1$ and 2 and $L = 2$ and 3 while $A \leq |A_{\text{ref}} \sin(\omega t)| \leq 2A$ and $2A \leq |A_{\text{ref}} \sin(\omega t)| \leq 3A$, respectively. For $L = 0, 1$, and 2, the energy loss occurring in the aforementioned states can be defined as follows [21]:

$$E_{\text{cond}}^{L \& L+1} = \int_{t_i}^{t_j} \left([I_{\text{out}} \sin(\omega t)]^2 \left[\frac{R_{L+1} \frac{A_{\text{ref}} \sin(\omega t) - L \times A}{A} + R_L \left(1 - \frac{A_{\text{ref}} \sin(\omega t) - L \times A}{A} \right)}{V_{L+1} \frac{A_{\text{ref}} \sin(\omega t) - L \times A}{A} + V_L \left(1 - \frac{A_{\text{ref}} \sin(\omega t) - L \times A}{A} \right)} \right] \right) dt. \quad (11)$$

Energy loss happens at the following time intervals:

$$[t_i - t_j]: \begin{cases} [t_0 - t_1], [t_4 - t_5], [t_5 - t_6], [t_9 - t_{10}] & L = 0 \\ [t_1 - t_2], [t_3 - t_4], [t_6 - t_7], [t_8 - t_9] & L = 1 \\ [t_2 - t_3], [t_7 - t_8] & L = 2. \end{cases} \quad (12)$$

In which, $t_1 = \frac{1}{\omega} \text{Arcsin}(\frac{A}{A_{\text{ref}}})$, $t_2 = \frac{1}{\omega} \text{Arcsin}(\frac{2A}{A_{\text{ref}}})$, $t_5 = \pi/\omega$, $t_{10} = 2\pi/\omega$, $t_3 = t_5 - t_2$, $t_4 = t_5 - t_1$, $t_6 = t_5 + t_1$, $t_7 = t_5 + t_2$, $t_8 = t_{10} - t_2$, and $t_9 = t_{10} - t_1$. Ultimately, the total conduction loss is

$$P_{\text{cond}} = f_{\text{ref}} (4E_{\text{cond}}^{L0\&1} + 4E_{\text{cond}}^{L1\&2} + 2E_{\text{cond}}^{L2\&3}). \quad (13)$$

TABLE III
COMPARISON OF THE SUGGESTED SEVEN-LEVEL INVERTER WITH RECENT TOPOLOGIES

NO.	Topology	N levels	N switches	N diodes	N drivers	N capacitors	N sources	PIV (%Vin)	TSV (%Vin)	Boost ratio	Regenerative	Pout (W)	Efficiency (%)	
													Theoretical	Experimental
1	[31] 2018	7	10	10	7	0	3	3	19	1x	Yes	50	N.A.	97.6
2	[32] 2017	7	8	8	8	0	2	2	12	1x	Yes	250 1000	N.A.	97 98
3	[3] 2017	7	8	8	8	0	2	3	18	1x	Yes	100	N.A.	94.3
4	[26] 2015	7	7	9	7	3	1	1	5	1x	Yes	500	N.A.	91
5	[34] 2017	7	12	12	12	4	1	1	3.33	1x	yes	500	N.A.	N.A.
6	[35] 2012	7	14	14	12	5	1	1	3.33	1x	yes	5000	N.A.	N.A.
7	[36] 2018	7	10	10	8	3	1	1	8	1.5x	yes	225	N.A.	N.A.
8	[37] 2019	7	10	10	8	4	1	1	7.5	1.5x	yes	266.2	96.5	96.5
9	[33] 2018	7	16	16	14	2	1	1	16	3x	Yes	40	N.A.	94
10	[23] 2014	7	10	10	10	2	1	3	18	3x	Yes	3.5	94.6	95.4
11	[24] 2016	7	16	16	14	2	1	1	16	3x	Yes	200 1000	93.8 90.2	N.A.
12	Proposed	7	9	12	9	2	1	3	17	3x	Yes	50 250 500	96.07 95.3 94.5	92 94.3 92.2
13	[38] 2018	7	9	10	8	3	1	1	7.5	1.5x	No	218	N.A.	97.29
14	[20] 2014	7	7	11	7	2	1	3	21	3x	No	247.5	N.A.	89.2
15	[28] 2018	7	14	14	14	2	1	1	14	3x	No	182.4	91.7	88.93
16	[39] 2019	7	8	6	8	2	1	3	18	3x	No	N.A.	N.A.	N.A.
17	[40] 2019	7	8	10	8	2	1	3	16	3x	No	189	N.A.	97.1
18	[11] 2014	7	8	10	8	2	1	3	18	3x	No	N.A.	N.A.	N.A.

3) *Capacitor Voltage Ripple Losses*: The power losses caused by the difference between the input and capacitors voltages, while they are paralleled to the source, can be calculated as follows:

$$P_C = \frac{1}{2} \sum_{k=1}^u C \cdot \Delta V_k^2 \cdot f_{\text{ref}}. \quad (14)$$

In which, u represents the number of both capacitors' charging states, and then ΔV_k is charging voltage ripple of the capacitors. Finally, based on [21] and [23], total power loss (P_{loss}) and efficiency (η) of the proposed converter can be calculated as follows:

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{cond}} + P_{C1} + P_{C2} \quad (15)$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100. \quad (16)$$

C. Comparison With Other Topologies

Table III reveals a detailed comparison over the proposed structure and other existing ones, in terms of number of circuit components (switches, driver circuits, capacitors, and diodes), number of input sources, peak inverse voltage (PIV), total standing voltage (TSV), regenerative load ability, and the boosting ratio. PIV implies the maximum voltage, which the switch has to bear in the OFF-state. In some applications, the number of switches may be low but some of the switches have to work with high voltages. Besides, TSV is the sum of standing/operating voltage (or simply sum of the PIV) of all the switches that should also be considered. The boost ratio is defined as the proportion

of the output amplitude to the input source or the sum of input sources in case if there is more than one source used.

In the context of step-up SC-MLI, it is essential to design a topology to use maximum possible standard rating of the switches. Therefore, reducing the number of switches by increasing the standing voltage in the standard range is an important aspect, which should be considered in comparison. In fact, the input voltage could be raised until the PIV is less than a certain acceptable percentage ($x\%$) of the switches rated voltage ($V_{\text{rated}}^{\text{SW}}$) as follows:

$$\text{PIV} < x\% \cdot V_{\text{rated}}^{\text{SW}}. \quad (17)$$

As can be described in Table III, unlike the proposed circuit, authors in [3], [31], and [32] introduced structures that require several isolated dc sources and the amplitude of the output does not exceed the sum of input voltages. In case of [3] and [32], it should be noted that using symmetric sources leads to a five-level output waveform.

Although [11], [20], [28], and [38]–[40] are single-source topologies with voltage boosting ability and have relatively less semiconductor devices (except for [28]), they cannot supply regenerative loads. The authors in [26] and [34]–[37] present single-source structures with a considerably low TSV. However, they either cannot boost the input voltage, or they have a low boosting ratio. Also, they require more capacitors.

It is noticeable that topologies presented in [23], [24], and [33] can meet both the boost ratio and regenerative capability requirements, whereas the introduced SCMLI requires less active switches and, therefore, less gate driver circuits for the same

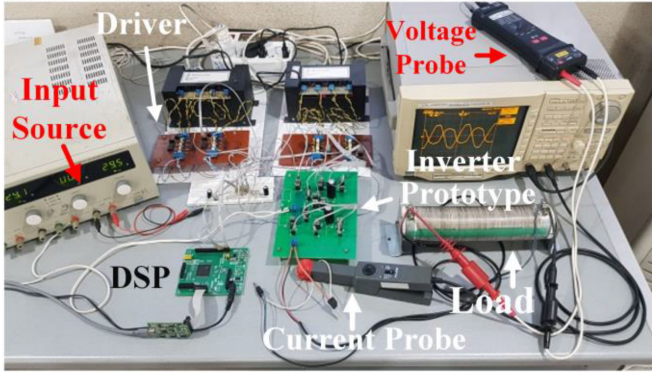


Fig. 3. Laboratory prototype of the proposed structure.

output levels. Considering a semiconductor count, boost factor, and regenerative load ability, the proposed topology should compete with [23], [24], and [33].

Selecting each switching device in an inverter is related to the maximum voltage impressed and the peak and average current going through it. Therefore, the product of voltage stress and current stress is introduced as a switching device power (SDP) index [41]. The sum of SDP of all the switching devices used in the circuit is an important factor of an inverter. Considering the number of switching devices used (N), the peak voltage impressed on the devices (V_k), $I_{k,average}$ and $I_{k,peak}$ as the average and peak current through the device, respectively, then we have

$$\text{Total Average SDP} = \text{SDP}_{\text{avg}} = \sum_{k=1}^N V_k \cdot I_{k, \text{average}} \quad (18)$$

$$\text{Total Peak SDP} = \text{SDP}_{\text{peak}} = \sum_{k=1}^N V_k \cdot I_{k, \text{peak}} \quad (19)$$

The SDP of all topologies with the boosting ability for the same conditions including semiconductor device properties, output power ($P_{\text{out}} = 750 \text{ W}$, $V_{\text{out_max}} = 375 \text{ V}$), load power factor ($\text{PF} = 1$), and input voltage ($V_{\text{in}} = 125 \text{ V}$) are summarized, as depicted in Fig. 3. As the number of semiconductors decreases, the amount of SDP_{ave} increases. Thus, nonregenerative structures with less semiconductors have a higher SDP_{ave} . Furthermore, for the switched-capacitor structures, the amount of SDP_{peak} directly depends on the resistance of capacitors charging paths. Changes in the charging paths resistance changes the peak current of the semiconductors. However, as (14) shows, it does not affect the capacitors charging loss. Consequently, the corresponding SDP_{peak} of the proposed SCMLI is better than the other topologies, whereas its SDP_{ave} is within the range of them.

IV. EXPERIMENTAL RESULTS

In this section, the design characteristics and experimental results of the proposed seven-level inverter under various conventional (static and transient) and regenerative load conditions are discussed. In order to verify the feasibility of the proposed topology and assess its performance, a laboratory prototype is

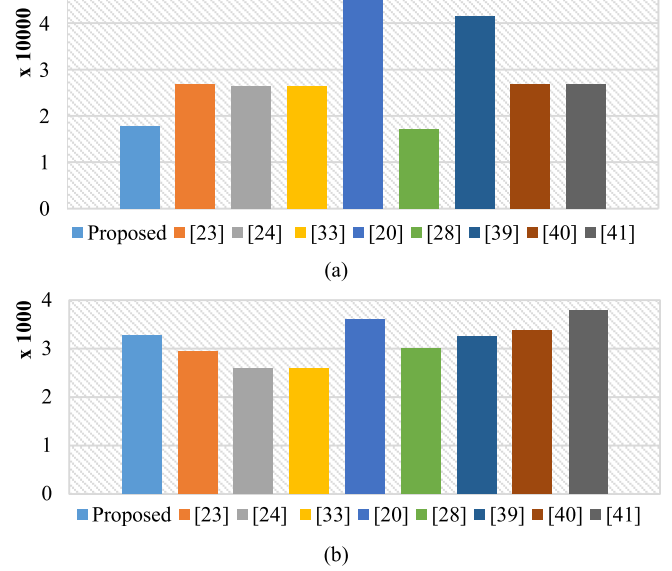


Fig. 4. Calculation results. (a) SDP peak. (b) SDP average.

TABLE IV
SPECIFICATIONS OF THE LAB PROTOTYPE PARAMETERS

Parameter/ Component	Value
Input Voltage	60V
Number of voltage levels	7
Maximum output voltage	180V
modulation index	0.9
Output Frequency	50Hz
PWM Frequency	3KHz
IGBT / Diode	12N60 / MUR860
Capacitors	C1=C2= 2200 μ F

implemented (see Fig 4). Furthermore, the specifications of this setup are brought in Table IV.

A TMS320F28335 DSP processor was used to create gate pulses based on the phase disposition technique. Then, these pulses were isolated and amplified by a circuit consisting of HCPL3120 isolator IC.

When the phase difference between load voltage and current is below 90° ($0 \leq \varphi < 90$), their polarity is the same for most of the cycle. Thus, the average power is supplied to the load and the overall performance of the inverter is considered to be inverting. Whenever the phase difference between load voltage and current is above 90° ($90 < \varphi < 180$), their polarity differs for most of the cycle. Hence, the inverter pumps average power from the ac to the dc side and the overall performance of the inverter is considered to be rectification (or regeneration) [22]. This feature is crucial in switched-capacitor structures to prevent the capacitors from overcharge, feeding the excess charge to the input source, instead.

A. Inverting Mode

Fig. 5(a) depicts the output voltage and current waveforms of the proposed converter for a pure resistive load of $R = 47.5 \Omega$ and the output frequency of 50 Hz. An input voltage of 60 V

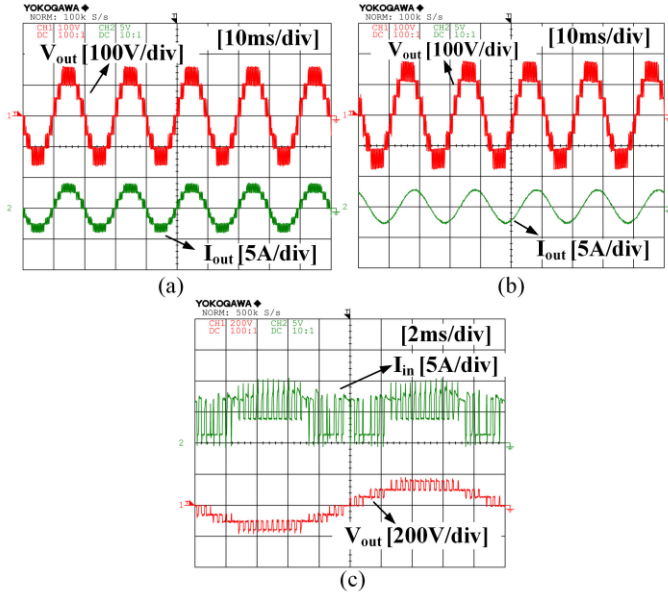


Fig. 5. Output voltage and current waveforms. (a) Pure resistive load of $R = 47.5 \Omega$. (b) Resistive-inductive load of $R = 47.5 \Omega$ and $L = 103 \text{ mH}$. (c) Input current of the inverter.

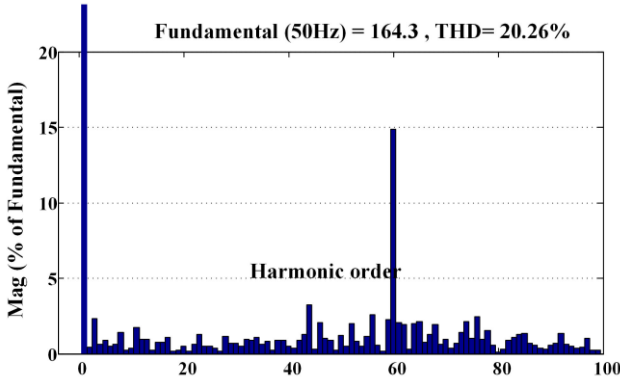


Fig. 6. Experimental harmonic spectrum of the output voltage.

was used to supply the converter, boosting it three times up to 180 V. The modulation index is set to $M = 0.9$. In the presence of a resistive-inductive load of $R = 47.5 \Omega$ and $L = 103 \text{ mH}$, the output waveform is illustrated in Fig. 5(b). The input current waveform of the inverter (I_{in}) can be seen in Fig. 5(c). Note that the input current increases while the circuit capacitors are being charged. In this case, the experimental harmonic spectrum of the output voltage is shown in Fig. 6. It can be seen that the amplitude of all unwanted harmonics are kept below 5% satisfying the IEEE-Std. 519-2014 (except for the 60th harmonic, which is due to the switching frequency). Also, the THD for the first 50 harmonic orders is 7.056%. Moreover, voltage and current waveforms of the inverter capacitors are presented in Fig. 7 for five continuous cycles. It can be seen that having about a 4 V ripple, the capacitors' voltages are well balanced. Additionally, for a pure inductive load of $L = 103 \text{ mH}$, Fig. 8(a) shows the inverter's output voltage and current. To investigate the performance of the proposed topology under nonlinear load

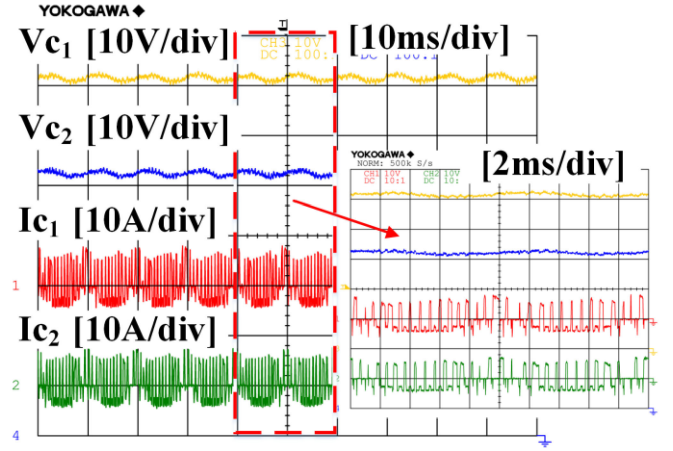


Fig. 7. Voltage and current waveforms of the inverter capacitors.

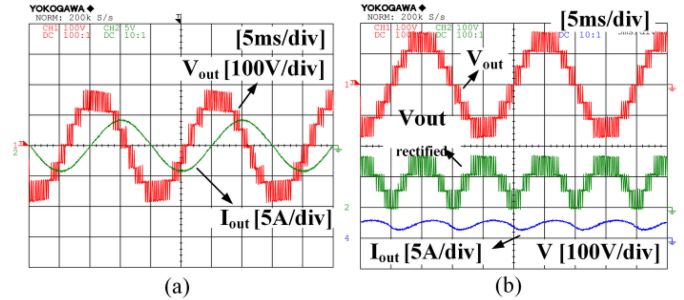


Fig. 8. Output voltage and current. (a) Pure inductive load ($L = 103 \text{ mH}$). (b) Output waveforms of the inverter after being rectified.

conditions, it was exposed to a single-phase rectifier with RL load. Fig. 8(b) shows the output voltage and current waveforms of the inverter after being rectified over a resistive-inductive load ($R = 47.5 \Omega$ and $L = 103 \text{ mH}$).

To test the proposed inverter in transient load conditions, different load transition cases have been studied. These tests suggest the proper performance of the inverter. Fig. 9(a) and (b) shows the effects of sudden load change from resistive ($R_1 = 95 \Omega$) to ($R_2 = R_1 || 95 \Omega$). The frequency of this periodic load transition is 1 Hz. Fig. 10 shows the collector-emitter voltage of two selected inverter switches (V_{s1} and V_{s5}). H-bridge switches (V_{s1}) have to withstand the output voltage but the rest of the switches only should bear the input voltage at most.

B. Regenerative Performance

In order to demonstrate the regenerative load performance of the proposed inverter, a test setup is devised as depicted in Fig. 11. The proposed inverter is connected to an H-bridge inverter via a line impedance (z) with the value of ($R = 2 \Omega$, $L = 107 \text{ mH}$).

Fig. 12 illustrates the experimental results under regenerative load condition. Fig. 12(a) presents the V_{load} and I_{load} , where they have a phase difference of more than 120° (lag). It also shows V_H , which has the same rms value as V_{load} with 15° leading the phase difference. Voltage ripple and current waveform of the capacitor C_1 is depicted in Fig. 12(b) under such conditions.

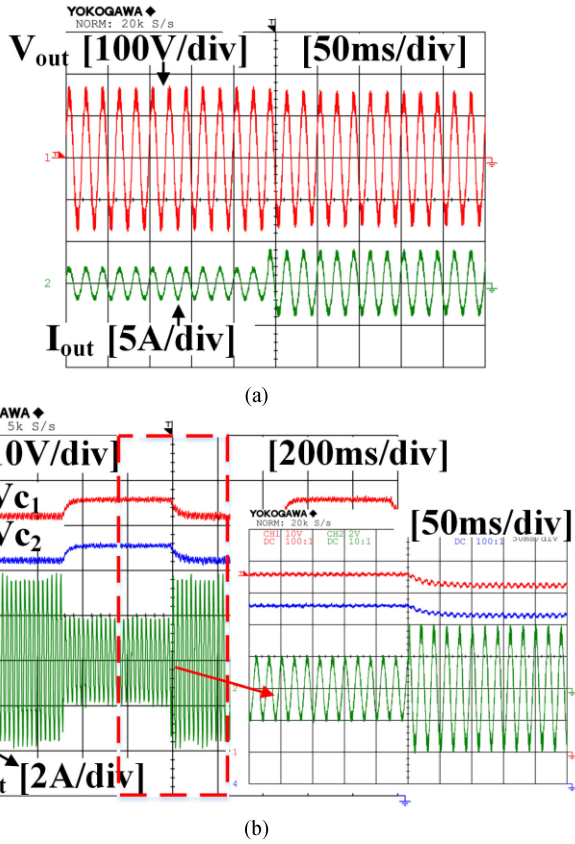


Fig. 9. Load waveforms under sudden change. (a) Output voltage and current. (b) Capacitors voltages and the load current.

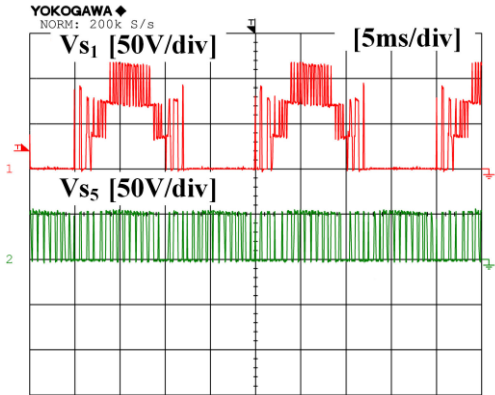


Fig. 10. Collector-emitter voltage across the switches S_1 and S_5 .

Note that, the capacitor C_1 is being charged from the output and is feeding the excess power back to the dc source, as depicted in Fig. 12(c), where I_{in} is negative for the most part. It goes exactly the same for the capacitor C_2 .

The experimental and theoretical efficiency of the proposed converter for different output powers is plotted in Fig. 13, which they reach 94.3% and 96.07% at peak, respectively. It can be seen that the efficiency of the converter is above 92% over a wide range of output power.

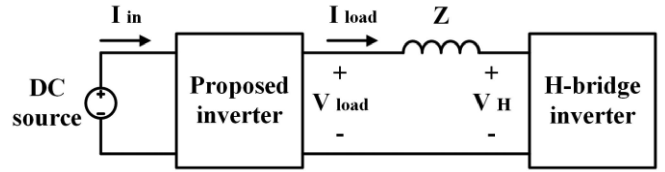


Fig. 11. Circuit diagram for regenerative performance test.

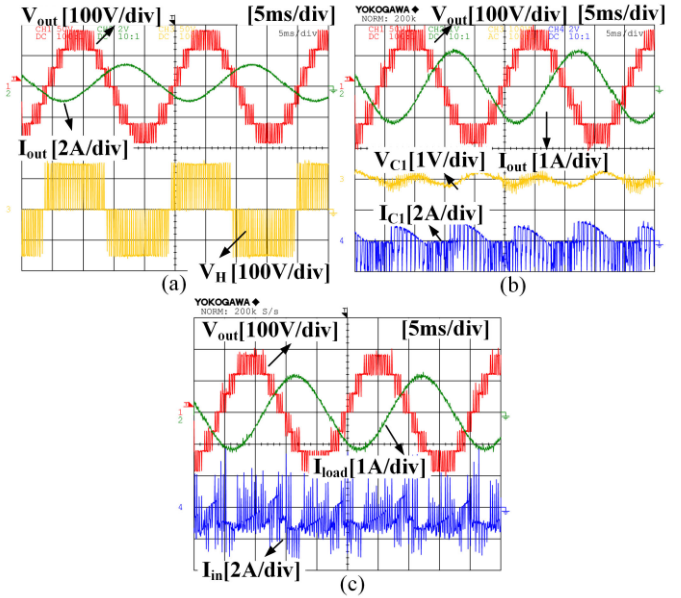


Fig. 12. Experimental results under regenerative load condition. (a) V_{load} , I_{load} , and V_H . (b) V_{C1} and I_{C1} . (c) I_{in} .

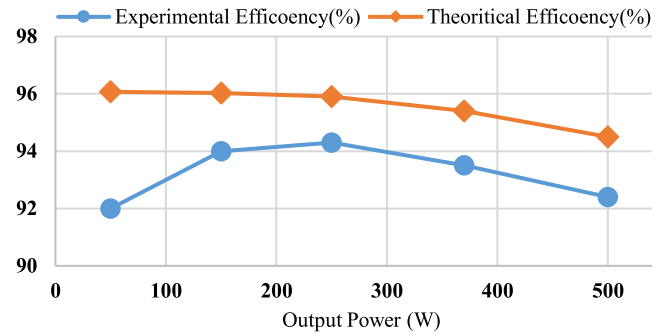


Fig. 13. Experimental and theoretical efficiency of the proposed converter for different output powers.

V. CONCLUSION

A new step-up single-source seven-level inverter topology aiming for circuit component reduction, including power and control circuit was introduced in this report. The proposed structure boosts the supply voltage based on the switched-capacitor concept by charging capacitors and combining them to generate the intended output. Applying the PD-PWM method led to not only an output with better quality but also lower stresses on circuit components. Self-voltage balancing and high efficiency were achieved by implementing the proposed concept under

different operating conditions. Experimental results prove that the structure performs appropriately under regenerative load condition by feeding the excess charge of the capacitors back to the input source. Moreover, a comparison to other recent topologies revealed that lower semiconductor counts and a simpler circuit were realized, considering the regenerative load feature, boost ratio, and TSV. Regarding the abovementioned pros, this circuit mostly suits for low-voltage renewable application.

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