Average Periodic Delay-Based Frequency Adaptable Repetitive Control With a Fixed Sampling Rate and Memory of Single-Phase PFC Converters

Seunghoon Baek, *Student Member, IEEE*, Younghoon Cho, *Member, IEEE*, and Jih-Sheng Lai, *Life Fellow, IEEE*

***Abstract*—This article proposes an average periodic delay-based repetitive controller for power factor correction (PFC) converters undergoing grid frequency variations. When the grid frequency is changed, a conventional repetitive controller requires an interpolation method or additional memory to achieve frequency adaptability. Furthermore, frequency adaptability can also be realized using a variable sampling frequency; however, this requires additional computation effort and a multirate digital control system. In this article, with a fixed sampling frequency and memory length, the proposed repetitive controller, which generates the average periodic delay unit, maintains its harmonic compensation performance under grid frequency variations. In the proposed method, the control variables are updated depending on the phase of the grid voltage to reflect the grid frequency deviations in the average period delay unit. Because no complicated software modification is necessary, the proposed scheme can be easily plugged in the existing control algorithm. The theoretical analysis and stability issues of the proposed scheme have been discussed in detail to ensure stable operation and disturbance rejection. Both the simulations and the experiments on a 1.5-kW PFC converter have been carried out to verify the effectiveness of the proposed repetitive control.**

***Index Terms*—Average periodic delay length, digital current control, frequency variations, harmonic distortion, power factor correction (PFC) converter, repetitive control.**

I. Introduction

VARIOUS power conversion systems have been widely used in grid-connected applications and distributed generation systems such as photovoltaic, wind power, and uninterruptible power supply (UPS) systems using dc–ac or ac–dc power converters [1]–[4]. In order to supply high quality electric power in such applications, well-designed controllers are essential, and numerous control strategies have been developed. Meanwhile, traditional linear control methods such as a proportional-integral (PI) and a proportional-resonant (PR) controller have been commonly adopted for commercial and industrial applications owing to their simplicity and ease of implementation [5]–[10]. However, in some cases, they cannot compensate for high order harmonic components because of their limited control bandwidth. Several control strategies, such as deadbeat predictive control [11]–[13] and hysteresis control method [14], [15], have been introduced to address this limitation. Although they can provide a fast response, the parameter sensitivity of deadbeat control in [11]–[13] and the variations of switching frequency for the hysteresis control in [14] and [15] are concerns.

On the other hand, repetitive controllers (RCs) have been popularly employed to compensate for the periodic tracking errors [16]–[21]. Based on the internal model principle, RCs can achieve nearly zero steady-state tracking error for high order harmonics. Accordingly, a conventional RC (CRC) is suitable for grid-connected applications where a periodic current or voltage error occurs. One significant limitation of CRCs, however, is that they cannot avoid a fractional delay (FD), which not only degrades the compensation performance of the CRC but also causes instability issues when the fundamental grid frequency f_g varies. To overcome this limitation caused by the FD, RCs should be able to adapt to varying grid frequencies. Regarding this issue, several studies have been conducted [22]–[37]. In [22]–[28], the repetitive control schemes with the variable sampling rate were proposed to deal with f_g variation. However, along with the adaptation for frequency change, the sampling rate should be continuously updated to ensure the fixed integer number of memory allocation. Variable sampling method can be realized through a multirate digital control system, but it is difficult to implement in a fixed sampling rate control system. Also, this method has a tradeoff between the disturbance rejection and overall system stability. In [29], a spatial repetitive controller using the phase sampling technique has been proposed. It can help in achieving dynamic change of the sampling frequency for RC, but it has the inherent problem of the variable sampling method as mentioned above. In [30]–[33], Lagrange-interpolation-based FD filter has been employed to enhance the frequency adaptability for the active power filters and the grid-connected inverters. Though it exhibits acceptable

Manuscript received December 15, 2019; revised May 18, 2020 and August 22, 2020; accepted October 20, 2020. Date of publication November 3, 2020; date of current version February 5, 2021. This work was supported by Konkuk University. Recommended for publication by Associate Editor G. Escobar. *(Corresponding author: Younghoon Cho.)*

Seunghoon Baek and Younghoon Cho are with the Electrical Engineering, Konkuk University, Gwangjin-gu, Seoul 05029, Republic of Korea (e-mail: honv@konkuk.ac.kr; yhcho98@konkuk.ac.kr).

Jih-Sheng Lai is with the Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, Virginia 24061-0111 USA (e-mail: laijs@vt.edu).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3035527

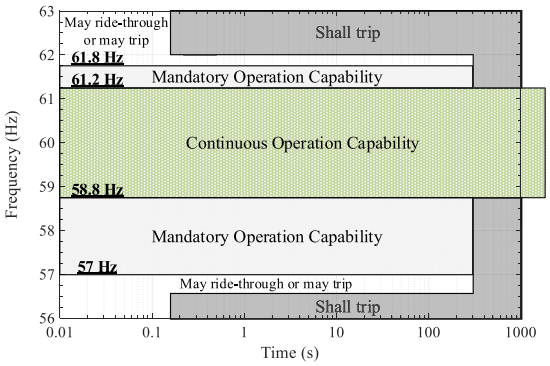

Fig. 1. Response to abnormal frequencies and frequency ride-through requirements in IEEE 1547-2018 [38].

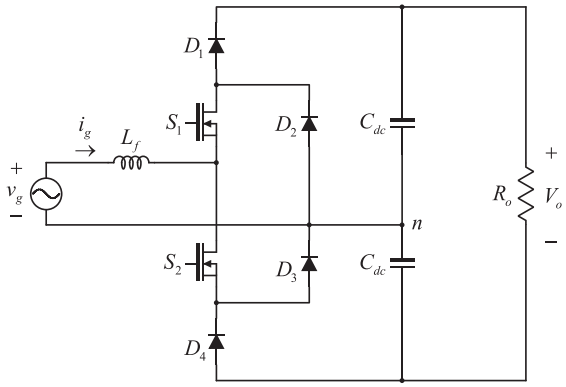

Fig. 2. Single-phase three-level PFC converter.

performance for frequency variations with a fixed sampling rate, the allowable frequency range is limited by the sampling rate and the number of memory blocks (e.g., 49.5–50.5 Hz, where 50 Hz is nominal grid frequency). Also, it needs 16 multiplications and 12 summations to calculate the interpolation coefficients in every cycle.

Recently, the RC proposed in [34] extends the frequency adaptive range using an improved FD filter design. However, it requires 50% more memory usage than the CRC, and this entails an additional computation effort for the 3rd order Lagrange interpolation coefficients, which should be updated every cycle. A bandwidth-based RC scheme was proposed in [35]. By enlarging the magnitude response near the control frequency, it could deal with the frequency deviation. However, it cannot be fully peaking the gain of the RC, so that normal regulation performance is not as good as CRCs. In [36] and [37], an angle-based RC was presented for torque ripple reduction in permanent magnet synchronous machines. Although it could mitigate the torque ripple in an extended frequency range with the fixed-sampling rate and memory length, a detailed description and analysis were not clearly stated.

Fig. 1 shows the IEEE 1547-2018 standard which specifies the abnormal frequencies and frequency ride-through requirements [38]. In Fig. 1, it is confirmed that the power converters' operation capability should be in the frequency range of 57–61.8 Hz, where 60 Hz is the nominal grid frequency. This indicates that in order to meet the grid standard requirements, an RC scheme that can be applied in spite of a wide range of frequency variation should be considered.

To this end, this article proposes an average periodic delay-based RC scheme with a fixed-sampling frequency and without additional memory usage for enhancing the frequency adaptability in a wide frequency range from 57 to 63 Hz. In accordance with the grid frequency of the phase-locked loop (PLL) output, the memory allocation (under the fixed sampling frequency) is updated, and an average periodic delay unit is generated for the proposed RC. In a way, it seems like the phase sampling technique suggested in [29] for the frequency adaptive capability; however, there is a big difference that the overall proposed RC scheme in this article operates at a fixed sampling frequency. Also, followed by [36] and [37], this article analyzes the operation principle of the frequency adaptive RC and the design procedure using the average periodic delay scheme. Based on this analysis, it is possible to use 50% less memory than the CRC methods. Compared to previous frequency adaptive RC methods, the proposed RC method can be not only implemented in the existing control platform of a fixed sampling rate but also realized with the reduced number of memory usage. This makes it possible to design an effective software architecture and cost-effective alternative.

The rest of this article is organized as follows. In Section II, the modeling of the single-phase three-level power factor correction (PFC) converter is performed, which is utilized to determine the control gain with the proposed method. Then the limitation of the CRC under a frequency variation is discussed. The proposed RC is presented to deal with the frequency deviations in Section III. The detailed design procedure and performance limitation of the proposed RC for stable operation is discussed. In Sections IV and V, both simulation and experimental results are provided including the comparison with the CRC to demonstrate the performance of the proposed RC. Finally, Section VI concludes this article.

II. Conventional Repetitive Controller for Grid-Connected PFC Converters

Fig. 2 shows the circuit diagram of a single-phase three-level PFC converter, which is used to regulate the dc-link voltage V_o across the load resistance R_o. In this study, the three-level PFC topology has been employed due to reduced switching losses and lower voltage ratings for the switching devices compared to a conventional two-level PFC converter [39], [40]. The converter comprises two active switches, S_1, S_2, four diodes D_1–D_4, and two dc-link capacitors whose capacitances are $C_{\rm dc}$. Here, S_1 and S_2 operate in a complementary manner. When S_2 is turned ON for a positive half cycle, the grid current i_g flows through the filter inductor L_f, S_2, and D_3. At this instant, the magnetic energy is stored in L_f. If S_2 is turned OFF in the positive half cycle, the stored energy in L_f is released via S_1 and D_1. A similar analysis can also be performed for the operation of the converter in a negative half cycle of the grid voltage v_g.

Fig. 3 depicts the control block diagram of the single-phase PFC converter, where $G_{\rm id}(s)$ is control-to-inductor current

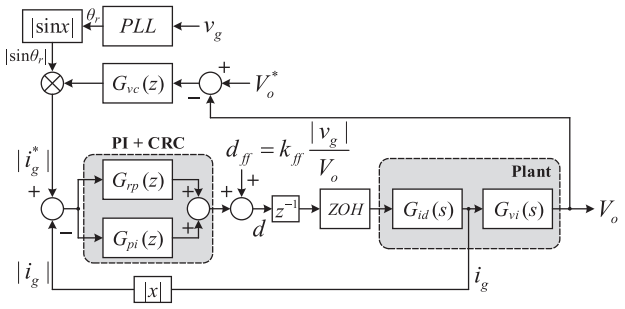

Fig. 3. Control block diagram of the single-phase PFC converter.

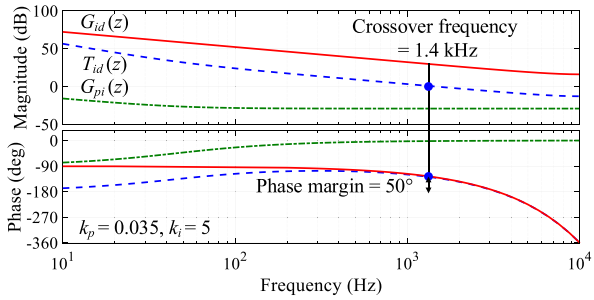

Fig. 4. Frequency responses of $G_{\mathrm{id}}(z)$, $T_{\mathrm{id}}(z)$, and $G_{\mathrm{pi}}(z)$.

model and $G_{\mathrm{vi}}(s)$ is inductor current to dc-link voltage transfer function. To regulate the dc-link voltage V_o, the outer PI voltage controller $G_{\mathrm{vc}}(z)$ generates the peak magnitude of the current reference $|i_g^*|$. Subsequently, the peak is multiplied by the rectified and normalized output of the PLL to achieve unity power factor. An all-pass filter (APF)-based single phase PLL algorithm [41] is used in this study. For the APF-based PLL, an optional low-pass filter is used to adapt the APF to frequency variations. To ensure accurate reference tracking as well as rejection of harmonic distortions, a feedback current controller is necessary. Here, both the PI $G_{\mathrm{pi}}(z)$ and the CRC $G_{\mathrm{rp}}(z)$ are employed as an example. Alternatively, $G_{\mathrm{pi}}(z)$ can also be replaced with other structure, e.g., a PR control scheme, but this may not alter the results of the analysis performed in this study. Also, a feedforward term d_{ff} with the gain k_{ff} is added to compensate the grid input admittance effect, so that the burden of feedback controllers can be significantly mitigated.

A. Modeling of the Power Stage

By assuming a large enough capacitance C_{dc}, the dc-link can be considered as voltage source. Then, the average control-to-inductor current model of the converter shown in Fig. 2 can be written as a first order form [21], [42] as follows:

$$G_{\mathrm{id}}(s) = \frac{V_{\mathrm{o}}/2}{sL_{\mathrm{f}}}. \tag{1}$$

Equation (1), which is also called as the high frequency approximation form, exactly models critical high frequency ranges, and simplifies the controller design. By using (1), the control-to-inductor current model in the z-domain can be derived as

$$G_{\mathrm{id}}(z) = \frac{T_s V_{\mathrm{o}}/2}{L_{\mathrm{f}}} \frac{1}{z\,(z-1)} \tag{2}$$

where T_{s} represents the sampling period. In (2), the zero-order hold transformation and z^{-1} are used to model the PWM update and the unit calculation delays [10], [43]–[45], respectively, as shown in Fig. 3.

B. Current Controller for the PFC Converter

The PI current controller is discretized using the backward Euler method as follows [45]:

$$G_{\mathrm{pi}}(z) = k_p + k_i T_s z/(z-1) \tag{3}$$

where k_p is the proportional gain and k_i is the integrator gains.

From Fig. 3, the open-loop gain of the current control system is given as

$$T_{\mathrm{id}}(z) = G_{\mathrm{pi}}(z) G_{\mathrm{id}}(z). \tag{4}$$

The design procedure of the PI controller is to determine the crossover frequency f_c and the phase margin ϕ_m of $T_{\mathrm{id}}(z)$. Considering the time delay caused by the digital calculation and the PWM update, the relationship between the maximum achievable f_c and ϕ_m is obtained as follows[6]:

$$f_{\mathrm{c}} = \frac{\pi/2 - \phi_{\mathrm{m}}}{2\pi \times 1.5 T_s}. \tag{5}$$

Here, ϕ_m is chosen as 50° for a fast and stable response, allowing for a slight overshoot. Then, f_c is obtained as 1.4 kHz by using (5). Once f_c and ϕ_m are determined, the control gains of the PI current controller can be easily calculated [6]. Fig. 4 represents the frequency response of the current control loop gain with the given phase margin and the crossover frequency.

For the CRC, the digital plug-in repetitive controller [21] is adopted. The CRC requires $N(= f_{\mathrm{s}}/2f_{\mathrm{g\_nom}})$ memory blocks where $f_{\mathrm{g\_nom}}$ is the nominal value of the grid frequency f_g. Here, the repetitive controller $G_{\mathrm{rp}}(z)$ is expressed as follows:

$$G_{\mathrm{rp}}(z) = k_{\mathrm{rp}} \frac{z^{-N+L}}{1 - z^{-N} q(z)}. \tag{6}$$

In (6), $q(z)$ is the stabilization filter of the RC method, and L represents the number of phase leading samples necessary to compensate the digital and propagation delays [21], [22]. Practically, considering the digital delay of $1.5T_{\mathrm{s}}$, L is chosen as 2. Also, a zero phase delay low-pass filter is employed for $q(z)$ as follows:

$$q(z) = 0.25z + 0.5 + 0.25z^{-1}. \tag{7}$$

C. Performance Degradation of CRC Under Frequency Variation

In [23]–[37], the drawbacks of the CRC were analyzed with regard to the frequency variations. According to the aforementioned studies, the gain of $G_{\mathrm{rp}}(z)$ decreases considerably as the grid frequency changes. Eventually, the CRC may no longer provide harmonic compensation due to the insufficient gains of $G_{\mathrm{rp}}(z)$ at abnormal critical frequencies. Besides, the CRC, which is not designed to address frequency variations,

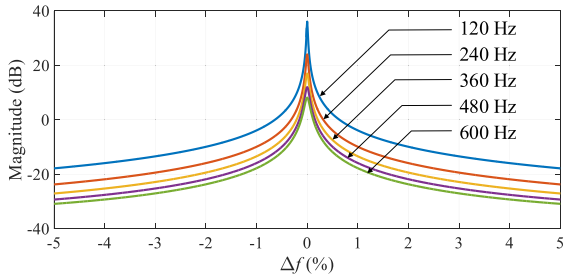

Fig. 5. Magnitude of $G_{\mathrm{rp}}(z)$ under grid frequency variation when $k_{\mathrm{rp}} = 0.024$.

TABLE I
SYSTEM PARAMETERS

Specification	Value
Output power (P_o)	1.5 kW
Filter inductance (L_f)	1.3 mH
Output capacitance (C_{dc})	2.4 mF
Grid voltage (v_g)	220 V_{rms}
Grid frequency (f_g)	57 ~ 63 Hz
DC-link voltage (V_o)	700 V
Switching frequency (f_{sw})	20 kHz
Sampling period (T_s)	50 μs

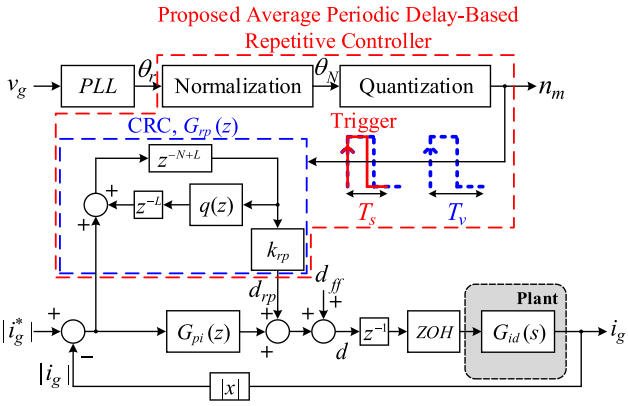

Fig. 6. Proposed repetitive current control block diagram of the single-phase PFC converter.

may cause a stability problem. Fig. 5 shows the magnitude response of $G_{\mathrm{rp}}(z)$ around the harmonic frequencies, where Δf is percentage of the nominal grid frequency. For the analysis, the system parameters which are listed in Table I and the gain of repetitive controller k_{rp} is 0.024. As shown in the figure, when 1% variation of the grid frequency occurs, the RC magnitude at first-order harmonic frequency (at 120 Hz) decreases from 38 to −3 dB.

III. PROPOSED AVERAGE PERIODIC DELAY-BASED REPETITIVE CONTROL

A. Operation Principle

To address the limitations of CRCs with regard to frequency adaptability, an average periodic delay-based RC is proposed as depicted in Fig. 6. The proposed method consists of three

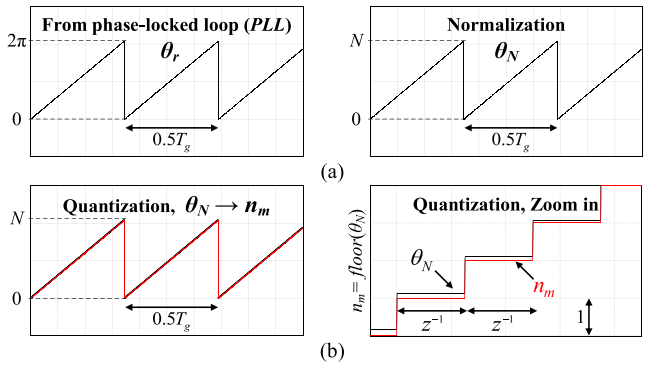

Fig. 7. Post-process for the memory update of the proposed repetitive control scheme. (a) Normalization. (b) Quantization.

parts: normalization, quantization, and the CRC. In the figure, T_{s} and T_v represent the fixed and variable intervals for iteration. A detailed discussion for T_{s} and T_v will be presented later in this section. Before starting the analysis of the proposed RC, two constraints are stated as follows by considering a practical aspect of the implementation in a digital controller.

Constraint 1: The iteration of the proposed RC is synchronized to the fixed sampling period T_{s} in a general digital controller, and T_{s} is also identical to the switching period. This means that the normal periodic interrupt or the corresponding timer structure of the microcontroller or field-programmable gate array should not be altered, and no variable frequency sampling is allowed.

Constraint 2: The performance of the proposed RC relies on the accuracy of the memory sampling instant. Even if there are sampling mismatches between ideal and practical sampling instants, the control loop including the proposed RC should be stable.

If f_{s} is properly selected for $f_{\mathrm{g\_nom}}$ without introducing the fractional order problem reported in [23]–[37], the number of the samples N in the proposed method is written as

$$N = \frac{f_s}{2f_{\mathrm{g\_nom}}} = \frac{1}{T_s \times 2f_{\mathrm{g\_nom}}} \tag{8}$$

where N is an integer number.

Assume that the PLL can extract the phase information accurately at the steady state regardless of the grid frequency. Then, the phase angle θ_{r} obtained from the PLL ranges between $0 \leq \theta_{\mathrm{r}} < 2\pi$ rad. The normalization process produces the normalized angle θ_N with respect to θ_{r} and N as

$$\theta_N = N\frac{\theta_r}{2\pi}. \tag{9}$$

In fact, N is also considered as the number of memory blocks in the algorithm. According to the aforementioned range definition of θ_N, the maximum value of θ_N is close to but less than N, as shown in Fig. 7(a). Subsequently, through the quantization process, the normalized and quantized index n_m is given as

$$n_{\mathrm{m}} = \mathrm{floor}\,(\theta_N) \tag{10}$$

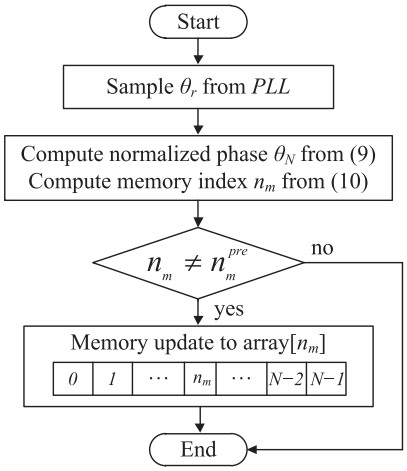

Fig. 8. Memory update flow of proposed RC scheme.

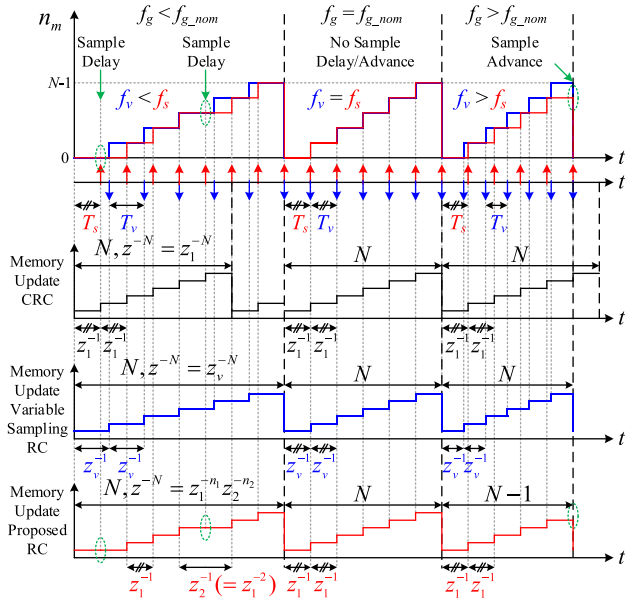

Fig. 9. Sample delay and advance in the memory update under f_g variation.

where floor(x) returns the nearest integer less than x as shown in Fig. 7(b). Equation (10) indicates that n_m can be a positive integer ranging from 0 to $N-1$. Using (9) to (10), the phase angle expressed in radian is easily converted to n_m with no unit. In the proposed RC, the memory update is synchronized to the changing moments of n_m and the iteration of the RC algorithm occurs whenever the change of the index n_m is detected. Here, T_v is defined as the update interval of n_m. If T_g denotes the inverse of f_g, n_m changes N times in $0.5T_g$ according to (9) and (10). Then, the relationship among T_v, N, and T_g can be written as follows:

$$0.5T_g = N \times T_v. \tag{11}$$

By substituting (8) into (11), T_v can be expressed as

$$T_v = T_s \times \frac{f_{\mathrm{g\_nom}}}{f_g}. \tag{12}$$

From (12), T_s and T_v are equal when f_g is the same as $f_{\mathrm{g\_mon}}$. In this case, the proposed RC operates in the same manner as the CRC. However, if f_g deviates from $f_{\mathrm{g\_nom}}$, T_s and T_v are no longer matched, and this may violate *Constraint 1*, because there could be a sampling mismatch which had been explained in *Constraint 2*. Fig. 8 shows the flow chart of the memory update for the proposed RC where the calculations and the memory update occur at every fixed sampling period T_s. Accordingly, the proposed RC is also susceptible to the fractional order problem, but the impact of this problem on the regulation performance of the proposed RC is relatively trivial compared to that in the CRC. This will be further elucidated in the following sections.

B. Sample Delay and Advance Phenomenon

To show this phenomenon, the proposed RC can be compared with the varying sampling RC [22]–[29]. Fig. 9 compares the memory update processes of the proposed RC and the RC that employs variable sampling, where the number of memory blocks is selected to satisfy $N(=f_\mathrm{s}/2f_{\mathrm{g\_nom}})$, $f_v\,(=2Nf_g)$ is the variable sampling frequency, and $T_v\,(=1/f_v)$ is the variable sampling period considering the variation in f_g.

1) Sample Delay ($f_v < f_s$): When f_g is below the nominal value, the variable sampling frequency f_v should be less than f_s to retain the entire number of memory blocks. Although the sampling operation of the proposed method should be ideally performed with f_v, the actual control action is synchronized with the fixed sampling frequency f_s, as discussed earlier. In this case, the sampling delay, where the memory update cannot be triggered by the n_m until the beginning of the next period T_s, occurs naturally. In other words, the periodic delay block and the memory update for the proposed RC comprise two types of unit delay $z_1{}^{-1}$ and $z_2{}^{-1}$ ($\equiv z_1{}^{-2}$).

Here, the number of memory blocks N can be selected to limit the delay element to $2T_\mathrm{s}$ as follows:

$$0.5f_s \leq 2Nf_{\mathrm{g\_min}} \tag{13}$$

where $f_{\mathrm{g\_min}}$ is the allowable minimum frequency.

2) No Sample Delay and Advance ($f_v = f_s$): When f_g is equal to the nominal frequency, f_v is the same as f_s. In this case, the operation of the proposed RC is identical to that of the CRC. Under this condition, the periodic delay unit (z^{-N}) for the RC consists of only the multiples of the single unit delay $z_1{}^{-1}$. This means that the proposed RC can be operated without being affected by the fractional order problem. As shown in Fig. 9, the memory update of the RC is the same for both the proposed RC and the variable sampling RC, which is an ideal case for RCs.

3) Sample Advance ($f_v > f_s$): When f_g becomes higher than the nominal value, the variable sampling frequency f_v should be larger than f_s. Similarly, it has the occurrence of sample advance due to discrepancy between f_v and f_s. As shown in Fig. 9, a partial sampling loss is observed in the triggering process (unit delay, $z_1{}^{-1}$).

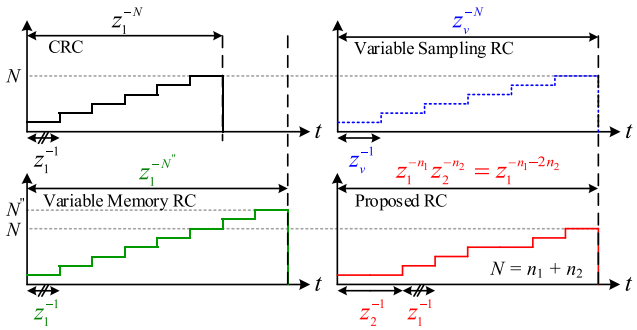

Fig. 10. Memory update comparison of different RC methods.

To avoid the partial memory loss due to the sample advance effect, the number of the memory blocks N should be limited as follows:

$$2Nf_{\mathrm{g\_max}} \le f_s \tag{14}$$

where $f_{\mathrm{g\_max}}$ represents the maximum allowable grid frequency. By considering the sample delay, the $G_{\mathrm{rp}}(z)$ of the proposed RC can be expressed as follows:

$$G_{\mathrm{rp}}(z_{1,2}) = k_{\mathrm{rp}} \frac{z_1^{-n_1} z_2^{-n_2} z_{1,2}^{L}}{1 - z_1^{-n_1} z_2^{-n_2} q(z_{1,2})} = k_{\mathrm{rp}} \frac{z_1^{-n_1-2n_2} z_{1,2}^{L}}{1 - z_1^{-n_1-2n_2} q(z_{1,2})}$$
$$z_{1,2} = \begin{cases} z = z_1 = e^{j\omega T_s}, & \text{without the sample delay} \\ z_2 = e^{j2\omega T_s}, & \text{with the sample delay} \end{cases} \tag{15}$$

where n_1 and n_2 are the number of memory blocks corresponding to $z_1{}^{-1}$ and $z_2{}^{-1}$, respectively.

For the number of memory blocks of the proposed RC which consists of n_1 and n_2 can be expressed as follows:

$$n_1 + n_2 = N. \tag{16}$$

According to the operation characteristics of the proposed RC with the sample delay as in Fig 9, the period that is equal to twice the fundamental frequency can be expressed as follows:

$$n_1 \cdot T_s + n_2 \cdot 2T_s = 1/(2f_g) \tag{17}$$

which can be generalized as follows:

$$n_1 + 2n_2 = \mathrm{floor}\left(\frac{f_s}{2f_g}\right). \tag{18}$$

Compared with the periodic delay block z^{-N} of the CRC, the proposed RC generates the average periodic signal for the grid frequency variation along with the unit delay blocks from $z_1{}^{-n1}$ and $z_2{}^{-n2}$ in the triggering process as follows:

$$z^{-N} = z_1^{-n_1} z_2^{-n_2} = z_1^{-(n_1+2n_2)}. \tag{19}$$

In other words, the memory sampling, which works in accordance with the grid frequency, is allocated to z^{-1} and z^{-2} owing to its sampling characteristics; this provides the average periodic delay unit of the fundamental frequency. Fig. 10 compares the memory update schemes of the different RC methods. Although the CRC cannot maintain the periodic delay length, variable sampling or memory RC methods ensure the periodic delay unit under an abnormal grid frequency. In the case of the proposed RC, it also keeps the periodic delay by combining two delay components, $z_1{}^{-1}$ and $z_2{}^{-1}$.

TABLE II
NUMBER OF MEMORY BLOCKS WITH DIFFERENT GRID FREQUENCIES

f_g	57 Hz	60 Hz	63 Hz
N'' (Variable memory RC)	175	166	158
N (Proposed RC)	158(=$N = n_1+n_2$), for f_{g_max}		
	$n_1+2n_2 = 175$ $n_1 = 141$ $n_2 = 17$	$n_1+2n_2 = 166$ $n_1 = 150$ $n_2 = 8$	$n_1+2n_2 = 158$ $n_1 = 158$ $n_2 = 0$
	88(=$N = n_1+n_2$), for f_{g_min}		
	$n_1+2n_2 = 175$ $n_1 = 1$ $n_2 = 87$	$n_1+2n_2 = 166$ $n_1 = 10$ $n_2 = 78$	$n_1+2n_2 = 158$ $n_1 = 18$ $n_2 = 70$

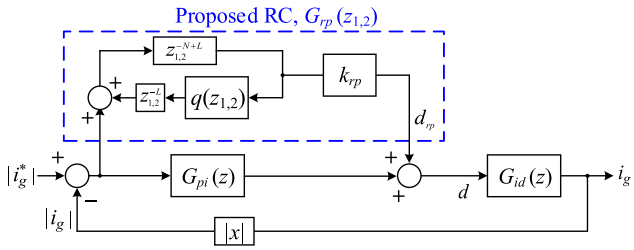

Fig. 11. Equivalent block diagram of proposed repetitive current controller.

Furthermore, the different number of memory blocks can be chosen for the proposed RC according to $f_{\mathrm{g\_min}}$ or $f_{\mathrm{g\_max}}$. By considering $f_{\mathrm{g\_max}}$ as 63 Hz, the number of samples N is obtained as 158 from (14). Next, the allowable minimum frequency is determined by (13) as 31.6 Hz. On the other hand, by considering $f_{\mathrm{g\_min}}$ as 57 Hz, N is chosen as 88 to satisfy (13) and the allowable frequency range is determined to be from 57 to 113.6 Hz using (14). Here, although it is efficient to use fewer memory blocks for the proposed RC, both values are considered to validate the proposed scheme in this article.

Table II compares the numbers of memory blocks n_1 and n_2 for various RC structures and different grid frequencies, 57, 60, and 63 Hz. For a variable memory RC, the maximum number of memory blocks is obtained as 175 to cover at 57 Hz. However, based on (13) to (18), the proposed RC only requires 88 or 158 memory blocks to function in the range of 57 to 63 Hz. It is also interesting that the proposed RC eventually exhibits the same periodic delay length as that of the variable sampling memory RC.

C. Stability Analysis of the Proposed Method

Fig. 11 shows an equivalent block diagram of the proposed repetitive current controller. As discussed above, the sampling delay is an inevitable element in constructing the periodic delay unit in the proposed RC, but it may affect the system stability. To examine the stability of the entire control system for the proposed method, the transfer function of the input current

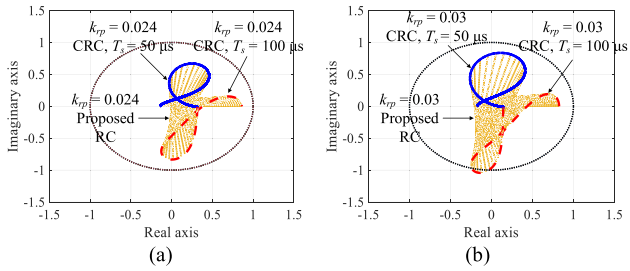

Fig. 12. The roots trajectories comparison of $H(z)$ for the CRC and the proposed RC. (a) $k_{\rm rp} = 0.024$. (b) $k_{\rm rp} = 0.03$.

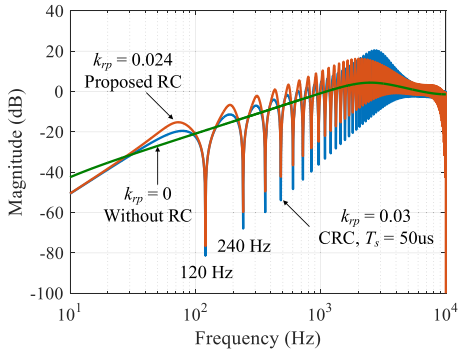

Fig. 13. Frequency response of $G_{\rm e}(z)$ for different control schemes.

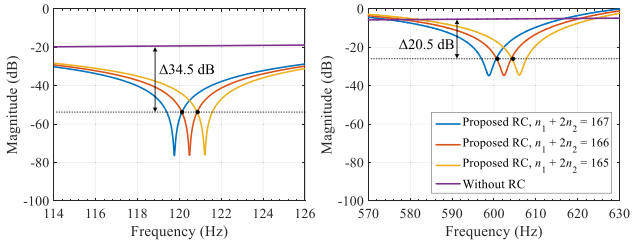

Fig. 14. Frequency response of $G_{\rm e}(z)$ for the proposed RC under f_g variation.

reference i_g^* to the current error $i_{\rm err}$ is written as follows:

$$G_{\rm e}(z) = \frac{i_{\rm err}(z)}{i_g^*(z)} = \frac{1}{1+T_{\rm id}(z)} \times \frac{1}{1+\frac{G_{\rm rp}(z_{1,2})G_{\rm id}(z)}{1+T_{\rm id}(z)}}$$
$$= \frac{1}{1+T_{\rm id}(z)} \times \frac{z_1^{n_1} z_2^{n_2} - q(z_{1,2})}{z_1^{n_1} z_2^{n_2} - H(z_{1,2})} \tag{20}$$

where $H(z_{1,2})$ is defined as

$$H(z_{1,2}) \equiv q(z_{1,2}) - k_{\rm rp} z_{1,2}^{L} \frac{G_{\rm id}(z)}{1+G_{\rm pi}(z)G_{\rm id}(z)}. \tag{21}$$

If all the poles of $G_{\rm e}(z)$ are located inside the z-plane unit circle, $G_{\rm e}(z)$ will not be divergent; thus, the overall system stability can be guaranteed. In (20), the denominator of the first term on the right-hand side is $1 + T_{\rm id}(z)$, and this is exactly the same as that of the closed-loop transfer function where only the PI current controller is adopted. If the all roots of $1 + T_{\rm id}(z)$ are placed in the unit circle, the stability is only affected by the eigenvalues of the remaining part $H(z_{1,2})$. Hence, $H(z_{1,2})$ should satisfy the condition below [21], [22]

$$|H(z_{1,2})| < 1. \tag{22}$$

Since $q(z)$, L, $G_{\rm id}(z)$, and $T_{\rm id}(z)$ are already determined, $k_{\rm rp}$ is the only design factor of $H(z)$ that is needed to satisfy (22) as well as to ensure control performance.

Equation (22) indicates that the sampling period of $H(z_{1,2})$ for the proposed RC alternates between $T_{\rm s}$ and $2T_{\rm s}$ in every sample delay occurrence of $G_{\rm rp}(z_{1,2})$. It should be noticed that the worst sample delay case is $2T_{\rm s}$. Consequently, the roots of $H(z_{1,2})$ are scattered for the different sampling periods, which is not observed in the CRC method. Fig. 12(a) and (b) compares the root trajectories of $H(z_{1,2})$, where the CRC and the proposed RC scheme with different $k_{\rm rp}$, respectively. Clearly, the roots trajectories of the proposed RC are travelled between the roots of the CRC with different sampling period $T_{\rm s}$ and $2T_{\rm s}$. Although scattered roots appear on $H(z_{1,2})$, a stable RC operation can be achieved using $k_{\rm rp} = 0.024$ because the trajectories converge into the unit circle as in Fig. 12(a). Furthermore, it is confirmed that the proposed RC becomes unstable even if $k_{\rm rp}$ is chosen as 0.03, which is the $k_{\rm rp}$ for stable operation of the CRC, as in Fig. 12(b). Thus, the gain $k_{\rm rp}$ of the proposed RC should be smaller than that of the CRC to ensure system stability.

Fig. 13 compares the frequency responses of $G_{\rm e}(z)$ for different control schemes. The RC methods can reduce the periodic current error in comparison with where $k_{\rm rp}$ is zero. In contrast with the CRC frequency response of $G_{\rm e}(z)$, different magnitude gains of the proposed RC are observed in the high frequency regions. It is worth noting that the operating point of the low-pass filter $q(z)$ is changed due to the sample delay of the proposed RC. However, it is not a problem in practical implementation because the bandwidth of the closed-loop system is lower than these high frequency regions, and the magnitude is sufficiently damped by selecting the proper $k_{\rm rp}$.

D. Performance Limitation of the Proposed Method

Although the proposed RC can generate the average periodic delay under frequency variations, it has an inherent limitation: it cannot compensate for the FD, z^{-F} $(0 < F < 1)$. If $f_{\rm s}/(2f_g)$ is not an integer value, an accurate periodic delay is $z^{-(N+F)}$, where N is an integer value. This degrades the error rejection capability of the proposed RC, which has a resolution of the unit delay (z^{-1}) for generating the periodic delay unit.

Fig. 14 shows the magnitude of $G_{\rm e}(z)$ for the proposed RC considering the average periodic delay unit. Due to the FD problem, it cannot always maintain the best performance of the harmonic compensation in accordance with the frequency change (e.g., f_g changes between 59.88 and 60.25 Hz, where the average periodic delay length $z_1^{-n1-2n2}$ is from z^{-167} to z^{-166}). Meanwhile, it is clear that the proposed RC provides a better compensation performance compared to the PI controller.

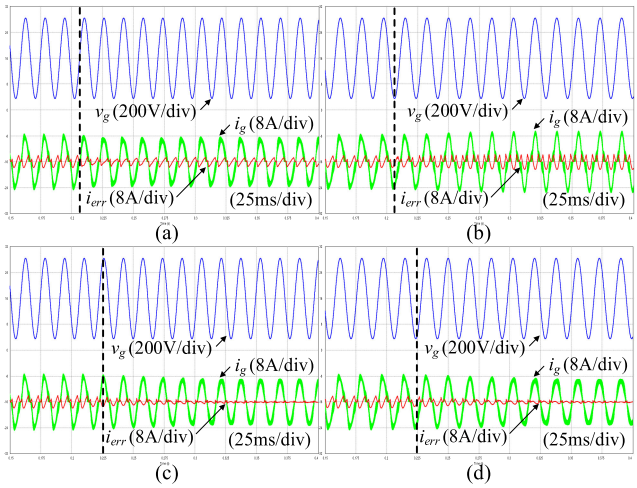

Fig. 15. Simulation results of the CRC and the proposed RC under different f_g at 1 kW load condition. (a) 63 Hz with the CRC. (b) 57 Hz with the CRC. (c) 63 Hz with the proposed RC. (d) 57 Hz with the proposed RC.

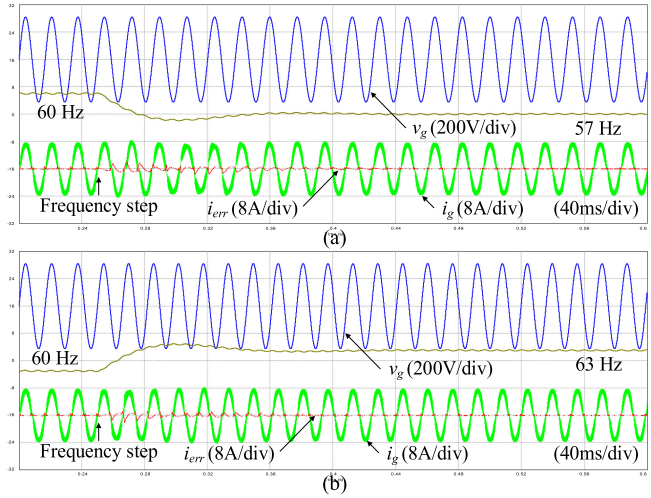

Fig. 16. Simulation results of transient response with the proposed RC under 1 kW load. (a) Grid frequency step change from 60 to 57 Hz. (b) Grid frequency step change from 60 to 63 Hz.

If the compensation gain of the proposed RC is enough to attenuate the current harmonic distortions, it can be an acceptable solution as a frequency adaptable RC method.

IV. Simulation Study

To demonstrate the feasibility and effectiveness of the proposed method, simulations have been conducted using the PSIM software. The proposed RC, which does not involve additional memory usage and computational load, is compared with the CRC. The simulation parameters are the same as listed in Tables I and II.

Fig. 15 compares the simulation results of the CRC and the proposed RC under an abnormal f_g and 1 kW load condition. In Fig. 15(a) and (b), the CRC method is applied at $t = 60$ ms. It is observed that the compensation performance of the CRC is degraded at abnormal frequencies. The current error $i_{\rm err}$ is even amplified at 57 Hz in the case of the CRC as in Fig. 15(b). In contrast, when the proposed RC is applied at $t = 75$ ms, $i_{\rm err}$ achieves the steady-state tracking error that is almost zero as in Fig. 15(c) and (d).

Fig. 16(a) and (b) shows the simulation results with the proposed method under the frequency jump conditions. In Fig. 16(a), f_g is changed from 60 to 57 Hz at $t = 50$ ms. Here, the PLL tracks f_g variation in six electrical cycles. Once f_g is fully detected after $t = 160$ ms, $i_{\rm err}$ is compensated within the subsequent six cycles, similar to the operation of the RC at 60 Hz. Similarly, when f_g jump occurs from 60 to 63 Hz, the proposed RC demonstrates the current tracking performance as in Fig. 16(b).

Fig. 17 compares the input current total harmonic distortion (THD) at different f_g values along with the current control methods. Compared to the proposed RC, the CRC shows higher THD of i_g for entire frequency range, except at 60 Hz. When f_g is less than 58 Hz, the CRC even shows worse performance than the PI controller only. Unlike the CRC, the proposed RC maintains

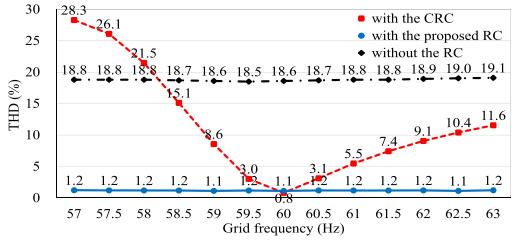

Fig. 17. Grid input current THD at different grid frequencies, where the output power is 1 kW.

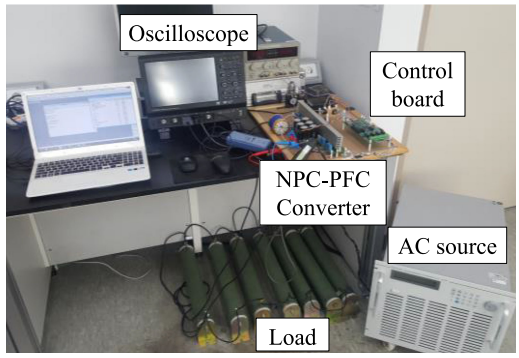

Fig. 18. Photograph of the experimental setup.

almost consistent THD of less than 1.2% for i_g, regardless of f_g. At 60 Hz, the proposed RC shows slightly higher THD than the CRC, and this is due to the previously discussed limitation of the proposed RC with regard to the selection of the control gain $k_{\rm rp}$. Among the three control structures, the only proposed RC satisfies the grid standard, where the THD of i_g is less than 5%, for the entire frequency range.

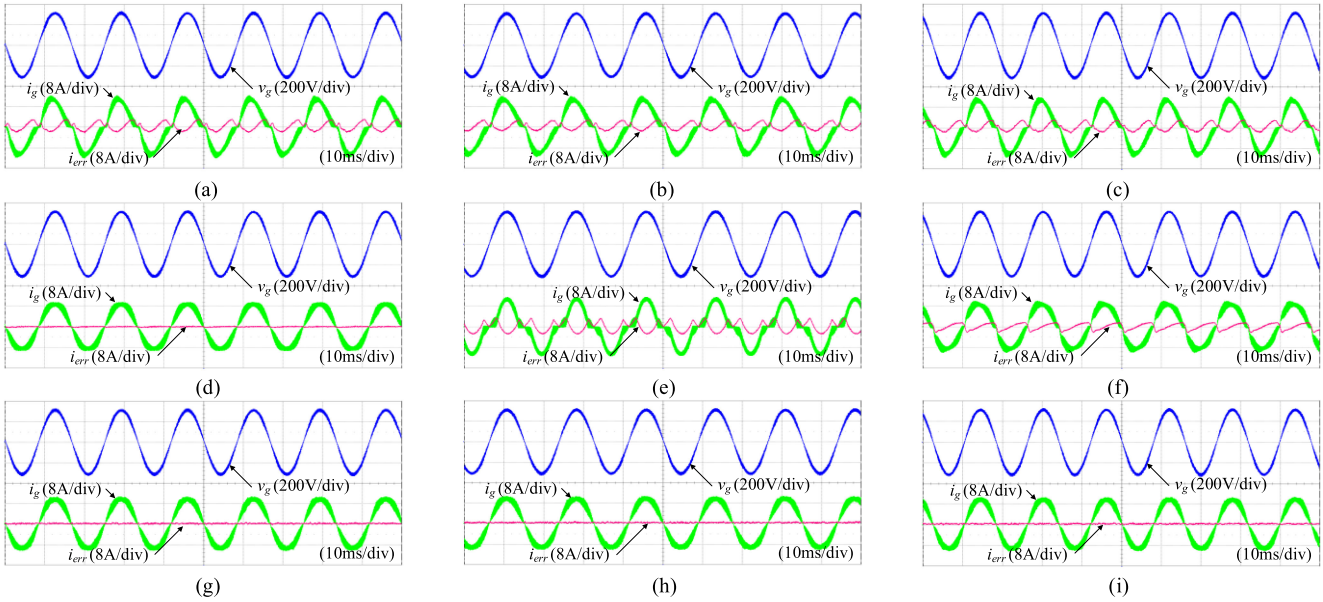

Fig. 19. Comparison of the grid input current waveform with and without the RCs current controller under different f_g at 1.5 kW condition. (a)–(c) Without the RC. (d)–(f) With CRC. (g)–(i) With the proposed RC. (a), (d), and (g) 60 Hz. (b), (e), and (h) 57 Hz. (c), (f), and (i) 63 Hz.

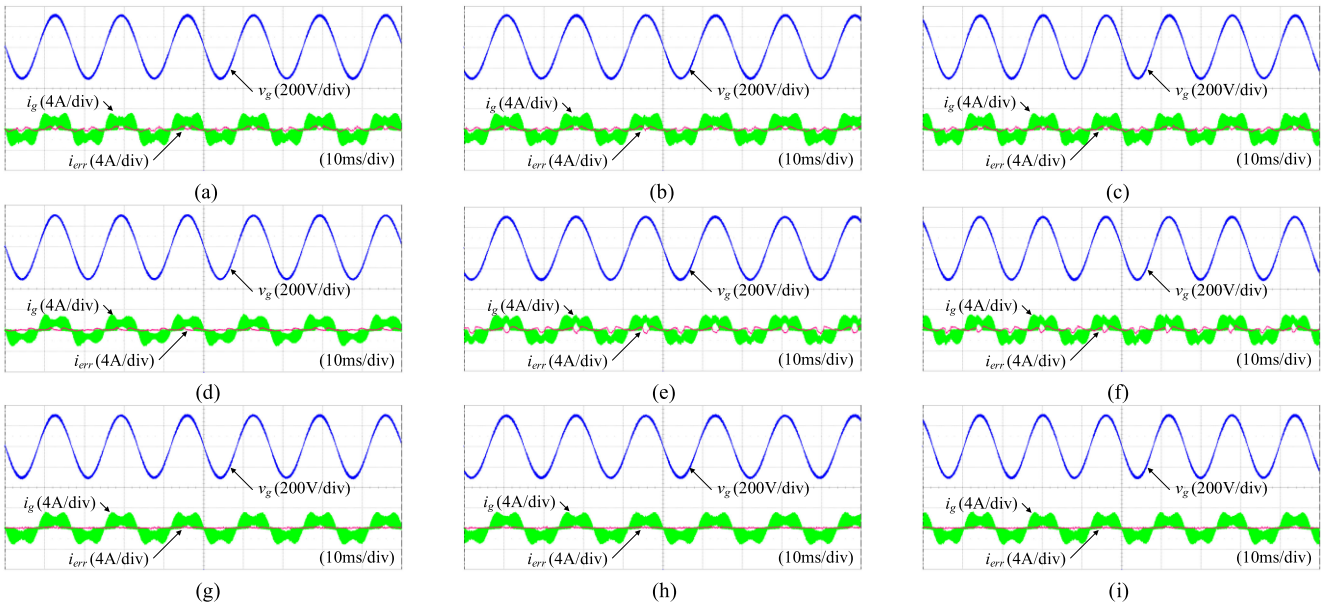

Fig. 20. Comparison of the grid input current waveform with and without the RCs current controller under different f_g at 0.25 kW condition. (a)–(c) Without the RC. (d)–(f) With CRC. (g)–(i) With the proposed RC. (a), (d), and (g) 60 Hz. (b), (e), and (h) 57 Hz. (c), (f), and (i) 63 Hz.

V. Experimental Results

To validate the proposed RC, experiments have been conducted on a single-phase 1.5 kW three-level PFC converter designed for a UPS system. Experimental setup is shown in Fig. 18.

All the digital controllers are implemented in TMS320F28335 DSP. A programmable ac power source (Chroma, 61704) is utilized to generate f_g variations within ± 3 Hz.

A. Steady-State Performance

Fig. 19 compares the grid voltage v_g, grid current i_g, and current error $i_{\rm err}$ under various f_g values at 1.5 kW operation. Even at the rated power, where the proposed method is not adopted, the grid current is still severely distorted with only the PI controller as shown in Fig. 19(a)–(c). For the CRC method, it can compensate for the grid current distortion at 60 Hz as shown in Fig. 19(d). Even if the CRC is utilized in Fig. 19(e) and (f), the

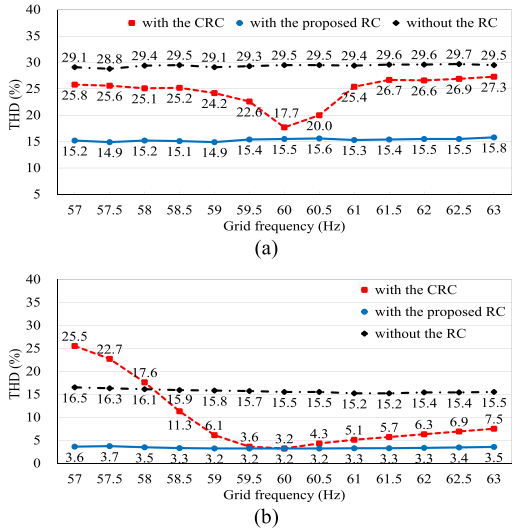

Fig. 21. Grid input current THD at different grid frequency. (a) Output power is 0.25 kW. (b) Output power is 1.5 kW.

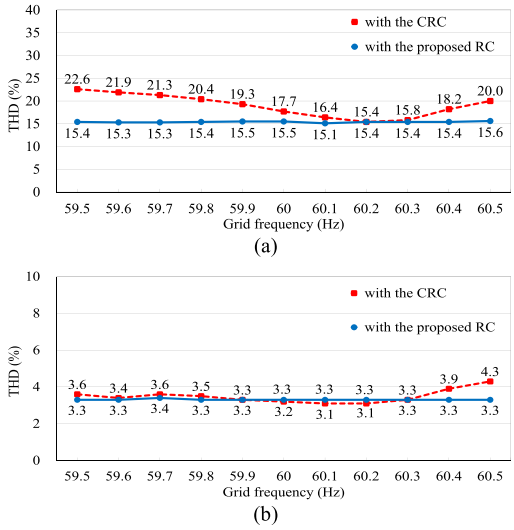

Fig. 22. Grid input current THD from 59.5 to 60.5 Hz. (a) Output power is 0.25 kW. (b) Output power is 1.5 kW.

grid current is still distorted under abnormal grid frequencies. This is because the CRC cannot provide a sufficient gain at frequencies other than 60 Hz, which is the target fundamental frequency of the CRC. In contrast, with the proposed RC, i_g keeps the sinusoidal shape, and thus the current error achieves considerably low amplitude irrespective of the grid frequency variation as shown in Fig. 19(g)– (i). Similarly, when the output load is 250 W, it is confirmed that the proposed RC provides a lower current error than the other methods regardless of f_g variations as in Fig. 20.

The measurement results of the THD for i_g at f_g values ranging from 57 to 63 Hz are summarized in Fig. 21, where the output power is 0.25 kW and 1.5 kW, respectively. With regard to only the PI controller and the plug-in CRC, the THD of i_g, with frequency deviations, exceeds the grid standard limitation (THD $< 5\%$). However, in the case of the proposed RC, it shows that the THD of i_g consistently complies with the grid standard regardless of the variations of f_g. Fig. 22 shows the measurement results of the THD for i_g at a relatively narrow f_g variation range. Here, it is confirmed that the CRC exhibits a relatively low grid current THD at 60.2 Hz. This is because the periodic delay length of the CRC is z^{-166}, which is equal to 60.2 Hz without FD. Although the proposed RC cannot achieve a grid current THD as much as the CRC at 60.2Hz due to the limitation of the control gain selection of the proposed RC, it maintains almost consistent and proper attenuation, even at the narrow f_g variation ranges.

Fig. 23 shows the experimental result of the single-phase PFC converter which operates over a range of input voltage. (typically, $+10\%$ to -15% of the nominal grid voltage for UPS system). Under the different input voltage, the proposed RC compensates for the harmonic distortion.

B. Transient Performance

Fig. 24 shows the transient response of the RC methods when f_g suddenly changes from 60 to 63 Hz and from 60 to 57

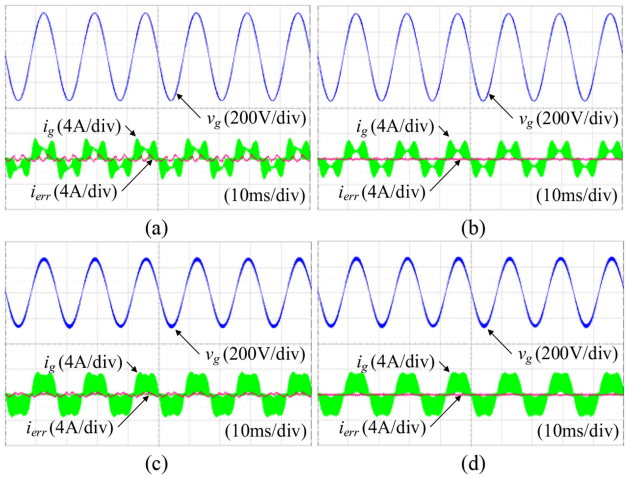

Fig. 23. Experimental results of different grid voltage under 0.25 kW. (a) and (b) $v_g = 242$ V. (c) and (d) $v_g = 187$ V. (a) and (c) Without the RC. (b) and (d) With the proposed RC.

Hz. In Fig. 24(a) and (b), the grid current error of the CRC increases under abnormal frequencies because the CRC has a periodic delay unit fixed at approximately 60 Hz. Fig. 24(c) and (d) indicates that the proposed RC operates without reliability issues under a sudden change in f_g. It takes 50 ms (three fundamental cycles) to compensate for the current error as soon as the PLL detects the change in f_g (the settling time is approximately 175 ms). Here, using a faster PLL method (e.g., a frequency-locked loop technique), it can improve the overall response time to deal with the sudden frequency variations by shortening the detection time of the frequency estimator [46]. However, it shows sufficient performance to demonstrate the frequency adaptability, considering the electric power system and generator inertia where the rate of frequency change is typically 1 Hz/s.

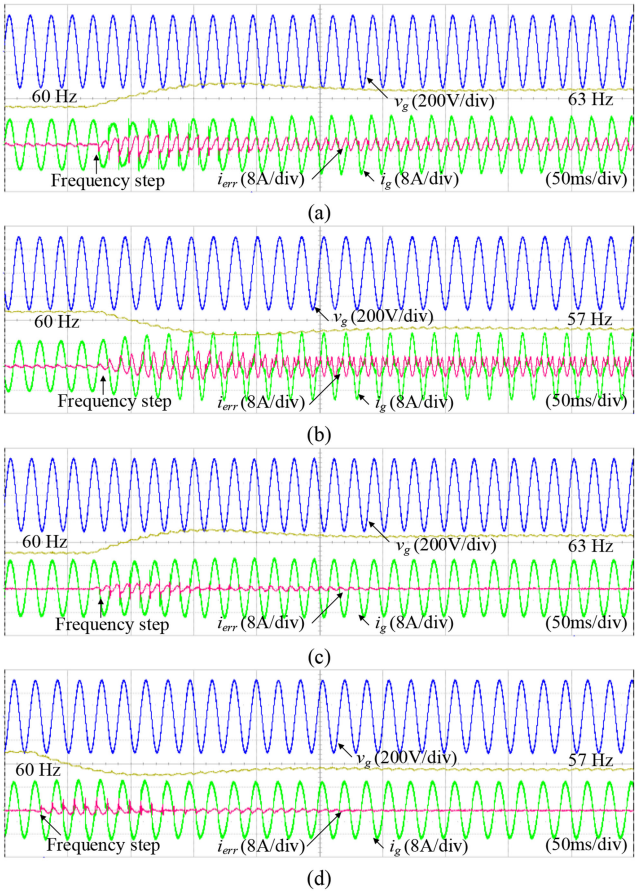

Fig. 24. Experimental results of the RCs under 1.5 kW. (a) and (b) CRC. (c) and (d) Proposed RC. (a) and (c) f_g step change from 60 to 63 Hz. (b) and (d) f_g step change from 60 to 57 Hz.

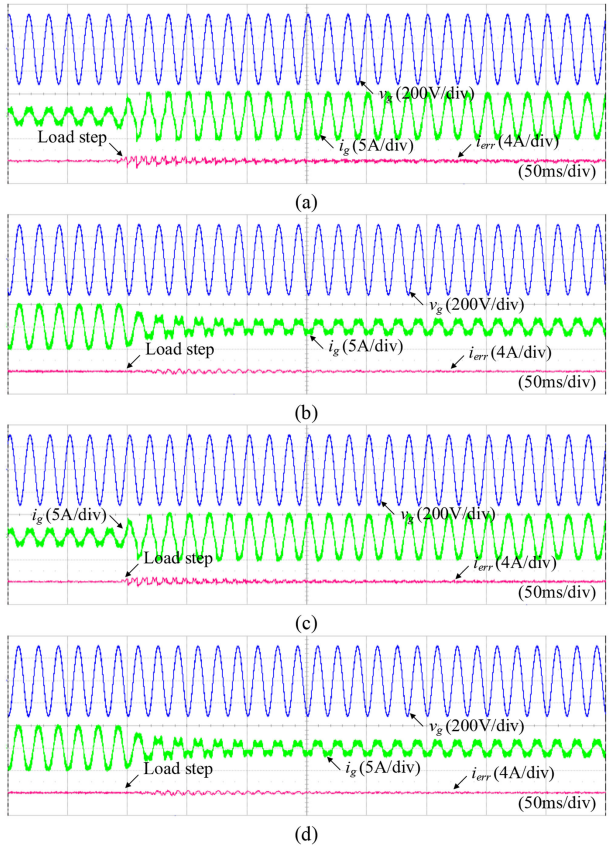

Fig. 25. Experimental results of transient response under 60 Hz grid frequency. (a) and (c) Load step from 250 to 750 W. (b) and (d) Load step from 750 to 250 W. (a) and (b) CRC. (c) and (d) Proposed RC.

The transient response of the step load change is also tested as shown in Fig. 25, where the load is changed from 750 to 250 W and from 250 to 750 W in steps, under a grid frequency of 60 Hz. In both cases, the proposed RC operates properly and there are no significant overcurrent issues. Then, the current error is again quickly reduced within several cycles.

C. Comparison of Proposed RC and Variable Sampling RC With Reduced Memory Block

As discussed in Section III, the number of memory block in the proposed RC can also be chosen as 88 considering the frequency range of 57–113 Hz. Additionally, a variable sampling RC method in [22]–[24] is adopted as a frequency adaptive current controller. For comparison, the proposed RC and the variable sampling RC with $N = 88$ and the identical gain are tested, and the experimental results are shown in Figs. 26 and 27. Without varying the sampling frequency or memory, the proposed RC offers a steady-state and transient performance as much as the variable sampling RC.

Fig. 28(a) and (b) shows the THD measurement results for the grid current at different output loads where f_g ranges from 57 to 63 Hz and from 59 to 60.5 Hz, respectively. The proposed RC with $N = 88$ keeps a satisfactory performance with regard to

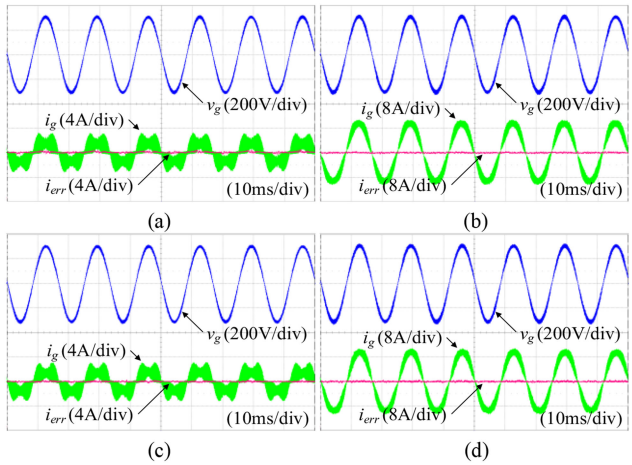

Fig. 26. Experimental results of steady-state response under 60 Hz grid frequency. (a) Proposed RC with $N = 88$ at 250 W. (b) Proposed RC with $N = 88$ at 1.5 kW. (c) Variable sampling RC at 250 W. (d) Variable sampling RC at 1.5 kW.

THD, similar to the case of the variable sampling RC. Compared to the CRC, it is worth noting that the proposed RC can be implemented with a 50% reduced number of memory blocks and it contributes to efficient system architecture.

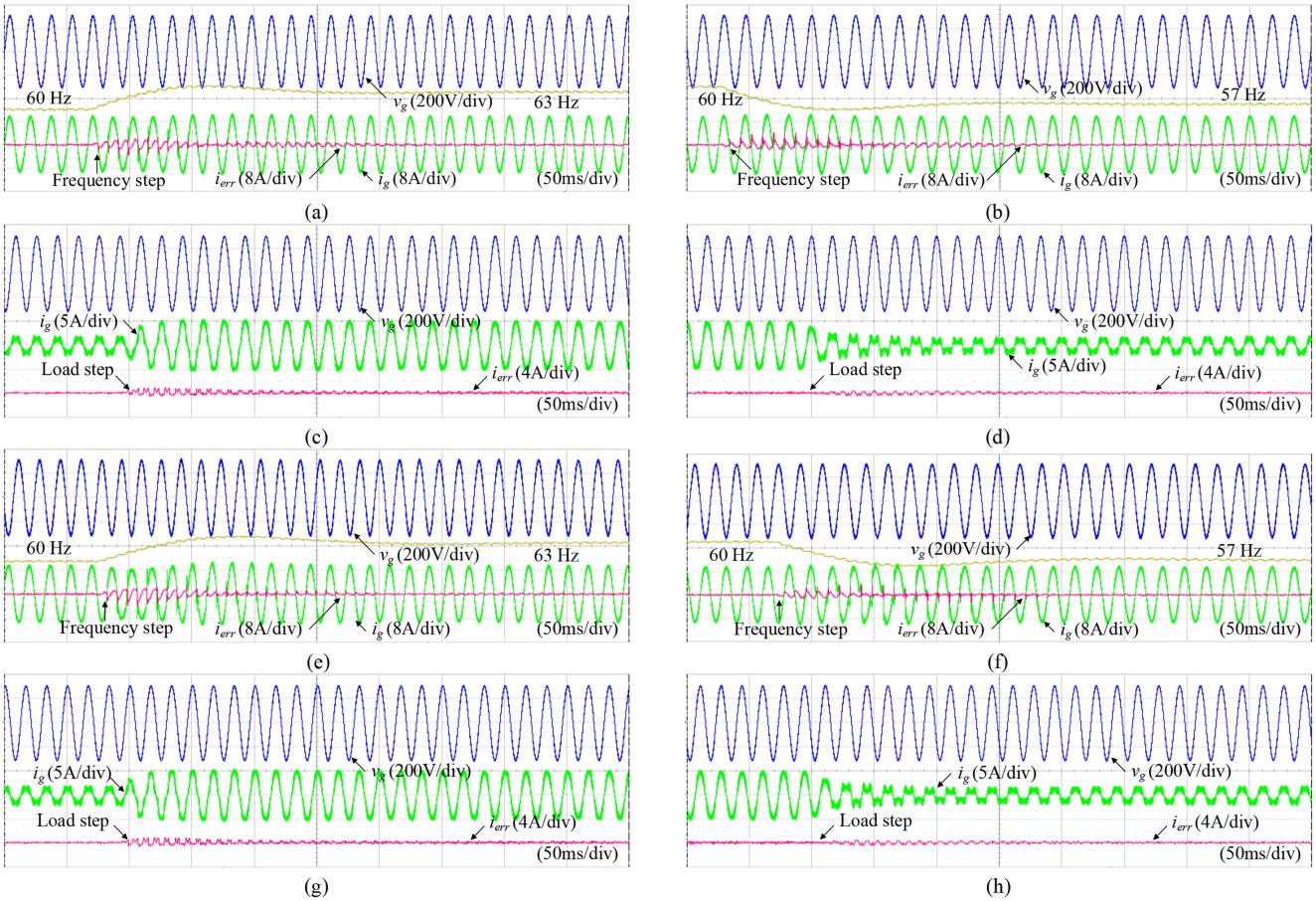

Fig. 27. Experimental results of transient response under frequency step change and load step change. (a)–(d) Proposed RC with $N = 88$. (e)–(h) Variable sampling RC with $N = 88$. (a) and (e) f_g step change from 60 to 63 Hz. (b) and (f) f_g step change from 60 to 57 Hz. (c) and (g) Load step from 250 to 750 W. (d) and (h) Load step from 750 to 250 W.

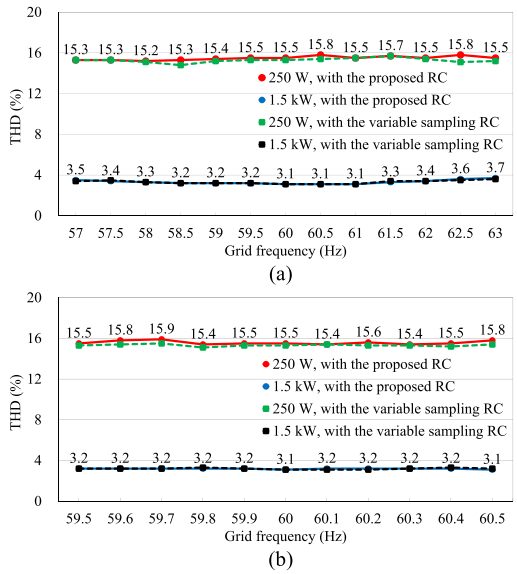

Fig. 28. Grid input current THD at different grid frequency with the proposed RC for $N = 88$ and the variable sampling RC. (a) From 57 to 63 Hz. (b) From 59.5 to 60.5 Hz.

VI. Conclusion

In this article, an average periodic delay-based RC scheme for grid-connected PFC converter has been proposed to address the adverse effect of frequency variation on the compensation performance of RCs. The proposed method constructs the average periodic delay by synchronizing the memory sampling with the phase angle of the PLL, which enables frequency adaptability under a constant-sampling rate and a fixed number of memory blocks. In this process, the effects of the sample delay and advance in the proposed RC are discussed to analyze the operation of the RC and to establish the design criteria. Based on the discussion, stability analysis is performed to determine the control parameters. As summarized in Table III, the proposed control scheme demonstrates a robust compensation performance under a wide grid frequency range.

The proposed RC scheme provides the following benefits.

1) By using the average periodic delay, a frequency adaptive RC for wide frequency variation can be achieved with the fixed sampling frequency. This provides portability and effectiveness to the digital control system of the fixed sampling frequency.

TABLE III
PERFORMANCE COMPARISON OF RC METHODS

		CRC	Variable Sampling RC	Proposed RC	
i_g THD (at 1.5 kW)	57 Hz	25.5%	3.4%	3.7%	3.5%
	60 Hz	3.2%	3.1%	3.2%	3.1%
	63 Hz	7.5%	3.6%	3.5%	3.7%
Sampling period (T_s)		Fixed (50 μs)	Varied (90.2–99.7 μs)	Fixed (50 μs)	
Number of the memory blocks (N)		Fixed (166)	Fixed (88)	Fixed (158)	Fixed (88)
Frequency range (Hz)		60	$57 < f_g < 63$	$32 < f_g < 63$	$57 < f_g < 113$

2) Reducing the memory usage makes it possible to design an effective software architecture and cost-efficient option for digital devices. It also contributes to the flexibility of the software configuration and management of power converter systems such as series, parallel, and polyphase converters.

Both the simulation and experimental results have demonstrated that the proposed RC satisfies the grid standard for the THD of the input current under various frequency deviations, where the traditional approaches cannot survive.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[4] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.

[5] S. Yang, Q. Lei, F. Z. Peng, and Z. Qian, "A robust control scheme for grid-connected voltage-source inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 202–212, Jan. 2011.

[6] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.

[7] A. Kuperman, "Proportional-resonant current controllers design based on desired transient performance," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5341–5345, Oct. 2015.

[8] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[9] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.

[10] X. Wang, P. C. Loh, and F. Blaabjerg, "Stability analysis and controller synthesis for single-loop voltage-controlled VSIs," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7394–7404, Sep. 2017.

[11] K. Nishida, T. Ahmed, and M. Nakaoka, "Cost-effective deadbeat current control for wind-energy inverter application with LCL filter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1185–1197, Mar./Apr. 2014.

[12] Y. A.-R. I. Mohamed and E. F. El-Saadany, "An improved deadbeat current control scheme with a novel adaptive self-tuning load model for a three-phase PWM voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 747–759, Apr. 2007.

[13] J. Rodriguez *et al.*, "Predictive current control of a voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 495–503, Feb. 2007.

[14] C. N. M. Ho, V. S. P. Cheung, and H. S. H. Chung, "Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2484–2495, Nov. 2009.

[15] M. Mohseni, S. M. Islam, and M. A. S. Masoum, "Enhanced hysteresis-based current regulators in vector control of DFIG wind turbines," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 223–234, Jan. 2011.

[16] Y. Y. Tzou, R. S. Ou, S. L. Jung, and M. Y. Chang, "High-performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 715–725, Jul. 1997.

[17] R. Costa-Castello, R. Grino, and E. Fossas, "Odd-harmonic digital repetitive control of a single-phase current active filter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1060–1068, Jul. 2004.

[18] P. Mattavelli and F. P. Marafao, "Repetitive-based control for selective harmonic compensation in active power filters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1018–1024, Oct. 2004.

[19] G. Escobar, A. A. Valdez, J. Leyva-Ramos, and P. Mattavelli, "Repetitive-based controller for a UPS inverter to compensate unbalance and harmonic distortion," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 504–510, Feb. 2007.

[20] G. Escobar, P. Martinez, J. Leyva-Ramos, and P. Mattavelli, "A negative feedback repetitive control scheme for harmonic compensation," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1383–1386, Jun. 2006.

[21] Y. Cho and J. S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165–175, Jan. 2013.

[22] P. Mattavelli, L. Tubiana, and M. Zigliotto, "Torque-ripple reduction in PM synchronous motor drives using repetitive current control," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1423–1431, Nov. 2005.

[23] B. Zhang, K. Zhou, and D. Wang, "Multirate repetitive control for PWM DC/AC converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2883–2890, Jun. 2014.

[24] F. Gonzalez-Espin, P. Mattavelli, E. Figueres, G. Garcera, and R. Foley, "A variable multi-rate plug in repetitive controller for single phase inverters operation in the islanding mode," in *Proc. 15th Int. EPE PEMC Conf.*, Sep. 2012.

[25] M. A. Herran, J. R. Fischer, S. A. Gonzalez, M. G. Judewicz, I. Carugati, and D. O. Carrica, "Repetitive control with adaptive sampling frequency for wind power generation systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 58–69, Mar. 2014.

[26] P. Zanchetta, M. Degano, J. Liu, and P. Mattavelli, "Iterative learning control with variable sampling frequency for current control of grid-connected converters in aircraft power systems," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1548–1555, Jul./Aug. 2013.

[27] M. Abusara, S. Sharkh, and P. Zanchetta, "Adaptive repetitive control with feedforward scheme for grid-connected inverters," *IET Power Electron.*, vol. 8, no. 8, pp. 1403–1410, Aug. 2015.

[28] M. Abusara, S. Sharkh, and P. Zanchetta, "Control of grid-connected inverters using adaptive repetitive and proportional resonant schemes," *J. Power Electron.*, vol. 15, no. 2, pp. 518–529, Mar. 2015.

[29] S. Kolluri, N. B. Y. Gorla, R. Sapkota, and S. K. Panda, "A new control architecture with spatial comb filter and spatial repetitive controller for circulating current harmonics elimination in a droop-regulated modular multilevel converter for wind farm application," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10509–10523, Nov. 2019.

[30] Y. Yang, K. Zhou, and F. Blaabjerg, "Enhancing the frequency adaptability of periodic current controllers with a fixed sampling rate for grid-connected power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7273–7285, Oct. 2016.

[31] Z. X. Zou, K. Zhou, Z. Wang, and M. Cheng, "Frequency-adaptive fractional-order repetitive control of shunt active power filters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1659–1668, Mar. 2015.
[32] D. Chen, J. Zhang, and Z. Qian, "An improved repetitive control scheme for grid-connected inverter with frequency-adaptive capability," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 814–823, Feb. 2013.
[33] G. Escobar, G. A. Catzin-Contreras, and M. J. Lopez-Sanchez, "Compensation of variable fractional delays in the 6k ± 1 repetitive controller," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6448–6456, Oct. 2015.
[34] Z. Liu, B. Zhang, K. Zhou, Y. Yang, and J. Wang, "Virtual variable sampling repetitive control of single-phase DC/AC PWM converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1837–1845, Sep. 2019.
[35] Y. Song and H. Nian, "Sinusoidal output current implementation of DFIG using repetitive control under a generalized harmonic power grid with frequency deviation," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6751–6762, Dec. 2015.
[36] M. Tang, A. Gaeta, A. Formentini, and P. Zanchetta, "A fractional delay variable frequency repetitive control for torque ripple reduction in PMSMs," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5553–5562, Nov./Dec. 2017.
[37] Y. Yuan, F. Auger, L. Loron, S. Moisy, and M. Hubert, "Torque ripple reduction in permanent magnet synchronous machines using angle-based iterative learning control," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2012, pp. 2518–2523.
[38] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, IEEE Standard 1547-2018, Apr. 2018.
[39] N. Schechter and A. Kuperman, "Zero-sequence manipulation to maintain correct operation of NPC-PFC rectifier upon neutral line disconnection and reconnection," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 866–872, Jan. 2017.
[40] S. Madishetti, B. Singh, and G. Bhuvaneswari, "Three-level NPC-inverter-based SVM-VCIMD with feedforward active PFC rectifier for enhanced AC mains power quality," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1865–1873, Mar./Apr. 2016.
[41] S. Golestan, J. M. Guerrero, J. Vasquez, A. M. Abusorrah, and Y. A. Al-Turki, "All-pass-filter-based PLL systems: Linear modeling, analysis, and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3558–3572, Apr. 2020.
[42] K. P. Louganski and J.-S. Lai, "Current phase lead compensation in single-phase PFC boost converters with a reduced switching frequency to line frequency ratio," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 113–119, Jan. 2007.
[43] X. Zhang, J. W. Spencer, and J. M. Guerrero, "Small-signal modeling of digitally controlled grid-connected inverters with LCL filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3752–3765, Sep. 2013.
[44] D. M. Van de Sype, K. De Gusseme, F. M. L. L. De Belie, A. P. Van den Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 470–478, Mar. 2006.
[45] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. San Rafael, CA, USA: Morgan & Claypool, 2006. [Online]. Available: https://ieeexplore.ieee.org/document/6813194
[46] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.

Seunghoon Baek (Student Member, IEEE) was born in Daejeon, South Korea, in 1991. He received the B.S. degree in electrical engineering from Konkuk University, Seoul, South Korea, in 2015, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include high-power converters, grid-connected systems, and electric machine drives.

Younghoon Cho (Member, IEEE) was born in Seoul, South Korea, in 1980. He received the B.S. degree in electrical engineering from Konkuk University, Seoul, South Korea, in 2002, the M.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2004, and the Ph.D. degree from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2012.

From 2004 to 2009, he was an Assistant Research Engineer with the Hyundai MOBIS R&D Center, Yongin, South Korea. Since 2013, he has been with the Department of Electrical and Electronics Engineering, Konkuk University, where he is currently an Associate Professor. His current research interests include digital control techniques for power electronic converters in vehicle and grid applications, multilevel converters, and high-performance motor drives.

Jih-Sheng (Jason) Lai (Life Fellow, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 1985 and 1989, respectively.

In 1989, he joined the Electric Power Research Institute (EPRI) Power Electronics Applications Center (PEAC), where he managed EPRI-sponsored power electronics research projects. In 1993, he then joined the Oak Ridge National Laboratory as a Power Electronics Lead Scientist, where he initiated a high power electronics program and developed several novel high power converters including multilevel converters and soft-switching inverters. In 1996, he joined Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, where he is currently the James S. Tucker Professor with the Electrical and Computer Engineering Department and a Director with Future Energy Electronics Center. His main research interests include high efficiency power electronics conversions for high power and energy applications. He has authored or coauthored more than 480 refereed technical papers, 1 book chapter, 2 books, and 29 patents.

Dr. Lai is the Founding Chairs of 2001 IEEE IFEC and 2016 IEEE ACEPT, General Chairs of IEEE COMPEL-2000, IEEE APEC 2005, IEEE SPEC-2018, IEEE IFEEC-2019, and IEEE STPEC-2020 conferences. He was the recipient of the Technical Achievement Award in Lockheed Martin Award Night, two Journal Paper Awards, and 13 Best Paper Awards from IEEE sponsored conferences. He was the recipient of the 2016 IEEE IAS Gerald Kliman Innovator Award. He led the student teams to win the Top Three Finalist in Google Little Box Challenge, in 2016, Grand Prize Award from International Future Energy Challenge (IFEC), in 2011, and Grand Prize Award from Texas Instruments Engibous Analog Design Competition, in 2009.