Analysis and Improvement of the Effect of Distributed Parasitic Capacitance on High-Frequency High-Density Three-Phase Buck Rectifier

Qiang Chen, Jianping Xu, *Member, IEEE*, Lei Wang, Rui Huang, and Hongbo Ma, *Member, IEEE*

***Abstract*—For high-density three-phase buck rectifier (3ph-BR), such as a standard full-brick size 3ph-BR, there exist obvious parasitic capacitances distributed between its dc-link output and the system ground, which lead to low-frequency distortion of input currents, and thus, serious deterioration of the input current total harmonics distortion (THD). The effect of the distributed parasitic capacitances becomes more obvious for the 3ph-BR under light load conditions. To improve the input current quality of the high-density 3ph-BR, a modified 3ph-BR is introduced in this article. The modified 3ph-BR has one low-frequency current path which realizes power transfer from ac input to dc output, and two high-frequency current paths which provide low-impedance path for high-frequency currents. The high-frequency current caused by the parasitic capacitance distributed between the dc-link output and the system ground circulates internally, rather than flow to the ac input side. Thus, input current THD of the modified 3ph-BR can be reduced. A 1-kW experimental prototype of the modified 3ph-BR with 200 kHz switching frequency and standard full-brick size is built to verify the analysis results.**

***Index Terms*—High density, high frequency, input current total harmonics distortion (THD), parasitic capacitance, three-phase buck rectifier (3ph-BR).**

I. Introduction

THREE-PHASE rectifiers can draw well-balanced and low-distortion sinusoidal currents from each phase of three-phase ac input [1], [2]. The three-phase boost-type rectifier and the three-phase buck-type rectifier (also known as the current-source rectifier) are two basic three-phase rectifiers [3]–[7]. Compared with the three-phase boost-type rectifier, the three-phase buck rectifier (3ph-BR) has the advantages of high reliability, small start-up current, and the ability of short-circuit current limiting. Thus, the 3ph-BR is most suitable for the more electric aircraft (MEA) application in terms of its high reliability [8]–[10]. Furthermore, the 3ph-BR can provide a wide output voltage range down to low voltage. The 3ph-BR with 400 V output is preferred as the front-end rectifier for some special applications, such as on-board chargers for the electric vehicle (EV) and the telecom and data center. Compared with the 3ph-BR, the three-phase boost-type rectifier produces high output voltage (typically, 650 to 800 V) which cannot be directly used as the low-voltage dc-bus. Thus, a step-down dc–dc converter is required to provide a low output voltage, which will seriously reduce the efficiency and increase the cost [11], [12]. Therefore, the 3ph-BR has a wide range of application prospects and is worthy of an in-depth study.

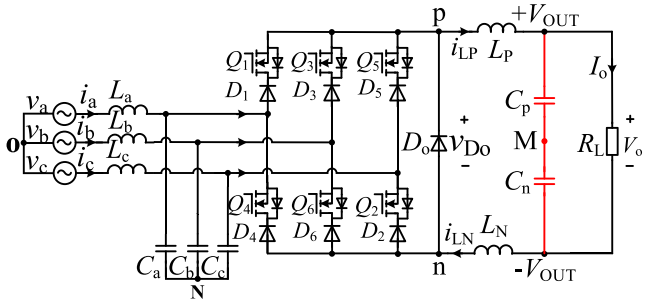

Fig. 1. Conventional 3ph-BR.

The conventional 3ph-BR, as shown in Fig. 1, is also known as the six-switch 3ph-BR. It consists of six bridge legs and one freewheeling diode [7], [11], [12]. Each leg of the conventional 3ph-BR includes one MOSFET and one diode in series. In [13]–[15], a three-switch 3ph-BR is studied. Each leg of three-switch 3ph-BR has one MOSFET and four diodes. The three-switch 3ph-BR has high number of semiconductors in each current path, which leads to higher conduction losses than the six-switch 3ph-BR.

To obtain higher efficiency, the switching frequency of the 3ph-BR is usually in the range of 20–50 kHz [1]–[17]. In some applications, such as aircraft applications, small size and lightweight are necessary [8]–[10]. In these applications, the 3ph-BR with high switching frequency and high power density are key features and main concerns. Silicon carbide (SiC) power devices provide opportunities to implement high efficiency three-phase rectifiers with high switching frequency and high power density [9], [18]. A 2-kW 3ph-BR using SiC devices with 150 kHz switching frequency is presented in [19] and [20], which demonstrated that the SiC power device is a viable device

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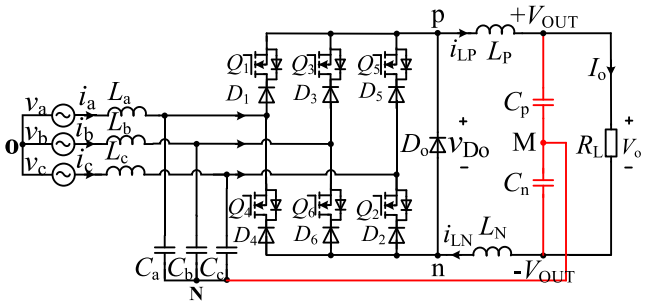

Fig. 2. Modified 3ph-BR.

for future high-frequency three-phase ac applications. In [21], a 3-kVA all-SiC current source converter (CSC), which consists of a 3ph-BR and a three-phase buck inverter, has been designed specifically for a switching frequency of 200 kHz. It enables a high-frequency CSC to reduce the size and weight of the dc-link inductor. In [22], a systematic evaluation approach of a 10-kVA high-density CSC has been developed. With the high-frequency capability of SiC devices, the impact of the switching frequency was carefully studied by considering loss, passive size, and electromagnetic interference (EMI) filter design.

Although lots of research works have been done to improve the efficiency and power density of the 3ph-BR, less attention has been paid on the input current quality of high-frequency high-density 3ph-BR. For the conventional 3ph-BR as shown in Fig. 1, the high-frequency common mode (CM) voltage between the dc-link buses (p and n, or $+V_{\rm OUT}$ and $-V_{\rm OUT}$) and the mains star-point (O) inevitably leads to the propagation of CM currents [16], [23], and these CM currents circulate through distributed parasitic capacitances [24]–[26]. When the switching frequency of the 3ph-BR is low, the dc-link current ripple and the three-phase current ripple are usually large. In this case, the CM currents caused by the distributed parasitic capacitances are small and the effect of distributed parasitic capacitance on the performance of 3ph-BR is not obvious, which only leads to high-frequency EMI interference. However, with the increase of switching frequency and power density, the parasitic capacitances distributed between the dc-link output and the system ground become obvious, which leads to serious low-frequency distortion on its input currents. The effects of parasitic capacitance cannot be omitted, which is particularly serious under light load conditions.

In order to reduce CM emissions, an additional two-stage CM input filter is designed for the conventional 3ph-BR in [26]. In this article, a modified 3ph-BR is proposed by connecting the common point of two output capacitors to the neutral point of ac input filter capacitors without additional CM filter, as shown in Fig. 2. The approach presented in this article has been used in the three-phase boost-type rectifier to mitigate high-frequency CM EMI [27], [28]. However, the modified 3ph-BR can not only suppress the high-frequency CM current flowing to the input side, but also effectively reduce the low-order harmonics in its input current. Therefore, the modified 3ph-BR presented in this article is more suitable for the high-density application.

So far, much attention has been paid on the model of the CM noise propagation and the design of EMI filter [26]–[28]. Less attention has been paid on the input current THD and the steady-state performance of these rectifiers. As the application of the presented approach in the 3ph-BR is quite different from that in the three-phase boost-type rectifier, it is worth studying the modified 3ph-BR. In this article, the effect of parasitic capacitances on input current quality of the 3ph-BR is analyzed. Furthermore, the operation modes of the modified 3ph-BR in each switching period are studied in detail, and the time-domain behaviors of the dc-link currents and the voltage ripples of output capacitors are derived.

The rest of this article is organized as follows. In Section II, the modulation strategy is briefly introduced. In Section III, the operation modes and the corresponding current paths of the conventional 3ph-BR with and without distributed parasitic capacitances are analyzed. In Section IV, the operation modes of the modified 3ph-BR are analyzed and the voltage ripples of output capacitances and the dc-link current ripples are derived. A 1-kW 3ph-BR with 200 kHz switching frequency and standard full-brick size is built in Section V. Experimental results of the prototype are provided to verify the analysis results. Finally, Section VI concludes the article.

II. Space Vector Pulsewidth Modulation (SVPWM) Strategy

Fig. 1 shows the conventional 3ph-BR. It consists of an input filter unit, a switch unit, and an output filter unit. The input filter unit consists of filter inductor $L_{\rm x}$ and filter capacitances $C_{\rm x}$ (x = a, b, c), which are used to filter ac side current harmonics. The bridge leg of each phase S_i (i = 1–6) in the switch unit is composed of a MOSFET Q_i and a diode connected in series to block the reverse current. Diode $D_{\rm o}$ provides a flowing path for the dc-link inductor current. The output filter unit is composed of the dc-link inductors $L_{\rm P}$ and $L_{\rm N}$, and the output capacitance $C_{\rm p}$ and $C_{\rm n}$. The inductors $L_{\rm P}$ and $L_{\rm N}$ at the positive and the negative ends of the output provide the symmetric attenuation impedance for the CM noise current, respectively. Besides, the output voltage of the three-phase rectifier is generally high, so it is necessary to avoid the use of high-voltage capacitance, which is usually composed of two low-voltage capacitances in series.

Define the three-phase ac input voltages as

$$\begin{cases} v_{\rm a}(t) = V_m \cos(2\pi f_L t) \\ v_{\rm b}(t) = V_m \cos(2\pi f_L t - 2\pi/3) \\ v_{\rm c}(t) = V_m \cos(2\pi f_L t + 2\pi/3) \end{cases} \tag{1}$$

where $v_{\rm a}$, $v_{\rm b,}$ and $v_{\rm c}$ are the instantaneous voltages of the three-phase ac input, $V_{\rm m}$ is the amplitude of the ac input phase voltage, and $f_{\rm L}$ is the frequency of the ac input.

In this article, the SVPWM strategy, which minimizes the switching losses, is utilized for the 3ph-BR. This SVPWM strategy is also called as the switching loss optimized (SLO) strategy [4], [5]. The SLO modulation has 12 sectors in one input voltage period, as shown in Fig. 3. As the bridge leg is composed of a MOSFET and a diode connected in series, the bridge leg can be turned ON only when the MOSFET has a driving

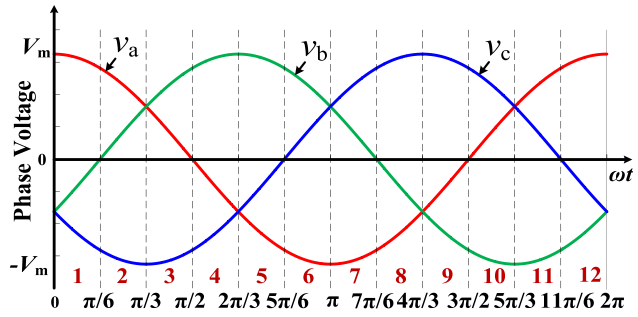

Fig. 3. Three-phase ac input voltages with 12 sectors.

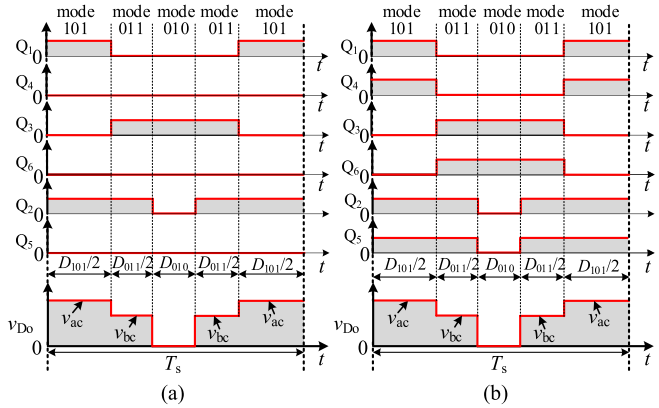

Fig. 4. PWM sequences of the bridge legs in one switching period in sector 2. (a) PWM sequences in [12]. (b) PWM sequences in [11].

TABLE I
DUTY RATIO OF EACH BRIDGE LEG IN ONE SWITCHING PERIOD IN 12 SECTORS

Sector	δ_1	δ_4	δ_3	δ_6	δ_5	δ_2
12, 1	Mv_a/V_m	0	0	$-Mv_b/V_m$	0	$-Mv_c/V_m$
2, 3	Mv_a/V_m	0	Mv_b/V_m	0	0	$-Mv_c/V_m$
4, 5	0	$-Mv_a/V_m$	Mv_b/V_m	0	0	$-Mv_c/V_m$
6, 7	0	$-Mv_a/V_m$	Mv_b/V_m	0	Mv_c/V_m	0
8, 9	0	$-Mv_a/V_m$	0	$-Mv_b/V_m$	Mv_c/V_m	0
10, 11	Mv_a/V_m	0	0	$-Mv_b/V_m$	Mv_c/V_m	0

signal and the diode is subjected to forward voltage. Therefore, there are two different PWM sequences which can realize the SLO modulation.

Fig. 4(a) and (b) shows two different PWM sequences in the sector 2. The PWM sequences of the bridge legs shown in Fig. 4(a) are reported in [12], and the PWM sequences of the bridge legs shown in Fig. 4(b) are studied in [11]. It can be known from Fig. 4 that the PWM sequences of the bridge legs are symmetrical in one switching period. The PWM sequences in both Fig. 4(a) and (b) share the same waveform of v_{Do}. In Fig. 4(b), the same driver is applied to the MOSFETs in two bridge legs of each phase. Thus, only three gate signals are used, which makes the implementation of its PWM sequences simple. In this article, the PWM sequences of the bridge legs in Fig. 4(b) are adopted.

Table I presents the duty ratio of each bridge leg in one switching period [7], [11]. In Table I, δ_i ($i = 1$–6) is the duty ratio of the *ith* bridge leg in one switching period. M is the modulation ratio of rectifier, with

$$M = \frac{2}{3}\frac{V_o}{V_m} \tag{2}$$

where V_o is the output voltage of the rectifier, and $M \in (0,1)$.

The operation mode of the 3ph-BR is defined by the switching states of the switches in each phase. In sector 2, there are three operation modes in one switching period. These three operation modes follow the order 101 → 011 → 010→011→101, where "1" denotes the ON-state of the switch and "0" denotes the OFF-state of the switch. Take mode 101 as example, as shown in Fig. 4(b), the switches of phase *A* and phase *C* are turned ON, and the switches of phase *B* are turned OFF. It is similar for mode 011 and mode 010.

Define D_x as the duty ratio of each operating mode in one switching period, where $x \in$ (101, 011, 010). For any switching period in sector 2, switch S_1 is turned ON only in mode 101. Thus, $D_{101} = \delta_1$, i.e., $D_{101} = Mv_a/V_m$ according to Table I. Similarly, $D_{010} = 1\delta_2 = 1+Mv_c/V_m$, $D_{011} = \delta_3 = Mv_b/V_m$.

III. EFFECT OF THE PARASITIC CAPACITANCE ON THE CONVENTIONAL 3PH-BR

In this section, the time-domain behaviors of the input currents and the ripple of dc-link current of the conventional 3ph-BR with and without distributed parasitic capacitances are analyzed, with circuit parameters $V_m = 162\,V, f_L = 50\,Hz, f_S = 200\,kHz$, $V_o = 200\,V$, $L_P = L_N = 300\,\mu H$. To simplify the analysis, the following assumptions are made.

1) The 3ph-BR operates in continuous conduction mode.
2) All of the switching devices are ideal.
3) The switching frequency is much higher than the ac input frequency, thus the three-phase input voltages are constant in each switching period.
4) The three-phase input voltages are balanced, and the points O and N are equal potential points.

A. Without Distributed Parasitic Capacitances

When distributed parasitic capacitances are not considered, the conventional 3ph-BR has only one current flowing path in any operation mode [2], [11], as shown in Fig. 5.

For the conventional 3ph-BR, the high-frequency ripple of the dc-link current can be effectively attenuated by the input *LC* filter. Therefore, the three-phase input currents are

$$\begin{cases} i_a = Mv_aI_o/V_m \\ i_b = Mv_bI_o/V_m \\ i_c = Mv_cI_o/V_m. \end{cases} \tag{3}$$

It can be obtained from (3) that the three-phase input currents follow the three-phase input voltages. The three-phase input currents are independent of the dc-link current ripple, which leads to the high-quality input currents.

Fig. 6 shows the equivalent current ripple path of the two dc-link inductors in the conventional 3ph-BR. The voltages v_{pn} and v_{Co} are given in Table II. The voltage v_{pn} is dependent on the PWM sequences of each sector. Assume the output capacitances are large enough that the voltage v_{Co} remains constant and equal

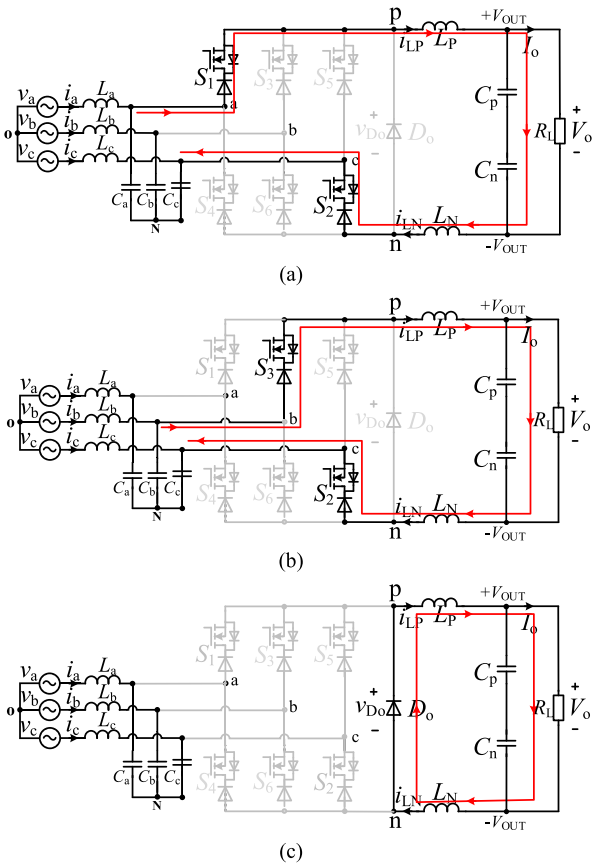

Fig. 5. DC-link current paths of the conventional 3ph-BR in three operation modes in sector 2. (a) Mode 101. (b) Mode 011. (c) Mode 010.

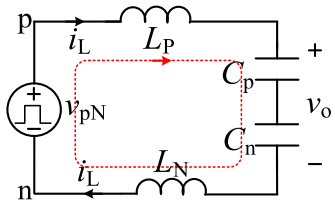

Fig. 6. Equivalent current ripple paths of the conventional 3ph-BR.

TABLE II
V_{PN} AND V_{CO} OF THE CONVENTIONAL 3ph-BR IN ONE SWITCHING PERIOD

Sector	Mode	v_{pn}	v_o	$v_{pO}(v_{pN})$	$v_{nO}(v_{nN})$
2	101	v_{ac}	V_o	v_a	v_c
	011	v_{bc}	V_o	v_b	v_c
	010	0	V_o	v_b	v_b
	011	v_{bc}	V_o	v_b	v_c
	101	v_{ac}	V_o	v_a	v_c

to the voltage V_o in one switching cycle. As the two dc-link inductors L_P and L_N withstand the same voltage, the inductors L_P and L_N have the same charging or discharging states.

In sector 2, the dc-link inductors have two working states, as illustrated in Fig. 7. From Table II, Δi_L in Fig. 7(a) is

$$\Delta i_L(t) = \frac{V_o}{(L_P+L_N)f_s} D_{010} + \frac{V_o - v_{bc}(t)}{(L_P+L_N)f_s} D_{011}$$

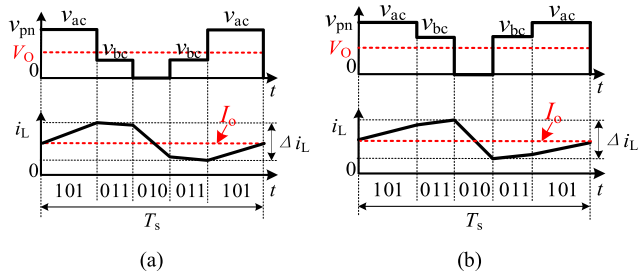

Fig. 7. DC-link current ripples of the conventional 3ph-BR in one switching period in sector 2. (a) $v_{bc} \geq V_o$. (b) $v_{bc} \leq V_o$.

TABLE III
ΔI_L OF ONE SWITCHING PERIOD IN 12 SECTORS

Sector	Δi_L
12, 1	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{-}M\frac{v_a(t)}{V_m}\right)$
2, 3	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{+}M\frac{v_c(t)}{V_m}\right)$
4, 5	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{-}M\frac{v_b(t)}{V_m}\right)$
6, 7	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{+}M\frac{v_a(t)}{V_m}\right)$
8, 9	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{-}M\frac{v_c(t)}{V_m}\right)$
10, 11	$\frac{V_o}{(L_P+L_N)f_S}\left(1\text{+}M\frac{v_b(t)}{V_m}\right)$

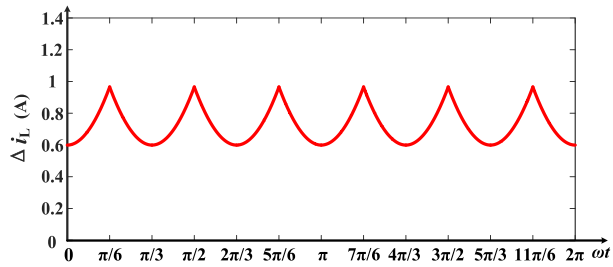

Fig. 8. Δi_L in one input voltage period.

$$= \frac{V_o}{(L_P+L_N)f_s}\left(1+\frac{Mv_c(t)}{V_m}\right) + \frac{V_o - v_{bc}(t)}{(L_P+L_N)f_s}\frac{Mv_b(t)}{V_m} \quad (4)$$

and Δi_L in Fig. 7(b) is

$$\Delta i_L(t) = \frac{V_o}{(L_P+L_N)f_s} D_{010} = \frac{V_o}{(L_P+L_N)f_s}\left(1+\frac{Mv_c(t)}{V_m}\right). \quad (5)$$

In sector 2, when $v_{bc} \geq V_o$, the voltages $(V_o - v_{bc})$ and v_b are small. Equation (5) can be adopted to calculate Δi_L. Similarly, Δi_L in other sectors can be calculated, as given in Table III.

Fig. 8 illustrates Δi_L in one ac input voltage period. As shown in Fig. 8, Δi_L varies slightly with a frequency six times that of the ac input frequency.

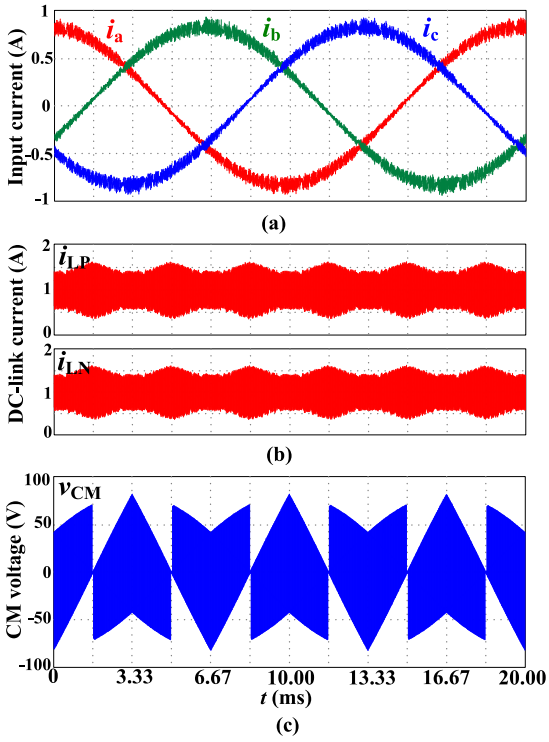

Fig. 9. Key waveforms of the conventional 3ph-BR without distributed parasitic capacitances under 200 W load in one input voltage period. (a) Three-phase input currents. (b) DC-link current i_{LP} and i_{LN}. (c) CM voltage v_{CM}.

Furthermore, for the conventional 3ph-BR, there is obvious high-frequency CM voltage between the dc-link output and the mains star-point O (O means system ground). The CM voltage is produced within each switching period, which depends on the SVPWM strategy.

The CM voltage is defined as

$$v_{\mathrm{CM}}(t) = \frac{v_{\mathrm{pO}}(t) + v_{\mathrm{nO}}(t)}{2} \tag{6}$$

where v_{pO} represents the voltage between the positive dc-link rail and the star-point O, and v_{nO} represents the voltage between the negative dc-link rail and star-point O, which have been given in Table II.

Fig. 9 shows the simulation results of the key waveforms of the conventional 3ph-BR under 200 W load. It can be seen from Fig. 9(a) that the conventional 3ph-BR can draw well-balanced and low-distortion sinusoidal currents from each phase of three-phase ac input. It can be known from Fig. 9(b) that dc-link current ripple varies slightly with a frequency six times that of ac input frequency, and it can be known from Fig. 9(c) that the CM voltage varies with a frequency three times that of the ac input frequency.

B. With Distributed Parasitic Capacitances

The conventional 3ph-BR inherently generates CM voltage between the dc-link output buses (p and n, or $+V_{\mathrm{OUT}}$ and $-V_{\mathrm{OUT}}$) and the point O, which will inevitably lead to the propagation of the CM currents. The CM currents circulate between the power line and the system ground through the distributed parasitic capacitances.

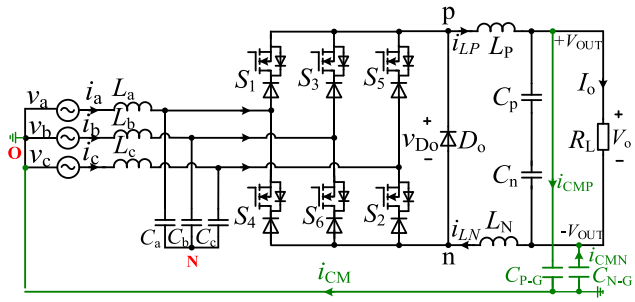

Fig. 10. Conventional 3ph-BR with the lumped parasitic capacitances.

In practical applications, distributed parasitic capacitances are unavoidable. Due to the complex distribution of the parasitic capacitances in the 3ph-BR, it is difficult to analyze the propagation path of the CM currents. Some research works adopt the equivalent lumped parasitic capacitances to study the propagation paths of CM noise [26], [27]. In these research works, the parasitic capacitances between the output terminals to the system GND are considered. Similarly, the equivalent lumped parasitic capacitances are considered in the 3ph-BR, as shown in Fig. 10. The capacitances $C_{\mathrm{P\text{-}G}}$ and $C_{\mathrm{N\text{-}G}}$ are used to represent the influence of the distributed parasitic capacitances between the output terminals of the circuit board and the system ground. The capacitances $C_{\mathrm{P\text{-}G}}$ and $C_{\mathrm{N\text{-}G}}$ in Fig. 10 may come from the rectifier itself or may be caused by the load. Besides, the class *Y* capacitances are usually required for safety reasons, which also contribute to the capacitances of $C_{\mathrm{P\text{-}G}}$ and $C_{\mathrm{N\text{-}G}}$ [29]. As the equivalent lumped parasitic capacitances are usually in the range of several pF to several nF [26], [27], in order to simplify the analysis, the parasitic capacitance is set as 500 pF, and the corresponding simulation analysis is carried out.

When the lumped parasitic capacitances are considered, the CM currents are produced by the CM voltage and the parasitic capacitances. CM currents flow through the input side, which will inevitably cause significant high-frequency CM noise in the input currents. From Fig. 10, it has

$$i_{\mathrm{a}}(t) + i_{\mathrm{b}}(t) + i_{\mathrm{c}}(t) = i_{\mathrm{CM}}(t). \tag{7}$$

As CM currents also flow through the dc-link inductors, CM currents will affect the time-domain behaviors of the dc-link currents. Therefore, the dc-link currents have obvious distortion, and the average dc-link currents are not equal to the load current I_{o}. According to the principle of the SVPWM modulation strategy described in Section II, the six bridge legs distribute the dc-link currents among the three phases by PWM at a fixed switching frequency. Hence, the distortion of dc-link current will inevitably lead to the distortion of the input current, which results in deterioration of the input current THD.

When the lumped parasitic capacitances are considered, the expressions of dc-link currents are

$$\begin{cases} i_{\mathrm{LP}}(t) = I_{\mathrm{o}} + i_{\mathrm{CMP}}(t) \\ i_{\mathrm{LN}}(t) = I_{\mathrm{o}} + i_{\mathrm{CMN}}(t) \\ i_{\mathrm{CMP}}(t) = -i_{\mathrm{CMN}}(t) = i_{\mathrm{CM}}(t)/2 \end{cases} \tag{8}$$

where the currents i_{CMP} and i_{CMN} denote the high-frequency CM currents flowing through the dc-link inductors. They depend on the CM voltage and the parasitic capacitances, and they increase with the increase of the parasitic capacitances.

When the CM currents are considered, the three-phase input currents are expressed as

$$\begin{aligned} i_{\mathrm{a}}(t) &= \begin{cases} Mv_{\mathrm{a}}(t)i_{\mathrm{LP}}(t)/V_{\mathrm{m}} & v_{\mathrm{a}}(t) \geq 0 \\ Mv_{\mathrm{a}}(t)i_{\mathrm{LN}}(t)/V_{\mathrm{m}} & v_{\mathrm{a}}(t) < 0 \end{cases} \\ i_{\mathrm{b}}(t) &= \begin{cases} Mv_{\mathrm{b}}(t)i_{\mathrm{LP}}(t)/V_{\mathrm{m}} & v_{\mathrm{b}}(t) \geq 0 \\ Mv_{\mathrm{b}}(t)i_{\mathrm{LN}}(t)/V_{\mathrm{m}} & v_{\mathrm{b}}(t) < 0 \end{cases} \\ i_{\mathrm{c}}(t) &= \begin{cases} Mv_{\mathrm{c}}(t)i_{\mathrm{LP}}(t)/V_{\mathrm{m}} & v_{\mathrm{c}}(t) \geq 0 \\ Mv_{\mathrm{c}}(t)i_{\mathrm{LN}}(t)/V_{\mathrm{m}} & v_{\mathrm{c}}(t) < 0. \end{cases} \end{aligned} \tag{9}$$

By substituting (8) into (9), the three phase input currents are

$$\begin{aligned} i_{\mathrm{a}}(t) &= \begin{cases} Mv_{\mathrm{a}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} + Mv_{\mathrm{a}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{a}}(t) \geq 0 \\ Mv_{\mathrm{a}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} - Mv_{\mathrm{a}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{a}}(t) < 0 \end{cases} \\ i_{\mathrm{b}}(t) &= \begin{cases} Mv_{\mathrm{b}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} + Mv_{\mathrm{b}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{b}}(t) \geq 0 \\ Mv_{\mathrm{b}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} - Mv_{\mathrm{b}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{b}}(t) < 0 \end{cases} \\ i_{\mathrm{c}}(t) &= \begin{cases} Mv_{\mathrm{c}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} + Mv_{\mathrm{c}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{c}}(t) \geq 0 \\ Mv_{\mathrm{c}}(t)I_{\mathrm{o}}/V_{\mathrm{m}} - Mv_{\mathrm{c}}(t)i_{\mathrm{CM}}(t)/2V_{\mathrm{m}} & v_{\mathrm{c}}(t) < 0. \end{cases} \end{aligned} \tag{10}$$

It can be obtained from (10) that the input current of each phase consists of two terms, the first term produces the fundamental component and the second term produces the low-order harmonics, which seriously affects input current THD. Moreover, with the increase of load current, the effect of CM current on input current THD becomes slight. Therefore, the effect is obvious under the light load conditions. As it is difficult to get accurate expressions of the input currents and the dc-link currents when the lumped parasitic capacitances are considered, these currents are analyzed by computer simulation.

Fig. 11 shows the simulation results of the key waveforms of the conventional 3ph-BR in one input voltage period when load power is 200 W and the lumped parasitic capacitances of $C_{\text{P-G}}$ and $C_{\text{N-G}}$ are 500 pF. It can be seen from Fig. 11 that the input currents have obvious distortion. The ripples of input currents i_{a}, i_{b}, and i_{c} in Fig. 11 are larger than those in Fig. 9(a). Current i_{CM} varies with a frequency three times that of the ac input frequency. Moreover, due to the effect of CM currents, the dc-link currents have obvious distortion, and they are not consistent in one input voltage period.

Fig. 12 shows the simulation results of the key waveforms of the conventional 3ph-BR in one switching period of sector 2. It can be seen from Fig. 12 that due to the influence of CM current, the input currents and the dc-link currents have obvious distortion. Moreover, the upper side dc-link current i_{LP} and the lower side dc-link current i_{LN} do not have the same charging or discharging state. Besides, the peak-to-peak value of current i_{LP} is different from that of current i_{LN}. Therefore, it can be obtained that although the same SLO modulation scheme is used, the parasitic capacitances affect the operation modes of the conventional 3ph-BR in each switching period, which results in serious distortion of input currents and dc-link currents.

Fig. 13 shows the fast Fourier transform (FFT) analysis results of input current in the conventional 3ph-BR with lumped parasitic capacitances when load power is 200 W. It can be seen from Fig. 13(a) that the harmonic component of switching frequency in the input current is obvious. Fig. 13(b) shows the distribution of low-order harmonic components of the input current. It can also be seen that there are obvious fifth and seventh harmonics in the input current.

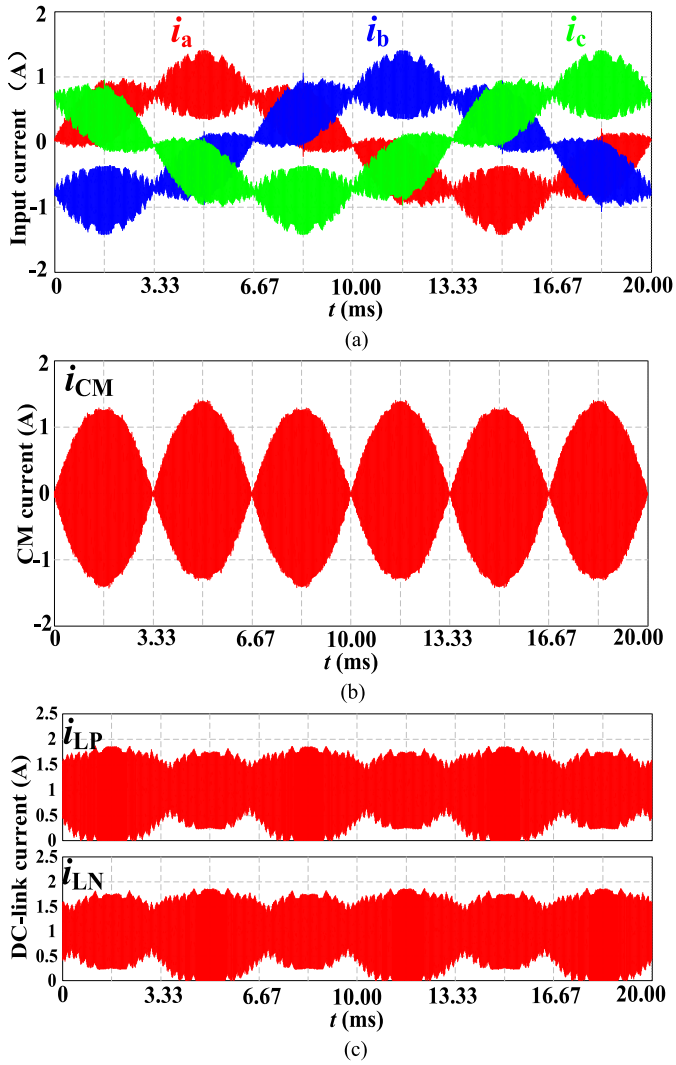

Fig. 11. Simulation results of the key waveforms of the conventional 3ph-BR with the lumped parasitic capacitances under 200 W load in one input voltage period. (a) Three-phase input currents. (b) CM current. (c) DC-link current i_{LP} and i_{LN}.

IV. Improvement of the 3ph-BR

A. Modified 3ph-BR

Due to the distributed parasitic capacitances, the CM currents in the high-density 3ph-BR will affect the input current THD, especially under light load conditions. To reduce the input current THD, a modified 3ph-BR is proposed, as shown in Fig. 14. In the modified 3ph-BR, only the common point (M) of C_{p} and C_{n} is connected to the neutral point N of input filter capacitances. Besides, the output capacitance C_{p}, C_{n} and dc-link inductance L_{p}, L_{n} should be split symmetrically to provide symmetric attenuation impedances for conducted CM noise, i.e., $L_{\mathrm{p}} = L_{\mathrm{n}}$

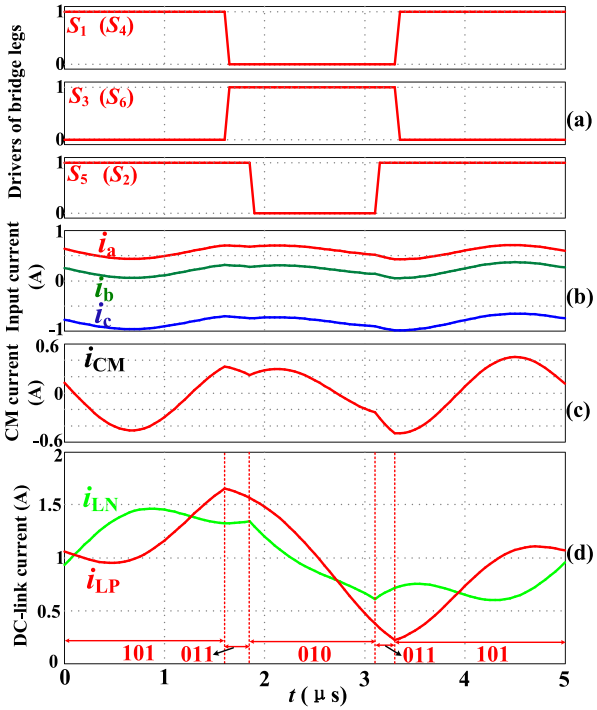

Fig. 12. Simulation results of the key waveforms of the conventional 3ph-BR with the lumped parasitic capacitances in one switching period of sector 2 when load power is 200 W. (a) Drive signals of the bridge legs. (b) Three-phase input currents. (c) CM current. (d) DC-link current i_{LP} and i_{LN}.

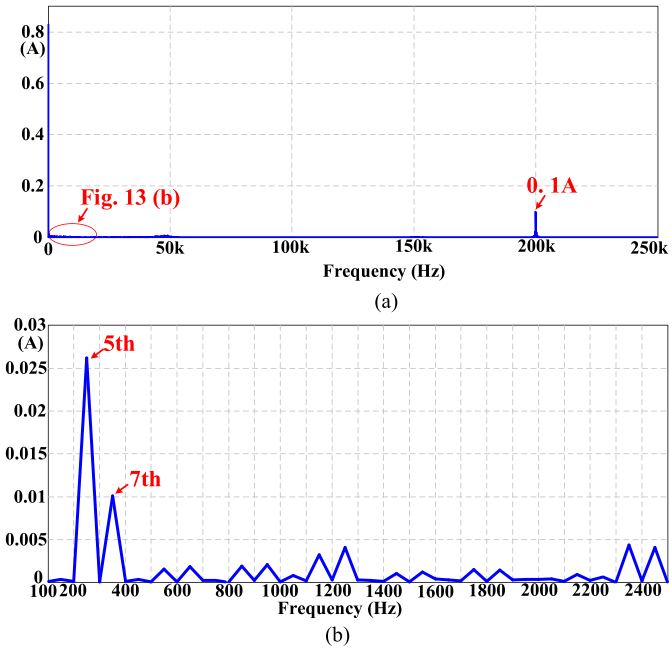

Fig. 13. FFT analysis results of input current in the conventional 3ph-BR with the lumped parasitic capacitances under 200 W load. (a) Input current spectrum in the range of 0–250 kHz. (b) Input current spectrum in the range of 0–2.5 kHz.

and $C_{\mathrm{p}} = C_{\mathrm{n}}$. The reduction of input current THD of the modified 3ph-BR is guaranteed by the hardware circuit, not affected by the modulation scheme. Thus, the SLO modulation scheme can also be applied to the modified 3ph-BR.

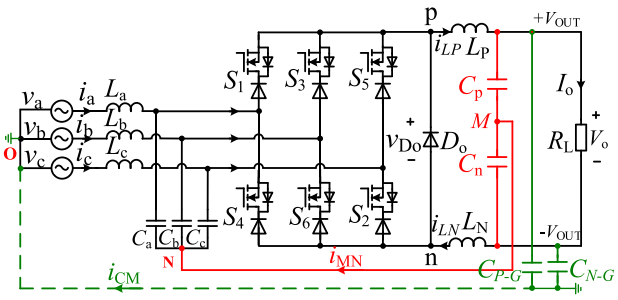

Fig. 14. Modified 3ph-BR with the lumped parasitic capacitances.

When the lumped parasitic capacitances are considered, the modified 3ph-BR can provide a low-impedance path for high-frequency CM currents by connecting the neutral point (N) to the common point (M) of two output capacitances. Thus, CM current circulates internally, rather than flowing to the ac input side. In other words, the lumped parasitic capacitances are bypassed by these two output capacitances, and CM currents flow from M to N, rather than from the common point of two lumped parasitic capacitances to O, which means that i_{CM} is 0. Therefore, input current THD of the modified 3ph-BR can be reduced compared with that of the conventional 3ph-BR.

B. *Operation Modes of the Modified 3ph-BR*

For the modified 3ph-BR, there are three current paths in each operation mode. Fig. 15 shows these three current paths in the three operation modes in sector 2. Current path 1 is low-frequency current path. Load current I_{o} flows through this path to realize power transfer from ac input to dc output and ensure sinusoidal ac input current. Current path 2 and current path 3 are current paths for CM currents, respectively.

In mode 101, as shown in Fig. 15(a), bridge legs S_1 and S_2 are turned ON, diode D_{o} is turned OFF as it withstands reverse voltage. Input voltage sources of phase *A* and phase *C* supply power to the load through S_1, S_2, L_{P} and L_{N}. S_1, L_{P}, C_{p}, and C_{a} provide current flowing path for current i_{Cp}, while S_2, L_{N}, C_{n}, and C_{c} provide current flowing path for current i_{Cn}.

In mode 011, as shown in Fig. 15(b), bridge legs S_3 and S_2 are turned ON, diode D_{o} is turned OFF as it withstands reverse voltage. Input voltage sources of phase *B* and phase *C* supply power to the load through S_3, S_2, L_{P} and L_{N}. S_3, L_{P}, C_{p}, and C_{b} provide current flowing path for current i_{Cp}, while S_2, L_{N}, C_{n}, and C_{c} provide current flowing path for current i_{Cn}.

In mode 010, as shown in Fig. 15(c), bridge legs of phase *A* and phase *C* are turned OFF, diode D_{o} is turned ON to provide a current flowing path for load current I_{o}. S_3 and S_6 of phase B are turned ON to provide current flowing paths for currents i_{Cp} and i_{Cn}.

For the modified 3ph-BR with the lumped parasitic capacitances, high-frequency CM currents circulate through path 2 and 3, respectively, and only input current flows to output through path 1. Hence, three-phase input currents follow three-phase input voltages without harmonic currents. Input currents are independent of CM currents, which result in the high-quality input currents.

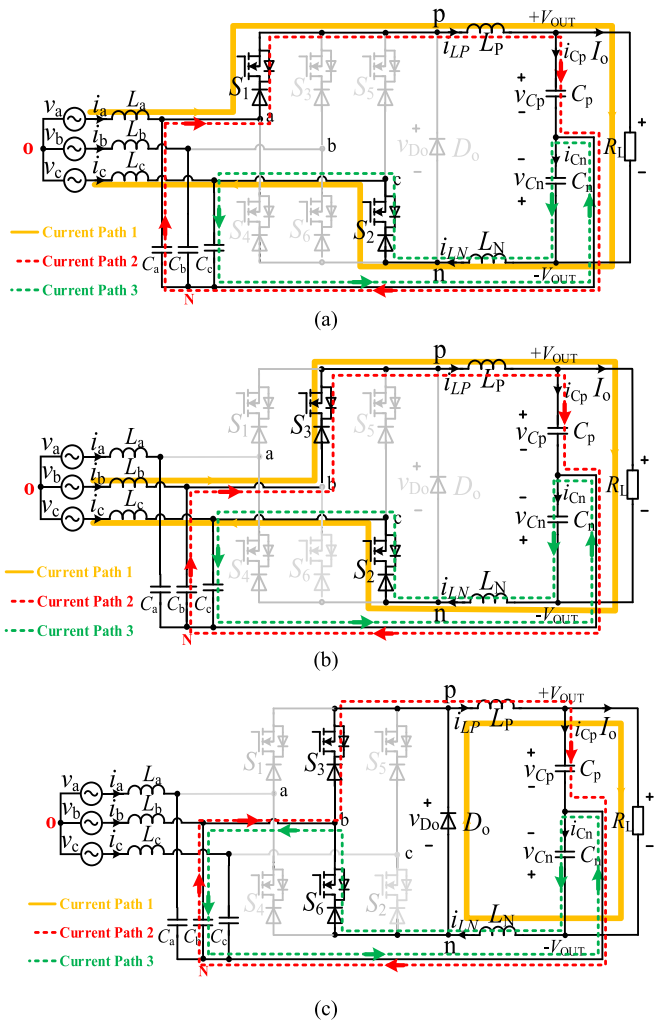

Fig. 15. Current paths of the modified 3ph-BR in three operation modes in sector 2. (a) Mode 101. (b) Mode 011. (c) Mode 010.

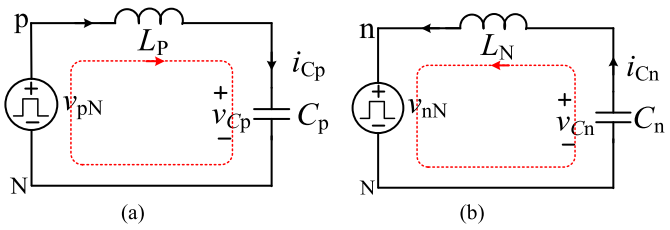

Fig. 16. Equivalent current ripple paths for the modified 3ph-BR. (a) Current ripple path of i_{LP}. (b) Current ripple path of i_{LN}.

C. Output Capacitance Voltage Ripple

The equivalent current ripple paths of i_{LP} and i_{LN} for the modified 3ph-BR can be obtained, as shown in Fig. 16. Voltages v_{pN} and v_{nN} are given in Table II, where v_{pN} and v_{nN} are dependent on the PWM sequences of each sector. When capacitances C_{p} and C_{N} are large enough, the ripple of the capacitance voltage is almost zero. It can be considered that the voltage rating of both output capacitances is $V_{\mathrm{o}}/2$.

Considering the size and weight of the power supply, C_{p} and C_{N} are usually selected to be small. In this case, the output capacitance voltage has low-frequency ripple due to the low-frequency

TABLE IV
VOLTAGES ACROSS OUTPUT CAPACITORS IN 12 SECTORS

Sector	v_{Cp}	v_{Cn}
1,2	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{a}}^2(t)-v_{\mathrm{a}}(t)v_b(t)\right)+v_b(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{c}}^2(t)-v_{\mathrm{c}}(t)v_b(t)\right)+v_b(t)$
3,4	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{b}}^2(t)-v_{\mathrm{a}}(t)v_b(t)\right)+v_{\mathrm{a}}(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{c}}^2(t)-v_{\mathrm{c}}(t)v_{\mathrm{a}}(t)\right)+v_{\mathrm{a}}(t)$
5,6	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{b}}^2(t)-v_{\mathrm{c}}(t)v_b(t)\right)+v_{\mathrm{c}}(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{a}}^2(t)-v_{\mathrm{c}}(t)v_{\mathrm{a}}(t)\right)+v_{\mathrm{c}}(t)$
7,8	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{c}}^2(t)-v_{\mathrm{c}}(t)v_b(t)\right)+v_{\mathrm{b}}(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{a}}^2(t)-v_{\mathrm{b}}(t)v_{\mathrm{a}}(t)\right)+v_b(t)$
9,10	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{c}}^2(t)-v_{\mathrm{c}}(t)v_{\mathrm{a}}(t)\right)+v_{\mathrm{a}}(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{b}}^2(t)-v_{\mathrm{b}}(t)v_{\mathrm{a}}(t)\right)+v_{\mathrm{a}}(t)$
11,12	$\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{a}}^2(t)-v_{\mathrm{c}}(t)v_{\mathrm{a}}(t)\right)+v_{\mathrm{c}}(t)$	$-\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{b}}^2(t)-v_{\mathrm{c}}(t)v_{\mathrm{b}}(t)\right)+v_{\mathrm{c}}(t)$

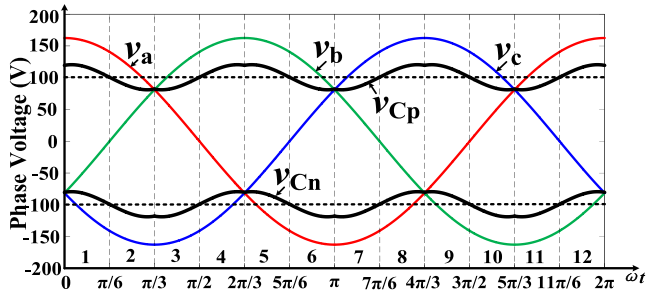

Fig. 17. v_{a}, v_{b}, v_{c}, v_{Cp}, and v_{Cn} in one input voltage period.

fluctuation of voltages v_{pN} and v_{nN}. In order to simplify the analysis, it is assumed that only high-frequency current ripples flow through capacitances C_{p} and C_{N}. Therefore, the low-frequency fluctuation of voltages v_{Cp} and v_{Cn} are the largest, which means that the voltage rating of the output capacitances is maximum.

In each switching period, the voltages across capacitances C_{p} and C_{n} can be considered to be constant and are equal to the average voltages of v_{pN} and v_{nN}. According to Table II, v_{Cp} and v_{Cn} in sector 2 are

$$\begin{aligned} v_{\mathrm{Cp}}(t) &= \bar{v}_{\mathrm{pN}} = v_{\mathrm{a}}(t)D_{101} + v_{\mathrm{b}}(t)(D_{010}+D_{011}) \\ &= \frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{a}}^2(t) - v_{\mathrm{a}}(t)v_{\mathrm{b}}(t)\right) + v_{\mathrm{b}}(t) \quad t \in \left(\frac{\pi}{6}, \frac{\pi}{3}\right) \end{aligned} \tag{11}$$

$$\begin{aligned} v_{\mathrm{Cn}}(t) &= \bar{v}_{\mathrm{nN}} = v_{\mathrm{b}}(t)D_{010} + v_{\mathrm{c}}(t)(D_{101}+D_{011}) \\ &= -\frac{M}{V_{\mathrm{m}}}\left(v_{\mathrm{c}}^2(t) - v_{\mathrm{c}}(t)v_{\mathrm{b}}(t)\right) + v_{\mathrm{b}}(t) \qquad t \in \left(\frac{\pi}{6}, \frac{\pi}{3}\right). \end{aligned} \tag{12}$$

Similarly, voltages v_{Cp} and v_{Cn} in other sectors can be carried out, as given in Table IV. Fig. 17 shows v_{Cp} and v_{Cn} in one input voltage period. It can also be seen that v_{Cp} and v_{Cn} vary with a frequency three times that of the ac input frequency and the average voltages of v_{Cp} and v_{Cn} are half of the output voltage. Moreover, according to (11) and (12), it can be obtained that $v_{\mathrm{Cp}} + v_{\mathrm{Cn}} = V_{\mathrm{o}}$, which means that the output voltage remains constant and independent of the output capacitance voltage ripple, although the ripples of v_{Cp} and v_{Cn} have obvious low-frequency

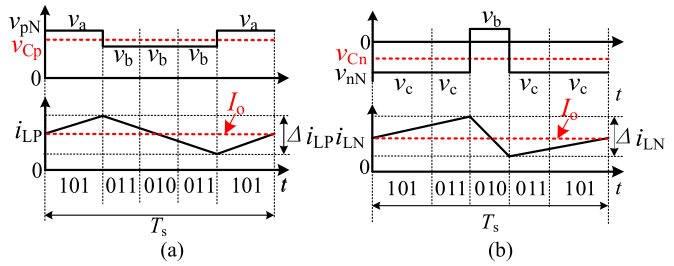

Fig. 18. DC-link current ripples of the modified 3ph-BR in one switching period in sector 2. (a) Voltages across inductor L_P and current i_{LP}. (b) Voltages across inductor L_N and current i_{LN}.

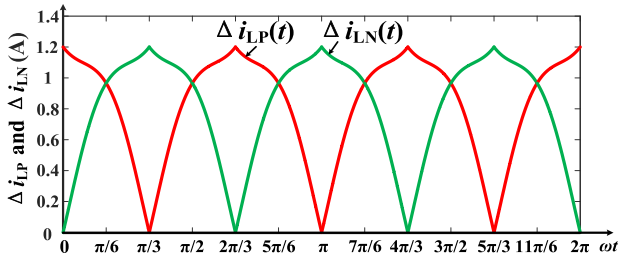

Fig. 19. Δi_{LP} and Δi_{LN} of the modified 3ph-BRin one input voltage period.

variation. Besides, according to Fig. 17, in the transition process from even sector to odd sector, the low-frequency voltage ripple of output capacitance is the largest. Therefore, the maximum voltage across capacitances C_p and C_N can be expressed as

$$v_{Cp\_MAX} = v_{Cn\_MAX} = V_o - V_m/2. \tag{13}$$

D. DC-Link Current Ripple

From (11), (12), and Table II, the voltages across inductors L_P and L_N can be known, and thus, the charging and discharging state of inductors L_P and L_N in each mode can be obtained, as given in Fig. 18. It can also be known that dc-link inductors L_P and L_N withstand different voltages when the operation mode is the same, which leads to different charging or discharging states.

Δi_{LP} and Δi_{LN} in sector 2 are

$$\Delta i_{LP}(t) = \frac{v_a(t) - v_{Cp}(t)}{L_P f_s} D_{101}$$
$$= \frac{M v_a(t)}{V_m L_P f_S}\left(1 - \frac{M v_a(t)}{V_m}\right)(v_a(t) - v_b(t)) \quad t \in \left(\frac{\pi}{6}, \frac{\pi}{3}\right) \tag{14}$$

$$\Delta i_{LN}(t) = \frac{v_b(t) - v_{Cn}(t)}{L_N f_s} D_{010}$$
$$= \frac{M v_c(t)}{V_m L_N f_S}\left(1 + \frac{M v_c(t)}{V_m}\right)(v_c(t) - v_b(t)) \quad t \in \left(\frac{\pi}{6}, \frac{\pi}{3}\right). \tag{15}$$

Similarly, Δi_{LP} and Δi_{LN} in other sectors can be calculated, as illustrated in Table V. Fig. 19 shows Δi_{LP} and Δi_{LN} in one input voltage period. Δi_{LP} and Δi_{LN} of the modified 3ph-BR vary obviously with a frequency three times that of the ac input frequency. The phase difference between Δi_{LP} and Δi_{LN} is 180°.

TABLE V
Δi_{LP} AND Δi_{LN} OF THE MODIFIED 3ph-BR IN 12 SECTORS

Sector	Δi_{LP}	Δi_{LN}
1, 2	$\frac{Mv_a(t)}{V_m L_P f_S}\left(1-\frac{Mv_a(t)}{V_m}\right)v_{ab}(t)$	$\frac{Mv_c(t)}{V_m L_N f_S}\left(1+\frac{Mv_c(t)}{V_m}\right)v_{cb}(t)$
3, 4	$\frac{Mv_b(t)}{V_m L_P f_S}\left(1-\frac{Mv_b(t)}{V_m}\right)v_{ba}(t)$	$\frac{Mv_c(t)}{V_m L_N f_S}\left(1+\frac{Mv_c(t)}{V_m}\right)v_{ca}(t)$
5, 6	$\frac{Mv_b(t)}{V_m L_P f_S}\left(1-\frac{Mv_b(t)}{V_m}\right)v_{bc}(t)$	$\frac{Mv_a(t)}{V_m L_N f_S}\left(1+\frac{Mv_a(t)}{V_m}\right)v_{ac}(t)$
7, 8	$\frac{Mv_c(t)}{V_m L_P f_S}\left(1-\frac{Mv_c(t)}{V_m}\right)v_{cb}(t)$	$\frac{Mv_a(t)}{V_m L_N f_S}\left(1+\frac{Mv_a(t)}{V_m}\right)v_{ab}(t)$
9, 10	$\frac{Mv_c(t)}{V_m L_P f_S}\left(1-\frac{Mv_c(t)}{V_m}\right)v_{ca}(t)$	$\frac{Mv_b(t)}{V_m L_N f_S}\left(1+\frac{Mv_b(t)}{V_m}\right)v_{ba}(t)$
11, 12	$\frac{Mv_a(t)}{V_m L_P f_S}\left(1-\frac{Mv_a(t)}{V_m}\right)v_{ac}(t)$	$\frac{Mv_b(t)}{V_m L_N f_S}\left(1+\frac{Mv_b(t)}{V_m}\right)v_{bc}(t)$

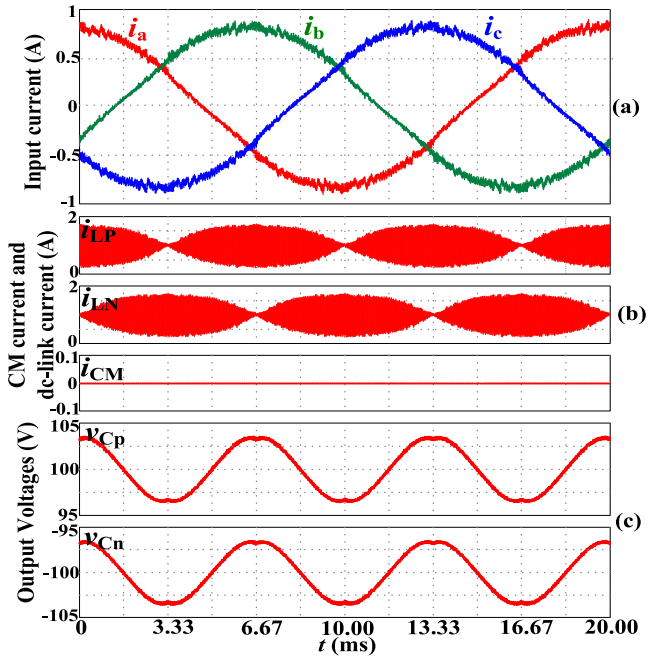

Fig. 20. Simulation results of key waveforms of the modified 3ph-BR with lumped parasitic capacitances in one input voltage period when load power is 200 W. (a) Three-phase input currents. (b) Currents i_{LP}, i_{LN} and i_{CM}. (c) Output voltages v_{Cp} and v_{Cn}.

Figs. 20 and 21 show the simulation results of the key waveforms of the modified 3ph-BR based on the same SLO modulation scheme for 200 W load when the capacitances C_p and C_n are 22 μF, and the lumped parasitic capacitances $C_{P\text{-}G}$ and $C_{N\text{-}G}$ are 500 pF.

Fig. 20 shows the simulation results in one input voltage period. It can be seen from Fig. 20 that the input currents have no obvious distortion; currents i_{LP} and i_{LN} vary with a frequency three times that of ac input frequency. When one inductor current ripple is the largest, the other inductor current ripple is the smallest. Besides, it can be seen from Fig. 20(b) that i_{CM} is almost zero, which means that even though there are parasitic capacitances in the modified 3ph-BR, there is no high-frequency

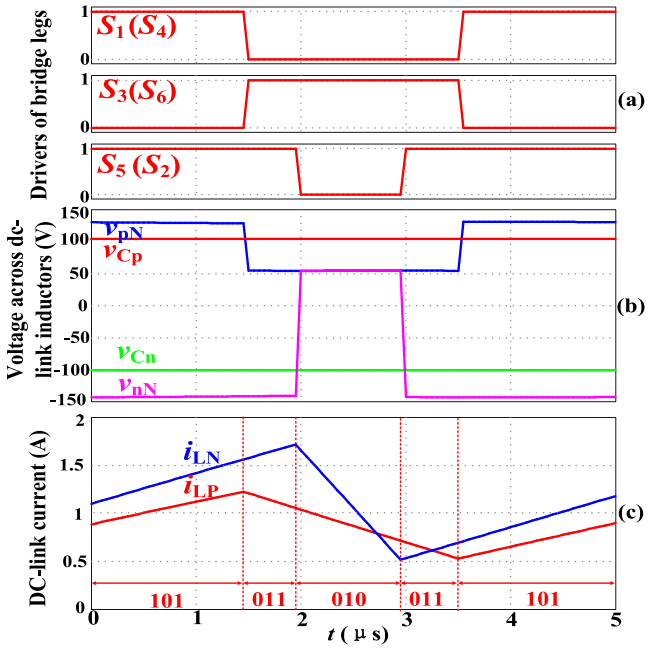

Fig. 21. Simulation results of key waveforms of the modified 3ph-BR in one switching period in sector 2, with the lumped parasitic capacitances under 200 W load. (a) Drives of bridge legs. (b) Voltages across inductor L_N and current i_{LN}. (c) DC-link current i_{LP} and i_{LN}.

CM current flowing to the input side, thus avoiding the pollution of the input currents. Moreover, v_{Cp} and v_{Cn} vary with a frequency three times that of the ac input frequency.

Fig. 21 shows the simulation results in one switching period in sector 2. Fig. 21(b) and (c) is in agreement with the analysis results in Fig. 18. As these two dc-link inductors withstand different voltages, they have different time-domain behaviors in one switching period. Besides, there is no distortion in these two dc-link current ripples.

Fig. 22 shows the FFT analysis results of the input current in the modified 3ph-BR with lumped parasitic capacitances when load power is 200 W. From Fig. 22(a), the switching frequency component in the input current is suppressed significantly, which means that the modified topology can mitigate high-frequency CM noises. Fig. 22(b) shows the distribution of low-order harmonic components of the input current. It can be seen from Fig. 22(b) that the fifth and seventh harmonics in the input current are obviously reduced compared with Fig. 13(b), and thus, a lower input current THD should be obtained.

V. Experimental Verification

A. Implementation of Experimental Prototype

To verify the analysis results of the modified 3ph-BR, a 1-kW experimental prototype of the modified 3ph-BR with standard full-brick size is developed, as shown in Fig. 23. To achieve high density, multilayer thick copper technology is adopted for the PCB layout of the main power supply board. In this application, distributed parasitic capacitances are inevitable. The main circuit parameters of the experimental prototype are given in Table VI. The conventional 3ph-BR is also evaluated by using the same

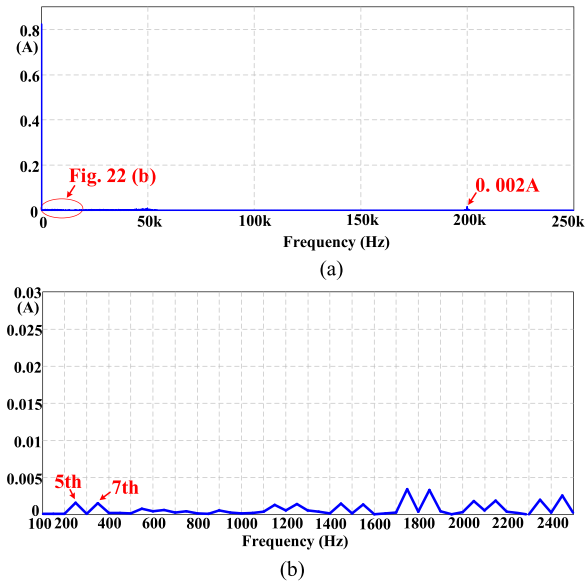

Fig. 22. FFT analysis results of input current in the modified 3ph-BR with lumped parasitic capacitances under 200 W load. (a) Input current spectrum at the range of 250 kHz. (b) Input current spectrum in the range of 2.5 kHz.

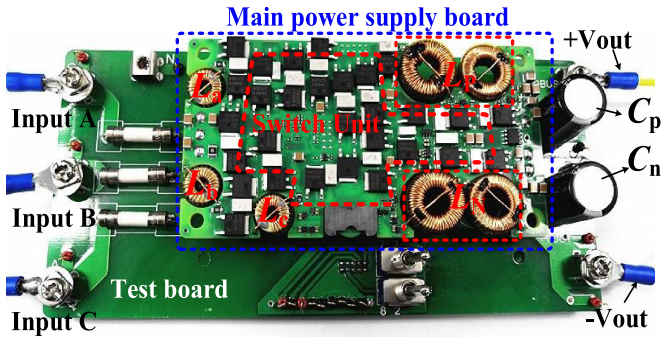

Fig. 23. Experimental prototype of the 3ph-BR. Mechanical dimensions of the main power supply board: 116.8 mm × 61 mm × 12.7 mm.

experimental prototype without connecting the neutral point (N) to the common point (M) of the two output capacitances. Besides, for a fair comparison, the control algorithms of these two prototypes are the same.

B. Experimental Results

Fig. 24(a) and (b) shows experimental results of the three-phase input currents of the conventional 3ph-BR under 20% and 100% of full load, respectively. The CM currents depend only on CM voltage and parasitic capacitances, and they are independent of load. In other words, when the parameters of the prototype are determined, the magnitude of the CM currents will also be determined. With the increase of load, the effect of CM current on input current becomes slight. As shown in Fig. 24(a), when the load is 20% of full load, distortions of three-phase input currents are obvious. However, when the load is heavy, distortions of three-phase input currents are not obvious, and it can be ignored, as shown in Fig. 24(b).

Fig. 25(a) and (b) shows experimental results of the three-phase input currents of the modified 3ph-BR under 20% and

TABLE VI
CIRCUIT PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Quantity	Symbol	Value
Phase voltage	v_a, v_b, v_c	$115V_{rms}$
Input frequency	f_L	50Hz
Output voltage	V_o	200V
Output power	P_o	1kW
Input inductor	L_a, L_b, L_c	50μH
Input capacitance	C_a, C_b, C_c	1μF
Output inductor	L_P, L_N	300μH
Output capacitance	C_p, C_n	22μF
Switching frequency	f_S	200kHz
MOSFET	—	STD18N55M5
Diode	—	STPSC8H065BY-TR

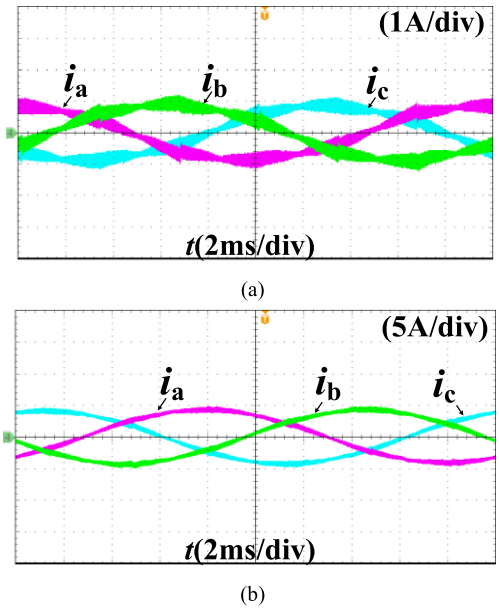

Fig. 24. Experimental results of input currents of the conventional 3ph-BR. (a) 20% of full load. (b) Full load.

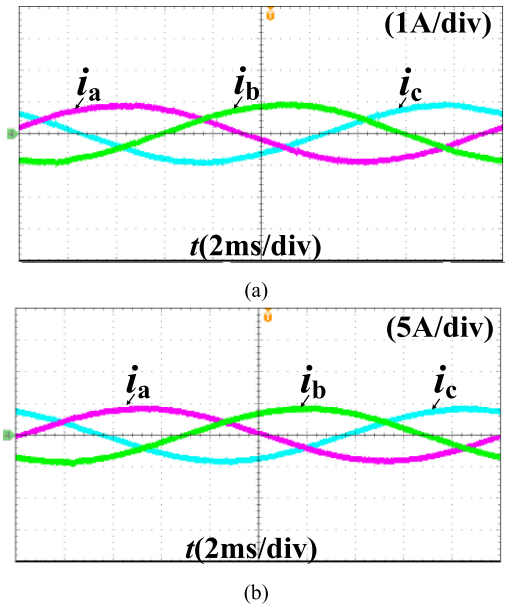

Fig. 25. Experimental results of input currents of the modified 3ph-BR. (a) 20% of full load. (b) Full load.

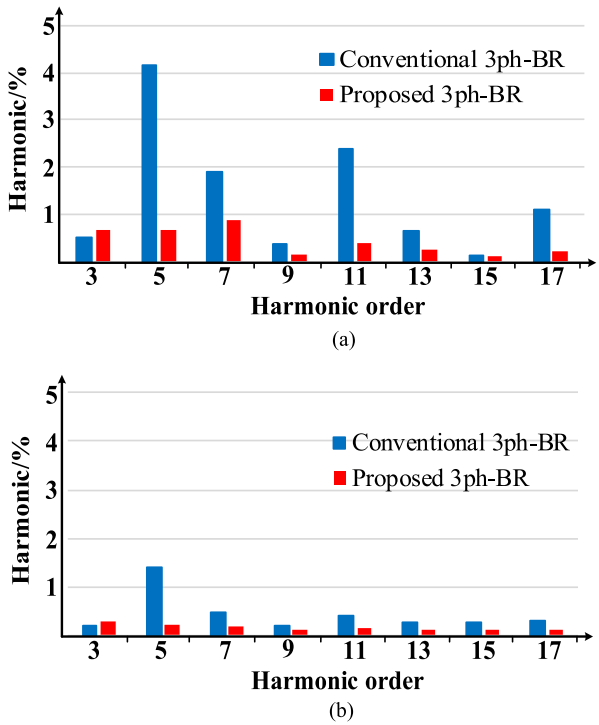

Fig. 26. Measured input current harmonic contents. (a) 20% of full load. (b) Full load.

100% of full load, respectively. It can be seen from Fig. 25(a) and (b) that the distortion of three-phase input currents has been significantly suppressed, both under 20% and 100% of full load.

Fig. 26 shows input current harmonic contents of the conventional 3ph-BR and the modified 3ph-BR under 20% and 100% of full load. Fig. 27 shows the measured input current THD of conventional 3ph-BR and the modified 3ph-BR under different loads. Compared with the conventional 3ph-BR, the input current harmonic contents and the input current THD of the modified 3ph-BR has been significantly reduced under light load conditions.

Fig. 28(a) and (b) shows experimental results of v_a, v_{Cp}, v_{Cn}, and the output voltage V_o of the modified 3ph-BR when the output capacitances are 22 and 2 μF, respectively. From Fig. 28, it can be known that v_{Cp} and v_{Cn} vary with a frequency three times that of the ac input frequency. Moreover, although the voltage ripples of v_{Cp} and v_{Cn} have obvious low-frequency variation, the output voltage remains constant. Comparing Fig. 28(a) with Fig. 28(b), it can be seen that the low-frequency ripple of v_{Cp} and v_{Cn} will decrease with the increase of the output capacitance.

Fig. 29(a) and (b) shows currents i_b, i_c, i_{LP}, and i_{LN} of the conventional 3ph-BR under 20% and 100% of full load. As shown in Fig. 29(a), due to the effect of CM currents, the input currents and the dc-link currents are disturbed irregularly, which are in agreement with Fig. 11(c). However, it can be seen from Fig. 29(b) that with the increase of load, the effect of CM currents

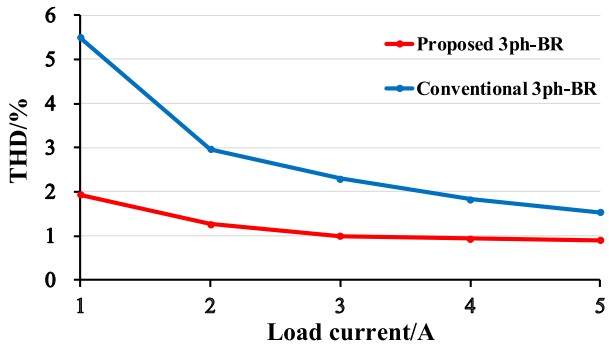

Fig. 27. Measured input current THD.

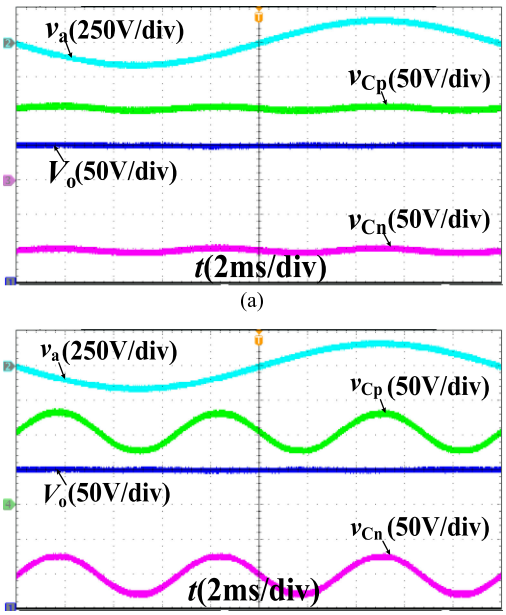

Fig. 28. Experimental results of $v_{\rm a}$, $v_{\rm Cp}$, $v_{\rm Cn}$, and $V_{\rm o}$ of the modified 3ph-BR when (a) $C_{\rm p}$ and $C_{\rm n}$ are 22 μF and (b) $C_{\rm p}$ and $C_{\rm n}$ are 2 μF.

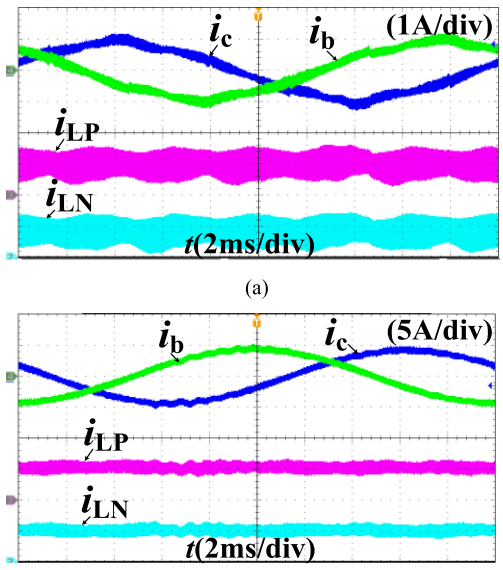

Fig. 29. Experimental results of $i_{\rm b}$, $i_{\rm c}$, $i_{\rm LP}$, and $i_{\rm LN}$ of the conventional 3ph-BR. (a) 20% of full load. (b) Full load.

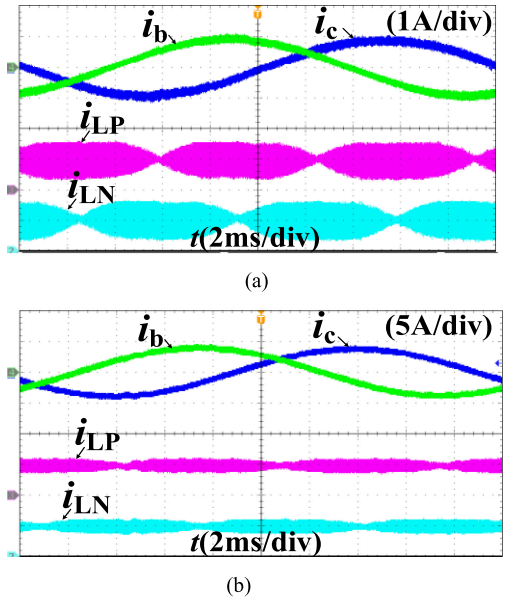

Fig. 30. Experimental results of $i_{\rm b}$, $i_{\rm c}$, $i_{\rm LP}$, and $i_{\rm LN}$ of the modified 3ph-BR. (a) 20% of full load. (b) Full load.

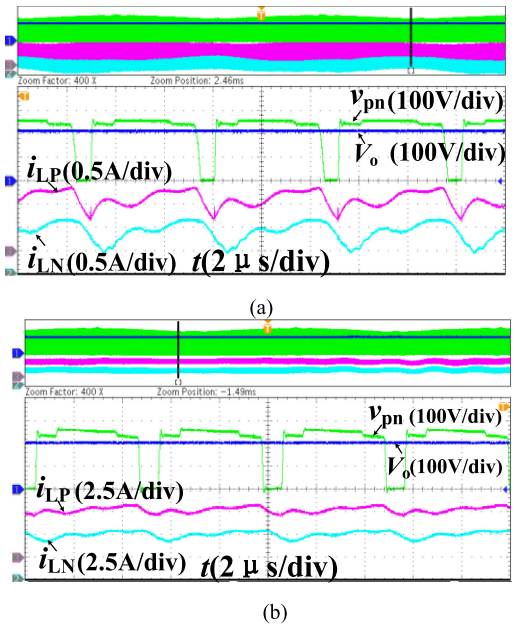

Fig. 31. Detailed waveforms of $v_{\rm pn}$, $V_{\rm o}$, $i_{\rm LP}$, and $i_{\rm LN}$ of the conventional 3ph-BR. (a) 20% of full load. (b) Full load.

on the input currents and the dc-link currents is slight, which can be ignored when the load is heavy enough.

Fig. 30(a) and (b) shows the experimental results of currents $i_{\rm b}$, $i_{\rm c}$, $i_{\rm LP}$, and $i_{\rm LN}$ of the modified 3ph-BR under 20% and 100% of full load, respectively. It can also be known that i_{LP} and i_{LN} vary with a frequency three times that of ac input frequency and the phase difference between these two ripple currents is 180°. In addition, there is almost no low-frequency current disturbance in the input currents.

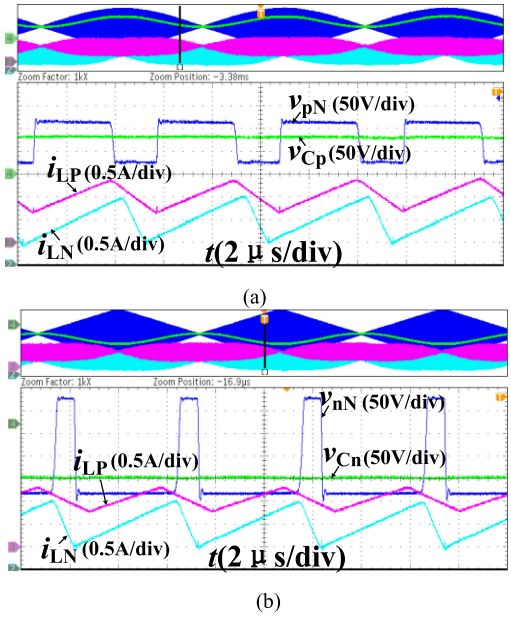

Fig. 32. Detailed waveforms of the modified 3ph-BR. (a) $v_{\rm pN}$, $v_{\rm Cp}$, $i_{\rm LP}$, and $i_{\rm LN}$. (b) $v_{\rm nN}$, $v_{\rm Cn}$, $i_{\rm LP}$, and $i_{\rm LN}$.

Fig. 31(a) and (b) shows the zoomed-in waveforms of the conventional 3ph-BR under 20% and 100% of full load, respectively. It can be seen from Fig. 31 that $v_{\rm pn}$ has a stepped shape, which is in agreement with the analysis of Fig. 7(b). These two dc-link currents have serious distortion, which are in agreement with the simulation waveform of Fig. 12(d). Comparing Fig. 31(a) and (b), it can be seen that when the load increases, the influence of CM currents on the dc-link currents becomes slight. When the load current is large enough, the influence can be ignored.

Fig. 32(a) and (b) shows the zoomed-in waveforms of the modified 3ph-BR under 20% of full load. The experimental results are in agreement with the simulation waveform in Fig. 21. From Fig. 32, it can be obtained that the charging and discharging states of dc-link inductor $L_{\rm P}$ depend on $v_{\rm pN}$ and $v_{\rm Cp}$, while, the charging and discharging states of dc-link inductor $L_{\rm N}$ depend on $v_{\rm nN}$ and $v_{\rm Cn}$. Furthermore, compared with Fig. 31, there is no distortion in these two dc-link current ripples.

VI. Conclusion

In this article, the effect of distributed parasitic capacitance on high-power density 3ph-BR is analyzed. The operation modes and the corresponding current paths of the conventional 3ph-BR with and without distributed parasitic capacitances are studied. For the conventional 3ph-BR, when the switching frequency and power density are high, the parasitic capacitances not only cause EMI interference, but also affect the input current quality, especially under light load conditions. A modified 3ph-BR with reduced input current THD is proposed. The operation modes of the modified 3ph-BR are analyzed. The modified 3ph-BR can suppress high-frequency currents flowing to the input. Therefore, the input current THD can be reduced. In addition, the time-domain behaviors of dc-link currents of the modified 3ph-BR are studied. It is found that two dc-link currents vary periodically with three times the ac input frequency, and the phase difference between two dc-link currents is 180°. A 1-kW experimental prototype with 200 kHz switching frequency and standard full-brick size is built. The experimental results show that the modified 3ph-BR can not only suppress the high-frequency distortion of three input currents, but also obtain a lower input current THD under light load conditions.

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