Letters

An Improved Three-Phase Buck Rectifier With Low Voltage Stress on Switching Devices

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***Abstract*—An improved three-phase buck rectifier (3ph-BR) with low voltage stress on switching devices is proposed in this letter. In the conventional 3ph-BR, the voltage stress on MOSFETs is higher than the amplitude of input phase voltage. However, in the proposed 3ph-BR, the voltage stress on MOSFETs is lower than the amplitude of input phase voltage, which results in reduction of voltage stress on MOSFETs. Therefore, the cost-efficient and low voltage rating MOSFETs with low on-resistance can be utilized, which makes the proposed 3ph-BR suitable for applications that require high-efficiency and high-density. A 1.5-kW experimental prototype of the proposed rectifier is built to verify the analysis results.**

***Index Terms*—High-efficiency, low voltage stress, three-phase buck rectifier (3ph-BR).**

I. Introduction

THREE-PHASE buck rectifier (3ph-BR) and three-phase boost rectifier are two basic three-phase rectifier topologies [1]. Compared with the three-phase boost rectifier, the 3ph-BR not only has a wide output voltage range down to low voltage, but also has small start-up current and ability of short-circuit current limiting [2]. Therefore, the 3ph-BR is widely used in applications such as more electric aircraft (MEA), on-board chargers for electric vehicle (EV), and motor drives for medium-voltage high-power applications [3]–[5].

The conventional 3ph-BR, as shown in Fig. 1, is also known as the current source rectifier (CSR). It consists of six bridge legs and one freewheeling diode. Its each bridge leg includes one MOSFET and one diode in series. The MOSFETs in the conventional 3ph-BR withstand the input line to line voltage. The voltage stress on its MOSFETs is higher than the amplitude of input phase voltage. The high voltage stress not only results in high loss, but also makes selection of MOSFET difficult. Although much

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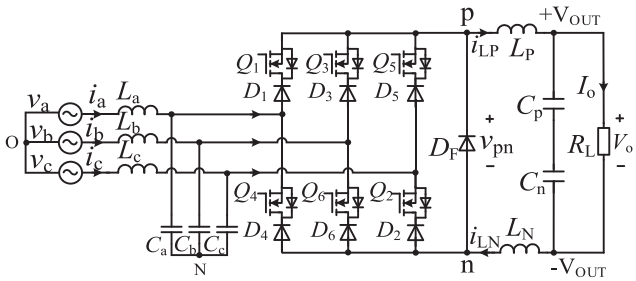


Fig. 1. Conventional 3ph-BR.

efforts in the term of modulation strategies and circuit topologies have been made to improve the efficiency of the 3ph-BR, the MOSFETs still withstand the input line to line voltage [6]–[9]. For $380V_{\rm rms}$ utility grid, the input voltage usually varies in the range of $303V{\sim}456V_{\rm rms}$. To ensure reliable operation of the 3ph-BR, the voltage rating of MOSFET is about two times higher than the voltage stress on the MOSFETs. Therefore, the voltage rating of MOSFETs should be at least 900V or higher.

In many applications, such as MEA and on-board chargers for EV applications, small size and lightweight are necessary. Therefore, the 3ph-BR with high switching frequency and high-density are the key features and the main concerns. The silicon (Si) MOSFETs have excellent performance of small size, low cost, and fast switching performance, which provide opportunities to implement high-efficiency three-phase rectifiers with high switching frequency. However, when their voltage ratings are higher than 650V, their on-resistances are large to affect efficiency. IGBTs can achieve higher voltage rating, but their switching performance is poor for high switching frequency operation. Silicon carbide (SiC) MOSFETs have higher voltage rating with outstanding switching performance, but they are expensive compared with the Si MOSFETs. Therefore, reducing the voltage stress on MOSFET is important for the efficiency improvement and device selection of the 3ph-BR with high switching frequency and high-density.

In this letter, an improved 3ph-BR with low voltage stress on switching devices is proposed, as shown in Fig. 2. The corresponding modulation strategy is also introduced. With the proposed topology and the corresponding modulation strategy, the voltage stress on MOSFETs is lower than the amplitude of input phase voltage. Thus, high-performance Si MOSFETs with low

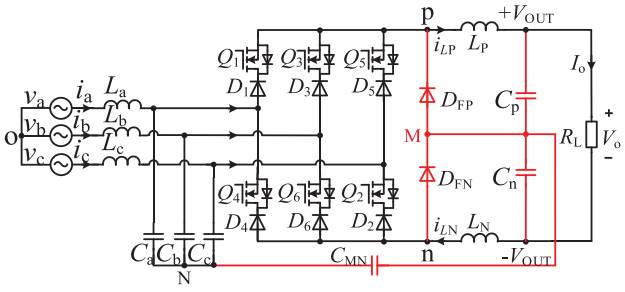


Fig. 2. Proposed 3ph-BR.

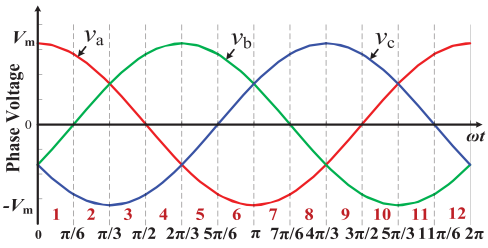


Fig. 3. Three-phase ac input voltages with 12 sectors.

voltage ratings (lower than 650V) can be utilized for $380V_{\rm rms}$ ac input. Therefore, the proposed 3ph-BR in this letter not only inherits similar operating characteristics as the conventional 3ph-BR but also has the desirable features of low-cost and high-efficiency.

II. The Conventional 3ph-BR

A. Conventional SVPWM Strategy and Operating Modes

Define three-phase ac input voltages as

$$\begin{cases} v_{\rm a}(t) = V_m \cos(2\pi f_L t) \\ v_{\rm b}(t) = V_m \cos(2\pi f_L t - 2\pi/3) \\ v_{\rm c}(t) = V_m \cos(2\pi f_L t + 2\pi/3) \end{cases} \quad (1)$$

where $v_{\rm a}$, $v_{\rm b}$, and $v_{\rm c}$ are the instantaneous three-phase ac input voltages, $V_{\rm m}$ is the amplitude of ac input phase voltage, and $f_{\rm L}$ is the frequency of ac input.

The SVPWM modulation strategy for the 3ph-BR with minimum switching loss, also known as switching loss optimized (SLO) modulation strategy [7]–[9], is widely used in the conventional 3ph-BRs. The SLO modulation strategy divides one input voltage period into 12 sectors, as shown in Fig. 3.

Fig. 4(a) and (b) shows the PWM sequences of bridge legs and the voltage $v_{\rm pn}$ across the freewheeling diode $D_{\rm F}$ in one switching period in sector 2 and 3, respectively. It can be known from Fig. 4 that there are three operation modes in one switching period. These operation modes are defined by switching states of the switches in each phase. In sector 2, three operation modes follow the order 101 → 011 → 010 → 011 → 101, where "1" denotes ON-state of MOSFET, and "0" denotes OFF-state of MOSFET. For example, in mode 101, MOSFETs of phases A and C are turned ON, and MOSFETs of phase B are turned OFF.

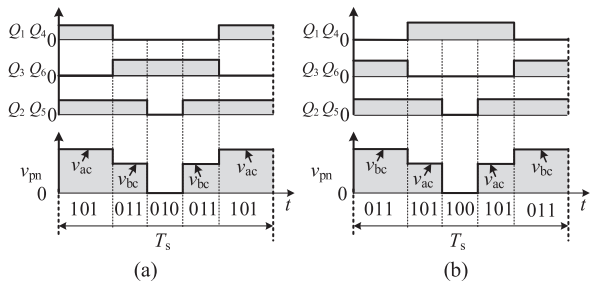


Fig. 4. PWM sequences of MOSFET's and the voltage $v_{\rm pn}$ across $D_{\rm F}$ in one switching period. (a) Sector 2 ($v_{\rm a} > v_{\rm b} > 0 > v_{\rm c}$). (b) Sector 3 ($v_{\rm b} > v_{\rm a} > 0 > v_{\rm c}$).

TABLE I
VOLTAGE STRESSES FOR ALL THE SWITCHING DEVICES OF THE CONVENTIONAL 3ph-BR IN SECTOR 2

	101	011	010
$v_{\rm Q1}$	0	$v_{\rm a}$-$v_{\rm b}$	$v_{\rm a}$-$v_{\rm b}$
$v_{\rm Q2}$	0	0	$v_{\rm b}$-$v_{\rm c}$
$v_{\rm Q3}$	0	0	0
$v_{\rm Q4}$	0	0	0
$v_{\rm Q5}$	0	0	0
$v_{\rm Q6}$	0	0	0
$v_{\rm D1}$	0	0	0
$v_{\rm D2}$	0	0	0
$v_{\rm D3}$	$v_{\rm b}$-$v_{\rm a}$	0	0
$v_{\rm D4}$	$v_{\rm c}$-$v_{\rm a}$	$v_{\rm c}$-$v_{\rm a}$	$v_{\rm b}$-$v_{\rm a}$
$v_{\rm D5}$	$v_{\rm c}$-$v_{\rm a}$	$v_{\rm c}$-$v_{\rm b}$	$v_{\rm c}$-$v_{\rm b}$
$v_{\rm D6}$	$v_{\rm c}$-$v_{\rm b}$	$v_{\rm c}$-$v_{\rm b}$	0
$v_{\rm pn}$	$v_{\rm a}$-$v_{\rm c}$	$v_{\rm b}$-$v_{\rm c}$	0

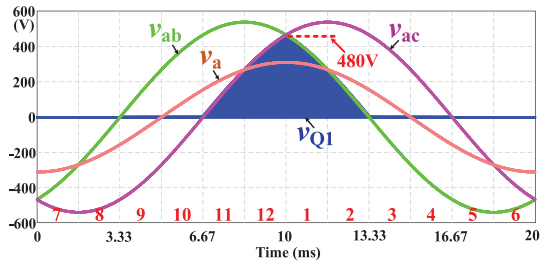


Fig. 5. Simulation results of key waveforms of the conventional 3ph-BR in one input voltage period.

B. Voltage Stress on Switching Devices of the Conventional 3ph-BR

The voltage stresses on all the switching devices in sector 2 are illustrated in Table I, where $v_{{\rm Q}i}$ and $v_{{\rm D}i}$ (i = 1, 2, …, 6) represent the voltage stresses on the MOSFET and diode of each bridge leg respectively. Similarly, voltage stresses on switching devices in other sectors can also be carried out. Fig. 5 shows simulation results of $v_{\rm Q1}$ in one input voltage period. It can be known from Fig. 5 that the voltage stress on Q_1 is higher than the amplitude of input phase voltage. For $380V_{\rm rms}$ input condition, the voltage stress on Q_1 is about 480V. Furthermore, Q_2–Q_6 has the same voltage stress as Q_1. Therefore, considering a certain

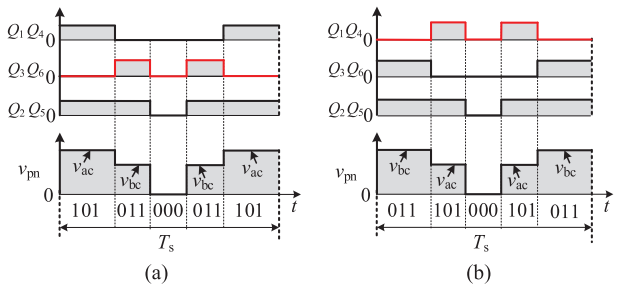


Fig. 6. PWM sequences of MOSFETs and the voltage v_{pn} across D_{FP} and D_{FN} in one switching period for the modified SLO modulation. (a) Sector 2 ($v_a > v_b > 0 > v_c$). (b) Sector 3 ($v_b > v_a > 0 > v_c$).

voltage margin, it is necessary to select MOSFET of the bridge leg with 900V or higher voltage rating.

III. The Proposed 3ph-BR

To reduce the voltage stress on the MOSFETs, an improved 3ph-BR is proposed, as shown in Fig. 2. In the proposed 3ph-BR, the freewheeling diode D_F in the conventional 3ph-BR is split into two diodes D_{FP}, and D_{FN}, in series. The common point of D_{FP} and D_{FN} are connected to the common point M of C_p and C_n. Furthermore, a small capacitance C_{MN} is inserted between M and the neutral point N of input filter capacitances.

A. Modified SVPWM Strategy and Operating Modes

For the proposed 3ph-BR, the SLO modulation should be modified in the term of PWM patterns. It should be noted that modes 010 and 100 in conventional SLO modulation are changed to mode 000 in the modified SLO modulation. In mode 000, the MOSFETs in all the bridge legs are turned OFF, as shown in Fig. 6.

The three operation modes of the modified SLO modulation in sector 2 follow the order 101 → 011 → 000 → 011 → 101. Similarly, the three operation modes in sector 3 follow the order 011 → 101 → 000 → 101 → 011. For other sectors, similar modifications are required. However, the sector identification and vector selection of SLO modulation can still be applied in the proposed 3ph-BR without change.

B. Voltage Stress on Switching Devices of the Proposed 3ph-BR

The voltage stresses on all the switching devices of the proposed 3ph-BR in sector 2 are illustrated in Table II. Compared with Table I, the voltages across the MOSFETs Q_1–Q_6 and the serial diodes D_1-D_6 in mode 000 depend on the corresponding input phase voltages and the voltage v_{MN}, which are significantly different from that of the conventional 3ph-BR in mode 010. However, in modes 101 and 011, the voltages across the MOSFETs and their serial diodes are the same as that in the conventional 3ph-BR.

To calculate voltage v_{MN}, the equivalent current ripple paths of i_{LP} and i_{LN} in the proposed 3ph-BR are provided, as shown in Fig. 7. When the capacitors C_p and C_n are large enough, the voltage of both output capacitances is $V_o/2$. Voltages v_{pN} and

TABLE II
Voltage Stresses for All the Switching Devices of the Proposed 3ph-BR in Sector 2

	101	011	000
v_{Q1}	0	v_a-v_b	v_a-v_{MN}
v_{Q2}	0	0	v_{MN}-v_c
v_{Q3}	0	0	v_b-v_{MN}
v_{Q4}	0	0	0
v_{Q5}	0	0	0
v_{Q6}	0	0	0
v_{D1}	0	0	0
v_{D2}	0	0	0
v_{D3}	v_b-v_a	0	0
v_{D4}	v_c-v_a	v_c-v_a	v_{MN}-v_a
v_{D5}	v_c-v_a	v_c-v_b	v_c-v_{MN}
v_{D6}	v_c-v_b	v_c-v_b	v_{MN}-v_b
v_{DFP}	v_a-v_{MN}	v_b-v_{MN}	0
v_{DFN}	v_{MN}-v_c	v_{MN}-v_c	0

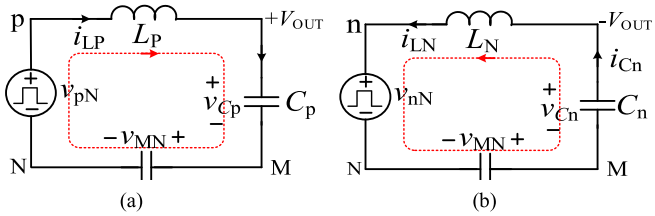


Fig. 7. Equivalent current ripple paths for the proposed 3ph-BR. (a) Current ripple path of i_{LP}. (b) Current ripple path of i_{LN}.

TABLE III
V_{PN}, V_{NN}, V_{CP}, V_{CN}, and δ_i of the Proposed 3ph-BR in One Switching Period

Sector	Mode	v_{Cp}	v_{Cn}	v_{pN}	v_{nN}	δ_i
2	101	$V_o/2$	$V_o/2$	v_a	v_c	$Mv_a/2V_m$
	011	$V_o/2$	$V_o/2$	v_b	v_c	$Mv_b/2V_m$
	000	$V_o/2$	$V_o/2$	v_{MN}	v_{MN}	$1+Mv_c/V_m$
	011	$V_o/2$	$V_o/2$	v_b	v_c	$Mv_b/2V_m$
	101	$V_o/2$	$V_o/2$	v_a	v_c	$Mv_a/2V_m$

v_{nN} are given in Table III, where v_{pN} and v_{nN} are dependent on the PWM sequences of each sector. In Table III, δ_i ($i = 101, 011, 000$) is the duty ratio of each mode in one switching period, which can be obtained in [7] and [8], M is the modulation ratio of the rectifier, and

$$M = \frac{2}{3}\frac{V_o}{V_m} \tag{2}$$

where V_o is the output voltage of the converter, and $M \in (0, 1)$.

The capacitance C_{MN} is used to provide a low impedance path for high-frequency ripple currents. When the capacitance C_{MN} is small, the voltage across the capacitance C_{MN} has low-frequency ripple due to the low-frequency fluctuation of v_{pN} and v_{nN}. According to Table III, v_{MN} in sector 2 is calculated as

$$\begin{aligned} v_{MN}(t) &= 2v_a(t)\delta_{101} + 2v_b(t)\delta_{011} - V_o/2 \\ &= \frac{M}{V_m}\left(v_a^2(t) + v_b^2(t)\right) - V_o/2 \quad t \in (\frac{\pi}{6}, \frac{\pi}{3}) \end{aligned} \tag{3}$$

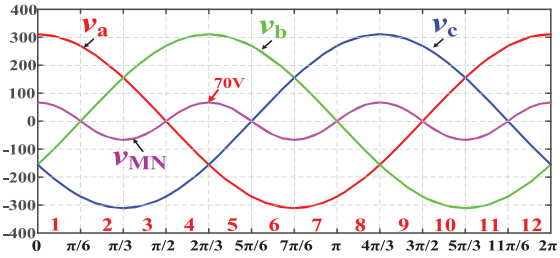


Fig. 8. Calculated v_{MN} in one input voltage period.

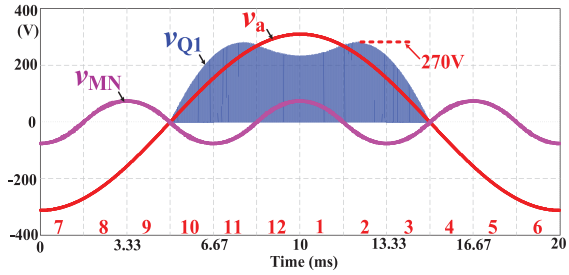


Fig. 9. Simulation results of key waveforms of the proposed 3ph-BR in one input voltage period.

Similarly, v_{MN} in other sectors can be carried out. Fig. 8 shows calculated v_{MN} in one input voltage period. It can be known from Fig. 8 that v_{MN} varies with a frequency of three times that of ac input frequency, and the amplitude of v_{MN} is about 70V.

Fig. 9 shows simulation results of the proposed 3ph-BR with the modified SLO strategy in one input voltage period. It can be known from Fig. 9 that for $380V_{\mathrm{rms}}$ ac input, the maximum voltage across Q_1 is 270V, which is lower than the amplitude of ac input phase voltage. Besides, v_{MN} is in agreement with the calculated waveform. Therefore, consider a certain voltage margin, the MOSFET with the voltage rating of 600V is enough for the application with $380V_{\mathrm{rms}}$ ac input.

From Fig. 9 and Fig. 5 it can be known that the voltage stresses of MOSFETs in the proposed 3ph-BR are obviously reduced, but it does not mean that the voltage across MOSFETs in the proposed topology is always lower than that in the conventional 3ph-BR. As an example, Fig. 10 shows simulation results of the voltage across Q_1 in sector 2. It can be known that the voltage across Q_1 in the conventional 3ph-BR is lower than that in the proposed 3ph-BR. In addition, for the conventional 3ph-BR, the maximum voltage across Q_1 appears during the transition from sector 12 to 1. While in the proposed 3ph-BR, the maximum voltage across Q_1 occurs in sector 2.

It should be noted that the voltage stress on the diodes D_1-D_6 in the bridge legs of the proposed topology is the same as that in the conventional topology, which is equal to the input line to line voltage, as shown in Fig. 11(a) and (b).

IV. Comparative Analysis of Power Loss

The power loss of the switching device mainly consists of the conduction loss and the switching loss. The conduction loss depends on the voltage drop of the device and the current

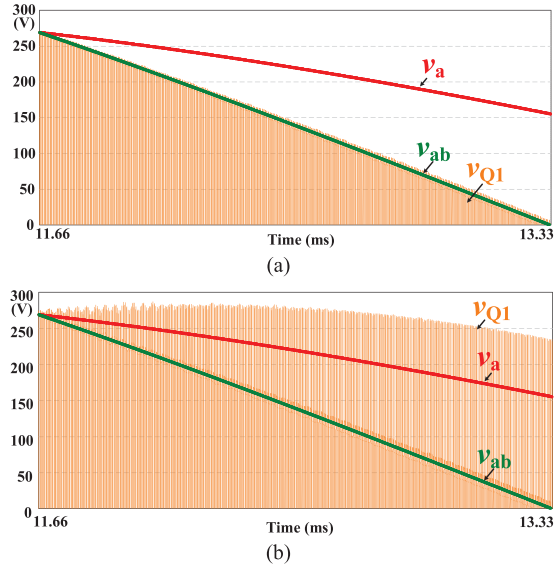


Fig. 10. Simulation results of the voltage across Q_1 in sector 2. (a) Conventional 3ph-BR. (b) Proposed 3ph-BR.

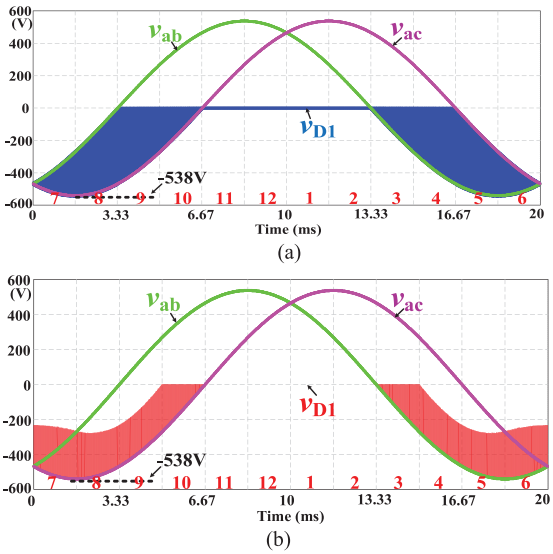


Fig. 11. Simulation results of the voltage across D_1 in one input voltage period. (a) Conventional 3ph-BR. (b) Proposed 3ph-BR.

flowing through it. The switching loss depends on the current flowing through the device and the voltage across it during the switching transition. The switching loss of the 3ph-BR has been well documented [8]–[11]. The dc-link inductor current flowing through the bridge leg is usually assumed constant and equal to the load current I_{o}, the switching loss of the bridge leg has been proved to be in proportional to the voltage across bridge leg, *i.e.*, the proportion between the switching loss and the voltage across bridge leg is a constant coefficient k.

A. Analysis of Conduction Loss

Compared with the conventional 3ph-BR, the proposed 3ph-BR does not change the switch states and conduction time of the

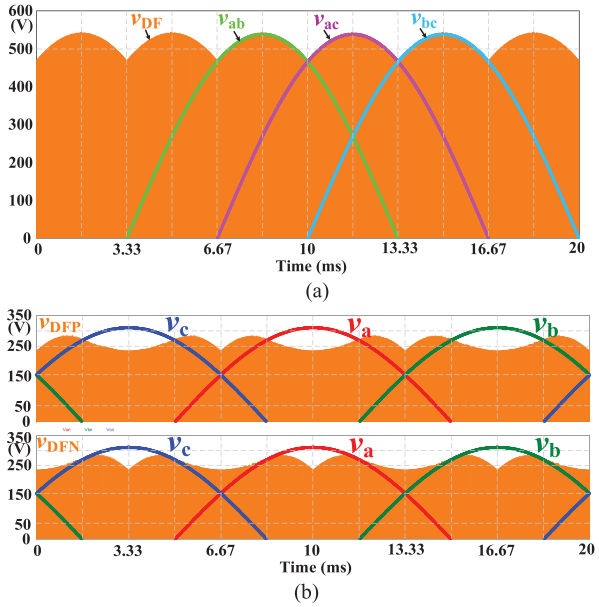


Fig. 12. Simulation results of the voltage across the freewheeling diodes in one input voltage period. (a) Conventional 3ph-BR. (b) Proposed 3ph-BR.

bridge legs, thus the conduction loss of the bridge legs in these two topologies is consistent.

Unlike the conventional 3ph-BR, two freewheeling diodes are required in the proposed 3ph-BR, which will inevitably lead to the increase of conduction loss. However, the increased conduction loss of freewheeling diodes is too small to be ignored [11]. The freewheeling diode in the conventional 3ph-BR always withstands the input line to line voltage, as shown in Fig. 12(a). For $380V_{\rm rms}$ utility grid, a 1200V SiC diode is utilized in the conventional 3ph-BR. For the proposed 3ph-BR, the voltage stress of the two freewheeling diodes is less than the amplitude of the input phase voltage, as shown in Fig. 12(b). Therefore, 600V SiC diodes with low voltage drop can be used to reduce conduction loss.

B. Analysis of Switching Loss

In this section, taking sector 2 as an example, the switching losses of bridge legs in these two topologies are analyzed. From Fig. 4 and Fig. 6, in each switching period of sector 2, the dc-link inductor current only commutates among the upper bridge leg of phases A and B, the lower bridge leg of phase C, and the freewheeling diodes [8]. Although the voltages of MOSFETs or the serial diodes in other bridge legs also vary in sector 2, there is no switching loss in those switching devices. Therefore, only the switching loss in Q_1–Q_3, D_1–D_3, and freewheeling diode need to be compared and analyzed.

According to Tables I and II, the calculation of switching loss in each switching cycle in sector 2 is shown in Table IV. To simplify the analysis of switching loss, the similar method in [8] and [10] is used. When calculating the switching loss, k_1 denotes the proportional coefficient for MOSFETs, k_2 denotes the proportional coefficient for serial diodes, and k_3 denotes the proportional coefficient for freewheeling diodes.

TABLE IV
SWITCHING LOSS IN ONE SWITCHING PERIOD OF SECTOR 2

Switching Devices	Conventional 3ph-BR	Proposed 3ph-BR
Q_1	$k_1I_o(v_a\text{-}v_b)$	$k_1I_o(v_a\text{-}v_b)$
Q_2	$k_1I_o\ (v_b\text{-}v_c)$	$k_1I_o(v_{MN}\text{-}v_c)$
Q_3	0	$k_1I_o(v_b\text{-}v_{MN})$
D_1	0	0
D_2	0	0
D_3	$k_2I_o\ (v_a\text{-}v_b)$	$k_2I_o\ (v_a\text{-}v_b)$
D_F	$k_3I_o\ (v_b\text{-}v_c)$	-
D_{FP}	-	$k_3I_o\ (v_b\text{-}v_{MN})$
D_{FN}	-	$k_3I_o\ (v_{MN}\text{-}v_c)$
The others	0	0
Total switching loss	$k_1I_o(v_a\text{-}v_c) + k_2I_o\ (v_a\text{-}v_b) + k_3I_o\ (v_b\text{-}v_c)$	$k_1I_o(v_a\text{-}v_c) + k_2I_o\ (v_a\text{-}v_b) + k_3I_o\ (v_b\text{-}v_c)$

According to Table IV, the total switching loss in these two topologies in sector 2 is the same. The switching loss in other sectors can be evaluated in a similar way, and they are still the same in 12 sectors. Furthermore, although the proposed 3ph-BR can reduce the voltage stress of the switching devices, it does not mean it can reduce switching loss.

Consider that the increase of conduction loss of the freewheeling diodes is too small to affect the efficiency when the same devices are utilized in two topologies, their efficiency will not be significantly different. However, the proposed 3ph-BR obviously reduces the voltage stress on MOSFETS, and the cost-efficient and low voltage rating MOSFETs with low on-resistance can be utilized. Therefore, the conduction loss of MOSFETs in the proposed 3ph-BR can be reduced significantly.

V. EXPERIMENTAL VERIFICATION

A. Implementation of Experimental Prototype

To verify the analysis results of the proposed 3ph-BR, a 1.5-kW experimental prototype of the proposed 3ph-BR is developed. The conventional 3ph-BR is also evaluated, and the high voltage MOSFET IPD95R750P7 is utilized. In the proposed 3ph-BR, the cost-effective MOSFET IPD60R145CFD7 with lower voltage rating and extremely low on-resistance is adopted. The main circuit parameters of the experimental prototype are given in Table V.

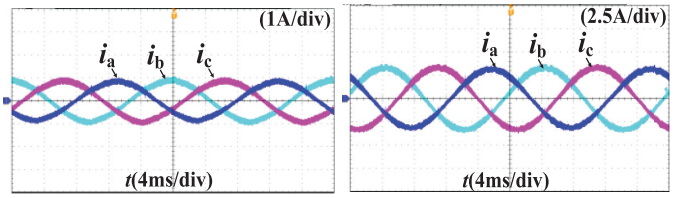
B. Experimental Results

Fig. 13(a) and (b) shows experimental results of three-phase ac input currents of the proposed 3ph-BR under 20% and 100% of full load respectively. From Fig. 13, the proposed 3ph-BR can draw well-balanced and low-distortion sinusoidal currents from each phase of three-phase ac input.

Fig. 14(a) and (b) shows experimental results of the conventional 3ph-BR and the proposed 3ph-BR respectively. From Fig. 14(a), it can be known that the voltage stress on Q_1 in the conventional 3ph-BR is about 480V, which is higher than the amplitude of input phase voltage. For the proposed 3ph-BR, it can be seen from Fig. 14(b) that the maximum voltage across

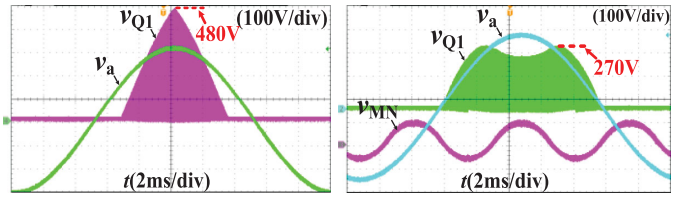
TABLE V
CIRCUIT PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Quantity	Symbol	Value
Phase voltage	v_a, v_b, v_c	$380V_{rms}$ (L-L)
Main frequency	f_L	50Hz
Output voltage	V_o	400V
Output power	P_o	1.5kW
Output inductor	L_P, L_N	300μH
Output capacitance	C_p, C_n	22μF
Capacitance	C_{MN}	0.22μF
Switching frequency	f_S	200kHz
Diode	D_1~D_6, D_F, D_{FP}, D_{FN}	IDM08G120C5
MOSFET (conventional 3ph-BR)	Q_1~Q_6	IPD95R750P7 950V, 750mΩ
MOSFET (proposed 3ph-BR)	Q_1~Q_6	IPD60R145CFD7 600V, 145mΩ



(a) (b)

Fig. 13. Experimental results of input currents of the proposed 3ph-BR, (a) 20% of full load. (b) Full load.



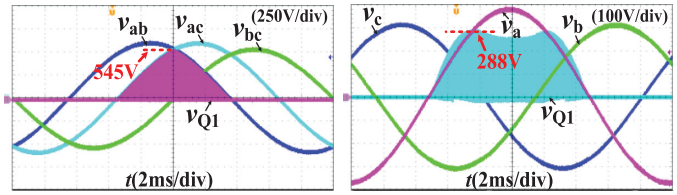
(a) (b)

Fig. 14. Experimental results of the voltage across Q_1 and input voltage of phase A. (a) Conventional 3ph-BR. (b) Proposed 3ph-BR.

on Q_1 is only 270V, which is lower than the amplitude of input phase voltage.

The unbalanced ac input voltages will deteriorate the performance of 3ph-BR. Some control strategies have been reported to improve the performance of the 3ph-BR under unbalanced three-phase ac input conditions [12]–[14]. These control strategies can still be used in this proposed 3ph-BR.

Figs. 15(a) and (b) shows experimental results of the conventional 3ph-BR and the proposed 3ph-BR under unbalanced ac input conditions. It can be seen from Fig. 15 that the proposed 3ph-BR can work reliably under unbalanced ac input conditions. The MOSFETs in the conventional 3ph-BR still withstand the input line to line voltage, i.e., the voltage stress of MOSFETs is higher than the amplitude of input phase voltage. However, the voltage stress on MOSFETs in the proposed 3ph-BR is lower than the amplitude of input phase voltage.



(a) (b)

Fig. 15. Experimental results of the voltage across Q_1 when $v_a = 264V_{rms}$, $v_b = 220V_{rms}$, $v_c = 220V_{rms}$. (a) Conventional 3ph-BR. (b) Proposed 3ph-BR.

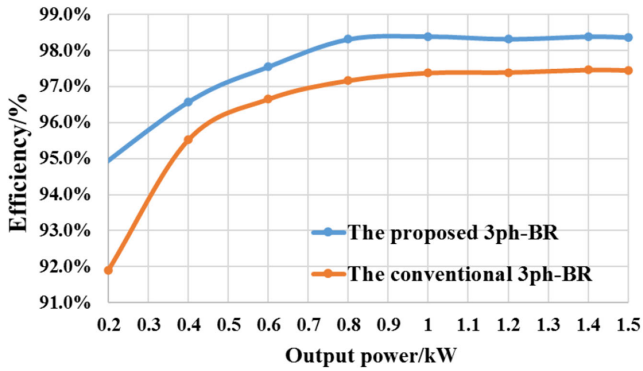


Fig. 16. The efficiency of these two topologies under different loads.

Based on the aforementioned analysis, the efficiency of these two topologies are not significantly different when the same switching devices are utilized. However, considering the safety issue, the high voltage rating MOSFET should be required in the conventional 3ph-BR, while low voltage rating MOSFET can be used in the proposed 3ph-BR. Fig. 16 shows the efficiencies of these two topologies under different loads. Compared with the conventional 3ph-BR with the high voltage rating MOSFETs, the efficiency of the proposed 3ph-BR is improved when the low voltage rating MOSFETs are utilized. The efficiency of the experimental prototype under full load is improved from about 97.3% to 98.4%. Comparing these two MOSFETs, they have similar switching characteristics, but the low voltage rating MOSFET has significantly lower on-resistance. It means that the switching loss of the MOSFETs in the proposed topology is almost the same as that of the conventional topology. But the conduction loss of the proposed topology is much lower than that of the conventional topology. Therefore, it can be considered that the reduction of the conduction loss leads to the improvement of the efficiency of the proposed topology.

VI. CONCLUSION

The MOSFETs in the conventional 3ph-BR withstand the input line to line voltage. An improved 3ph-BR and the modified SLO modulation are proposed in this letter. The voltage stress on MOSFETs in the proposed 3ph-BR is lower than the amplitude of input phase voltage. Therefore, the more cost-efficient MOSFETs with extremely low ON-resistance can be utilized, which results in the improvement of efficiency. The proposed 3ph-BR with low voltage stress on switching devices provides

opportunities to implement 3ph-BR with low-cost and high-efficiency.

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