A Leakage Current Eliminated and Power Oscillation Suppressed Single-Phase Single-Stage Nonisolated Photovoltaic Grid-Tied Inverter and Its Improved Control Strategy

Jianbo Jiang, *Student Member, IEEE*, Shangzhi Pan, *Senior Member, IEEE*, Jinwu Gong, *Member, IEEE*, Fei Liu, *Senior Member, IEEE*, Xiaoming Zha, *Member, IEEE*, and Yizhan Zhuang, *Student Member, IEEE*

***Abstract*—Single-phase single-stage nonisolated photovoltaic (PV) grid-tied inverters mainly suffer from issues of the common-mode leakage current and double-line-frequency power oscillation. Aiming to address these issues, this article designs a new single-phase PV grid-tied inverter with only two switches. The structure of the proposed inverter allows the neutral line of the alternating current (ac) grid to be directly connected to the negative pole of the PV panel so that the common-mode leakage current can be completely eliminated. Additionally, a power decoupling method is proposed to suppress the double-line-frequency power oscillation. Then an improved control strategy is presented in this article to solve the stability problem of the proposed inverter when it is connected to a weak grid. It should be noted that the designed inverter can also output reactive power, achieve zero-voltage switching, track the maximum power point, and step up the input voltage. The validity of the proposed inverter and improved control strategy is verified by simulation and experimental results.**

***Index Terms*—Common-mode leakage current, double-line-frequency power oscillation, photovoltaic (PV) grid-tied inverter, power decoupling method.**

I. Introduction

CLEAN energy generation, such as photovoltaic (PV) generation, is becoming increasingly popular due to its advantages of being pollution free and renewable. The form of PV generation includes large-scale PV plants and small-scale distributed PV generation, in which distributed PV generation is an important part of PV generation. PV generation is direct current (dc), but current utility grids are mainly dominated by alternating current (ac); therefore, an inverter is needed to integrate PV generation into the utility grid. Single-phase single-stage nonisolated inverters, due to their advantages in terms of size, cost, and efficiency, have become the first choice for distributed PV grid-connected applications [1].

However, single-phase single-stage nonisolated inverters suffer from the issue of the common-mode leakage current, resulting from the absence of transformers [2]–[4]. The hazards of the common-mode leakage current include a decrease in the lifetime of the PV panel [5], electric shock [6], and electromagnetic interference [7]. There are many solutions to eliminate the common-mode leakage current, and these solutions can be divided into two categories. One category of solutions is to add auxiliary switches to a single-phase full-bridge inverter to cut off the common-mode current path, such as an H5 inverter [8], H6 inverter [9], HERIC inverter [10], or active virtual ground inverter [11]. The operation principles of these inverters are to isolate the PV panel from the ac grid during a certain operating interval to diminish the common-mode leakage current [7]. However, these inverters all need to add additional semiconductor devices, which increases the control complexity and reduces the efficiency [5]. The other category of solutions is to propose a topology that shares one common terminal between the PV panel and the ac grid [5]. In [5], a four-switch single-phase inverter with buck–boost capability is introduced, and this approach is feasible for PV grid-tied applications. Yet, different control strategies for different ac voltage polarities are needed, which increases the control complexity. Based on the charge pump circuit concept, a single-phase transformerless inverter that eliminates the common-mode leakage current is proposed in [6]; this solution is an inverter without a boost capability. A modified Y-source PV grid-connected inverter is proposed in [12], and this solution allows the negative terminal of the PV panel to directly connect to the neutral line of the AC grid, and then, the leakage current is eliminated completely. However, the structure of this inverter is relatively complicated and the cost is high. In [13], a series of flying capacitor single-phase transformerless inverters are proposed, and these inverters are either common ground or common positive. In [14], a common ground single-phase inverter is also proposed, but it contains five switches, which make the topology and control strategies more complicated.

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The authors are with the School of Electrical Engineering and Automation, Wuhan University, Wuhan 430072, China (e-mail: jianbo_jiang@whu.edu.cn; shangzhi.pan@whu.edu.cn; gongjinwu@whu.edu.cn; dyj_lf@163.com; xmzha@whu.edu.cn; zyz_joe@163.com).

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Single-phase single-stage nonisolated inverters also have the problem of double-line-frequency power oscillation [15], [16]. Regrettably, none of these previous studies take this problem into account. Double-line-frequency power oscillations will cause double-line-frequency voltage fluctuations across the PV terminals [17], and then, a high-capacity capacitor needs to be employed on the dc side, which results in an increase in the inverter size. Due to the capacitance requirements, electrolytic capacitors must be applied, but their service lives are limited [18]. There are other methods to suppress double-line-frequency power oscillation. In [19], an active power decoupling circuit is added to a single-phase dual-buck inverter. However, more switches and components are required, which increases the complexity of the system and control strategies. In [20], an active buffer is installed on the dc side of the inverter to reduce the double-line-frequency voltage fluctuations, and this method also requires additional switches and components. Similarly, these two studies [20], [21] cannot solve the problem of common-mode leakage currents. In addition, an improved modulation strategy is proposed for a quasi-Z source inverter to suppress double-line-frequency power oscillations [15], but it is only applicable for Z-source derived inverters.

Only a small amount of research addresses both the common-mode leakage current and double-line-frequency power oscillation issues. A Cuk-derived single-phase inverter [17] has been proposed. This inverter allows the negative pole of the PV panel to directly connect to the neutral line of the ac grid and applies an embedded decoupling capacitor to handle the issue of power oscillation. Yet, this kind of inverter contains five switches and requires diverse control strategies for different ac voltage polarities. A dual-buck based nonisolated inverter is introduced to suppress the leakage current and power oscillation [21], and this inverter requires a higher dc side voltage than a single-phase full-bridge inverter. Xia et al. [22] presents a doubly grounded transformerless PV inverter that can address both the leakage current and power oscillation issues. However, this proposed converter also requires a higher dc side voltage than the conventional H-bridge inverter.

Aiming to address the issues outlined above, this article proposes a single-phase single-stage nonisolated inverter [23] for distributed PV grid-tied applications. This proposed inverter is composed of two switches, two capacitors, two inductors, and a diode. The designed inverter shares a common terminal with the PV panel and ac grid so that the common-mode leakage current is completely eliminated. A power decoupling method is developed to suppress the double-line-frequency power oscillation and decrease the capacitor capacitance without any extra switches or energy storage components. The small-signal stability of the proposed inverter system is analyzed, and the system is found to be unstable when the inverter is connected to a weak grid. Then, an improved control strategy is proposed to solve this problem. The designed inverter can not only eliminate the common-mode leakage current and double-line-frequency power oscillation, but can also achieve zero voltage switching (ZVS), has output reactive power, realize maximum power point tracking (MPPT), and step up the input voltage. The validity of the proposed inverter and improved control strategy is verified by simulation and experimental results.

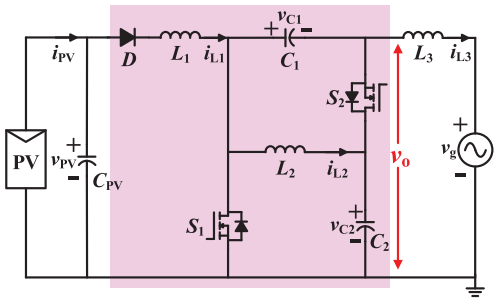

Fig. 1. Topology of the proposed inverter.

TABLE I
SYSTEM PARAMETERS OF THE PROPOSED INVERTER

Parameter	Value
V_{MPP}, I_{MPP}, V_g, v_{ave_ref}	51.7 V, 3.48 A, 100 V, 500 V
C_{PV}, C_1, C_2	40 μF, 20 μF, 20 μF
L_1, L_2, L_3	20 μH, 3.3 mH, 3 mH
P_{MPP}, I_{sc}, V_{oc}	180 W, 4 A, 70 V

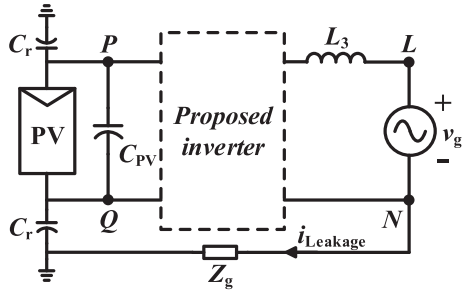

Fig. 2. Schematic diagram of the proposed inverter with common-mode leakage current path.

II. OPERATING PRINCIPLES OF THE PROPOSED INVERTER

The proposed inverter is shown in Fig. 1 and contains only two switches (S_1 and S_2), two inductors (L_1 and L_2), three capacitors (C_1, C_2, and C_s), and a diode (D). Both the L-type filter and the LCL-type filter are suitable for the proposed inverter. An L-type filter is selected in this paper and L_3 is a filter inductor. C_{PV} is the terminal capacitor of the PV panel. When switch S_1 is turned on, the output voltage of the proposed inverter v_o is equal to $-v_{C1}$, and when switch S_2 is turned on, v_o is equal to v_{C2}. Therefore, the grid-connected current i_{L3} can be outputted in the form of a sine wave by adjusting the duty cycle of the switches S_1 and S_2. The parameters of the proposed inverter are shown in Table I.

A. Common-Mode Leakage Current Analysis

The schematic diagram of the proposed inverter with the common-mode leakage current path is shown in Fig. 2, where C_r, Z_g, and $i_{Leakage}$ are the parasitic capacitance between the PV panel and ground, the impedance between the neutral line of

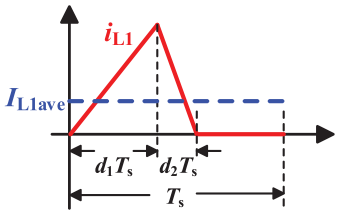

Fig. 3. Waveform of i_{L1}.

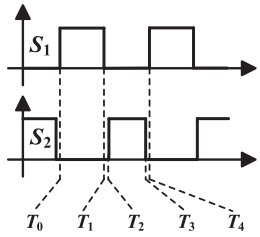

Fig. 4. Switching pattern of the proposed inverter.

the ac grid and ground, and the common-mode leakage current, respectively. Then, the common-mode voltage of the proposed inverter can be derived as

$$v_{cm} = \frac{v_{LQ} + v_{NQ}}{2}. \tag{1}$$

Since the neutral line of the ac grid is directly connected to the negative pole of the PV panel, v_{LQ} is equal to v_g and v_{NQ} is equal to zero in all switch states. The common-mode voltage v_{cm} is found to always equal v_g /2, and there are no high-frequency components in v_{cm}. Therefore, the common-mode leakage current of the proposed inverter is completely eliminated.

B. Power Decoupling Method

The instantaneous power of the ac side of the single-phase inverter can be derived as (2), and this power consists of the average power and double-line-frequency power. Existing power decoupling methods [24] require energy storage components and switches for which the main principle is to utilize an additional switch to buffer the double-line-frequency power into the energy storage components to achieve power decoupling between the ac side and the dc side. As seen in Fig. 1, the proposed topology contains two inductors (L_1 and L_2) and two capacitors (C_1 and C_2), where L_2 is used to assist switch S_1 to achieve ZVS. In contrast, capacitors C_1 and C_2 are more feasible for buffering the double-line-frequency power, while inductor L_1 is only responsible for transmitting energy

$$p_{AC} = v_{AC} i_{AC} = \frac{VI\cos(\varphi)}{2} + \frac{VI\cos(2\omega t + \varphi)}{2}. \tag{2}$$

To employ capacitors C_1 and C_2 to buffer the double-line-frequency power so that the double-line-frequency power oscillation can be suppressed, current i_{L1} must be a constant value. Therefore, this paper proposes a power decoupling method that makes inductor L_1 operate in the discontinuous current mode (DCM) and changes the switching frequency. As a result, the switching periodic average of i_{L1} is a constant value. The proposed power decoupling method does not require any extra switches or energy storage components, and the detailed derivation process is as follows.

Fig. 3 shows the waveform of one switching cycle of i_{L1}, where d_1 and d_2 denote the duty cycle when i_{L1} rises and falls, respectively. T_s is the switching cycle, and I_{L1ave} is the periodic average of i_{L1}. The slope when i_{L1} rises and falls can be expressed as

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{PV}}{L_1} \\ \frac{di_{L1}}{dt} = \frac{v_{PV} - v_{C1} - v_{C2}}{L_1}. \end{cases} \tag{3}$$

Then, combining Fig. 3 and (3), the switching periodic average of i_{L1} is derived as

$$I_{L1ave} = \frac{v_{PV} d_1^2 (v_{C1} + v_{C2})}{2L_1 f_s (v_{C1} + v_{C2} - v_{PV})}. \tag{4}$$

Because $i_{PV} = I_{L1ave}$ at steady state, the condition for suppressing the double-line-frequency power oscillation can be derived as

$$f_s = \frac{v_{PV} d_1^2 (v_{C1} + v_{C2})}{2 i_{PV} L_1 (v_{C1} + v_{C2} - v_{PV})} \tag{5}$$

where f_s is the switching frequency. It can be seen from (5) that the double-line-frequency power oscillation can be suppressed by adjusting the switching frequency. Since $v_{C1} + v_{C2}$ is much larger than v_{PV}, (5) can be simplified as

$$f_s \approx \frac{v_{PV} d_1^2}{2 i_{PV} L_1}. \tag{6}$$

There is no double-line-frequency component in (6), so the double-line-frequency power oscillation on the dc side can be eliminated.

C. Operating Principles of the Proposed Inverter

The operating principles of the two switches S_1 and S_2 are complementary conduction, and it is necessary to add the dead band to achieve ZVS. The switching pattern of the proposed inverter is shown in Fig. 4, and the switching cycle can be divided into four stages.

The first stage is from T_0 to T_1, when switch S_1 is turned ON and S_2 is turned OFF. The equivalent circuit of the first stage of the proposed inverter is shown in Fig. 5. The PV panel charges inductor L_1. Switch S_1, inductor L_2 and capacitor C_2 form an energy transfer loop. Switch S_1, inductor L_3, capacitor C_1, and the AC grid form another energy transfer loop. In this stage, the current slope of each inductor and the voltage slope of each capacitor are shown as

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{PV}}{L_1}, \frac{di_{L2}}{dt} = -\frac{v_{C2}}{L_2}, \frac{di_{L3}}{dt} = \frac{-v_{C1} - v_g}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L3}}{C_1}, \frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2}. \end{cases} \tag{7}$$

The second stage is a dead band from T_1 to T_2. In this stage, switch S_1 is turned OFF but switch S_2 has not yet been

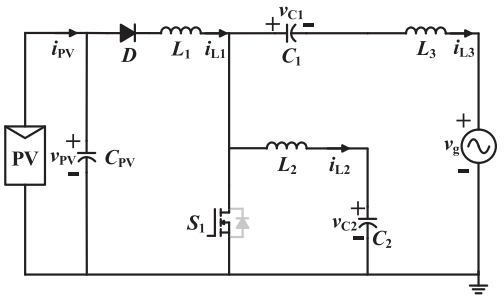

Fig. 5. Equivalent circuit of the first stage of the proposed inverter.

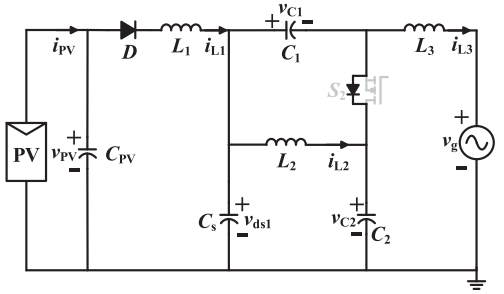

Fig. 6. Equivalent circuit of the second stage of the proposed inverter.

turned ON. The equivalent circuit of the second stage of the proposed inverter is shown in Fig. 6, where C_s is the parasitic capacitance between the drain and source of switch S_1. Due to the characteristic of the inductor that prevents the current from changing, and because i_{L1} is much larger than i_{L2} and i_{L3} at time T_1, the antiparallel diode of switch S_2 is turned ON, thereby achieving ZVS of switch S_2. At the same time, the voltage of capacitor C_s rises rapidly to $v_{C1} + v_{C2}$.

The third stage is from T_2 to T_3, when switch S_1 is turned OFF and S_2 is turned ON. Since inductor L_1 is operating in DCM, this stage can be divided into two intervals. The first interval is before i_{L1} falls to zero, and the second interval is after i_{L1} falls to zero. The equivalent circuits of these two intervals of the proposed inverter are shown in Fig. 7. In the first interval and the second interval, the current slope of each inductor and the voltage slope of each capacitor are shown as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{PV}-v_{C1}-v_{C2}}{L_1}, \frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{v_{C2}-v_g}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L1}-i_{L2}}{C_1}, \frac{dv_{C2}}{dt} = \frac{i_{L1}-i_{L3}}{C_2} \end{cases} \tag{8}$$

$$\begin{cases} i_{L1} = 0, \frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{v_{C2}-v_g}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1}, \frac{dv_{C2}}{dt} = \frac{-i_{L3}}{C_2}. \end{cases} \tag{9}$$

The last stage is the other dead band from T_3 to T_4. In this stage, switch S_2 is turned OFF but S_1 has not yet turned ON. The equivalent circuit of the last stage of the proposed inverter is shown as Fig. 8. When i_{L2} is positive, v_{Cs} will slump to zero, thus achieving ZVS of switch S_1. However, ZVS of switch S_1 cannot be achieved when i_{L2} is negative.

D. Steady State Analysis

The voltage, current, and duty cycle indicated by capital letters in this article are the steady-state values of the corresponding variables. When the system is running in steady state, for inductors L_2 and L_3, according to the volt-second balance principle

$$\begin{cases} \frac{D_1 V_{C2}}{L_2} = \frac{(1-D_1)V_{C1}}{L_2} \\ \frac{D_1(V_{C1}+v_g)}{L_3} = \frac{(1-D_1)(V_{C2}-v_g)}{L_3}. \end{cases} \tag{10}$$

Based on (10), it can be further derived

$$\begin{cases} V_{C1} = D_1 v_g/(1-2D_1) \\ V_{C2} = (1-D_1)v_g/(1-2D_1) \end{cases} \tag{11}$$

$$\begin{cases} \frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{v_{C2}-v_g}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L1ave}-i_{L2}}{C_1}, \frac{dv_{C2}}{dt} = \frac{i_{L1ave}-i_{L3}}{C_2}. \end{cases} \tag{12}$$

Since the terminal voltage of the PV panel can be adjusted to a constant value by the proposed power decoupling method, the PV panel, capacitor C_{PV}, diode D, and inductor L_1 can be equivalent to a constant current source with a current of i_{L1ave}. Then, (8) and (9) can be replaced by (12).

For capacitors C_1 and C_2, according to the ampere-second balance principle:

$$\begin{cases} \frac{D_1 I_{L3}}{C_1} = \frac{(1-D_1)(I_{L2}-I_{L1ave})}{C_1} \\ \frac{D_1 I_{L2}}{C_2} = \frac{(1-D_1)(I_{L3}-I_{L1ave})}{C_2}. \end{cases} \tag{13}$$

Based on (13), it can be further derived

$$I_{L2} = I_{L3}. \tag{14}$$

E. Voltage Stress of Semiconductors

The semiconductor device in the proposed inverter contains a diode (D) and two switches (S_1 and S_2). According to the third stage equivalent circuit shown in Fig. 7, the voltage stress of switch S_1 is $v_{C1} + v_{C2}$. Similarly, the first stage equivalent circuit shown in Fig. 5 shows that the voltage stress of switch S_2 is $v_{C1} + v_{C2}$. When i_{L1} drops to zero, D has the highest reverse voltage, which is $v_{C1} + v_{C2}$ - v_{PV}.

III. Control Strategies Design and Parameters Selection

A. Control Strategies Design

The first target of the proposed inverter is to output the grid-connected current in the form of a sine wave. A PI or PR controller can be selected to achieve this target; however, a PR controller has better tracking performance for AC signals than a PI controller. Therefore, a PR controller (*PR*) is chosen to adjust the grid-connected current.

According to (5), the double-line-frequency power oscillation can be suppressed by adjusting the switching frequency. However, this condition is derived based on ideal conditions and is not robust to changes in parameters. Therefore, a PI controller (PI_F) is employed to adjust the switching frequency.

Finally, the amplitude of the grid-connected current must also be determined. Due to the uncertainty of factors, such

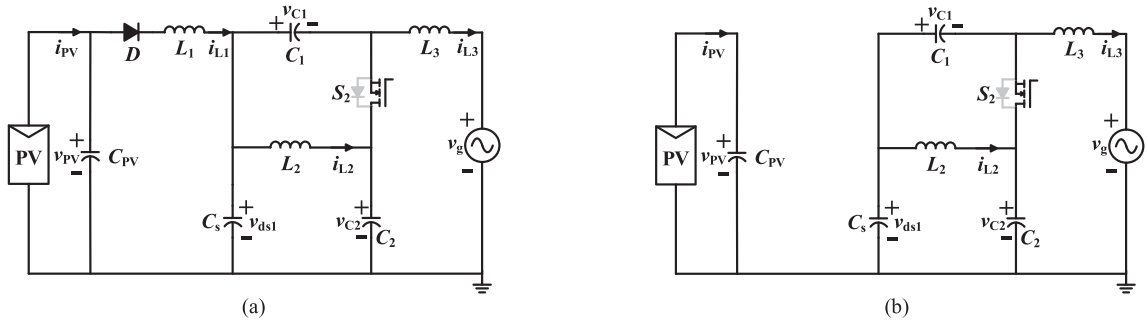

Fig. 7. Equivalent circuit of the third stage of the proposed inverter. (a) $T_2 \le t < T_2+d_2T_s$. (b) $T_2+d_2T_s \le t < T_3$.

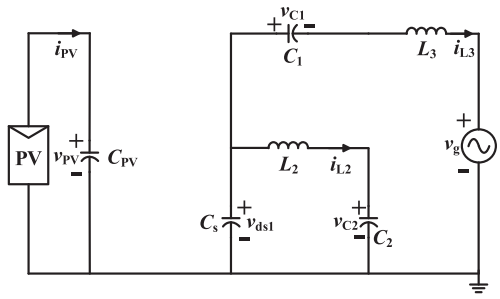

Fig. 8. Equivalent circuit of the last stage of the proposed inverter.

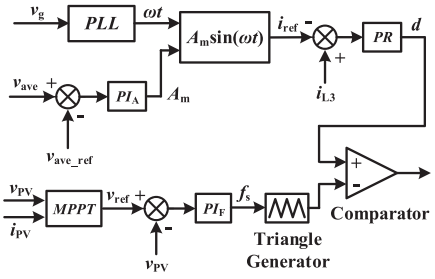

Fig. 9. Control block diagram.

as the irradiance, temperature, inverter loss, and grid voltage, the amplitude of the grid-connected current cannot be obtained by direct calculation. Aiming to address this issue, this article proposes an adaptive method that uses a PI controller ($PI_{\rm A}$) to adjust the periodic average of $v_{\rm C1}+v_{\rm C2}$ to be a fixed constant to indirectly determine the amplitude of the grid-connected current

$$\begin{cases} PR = k_{\rm p} + \frac{2k_{\rm r}\omega_{\rm c}s}{s^2+2\omega_{\rm c}s+\omega_0^2} \\ PI_{\rm F} = k_{\rm pF} + \frac{k_{\rm iF}}{s} \\ PI_{\rm A} = k_{\rm pA} + \frac{k_{\rm iA}}{s}. \end{cases} \tag{15}$$

The transfer function of the above controllers is expressed as (15). The control block diagram is shown in Fig. 9, where $v_{\rm ave}$, $v_{\rm ave\_ref}$, $A_{\rm m}$, $i_{\rm ref}$, and $v_{\rm ref}$ denote the half grid periodic average of $v_{\rm C1}+v_{\rm C2}$, the reference value of $v_{\rm ave}$, the amplitude of the grid-connected current, the reference value of the grid-connected current, and the reference value of PV terminal voltage, respectively. d represents the duty cycle before normalization, and $d_1 = 0.5*(d+1)$.

B. Parameters Selection Principles

The capacitance of $C_{\rm PV}$ is mainly determined by the amplitude of the terminal voltage switching ripple of the PV panel due to the double-line-frequency power oscillation that is handled by capacitors C_1 and C_2. Similarly, the inductance of L_3 is determined by the amplitude of the grid-connected current ripple.

The functions of C_1 and C_2 ($C_1 = C_2$) include buffering the double-line-frequency power oscillation and providing positive and negative voltages to the output port. The relationship between the charge and discharge power of the capacitor and the voltage is as shown in (16). When the periodic average of $v_{\rm C1}+v_{\rm C2}$ and the oscillation power are fixed, it can be found from (16) that the smaller the capacitance, the greater the fluctuation of the capacitor voltage, which then increases the voltage stress of switches. Therefore, the capacitances of C_1 and C_2 are determined by the amplitude of the oscillation power.

$$\int Pdt = \frac{C(\Delta v_{\rm C}^2 + 2v_{\rm C}\Delta v_{\rm C})}{2}. \tag{16}$$

It can be seen from (5) that L_1 is inversely proportional to the switching frequency. An extremely low switching frequency means that a larger filter inductor or capacitor is needed, and an extremely high switching frequency will increase the influence of parasitic parameters on the system. Assuming that the maximum allowable switching frequency is $f_{\rm smax}$ ($f_{\rm smax} = 300$ kHz) and that the minimum switching frequency is $f_{\rm smin}$ ($f_{\rm smin} = 20$ kHz), the range of L_1 can be expressed as (17).

The value of L_3 is mainly determined by the minimum switching frequency $f_{\rm smin}$. In addition, L_2 and L_3 influence the stability of the proposed inverter, and the selection principle needs to be combined with the results of the stability analysis

$$\begin{cases} L_1 \ge \frac{v_{\rm PV}d_1^2(v_{\rm C1}+v_{\rm C2})}{2i_{\rm PV}f_{\rm smax}(v_{\rm C1}+v_{\rm C2}-v_{\rm PV})} \\ L_1 \le \frac{v_{\rm PV}d_1^2(v_{\rm C1}+v_{\rm C2})}{2i_{\rm PV}f_{\rm smin}(v_{\rm C1}+v_{\rm C2}-v_{\rm PV})}. \end{cases} \tag{17}$$

C. Small Signal Stability Analysis and Improved Control Strategies

Single-phase PV grid-tied inverters are usually connected to low-voltage AC distribution networks. The characteristics of weak grids are highlighted as the transmission distance increases. Therefore, it is necessary to analyze the stability of

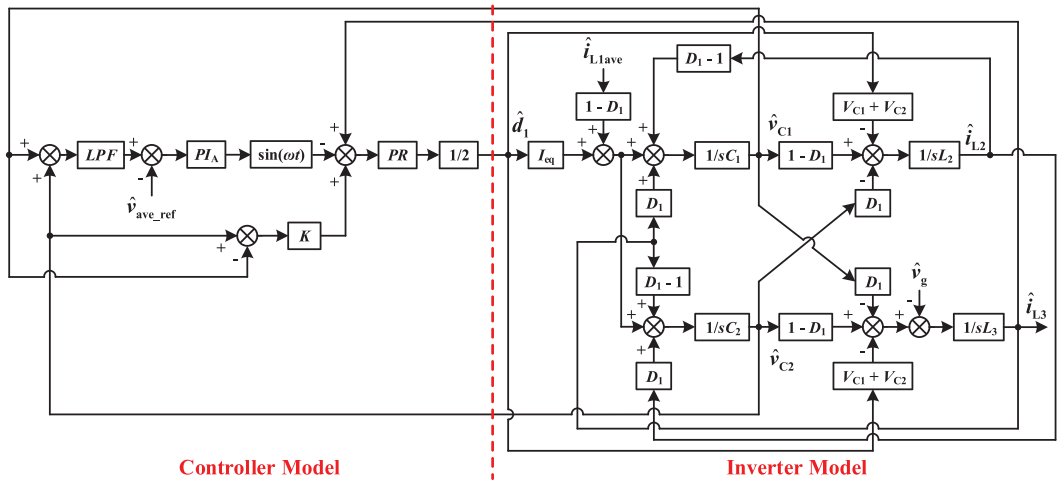

Fig. 10. Control block diagram of whole system.

the proposed inverter when it is connected to a weak grid. The grid impedance is defined as L_{g}. Combining (7) with (12), the large-signal model of the proposed inverter can be obtained by the state space averaging method and is expressed as

$$\begin{cases} L_2\frac{di_{\mathrm{L2}}}{dt} = (1-d_1)v_{\mathrm{C1}} - d_1 v_{\mathrm{C2}} \\ (L_3+L_{\mathrm{g}})\frac{di_{\mathrm{L3}}}{dt} = -d_1 v_{\mathrm{C1}} + (1-d_1)v_{\mathrm{C2}} - v_{\mathrm{g}} \\ C_1\frac{dv_{\mathrm{C1}}}{dt} = (d_1-1)i_{\mathrm{L2}} + d_1 i_{\mathrm{L3}} + (1-d_1)i_{\mathrm{L1ave}} \\ C_2\frac{dv_{\mathrm{C2}}}{dt} = d_1 i_{\mathrm{L2}} + (d_1-1)i_{\mathrm{L3}} + (1-d_1)i_{\mathrm{L1ave}}. \end{cases} \tag{18}$$

By linearizing the mathematical model of the controller and the large-signal model of the proposed inverter, the small-signal model of the whole system can be derived as (19).

Based on the small signal model shown in (19), the control block diagram of the entire system can be obtained as shown in Fig. 10, where $LPF = 1/(0.01s+1)$. It can be seen from Fig. 10 that the transfer function in symbol form is too complicated and difficult to obtain and is not conducive to stability analysis. Therefore, this article mainly uses matrix operations to obtain the transfer function of the system, as shown in (20).

$$\begin{cases} \frac{d\hat{i}_{\mathrm{L2}}}{dt} = \frac{1-D_1}{L_2}\hat{v}_{\mathrm{C1}} - \frac{D_1}{L_2}\hat{v}_{\mathrm{C2}} - \frac{V_{\mathrm{C1}}+V_{\mathrm{C2}}}{L_2}\hat{d}_1 \\ \frac{d\hat{i}_{\mathrm{L3}}}{dt} = \frac{1-D_1}{L_{\mathrm{eq}}}\hat{v}_{\mathrm{C2}} - \frac{D_1}{L_{\mathrm{eq}}}\hat{v}_{\mathrm{C1}} - \frac{V_{\mathrm{C1}}+V_{\mathrm{C2}}}{L_{\mathrm{eq}}}\hat{d}_1 - \frac{\hat{v}_{\mathrm{g}}}{L_{\mathrm{eq}}} \\ \frac{d\hat{v}_{\mathrm{C1}}}{dt} = \frac{D_1-1}{C_1}\hat{i}_{\mathrm{L2}} + \frac{D_1}{C_1}\hat{i}_{\mathrm{L3}} + \frac{I_{\mathrm{eq}}}{C_1}\hat{d}_1 + \frac{1-D_1}{C_1}\hat{i}_{\mathrm{L1ave}} \\ \frac{d\hat{v}_{\mathrm{C2}}}{dt} = \frac{D_1-1}{C_2}\hat{i}_{\mathrm{L3}} + \frac{D_1}{C_1}\hat{i}_{\mathrm{L2}} + \frac{I_{\mathrm{eq}}}{C_1}\hat{d}_1 + \frac{1-D_1}{C_1}\hat{i}_{\mathrm{L1ave}} \\ I_{\mathrm{eq}} = I_{\mathrm{L2}} + I_{\mathrm{L3}} - I_{\mathrm{L1ave}}, L_{\mathrm{eq}} = L_3 + L_{\mathrm{g}} \\ \hat{d}_1 = \frac{1}{2}PR(\hat{i}_{\mathrm{L3}} - PI_{\mathrm{A}}(\frac{\hat{v}_{\mathrm{C1}}+\hat{v}_{\mathrm{C2}}}{0.01s+1} - \hat{v}_{\mathrm{ave\_ref}})) \end{cases} \tag{19}$$

$$\begin{aligned} \hat{i}_{\mathrm{L3}}(s) = {} & C(sI-A)^{-1}B_1\hat{v}_{\mathrm{g}}(s) + C(sI-A)^{-1}B_2\hat{i}_{\mathrm{L1ave}}(s) \\ & + C(sI-A)^{-1}B_3\hat{v}_{\mathrm{ave\_ref}}(s) \end{aligned} \tag{20}$$

where I is the fourth-order identity matrix, $C = [0\ 1\ 0\ 0]$, $A = \begin{bmatrix} 0 & a_{12} & a_{13} & a_{14} \\ 0 & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{bmatrix}$, $B_1 = \begin{bmatrix} 0 \\ -\frac{1}{L_{\mathrm{eq}}} \\ 0 \\ 0 \end{bmatrix}$, $B_2 = \begin{bmatrix} 0 \\ 0 \\ \frac{1-D_1}{C_1} \\ \frac{1-D_1}{C_2} \end{bmatrix}$,

$B_3 = \begin{bmatrix} b_1\ b_2\ b_3\ b_4 \end{bmatrix}^{\mathrm{T}}$, $b_1 = -0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}/L_2$

$b_2 = -0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}/L_{\mathrm{eq}}$,

$b_3 = 0.5I_{\mathrm{eq}}PI_{\mathrm{A}}PR/C_1$

$b_4 = 0.5I_{\mathrm{eq}}PI_{\mathrm{A}}PR/C_2$,

$a_{12} = -0.5(V_{\mathrm{C1}}+V_{\mathrm{C2}})PR/L_2$

$a_{13} = [1 - D_1 + 0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}LPF]/L_2$

$a_{14} = [-D_1 + 0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}LPF]/L_2$

$a_{22} = -0.5(V_{\mathrm{C1}}+V_{\mathrm{C2}})PR/L_{\mathrm{eq}}$,

$a_{31} = (D_1-1)/C_1$,

$a_{41} = D_1/C_2$,

$a_{23} = [-D_1 + 0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}LPF]/L_{\mathrm{eq}}$

$a_{24} = [1 - D_1 + 0.5PR(V_{\mathrm{C1}}+V_{\mathrm{C2}})PI_{\mathrm{A}}LPF]/L_{\mathrm{eq}}$

$a_{32} = [D_1 + 0.5I_{\mathrm{eq}}PR]/C_1$,

$a_{42} = [D_1 - 1 + 0.5I_{\mathrm{eq}}PR]/C_2$

$a_{33} = a_{34} = -0.5I_{\mathrm{eq}}PR \cdot PI_{\mathrm{A}}LPF/C_1$

$a_{43} = a_{44} = -0.5I_{\mathrm{eq}}PR \cdot PI_{\mathrm{A}}LPF/C_2$.

Then, the transfer function of input current i_{L1ave} to grid-connected current i_{L3} can be obtained as follows:

$$G = C(sI-A)^{-1}B_2. \tag{21}$$

To obtain a numerical expression of the transfer function, the steady-state value of each variable at the steady-state operating point needs to be calculated. Since the voltage and current on the ac side of the inverter are sinusoidal, there is no actual steady-state operating point. Therefore, a *d-q* transformation is required to obtain a steady-state operating point. Under the condition of the unit power factor, the steady-state values of the voltage and current on the ac side are positive peak values. The steady state value of I_{L1ave} is equal to the output current when the PV panel

TABLE II
CONTROLLER PARAMETERS OF THE PROPOSED INVERTER

Parameter	Value
k_{pA}, k_{iA}	0.01, 0.1
k_p, k_r	0.3, 100
k_{pF}, k_{iF}	4*10^5, 2*10^7
ω_c, ω_0	10 rad/s, 314.16 rad/s

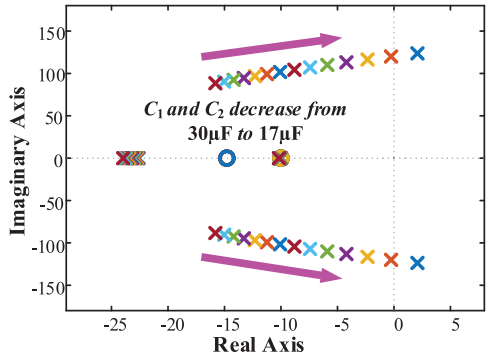

Fig. 11. Root locus plots (C_1 and C_2 decrease from 30 μF to 17 μF).

is operating at the maximum power point ($I_{L1ave} = 3.48$ A). Combining (14) and ignoring the energy loss of the converter results in $I_{L2} = I_{L3} = 3.6$ A. Based on (11),V_{C1}, V_{C2}, and D_1 can be approximated by

$$\begin{cases} V_{C1} + V_{C2} = v_{ave\_ref} \\ V_{C2} - V_{C1} = V_g \\ D_1 = V_{C1}/(2V_{C1} + V_g). \end{cases} \tag{22}$$

The controller parameters selected in this paper are shown in Table II. Based on the obtained transfer function, the influence of different parameters on small-signal stability of the whole system can be investigated. First of all, fixed controller parameters and rest of system parameters, when C_1 and C_2 decrease from 30 μF to 17 μF, the root locus of the partial closed-loop poles are shown in Fig. 11. The system is found to be unstable when C_1 and C_2 are less than 17 μF. This is because the smaller the capacitance, the greater the fluctuation of the capacitor voltage, which is more detrimental to the stable operation of the system.

Then, the effect of a weak grid on the system stability is studied, and the moving trajectory of the partial closed-loop poles with a change in grid impedance L_g is shown in Fig. 12. Fig. 12 shows that the system is unstable when the sum of L_3 and L_g exceeds L_2. This situation means that to ensure the stable operation of the inverter in a weak grid, the inductance of L_2 needs to be larger but does not meet the actual application demands, and it is necessary to find some way to improve it.

In view of the instability of the proposed inverter under weak grid conditions, this article proposes an improved control strategy, as shown in Fig. 12, by adding a state feedback branch based on the original control strategy, where K is a scale factor. Then, the modified transfer function of the input current i_{L1ave} to the grid-tied current i_{L3} can be derived as

$$G_{imp} = C(sI - A_{imp})^{-1}B_2 \tag{23}$$

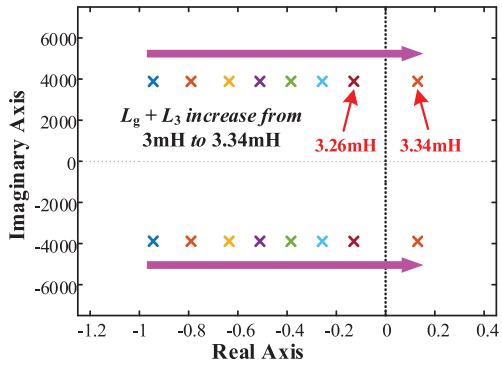

Fig. 12. Root locus plots ($L_g + L_3$ increase from 3 to 3.34 mH).

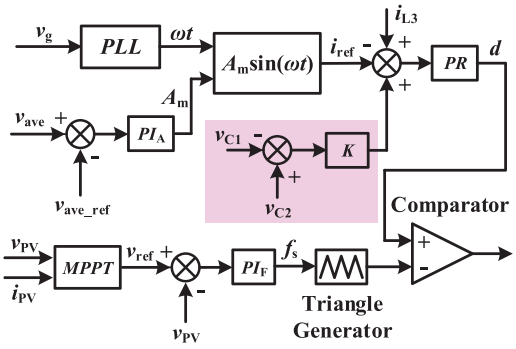

Fig. 13. Diagram of the improved control strategy.

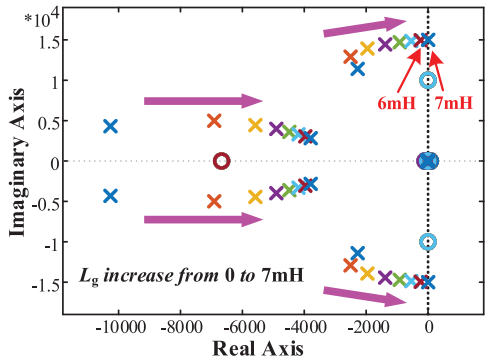

Fig. 14. Root locus plots (L_g increase from 0 to 7 mH).

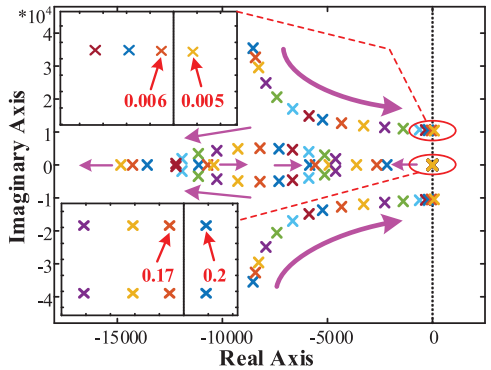

Fig. 15. Root locus plots (K decrease from 0.2 to 0.005).

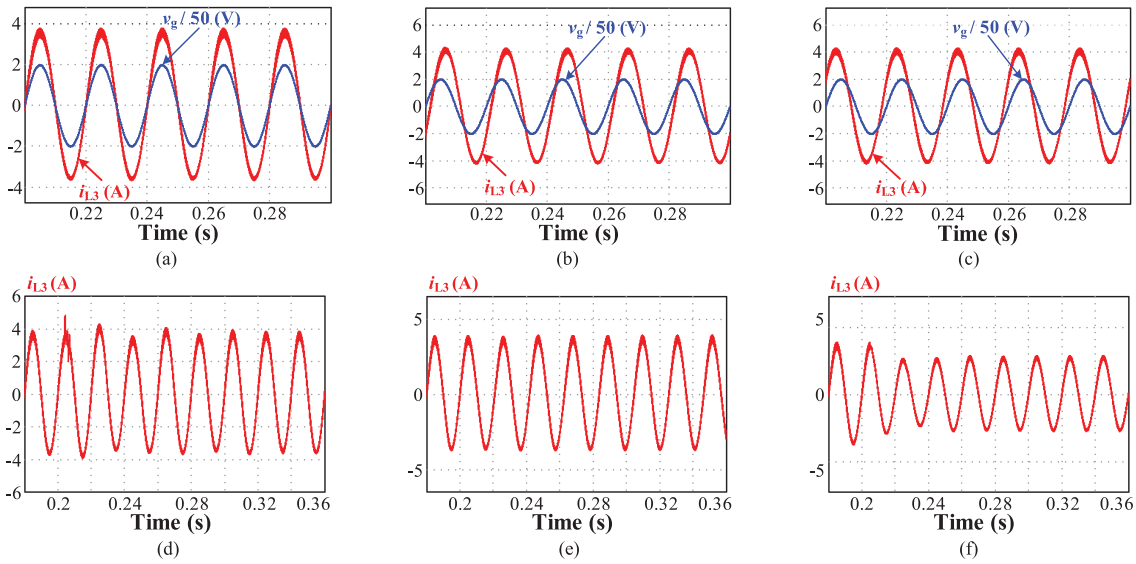

Fig. 16. Simulated waveform of grid-connected current. (a) Unit power factor. (b) Inductive reactive output (power factor: 0.8). (c) Capacitive reactive output (power factor: −0.8). (d) Grid voltage sags. (e) Grid frequency sudden changes. (f) Irradiance sudden changes.

where A_{imp} is the modified characteristic matrix based on the improved control strategy. The matrix A_{imp} can be obtained by correcting the relevant elements of matrix A based on (24). In addition, redefine $L_2 = 500$ μH and $K = 0.02$.

After adopting the improved control strategy, the influence of the grid impedance L_{g} on the stability of the inverter is shown in Fig. 14. The inverter will be unstable only when the grid impedance is overlarge ($L_{\mathrm{g}} > 6$ mH). Therefore, the improved control strategy not only makes the proposed inverter suitable for weak grids, but also reduces the volume and weight of the inverter.

Next, the effect of the scale factor K on the small-signal stability of the system must also be studied. L_{g} is defined as 0, the root locus, as shown in Fig. 15, and it can be obtained by continuously reducing K from 0.2 to 0.005. Considering the small-signal stability and response speed of the system, K is chosen to be 0.02.

IV. Simulation and Experimental Verification

Based on the parameters listed in Table I and Table II, the simulation model and the laboratory prototype were built to verify the proposed inverter and improved control strategy.

$$\begin{cases} a_{13} = [1 - D_1 + 0.5PR(V_{\mathrm{C1}} + V_{\mathrm{C2}})(PI_{\mathrm{A}}LPF + K)]/L_2 \\ a_{14} = [-D_1 + 0.5PR(V_{\mathrm{C1}} + V_{\mathrm{C2}})(PI_{\mathrm{A}}LPF - K)]/L_2 \\ a_{23} = [-D_1 + 0.5PR(V_{\mathrm{C1}} + V_{\mathrm{C2}})(PI_{\mathrm{A}}LPF + K)]/L_{\mathrm{eq}} \\ a_{24} = [1 - D_1 + 0.5PR(V_{\mathrm{C1}} + V_{\mathrm{C2}})(PI_{\mathrm{A}}LPF - K)]/L_{\mathrm{eq}} \\ a_{33} = -0.5I_{\mathrm{eq}}PR(PI_{\mathrm{A}}LPF + K)/C_1 \\ a_{34} = -0.5I_{\mathrm{eq}}PR(PI_{\mathrm{A}}LPF - K)/C_1 \\ a_{43} = -0.5I_{\mathrm{eq}}PR(PI_{\mathrm{A}}LPF + K)/C_2 \\ a_{44} = -0.5I_{\mathrm{eq}}PR(PI_{\mathrm{A}}LPF - K)/C_2. \end{cases} \tag{24}$$

A. Simulation Verification

The simulation model was built using PSIM software. When the grid impedance is 0, the simulation shows that reducing $v_{\mathrm{ave\_ref}}$ to 350 V can also keep the system stable. Therefore, $v_{\mathrm{ave\_ref}}$ is redefined as 350 V. Simulation verification under conditions of the unit power factor, inductive reactive output, and capacitive reactive output is carried out, and the waveforms of the grid-connected current are shown in Fig. 16(a), (b), and (c). In addition, the dynamic performance of the proposed inverter under sudden changes in grid voltage and frequency is verified by simulation. Fig. 16(d) shows the waveform of the grid-connected current when a 30% grid voltage sag occurs at 0.205 seconds. When the grid frequency suddenly changes from 50 to 48 Hz at 0.205 seconds, the waveform of the grid-connected current is shown in Fig. 16(e). Finally, Fig. 16(f) shows the simulation results when the irradiance changes from 1000 W/m^2 to 750 W/m^2 at 0.205 seconds. The simulation results shown in Fig. 16 verify the effectiveness of the proposed inverter and controller and also demonstrate the good dynamic performance of the inverter.

Fig. 17(a) shows the terminal voltage of the PV panel, and the peak-to-peak value of the ripple is only 1.2 V. The ripple accounts for only 2.3% of the terminal voltage of the PV panel and requires only a small capacitor ($C_{\mathrm{PV}} = 40$ μF) to achieve this. As seen from Fig. 17(b), $v_{\mathrm{C1}} + v_{\mathrm{C2}}$ fluctuates at a frequency of 100 Hz, which proves that the double-line-frequency power is handled by capacitors C_1 and C_2. Therefore, the validity of the power decoupling method has been verified. Additionally, the simulation results for ZVS of the two switches S_1 and S_2 are shown in Fig. 18.

B. Experimental Verification

To further verify the accuracy of the theoretical analysis and simulation results, a laboratory prototype was built. The

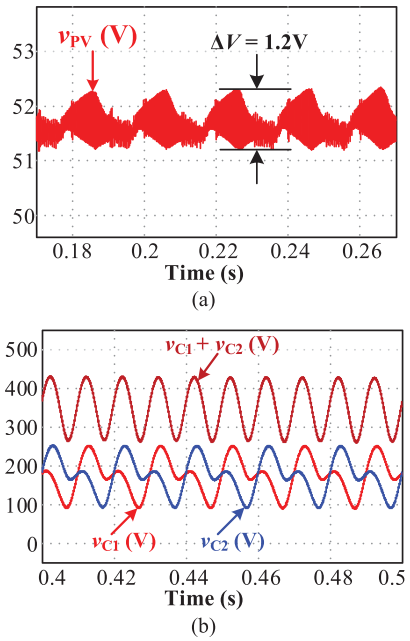

Fig. 17. Simulated waveform. (a) Waveform of the terminal voltage of the PV panel. (b) Waveforms of the voltage of capacitors C_1 and C_2.

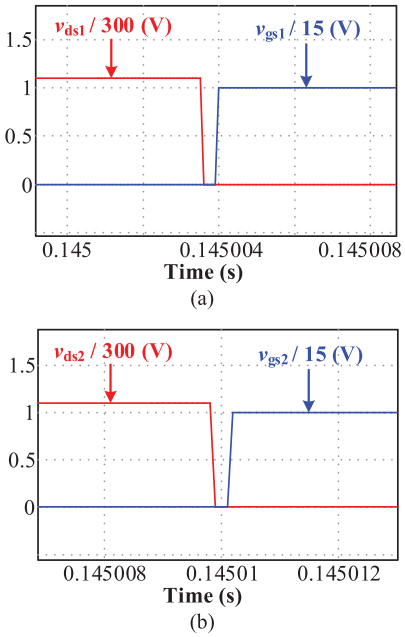

Fig. 18. Simulation results of ZVS of two switches.

laboratory prototype is shown in Fig. 19. A programmable dc power supply is used to simulate the PV panel, and a single-phase programmable ac power supply is used to simulate the ac grid. Limited by the experimental conditions and considering the safety of the test, the experimental platform built in this paper reduces the peak voltage of the power grid from the standard 311 to 100 V, and the maximum power of the PV panels is also reduced to 180 W. In practical applications, the inverter parameters can be redesigned according to the parameter selection principles described in Section III of this article.

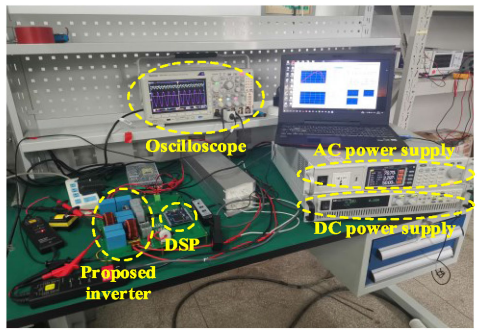

Fig. 19. Laboratory prototype of the proposed inverter.

The improved control strategies, pulse width modulation, pulse frequency modulation, phase-locked loop, and analog-to-digital conversion are all implemented by a DSP controller (TMS320F28335). Table II shows that k_{pF} and k_{iF} are significantly larger. However, the DSP controller mainly utilizes the built-in EPWM module to implement pulse width modulation and frequency modulation. When the switching frequency is 100 kHz, the precision of the EPWM is approximately 140 Hz, but the unit of the output of the frequency loop is Hz. Therefore, the effects of noise and floating-point calculation accuracy on EPWM are not significant. Additionally, an RC low-pass filter with a cutoff frequency of 5 kHz is added to the voltage v_{PV} acquisition circuit to avoid interference from sampling noise. A digital low-pass filter with a cut-off frequency of 200 Hz is also added to the DSP controller to filter out the high-frequency interference generated in the analog-to-digital conversion. C_{PV}, C_1, and C_2 are film capacitors. The maximum power point of the PV panel is set to 180 W, and the corresponding terminal voltage is set to 51.7 V. It is true that the use of film capacitors will increase the size of the inverter. However, considering the large fluctuation range of the capacitor voltages v_{C1} and v_{C2}, the use of electrolytic capacitors will reduce the service life of the inverter, thereby indirectly increasing costs. Therefore, the film capacitor is selected to realize power decoupling after weighing its advantages and disadvantages.

Experimental verification under the condition of unit power factor is carried out. Fig. 20 shows the waveforms of the inductor current i_{L1} and i_{L2}, the grid-connected current i_{L3}, the AC grid voltage v_g, the capacitor voltages v_{C1} and v_{C2}, the terminal voltage of the PV panel v_{PV}, and the ZVS of switches S_1 and S_2. The current ripple of i_{L3} is less than 0.15 A (4.5%). As seen from Fig. 21, the total harmonic distortion (THD) of i_{L3} is 3.82%, which meets IEEE Std. 519-1992 (THD is less than 5%, and the high frequency ripples are all less than 0.4% of the fundamental component). Therefore, the effectiveness of the proposed inverter and the improved control strategy is verified. Furthermore, the switching frequency can be increased by appropriately reducing the inductance of L_1 to suppress the switching ripple of the grid-connected current. Fig. 20(b) shows that the voltage ripple of v_{PV} is only about 1 V (2%), so the validity of the power decoupling method has been verified. Besides, the step-up capability of the proposed inverter is also verified ($v_{PV} < V_g$).

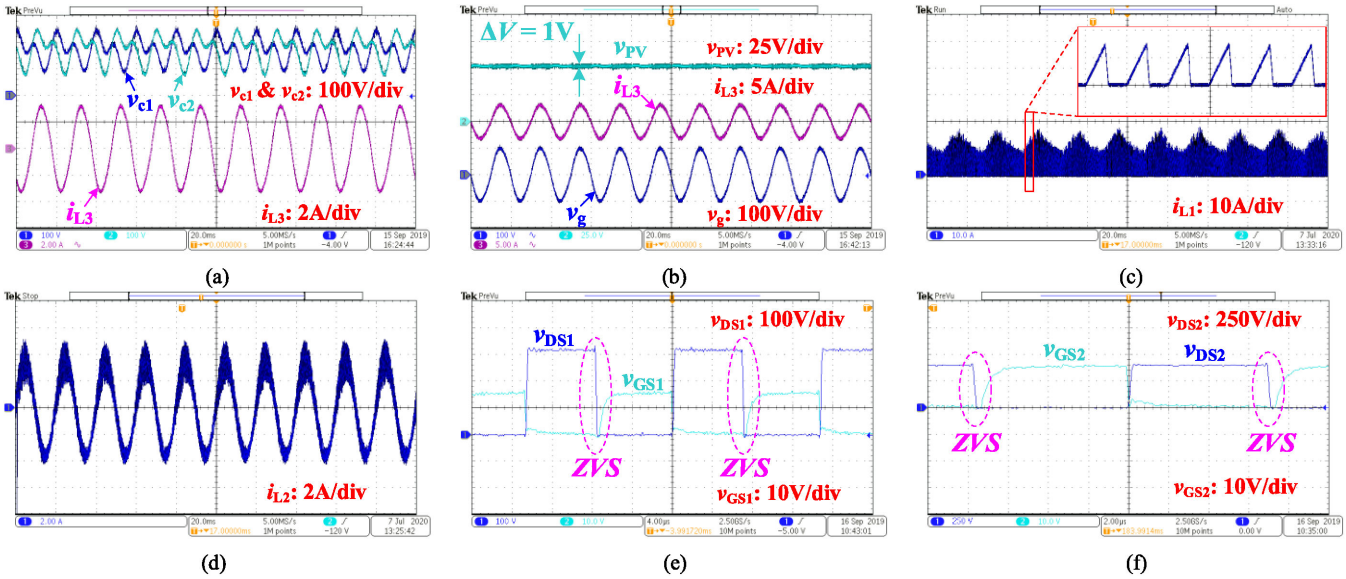

Fig. 20. Experimental results. (a) Waveforms of i_{L3}, v_{C1}, and v_{C2}. (b) Waveforms of v_{PV}, i_{L3}, and v_g. (c) Waveform of i_{L1}. (d) Waveform of i_{L2}. (e) ZVS of switch S_1. (f) ZVS of switch S_2.

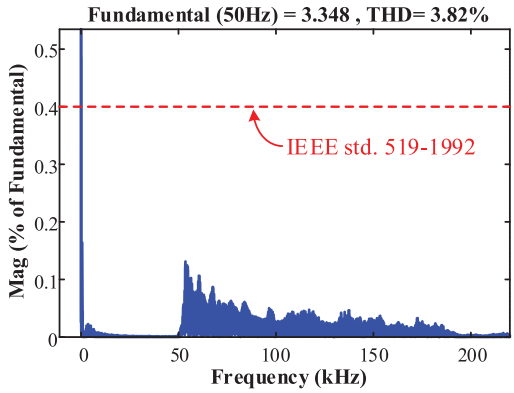

Fig. 21. Spectra of i_{L3}.

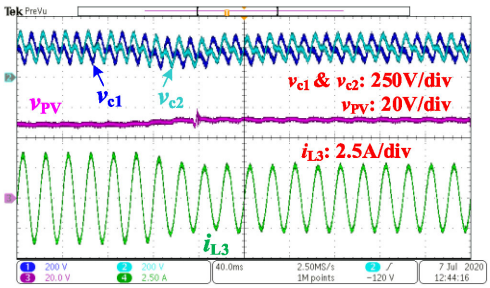

Fig. 22. Experimental results of dynamic characteristics of the proposed inverter.

To verify the dynamic performance of the proposed inverter, another set of experiments are performed in this paper. When the inverter is in a steady state, the irradiance is reduced from 1000 to 700 W/m^2, and the corresponding maximum power point is increased from 51.7 to 53.3 V. The other parameters are fixed. Fig. 22 shows the experimental results. It can be found that the inverter has entered a new steady state after a short transient process. The experimental results prove that the proposed control strategy is robust to changes in the operating conditions.

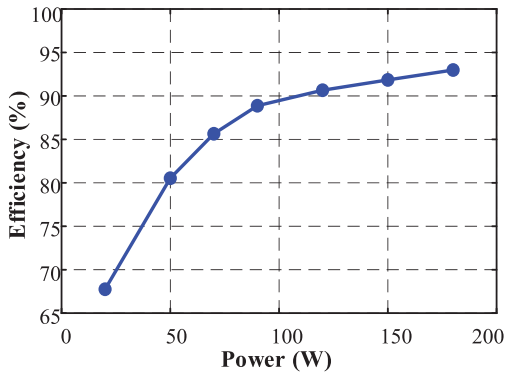

Fig. 23. Efficiency curve of the proposed inverter.

The efficiency of the proposed inverter under different power conditions are measured, and the efficiency curve is shown in Fig. 23. The energy losses of the inverter are mainly concentrated on the turn-ON loss of switch S_1 when the polarity of i_{L2} is negative (P_{on}), the turn-OFF loss of the switches (P_{off}), the conduction loss of the switches (P_{con}), the parasitic losses of inductance (P_L) and capacitance (P_C), and the conduction loss of the diode (P_D). These losses are expressed as

$$\begin{cases} P_{on} = \frac{f_s V_{DS} I_D t_{on}}{2}, P_{off} = \frac{f_s V_{DS} I_D t_{off}}{2}, P_{con} = R_{DS\_on} I_D^2 \\ P_L = R_L I_L^2, P_C = R_C I_C^2, P_D = V_F I_F. \end{cases} \tag{25}$$

As seen in (25), both P_{on} and P_{off} are proportional to the switching frequency f_s, the voltage stress V_{DS}, and the ON-state current I_D. Since the ON-resistance of the switch $R_{DS\cdot on}$, the ESR of the inductor R_L, the ESR of the capacitor R_C and

the forward voltage of the diode V_F can all be regarded as fixed parameters, P_{con}, P_L, P_C, and P_D only depend on I_D, the inductor current I_L, the capacitor current I_C, and the diode forward current I_F, respectively. The range of f_s is set to (f_{smax}, f_{smin}) by selecting the inductor L_1 reasonably, and then, f_s is the same as that used in this article under the same power condition. Thus, P_{on} and P_{off} are only determined by V_{DS} and I_D. When the proposed inverter is applied to the actual utility grid, $v_{ave\cdot ref}$ needs to be increased appropriately, which inevitably causes the voltage stress of the switch (V_{DS}) to increase. In an actual utility grid, $v_{ave\cdot ref}$ is selected to 500 V, which is 1.43 times the value used in this article (350 V). Since the peak value of the utility grid voltage is 311 V, the current in (25) will be reduced 3.11 times under the same power condition. Therefore, it can be found from (25) that applying the proposed inverter to the utility grid will further improve the efficiency. It is true that, like ordinary H-bridge inverters, as the power increases, P_{con}, P_L, and P_C will gradually become dominant losses and reduce the system efficiency. However, the proposed inverter is mainly used in low-power building integrated photovoltaic (BIPV) power generation systems, and the resistive loss has little effect on the efficiency.

V. Conclusion

In this article, a single-phase single-stage nonisolated inverter is designed for PV grid-tied applications. The functions of the proposed inverter include the elimination of the common-mode leakage current, suppression of double-line-frequency power oscillation, increase of the input voltage, achievement of ZVS, realization of MPPT, and output of reactive power. The proposed inverter has a simple structure with only two switches. The reduction of switches will inevitably increase the stress on semiconductor devices, but it is conducive to improving the efficiency of the inverter, and the silicon carbide MOSFET is suitable for this application scenario. The efficiency can exceed 90% under low-power conditions (>110 W), and a higher efficiency can be achieved through circuit optimization design such as adjusting the switching frequency appropriately to decrease the switching losses or the parasitic losses of resistance and capacitance. In addition, the inverter proposed in this article is robust to sudden changes (voltage sag, frequency change, or irradiance change) and is suitable for weak grids, which further increase its practical application value.

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Jianbo Jiang (Student Member, IEEE) was born in Baoshan, Yunnan Province, China, in 1992. He received the B.S. and M.S. degrees from Yunnan University, Kunming, China, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Wuhan University, Wuhan, China.

His research interests include the topology and control of photovoltaic inverter and transient stability of dc microgrid.

Shangzhi Pan (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, China, in 1998 and 2001, respectively, and the Ph.D. degree from Queen's University, Kingston, ON, Canada in 2008.

He joined the College of Electrical Engineering, Wuhan University, China in 2018, where he is currently a Professor. He is also an Adjunct Faculty at the Queen's Center of Energy and Power Electronics Applied Research Laboratory (ePOWER), since 2014. Previously he worked as the VP of research and development at SPARQ Systems, a Queen's SpUn-off photovoltaic microinverter company, since 2010. He was a Senior Research Engineer at Queen's University from 2008 to 2013. His research interests include digital control techniques for power converters, grid-connected inverters, voltage regulators for computing systems, power converters for renewable energy sources, and power converters for electric vehicles.

Jinwu Gong (Member, IEEE) received the B.Eng. and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2004 and 2012, respectively.

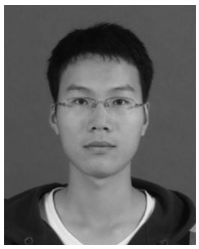
From 2017 to 2018, he was a Visiting Scholar at Future Energy Electronics Center (FEEC). He is currently an Associate Professor at Wuhan University. His current research interests include wide bandgap devices, design of high-efficiency and high-power-density power electronic converters, applications of power electronics technology in power system, key technologies of large-capacity power quality control equipment.

Fei Liu (Senior Member, IEEE) was born in Hanchuan, Hubei, China, in 1977. He received the B.S., M.S., and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2000, 2004, and 2008, respectively.

Since 2010, he has been a Faculty Member with Wuhan University, Wuhan, where he is currently an Associate Professor with the School of Electrical Engineering. His current research interests include dc microgrids and cascaded multilevel converters.

Xiaoming Zha (Member, IEEE) was born in Huaining, Anhui Province, China, in 1967. He received B.S., M.S., and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 1989, 1992, and 2001.

He was a Postdoctoral Fellow with University of Alberta, Canada, from 2001 to 2003. Since 1992, he has been a Faculty Member at Wuhan University became a Professor in 2003, and is currently the Deputy Dean with the School of Electrical Engineering. His research interests include power electronic converters, applications of power electronics in smart grid and renewable energy generation, analysis and control of microgrids, analysis and control of power quality, and frequency control of high-voltage high-power electric motors.



Yizhan Zhuang (Student Member, IEEE) was born in Fujian, China, in 1994. He received the B.S. degree from the College of Electrical Engineering and Automation, Fuzhou University, Fuzhou, China, in 2017. He is currently working toward the M.S. degree with the School of Electrical Engineering, Wuhan University, Wuhan, China.

His current research interests include LLC resonant converter and interface of photovoltaic conversion systems.