# A Constant Current Digital Control Method for Primary-Side Regulation Active-Clamp Flyback Converter

Chong Wang, Daying Sun, Xiang Zhang, Jiayi Hu, Wenhua Gu, and Sang Gui

***Abstract*—Constant current controlled flyback converter is widely used in low power applications for its simple structure and low cost. In order to further improve the output power and the efficiency, active-clamp flyback converter with soft-switching technique is always used. To avoid the nonlinearity and temperature drift of opto-coupler in the feedback circuit, a constant current digital control method is proposed for a primary-side regulation active-clamp (PSRAC) flyback converter in this article. Soft-switching technique is realized in discontinuous conduction modulation mode with a modified active-clamp technique. To compensate the nonlinearity of the secondary diode current with primary-side regulation, a new output current estimation algorithm is put forward based on the charge balance principle. The output current is predicted from primary current and the auxiliary winding voltage, and constant output current control is realized with primary peak current control method. The cost is low as only one low speed digital-to-analog converter, three comparators and a digital controller are required. The proposed control scheme was verified by a field-programmable gate array controlled 5.4–10.8 V/1.80 A PSRAC flyback converter. The output current accuracy is within in 1.2% in different input and output condition and the peak efficiency is improved by 3.6% after active-clamp technique is used.**

***Index Terms*—Constant current control, digital control, discontinuous conduction modulation (DCM) mode, peak current control, primary-side regulation active-clamp (PSRAC) flyback converter.**

## I. Introduction

POWER converters with constant current control are widely used in small power ac–dc converters, such as adapters, LED drivers and chargers [1], [2]. Primary-side regulation (PSR) flyback converter eliminates the opt-coupler used in traditional secondary-side regulation (SSR) flyback converter which suffers from the current transfer ratio (CTR) degradation due to temperature rise. It becomes one of the most popular power converter for its simple structure, high power density, and small standby power [3]–[5].

In small power application, discontinuous conduction modulation (DCM) mode is always used in PSR flyback converter. To realize constant output current control with primary-side regulation, peak current control method is always used. Considering that the output diode current is linear, the output current can be predicted based on the primary peak current, the demagnetization time, and the switching period [7]–[12]. As the primary peak current and the switching period are given by the control loop, only the demagnetization time needs to be detected. In [7], pulse frequency modulation (PFM) mode is used and the primary peak current is fixed. To realize constant output current, the demagnetization time is first measured and the ratio between the switching period and the demagnetization time is kept constant by modifying the switching period. In [7]–[10], the detection of the primary peak current and the demagnetization time are studied. In [11], the primary peak current is set and modified by a digital-to-analog converter (DAC). The demagnetization time is acquired by comparing the auxiliary winding voltage with zero voltage. Only a DAC and two comparators are used and multimode digital control can be realized. In [12], an average current control method is put forward for PSR flyback converter to realize constant output current. The average current is realized with a DAC and one comparator, and the switch turn-OFF delay is also compensated.

As the switch turn-OFF delay exits, the actual primary peak current is larger than the set value and the load current will be larger. To compensate the switch turn-OFF delay, several compensation methods are put forward [8], [13], [14]. In [8], a reduction of the peak current is committed based on the total switch-ON time and the switch turn-OFF delay, and the actual peak current will be equal to the set value. In [13], the actual peak current will be calculated from the turn-ON time and delay time of the switch. In [14], two switching cycles are used as a union. In the first switching cycle, normal peak current control is used and the switching delay is detected. In the second switching cycle, the switch-ON time is reduced by two times of the switch turn-OFF delay. The average peak current of the two switching cycles will be equal to the set value. Although the switching

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turn-OFF delay is compensation, the output current will still be a little larger than the idea value. In the above constant current controlled PSR flyback converters [6]–[14], the energy of leakage inductance is wasted and hard-switching turn-ON of the switch is used. It will be difficult to improve the efficiency to a high level.

To improve the power efficiency, active-clamp flyback converters with soft-switching technique are applied [15]–[20]. In [15], the energy of the transformer leakage inductance is recycled and used to realize zero-voltage switching (ZVS) turn-ON of switch. The switching loss is also reduced. In the traditional active-clamp flyback converters, continuous conduction modulation (CCM) mode is always used. In [17]–[20], boundary conduction modulation mode is satisfied and the leakage inductance can be very small. In the above works, the switching turn-OFF time is often not adjustable and the switching frequency keeps high in different load conditions, making it hard to acquire higher efficiency when the load gets light. To modify the switching frequency with different loads, in [16], soft-switching technique and constant output voltage are realized in DCM mode with a modified active-clamp technique. There are two turn-ON periods of the auxiliary switch during the main switch turn-OFF time. The switching period can be modified with different turn-ON time of main switch. However, SSR control method is used in these converters, the disadvantages introduced by the optocoupler are unavoidable.

To eliminate the optocoupler in the feedback loop and improve the efficiency, a primary-side regulation active-clamp (PSRAC) flyback converter is proposed in this article. However, as the current of the output diode is nonlinear, the existing output current prediction methods for PSR flyback converter are not applicable. Thus, a constant current digital control method is proposed. Based on the charge balance principle, the output current is calculated with the primary peak current, the demagnetization time, the turn-ON time of auxiliary switch and the switching period. Peak current control method is used and constant current control can be realized in DCM mode even when the current of the output diode is nonlinear. The cost is low as only one low speed digital-to-analog converter (DAC), three comparators, and a digital controller are required. The proposed control method is verified in pulse frequency modulation (PFM) mode through a field-programmable gate array (FPGA) controlled prototype. The efficiency improvement and high accuracy of output current are confirmed.

The rest of the article is structured as follows: In Section II, the principle of PSRAC flyback converter is introduced. In Section III, the proposed constant current controlled method is analyzed. In Section IV, the realization of the proposed control method is discussed. In Section V, experiments have been performed to verify the proposed digital control scheme. Finally, the conclusion is given in Section VI.

## II. Working Principle of the PSRAC Flyback Converter

The circuit configuration of PSRAC flyback converter is shown in Fig. 1. The input voltage is an ac voltage and it is sent to a rectifier bridge. Considering the large capacitance of filter capacitor $C_{in}$ and low frequency of input voltage, the actual input voltage $V_{in}$ can be seen as a dc voltage.

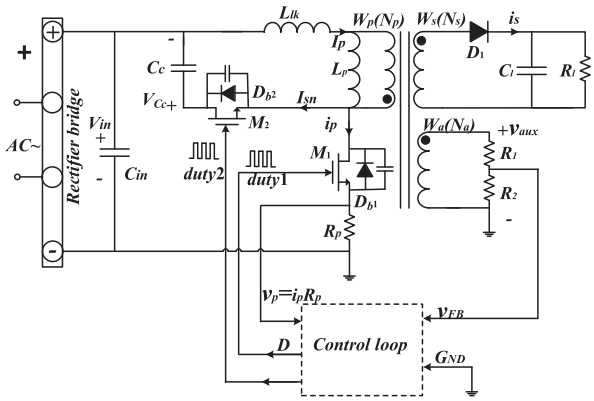



Fig. 1 Configuration of PSRAC flyback converter.

There are two switches, the main switch $M_1$ and the auxiliary switch $M_2$. $M_2$ and capacitor $C_c$ compose the active-clamp circuit. The transformer contains three windings, the primary winding $W_p$, the secondary winding $W_s$, and the auxiliary winding $W_a$. $N_p$, $N_s$, and $N_{\rm a}$ are the corresponding winding numbers. $L_m$ is the magnetizing inductance of transformer and $L_{lk}$ is the equivalent primary leakage inductance including the transformer leakage inductance and the external series-connected inductance. $R_p$ is a small resistor which is the current sensor to acquire the primary current $i_p$. The resistances of $R_1$ and $R_2$ are large enough, and the primary auxiliary circuit which is composed of $W_a$, $R_1$, and $R_2$ can be seen as an open loop. The auxiliary circuit works as a sensor to acquire the demagnetization time. Primary-side regulation is realized based on the current sensing voltage $v_p$ and the auxiliary winding voltage $v_{aux}$.

After the main switch is turned OFF, the energy of the leakage inductance is first stored in the clamp capacitor $C_c$ and then transferred to the output.

In stable condition, the converter works in DCM mode. The working waveforms can be seen in Fig. 2. The duty cycles of the main switch $M_1$ and the auxiliary switch $M_2$ are represented by duty1 and duty2. $i_p$, $i_m$, and $i_s$ are the primary winding current, the magnetizing current, and the secondary current of the transformer. $v_{Cc}$ is the voltage of the clamp capacitor $C_{\rm c}$. $v_{ds1}$ is the drain-to-source voltage of $M_1$ and $v_{aux}$ is the voltage of the auxiliary winding $W_a$. The switching cycle can be divided into nine intervals and the equivalent circuits in different intervals are shown in Fig. 3. These intervals are analyzed as follows.

*Mode 1 [$t_0$, $t_1$]:* At $t_0$, the secondary current $i_s$ drops zero and the output diode is turned OFF. The main switch $M_1$ is turned ON and the auxiliary switch $M_2$ is turned OFF in this period. The output diode $D_1$ is OFF and the equivalent circuit is shown in Fig. 3(a). At $t_0$, $v_{ds1}$ equals zero as the main switch $M_1$ is turned ON. The primary winding current $i_{\rm p}$, increases linearly which can be expressed as in (1). $V_{in}$ is the equivalent input dc voltage. The primary current $i_{\rm p}$ reaches the peak current $i_{\rm pp}$ at $t_1$ and the main switch $M_1$ is turned OFF. In this interval, the

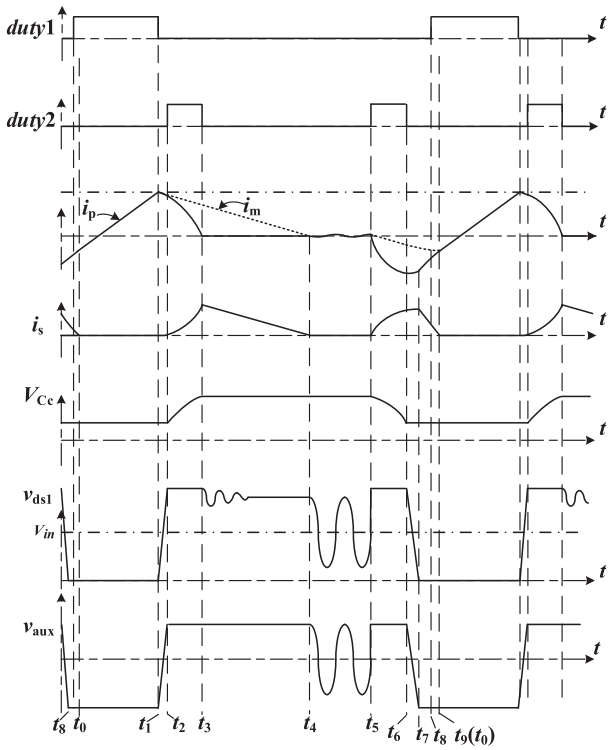



Fig. 2 Working waveforms of the proposed PSRAC flyback converter.

auxiliary winding voltage $v_{\rm aux}$ can be expressed as in (2). $v_{\rm aux}$ is proportional to the input capacitor voltage $V_{in}$

$$(Lm + Llk)\frac{dip(t)}{dt} = Vin \tag{1}$$

$$\text{vaux} = -\frac{Lm}{Lm + Llk}\frac{Na}{Np}Vin. \tag{2}$$

*Mode 2 [$t_1$, $t_2$]:* The main switch $M_1$ is turned OFF in this period. The equivalent circuit is shown in Fig. 3(b). $C_{oss1}$ and $C_{oss2}$ are the equivalent drain-to-source capacitors of $M_1$ and $M_2$. $C_{oss1}$ and $C_{oss2}$ will be charged and discharged by the primary winding current $i_{\rm p}$ in this mode, respectively. Since $C_{oss1}$ and $C_{oss2}$ are small, the drain-to-source voltage of $M_1$ $v_{ds1}$ increases very quickly in this period and the increasing slope is nearly constant. When $v_{ds1}$ get higher and the voltage of secondary winding $v_s$ is higher than the output voltage, the output diode is turned ON. At $t_2$, the auxiliary switch $M_2$ is turned ON when $v_{ds1}$ reaches the drain voltage of $M_2$, and soft-switching turn-ON of $M_2$ is obtained.

The drain voltage of $M_2$ at $t_2$ can be represented by $V_{ds1\_\rm dra}$ as in (3). $V_{Cc}(t_2)$ is the capacitor voltage of $C_c$ at $t_2$. Considering the energy conservation principle, as $t_{21}$ (the time length between $t_1$ and $t_2$) is very short compared to the switching period, the primary current $i_p$ at $t_2$ can be calculated as in (4). $i_{pp}$ is the primary current $i_p$ at $t_1$ which is also the set value of primary peak current. $V_{Cc}(t_2)$ is determined by the leakage inductance and the auxiliary switch turn-ON time

$$Vds1\_\rm dra = Vin + VCc(t2) \tag{3}$$

$$\frac{1}{2}(Coss1 + Coss2)Vin^2 + \frac{1}{2}(Lm + Llk)ipp^2 = \frac{1}{2}(Coss1 + Coss2)VCc(t2)^2 + \frac{1}{2}(Lm + Llk)ip(t2)^2. \tag{4}$$

*Mode 3 [$t_2$, $t_3$]:* The equivalent circuit is shown in Fig. 3(c). At $t_2$, the auxiliary switch is turned ON and the output diode is ON. The voltage of the magnetizing inductance $L_m$ is thus clamped at $n_{ps}V_{\rm o}$, and the magnetizing current $i_m$ decreases linearly. The decreasing ratio of $i_m$ can be expressed in (5). $n_{ps}$ is the turns' ratio between the primary winding and secondary winding of the transformer. In this period, the equivalent primary leakage inductance $L_{lk}$ starts to resonate with the clamp capacitor $C_c$. The voltage of $C_c$ increases and $i_p$ decreases. At $t_3$, $i_p$ drops to zero current and the auxiliary switch is turned OFF

$$Lm\frac{dim(t)}{dt} = -npsVo, nps = \frac{Np}{Ns}. \tag{5}$$

*Mode 4 [$t_3$, $t_4$]:* In this interval, the switches $M_1$ and $M_2$ are turned OFF and the output diode is turned ON. The equivalent circuit can be shown in Fig. 3(d). The voltage of $L_m$ is still clamped at $n_{ps}V_o$, and the decreasing ratio of $i_m$ is the same as that in Mode 3. $L_{lk}$ will resonate with the equivalent switch capacitor $C_{oss1}$ and $C_{oss2}$ in this interval. As the resonant frequency is high and the resistor of the primary winding exists, the amplitude of this resonance will be attenuated to zero soon and $v_{ds1}$ will be stable at $V_{in}+n_{ps}V_o$. At $t_4$, the secondary current $i_s$ decreases to zero and the output diode is turned OFF.

*Mode 5 [$t_4$, $t_5$]:* The switches and the output diode are all turned OFF and the equivalent circuit can be seen in Fig. 3(e). In this period, the primary inductor $L_m$ and $L_{lk}$ will resonate with $C_{oss1}$ and $C_{oss2}$, thus the voltage of $v_{ds1}$ oscillates in this period. This voltage oscillation can also be detected from the auxiliary winding voltage $v_{aux}$.

*Mode 6 [$t_5$, $t_6$]:* The auxiliary switch $M_2$ and the output diode are turned ON at $t_5$. The equivalent circuit is the same as Fig. 3(c). As the voltage of magnetizing inductor $L_m$ is clamped at $n_{ps}V_o$, the magnetizing current $i_m$ will decrease linearly below zero. The primary leakage inductance $L_{lk}$ will resonate with the clamp capacitor $C_c$, and $i_p$ drops below $i_m$. $t_{65}$ is set equal to $t_{32}$, and the charge quantity flow into $C_c$ in $t_{32}$ period will be equal to the discharge quantity flow out of $C_c$ in $t_{65}$ period. At $t_6$, $M_2$ is turned OFF.

*Mode7 [$t_6$, $t_7$]:* The auxiliary switch is turned OFF at $t_6$. $M_1$ is kept off and the output diode is ON in this interval. The equivalent circuit is the same as Fig. 3(d). $L_{lk}$ resonates with $C_{oss1}$ and $C_{oss2}$ in this period, and $v_{\rm ds1}$ drops as the primary current $i_p$ is below zero current in this period.. At $t_7$, $v_{ds}$ drops to zero voltage and the body diode of the main switch $D_{b1}$ conducts.

*Mode 8 [$t_7$, $t_8$]:* The channel of main switch is OFF, but the body diode conducts. The auxiliary switch is OFF and the output diode is ON in this period. The equivalent circuit is shown in Fig. 3(f). The voltage of magnetizing inductor $L_m$ is clamped at $n_{ps}V_o$, and the decreasing ratio of $i_m$ is the same as that in Mode 3. The primary current $i_p$ increases very quickly as the voltage of leakage inductance is large. The increasing slope can

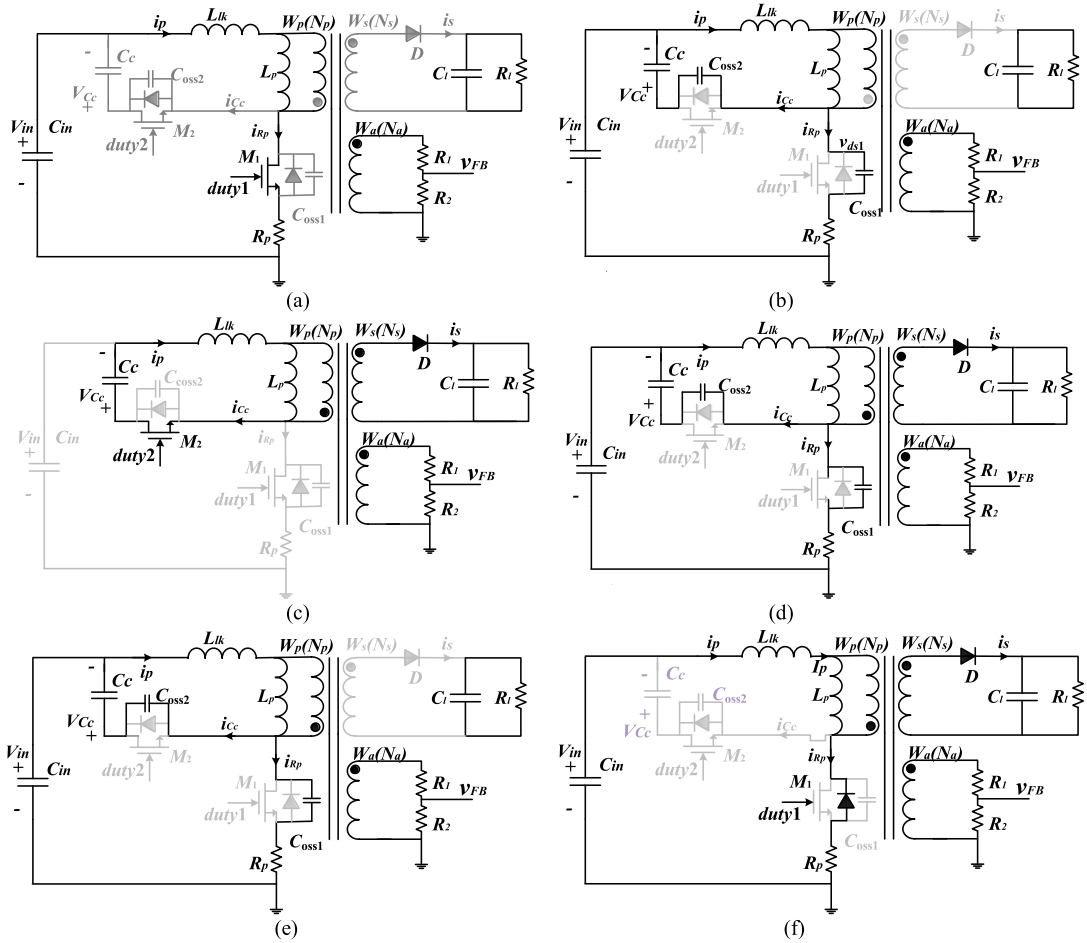



Fig. 3 Equivalent circuits in different intervals: (a) $[t_0, t_1]$; (b) $[t_1, t_2]$; (c) $[t_2, t_3]$ and $[t_5, t_6]$; (d) $[t_3, t_4]$ and $[t_6, t_7]$; (e) $[t_4, t_5]$; (f) $[t_7, t_8]$ and $[t_8, t_9]$.

be expressed as in (6). At $t_8$, the main switch is turned ON

$$Llk\frac{dip(t)}{dt} = Vin + npsVo. \tag{6}$$

*Mode 9 [$t_8$, $t_9$]:* At $t_8$, the channel of main switch is turned ON. The auxiliary switch is OFF and the output diode is ON in this period. The equivalent circuit is shown in Fig. 3(f) which is almost the same as that in Mode 8. At $t_9$, the secondary current $i_s$ drops to zero and another switching cycle begins.

Based on the above analysis, ZVS turn-ON of the main switches is realized. When the voltage of $v_{Cc}$ is close to $n_{ps}V_o$, ZVS turn-ON of the auxiliary switch can be realized. This will be studied in the future work.

## III. Proposed Constant Current Control Method

The output current cannot be sampled directly in the PSRAC flyback converter. Thus, the average current flows through the output diode $I_d$ is kept unchanged as the target output $I_{o\_\mathrm{REF}}$. The equivalent output circuit can be simplified as in Fig. 4. The output load current $i_o$ can be acquired as in (7). $i_o$ contains two part. The first part will decay at a fixed exponential ratio and this part exists only when the load changes. The decay exponential ratio is determined by the time constant of output circuit $\tau$. The second part is equal to the reference output current in stable

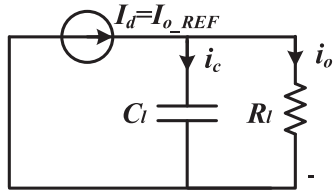



Fig. 4. Equivalent output circuit.

condition. Thus, just keep $I_d$ equal to $I_{o\_\mathrm{REF}}$ and constant output current will be realized. The output load current is equal to the average current of the output diode $I_d$. The current precision of $I_d$ is the current precision of the output load current

$$io(t) = (io(0) - Io\_REF)e^{(-\frac{t}{\tau})} + Io\_REF,\ \tau = ClRl. \tag{7}$$

As in (8), the average diode current $I_d$ is calculated from the integration of the secondary current $i_s$. $T_s$ is the switching period. As $i_s$ is proportional to the difference between the magnetizing current $i_m$ and the primary current $i_p$, $I_d$ can be acquired from the primary parameters. As in (9), $I_d$ is acquired based on $i_p$ and $i_m$.

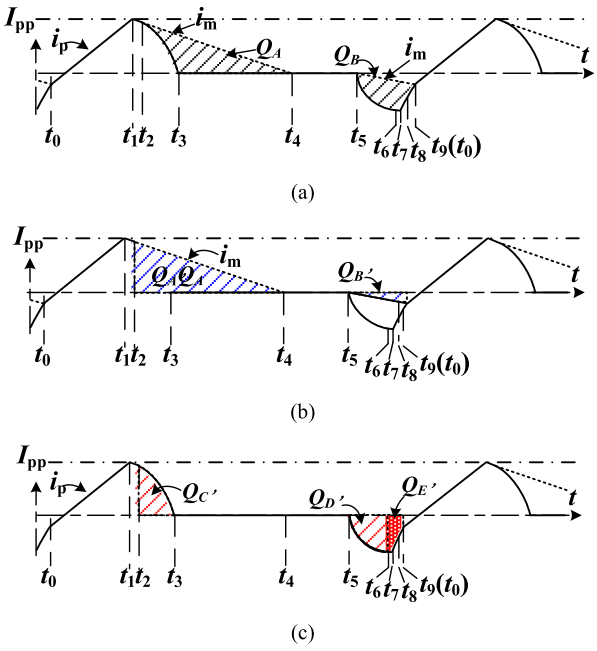



Fig. 5. Current waveforms of $i_p$ and $i_m$. (a) $Q_A$ and $Q_B$. (b) $Q_{A'}$ and $Q_{B'}$. (c) $Q_{C'}$, $Q_{D'}$ and $Q_{E'}$.

As in Fig. 5(a), $Q_A$ and $Q_B$ are two areas where $i_m$ is larger than $i_p$. To keep $I_d$ constant, $Q_A$ and $Q_B$ need to be calculated. $i_m$ can be seen as a linear current in the different modes of the switching cycle. However, $i_p$ is not linear especially in Modes 3, and 6–9. Thus, the output current cannot be acquired directly

$$Id = \frac{1}{Ts}\int_{t0}^{t9} is(t)dt \tag{8}$$

$$Id = \frac{1}{Ts}\int_{t0}^{t9} is(t)dt = \frac{1}{Ts}\int_{t0}^{t9} nps(im(t) - ip(t))dt = \frac{nps(QA + QB)}{Ts}$$

$$QA = \frac{1}{Ts}\int_{t2}^{t4} (im(t) - ip(t))dt,\ QB = \frac{1}{Ts}\int_{t5}^{t9} (im(t) - ip(t))dt. \tag{9}$$

When $i_m$ is equal to $i_p$, $i_s$ is equal to zero, the output current can be re-expressed as in (10). To eliminate the nonlinearity in the output current estimation, the integration of $i_m$ from $t_2$ to $t_9$ can be calculated as $i_m$ is linear. $Q_{A'}$ and $Q_{B'}$ are the shadow area in Fig. 5(b). The integration of $i_p$ from $t_2$ to $t_9$ can divided into three parts as in Fig. 5(c). $Q_{C'}$, $Q_{D'}$, and $Q_{E'}$ are the shadow areas. The clamp capacitor $C_c$ is only charged by the primary current $i_p$ during Mode 3 and the charge quantity is represented by $Q_{C'}$. $C_c$ is only discharged by $i_p$ during Mode 6 and the discharge quantity is represented by $Q_{D'}$. In stable control, considering the charge balance of the clamp capacitor, $Q_{C'}$ is equal to $Q_{D'}$. Since $Q_{E'}$ is very small compared to $Q_{A'}$ and $Q_{B'}$, the output current can be nearly acquired just based on $Q_{A'}$ and $Q_{B'}$. As $Q_{B'}$ is rather smaller than $Q_{A'}$, $I_d$ can be further simplified as in (11) and this is same as the current calculation method in traditional PSR flyback converter

$$\begin{aligned} Id &= \frac{nps}{Ts}\int_{t2}^{t9} im(t)dt - \frac{nps}{Ts}\int_{t2}^{t9} ip(t)dt \\ &= \frac{nps}{Ts}\left(\int_{t2}^{t4} im(t)dt + \int_{t5}^{t9} im(t)dt\right) \\ &\quad - \frac{nps}{Ts}\left(\int_{t2}^{t3} ip(t)dt + \int_{t5}^{t6} ip(t)dt + \int_{t6}^{t9} ip(t)dt\right) \\ &= \frac{nps}{Ts}(Q_{A'} - Q_{B'}) - \frac{nps}{Ts}(Q_{C'} - Q_{D'} - Q_{E'}) \\ &= \frac{nps}{Ts}(Q_{A'} - Q_{B'}) + \frac{nps}{Ts}Q_{E'} \\ &\approx \frac{nps}{Ts}(Q_{A'} - Q_{B'}) \end{aligned} \tag{10}$$

$$Id \approx \frac{nps}{Ts}Q_{A'}. \tag{11}$$

The shadow area of $Q_{A'}$ and $Q_{B'}$ can be predicted as in (12) and (13). $t_{95}$ can be nearly represented by $t_{75}$ as $t_{97}$ is rather small compared to $t_{75}$. As $C_{oss1}$ and $C_{oss2}$ are very small, $t_{21}$ is very small and $i_p$ is nearly unchanged. Thus, $i_p$ at $t_2$ is equal to $I_{pp}$. As the shadow areas of $Q_{A'}$ and $Q_{B'}$ are linear, (10) can be expressed as in (14). $I_{pp}$ is the peak current which is already known. $t_{42}$ is the demagnetization time which can be acquired based on the feedback voltage $v_{FB}$. As $t_{76}$ is negligible compared to $t_{65}$, $t_{75}$ is replaced by $t_{65}$ which is the switch turn-ON time of auxiliary switch. Equation (11) can be calculated as in (15)

$$QA' = \int_{t2}^{t4} im(t)dt = \frac{t42ip(t2)}{2} \tag{12}$$

$$QB' = -\int_{t5}^{t9} im(t)dt \approx \frac{t75ip(t7)}{2} \tag{13}$$

$$Id = Io \approx \frac{npst42ip(t2)}{2Ts}\left(1 - \frac{t75^2}{t42^2}\right) \approx \frac{npsIppt42}{2Ts}\left(1 - \frac{t65^2}{t42^2}\right) \tag{14}$$

$$Id \approx \frac{npst42ip(t2)}{2Ts} = \frac{npsIppt42}{2Ts}. \tag{15}$$

After $I_d$ is acquired, the current error is calculated and proportional-integral-differential (PID) modulation method is used to calculate the control parameters including the primary peak current, the auxiliary switch turn-ON time, and the switching period. $I_d$ is kept equal to the target output current $I_{o\_\mathrm{REF}}$ to realize constant output current control.

## IV. Realization of the Proposed Control Method

The realization method of the proposed control will be analyzed in this part. The closed control loop is shown in Fig. 6. Only a DAC, three comparators, and a digital controller are used. The average diode current $I_d$ is first calculated and then

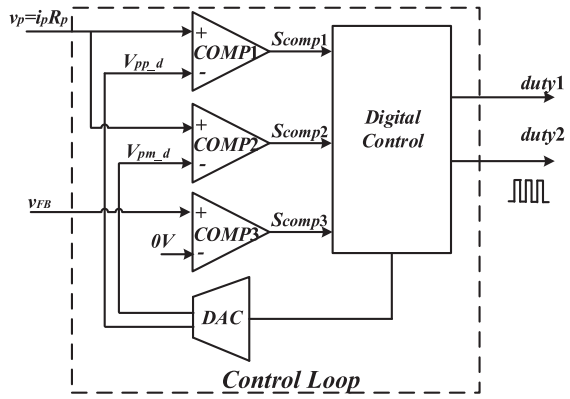



Fig. 6. Components of the control loop.

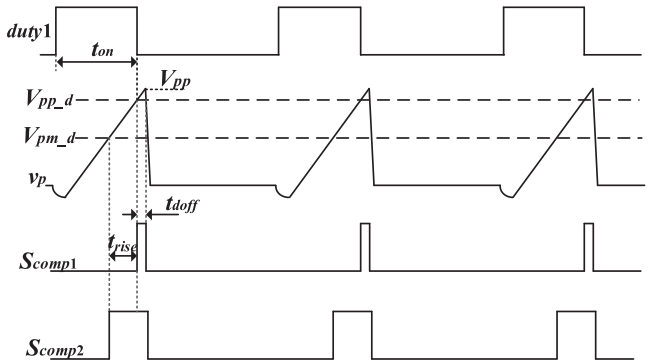



Fig. 7. Peak current calculation waveforms.

controlled with PID modulation method. PFM mode with peak current control is used to modify the control parameters.

### A. Average Diode Current Calculation

As analyzed in the previous part, to calculate the average output current $I_d$, the primary peak current $I_{pp}$, the demagnetization time $t_{42}$, the auxiliary switch turn-ON time $t_{75}$, and the switching period $T_s$ are required. $T_s$ and $t_{75}$ are given by the control loop. As the switch turn-OFF delay exists, the actual peak current $I_{pp}$ is larger than the peak current $I_{pp\_d}$ set by the DAC. To calculate the output current, the accurate value of $I_{pp}$ needs to be acquired and $t_{42}$ should also be detected.

*1)* $\mathrm{I_{pp}}$ *Calculation:* Peak current control method is used for its simple control and low cost. The waveform is shown in Fig. 7. The corresponding current sensing voltage $v_p$ is compared with $V_{pp\_d}$ and $V_{pm\_d}$, and the comparison results are $S_{comp1}$ and $S_{comp2}$, respectively. $V_{pp\_d}$ and $V_{pm\_d}$ are the two output voltages of the DAC, and they are determined by the corresponding digital values $V_{pp\_dig}$ and $V_{pm\_dig}$ as in (16). $V_{DAC}$ and $N$ are the reference voltage and the bit number of the DAC, respectively. $V_{pp\_dig}$ is used to define the primary peak current, and $V_{pm\_dig}$ is used to detect the increasing current slope and calculate the actual peak current $I_{pp}$. $V_{pm\_dig}$ is defined as in (17), where $k$ is a positive constant value smaller than 1. Current

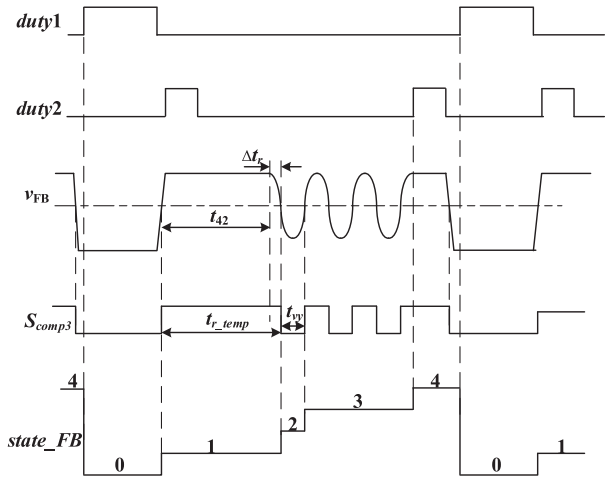



Fig. 8. Demagnetization time calculation.

$i_p$, $I_{pp\_d}$, $I_{pm\_d}$, and $I_{pp}$ can be acquired from $v_p$, $V_{pp\_d}$, $V_{pm\_d}$, and $V_{pp}$ as in (18).

When $v_p$ is higher than $V_{pp\_d}$, $S_{comp1}$ turns high, and the control signal of main switch *duty*1 turns low. As the turn-OFF delay $t_{\mathrm{doff}}$ exists, the main switch is actually turned OFF after a time period of $t_{doff}$, and $v_p$ rises above $V_{pp\_d}$. $t_{doff}$ can be acquired by calculating the time length when $S_{\mathrm{comp1}}$ is high. The time length when $v_p$ rises from $V_{pm\_d}$ to $V_{pp\_d}$ is represented by $t_{\mathrm{rise}}$ which can be obtained from the time length when $S_{\mathrm{comp1}}$ is low and $S_{\mathrm{comp2}}$ is high. As $v_p$ is linear during the switch-ON period $t_{\mathrm{on}}$, the peak voltage $V_{pp}$ can be acquired as in (19). Based on (16)–(19), the actual primary peak current $I_{pp}$ can be obtained as in (20). As $V_{DAC}$, $R_p$, $N$, and $k$ are unchanged, $I_{pp}$ can be calculated from $V_{pp\_\mathrm{dig}}$, $t_{\mathrm{rise}}$, and $t_{\mathrm{dof}}$

$$\begin{cases} Vpp\_d = \frac{Vpp\_\mathrm{dig}}{2^N} VDAC \\ Vpm\_d = \frac{Vpm\_\mathrm{dig}}{2^N} VDAC \end{cases} \tag{16}$$

$$Vpm\_\mathrm{dig} = k \bullet Vpp\_\mathrm{dig} \tag{17}$$

$$\begin{cases} vp = ipRp \\ Vpp\_d = Ipp\_dRp \\ Vpm\_d = Ipm\_dRp \\ Vpp = IppRp \end{cases} \tag{18}$$

$$\frac{Vpp\_d - Vpm\_d}{t\mathrm{rise}} = \frac{Vpp - Vpp\_d}{td\mathrm{off}} \tag{19}$$

$$Ipp = \frac{VDAC}{2^N Rp}\left[1 + \frac{td\mathrm{off}}{t\mathrm{rise}}(1-k)\right] Vpp\_\mathrm{dig}. \tag{20}$$

*2) Detection of the Demagnetization Time* $\mathrm{t}_{42}$*:* As in Fig. 8, the demagnetization time $t_{42}$ is acquired by comparing the feedback voltage $v_{FB}$ with zero voltage. $S_{\mathrm{comp3}}$ is the comparison result and *state_FB* is a state variable derived from *duty*1 and $S_{\mathrm{comp3}}$. As in (21), the demagnetization time $t_{42}$ can be acquired from $t_{r\_\mathrm{temp}}$ and $\Delta t_r$. $t_{r\_\mathrm{temp}}$ is the time length when *state_FB* equals 1. $\Delta t_r$ is one quarter of the resonance period in dead time period which can be acquired from $t_{vy}$. $t_{vy}$ is half the resonance period which is the time length when *state_FB* equals 2. Thus,

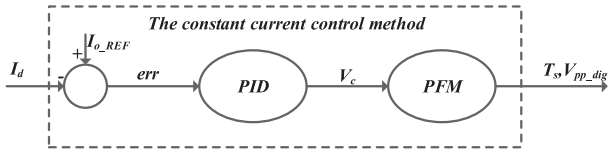



Fig. 9. Constant current control method.

$t_{42}$ can be obtained from $t_{r\_\mathrm{temp}}$ and $t_{vy}$ as in (22)

$$t42 = tr\_\mathrm{temp} - \Delta tr \tag{21}$$

$$t42 = tr\_\mathrm{temp} - tvy/2. \tag{22}$$

After $I_{pp}$ and $t_{42}$ are obtained, as $T_s$ and $t_{75}$ are already known, the average diode current $I_d$ can be calculated based on (14).

### B. Control Method

The control method is shown in Fig. 9. As the average diode current $I_d$ is obtained, PFM mode is used in the closed control loop. The primary peak current is kept unchanged, and $V_{pp\_pfm}$ is the corresponding voltage. As in (23), $V_{pp\_d}$ of the $n$th switching cycle is equal to $V_{pp\_pfm}$. The difference between the reference load current $I_{o\_\mathrm{REF}}$ and the average diode current $I_d$ is first calculated and then PID modulation method is used to calculate the switching period $T_s$

$$Vpp\_d(n) = Vpp\_pfm. \tag{23}$$

In stable conditions, the auxiliary switch turn-ON time $t_{65}$ is equal to $t_{32}$ and the active clamp voltage $V_{Cc}$ is kept higher than $n_{ps}I_oR_l$. As the clamp capacitance is large enough, the voltage ripple of clamp voltage $V_{Cc}$ is negligible and it can be seen as a dc voltage. The primary current decreases linearly in Mode 3 as in (24). $V_{\mathrm{con}}$ is a constant voltage which is the difference between $V_{Cc}$ and $n_{ps}I_oR_l$. As in (25), $V_{con}$ is kept unchanged in different input and output conditions when $t_{32}$ is set proportional to the actual primary peak current $I_{pp}$. Considering the charge balance principle, $t_{65}$ is equal to $t_{32}$

$$VCc - npsIoRl = Llk\frac{Ipp}{t32} = V\mathrm{con} \tag{24}$$

$$t32 = \frac{Llk}{V\mathrm{con}}Ipp. \tag{25}$$

In $t_{32}$ or $t_{65}$ period, $i_p$ decreases faster than $i_m$, and $V_{\mathrm{con}}$ should be larger than a critical value. To avoid potential drain–source breakdown voltage, $V_{\mathrm{con}}$ should be smaller than a maximum value. Thus, $V_{\mathrm{con}}$ should satisfy (26). $R_{l\max}$ is the maximum load resistance. The minimum is determined by the leakage inductance $L_{lk}$. The maximum value is limited by the maximum drain-to-source voltage $V_{ds\max}$, the maximum input dc voltage $V_{in\max}$ and the maximum load resistance $R_{l\max}$. When $V_{\mathrm{con}}$ gets lower, $t_{32}$ and $t_{65}$ is larger and the conduction loss gets larger. When $V_{\mathrm{con}}$ is higher, $t_{32}$ and $t_{65}$ is smaller and the conduction loss gets smaller. But the maximum drain-to-source voltage is improved and the leakage inductance needs to be improved

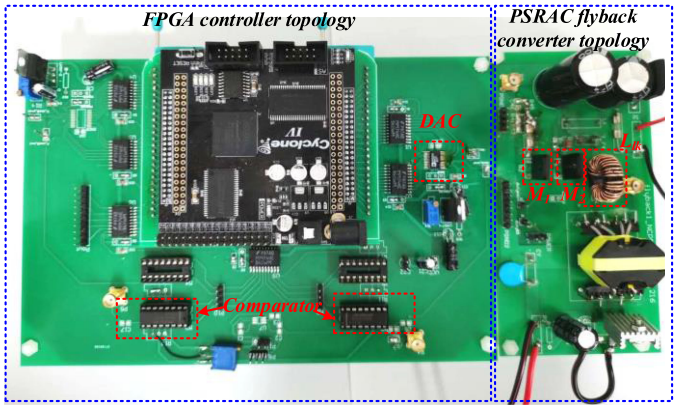



Fig. 10. Prototype of the CC controlled PSRAC flyback converter.

$$npsIoRl\max\frac{Llk}{V} < Lpcon < VBD\_DSS - Vin\max - npsIoRl\max. \tag{26}$$

With the proposed control method, actual primary peak current and the demagnetization time are obtained and the output current can be acquired. The cost is low as only three comparators, one DAC and a digital controller are used.

## V. Experimental Verification

A constant current digital control method with peak current control for a PSRAC flyback converter is analyzed in Section III and IV. To verify the presented control, an experimental prototype of PSRAC flyback converter is established. The output of the ac–dc converter is 5.4–10.8 V/1.80 A. The prototype is shown in Fig. 10. The FPGA controller topology contains a DAC, three comparators, and an FPGA which is used to realize the digital control algorithm. A 100 MHz clock is used in the digital control algorithm.

As seen in Fig. 1, the main parameters of this prototype for calculation and experiment are listed in Table I.

### A. Working Waveforms

The realization of the proposed control is described in the following part. $V_{pp\_d}$ and $V_{pm\_d}$ are the two output voltages of a 10 bit DAC, and the reference voltage of the DAC is 2.5 V. For simplicity, $k$ in (17) is equal to 1/2. In PFM mode, $V_{pp\_\mathrm{dig}}$ is equal to 650 and the corresponding current is 1.443 A. The switching frequency varies from 16.1 to 38.5 kHz. The turn-ON time of auxiliary switch $M_2$ is proportional to the actual peak current $I_{pp}$. When $I_{pp}$ is equal to 1 A, $t_{32}$ and $t_{65}$ are set as 2.25 $\mu$s and the difference between $v_{Cc}$ and $n_{ps}I_oR_l$ is nearly around 40 V.

Fig. 11shows the stable working waveforms in different input and output conditions. The output diode current $i_s$ is not linear. Thus, traditional constant current control methods in PSR flyback converter need modification. Before the main switch is turned ON, the drain-to-source voltage of main switch $v_{ds1}$

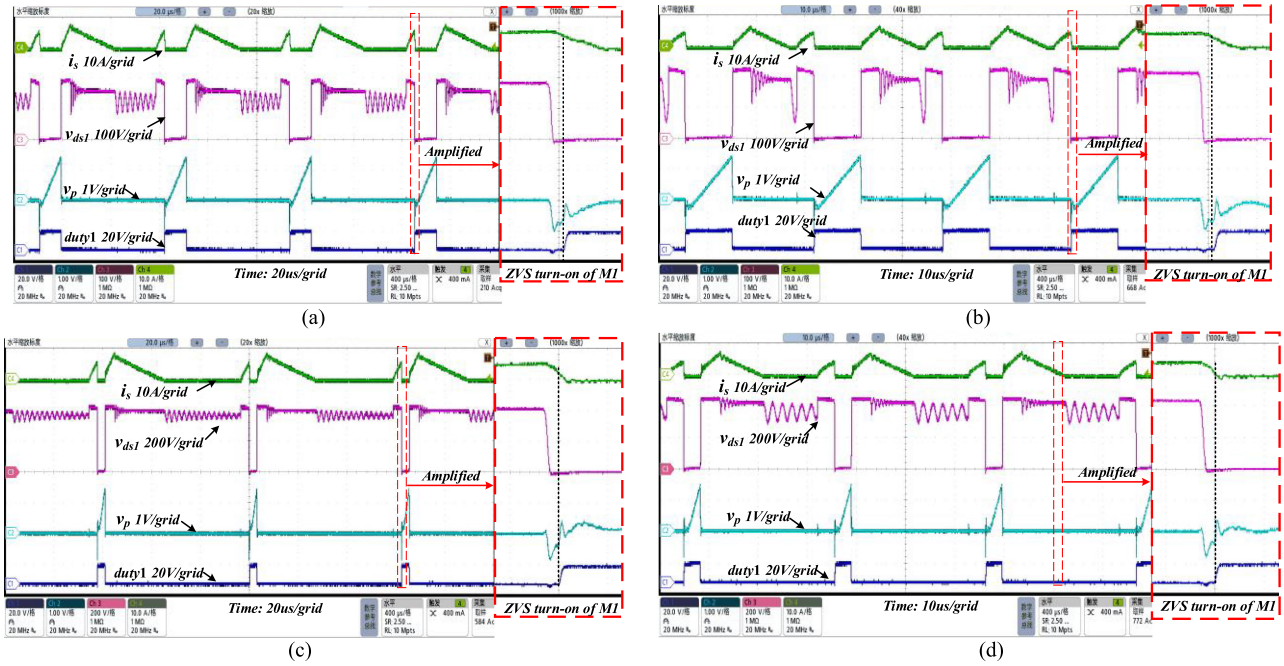



Fig. 11 Working waveforms of the proposed PSRAC flyback converter. (a) 90 Vac, 3 Ω. (b) 90 Vac, 6 Ω (c) 265 Vac, 2 Ω. (d) 265 Vac, 5 Ω.

TABLE I
PARAMETERS OF THE PROTOTYPE

| Quantity | Value | Unit | Remarks |
|---|---|---|---|
| M1, $M_2$ | -- | -- | STF5N62K3 |
| $V_{in}$ | 90~265 | $V_{ac}$ | -- |
| $R_L$ | 3~6 | Ω | |
| $R_p$ | 1.0 | Ω | -- |
| $I_o$ | 1.80 | A | -- |
| $N_p$:$N_s$:$N_a$ | 48:8:4 | -- | RM10 bobbin and PC40 core |
| $L_p$ | 636 | uH | -- |
| $L_{lk}$ | 76 | uH | -- |
| $C_l$ | 680 | uF | -- |
| $C_c$ | 220 | nF | CGA5L3X7T2E224K160AE |
| $D_l$ | -- | -- | NTST30100CTG |
| $R_1$ | 40k | Ω | -- |
| $R_2$ | 10k | Ω | -- |
| *DAC* | -- | -- | AD5333BRUZ |
| *Comparator* | -- | -- | Max912CPE |
| *FPGA* | -- | -- | Cyclone IV(EP4CE15F17C8N) |

drops to zero and ZVS turn-ON of the main switch is realized. The primary peak voltage of $v_p$ is around 1.46 V.

In stable condition, the primary current sensing voltage $v_p$, the auxiliary winding voltage $v_{\rm aux}$, and the two output voltage of DAC $V_{pp\_d}$ and $V_{pm\_d}$ are shown in Fig. 12. For simplicity, $k$ in (17) is equal to 1/2 and $V_{pm\_d}$ is half of $V_{pp\_d}$. Peak current control is realized with $v_p$ and $V_{pp\_d}$. The demagnetization time $t_{42}$ is acquired by comparing $v_{\rm aux}$ with zero voltage.

Fig. 13 shows the dynamic waveforms when the load changes. The input voltage is 220Vac. When the load changes from 3 to 6 Ω, a current shrink is observed in the output load current and it returns to the stable value within 21.3 ms after the load changes. When the load changes from 6 to 3 Ω, a current spike is observed in the output load current and it returns to the stable value within 14.9 ms after the load changes. The control is stable in the dynamic transition.

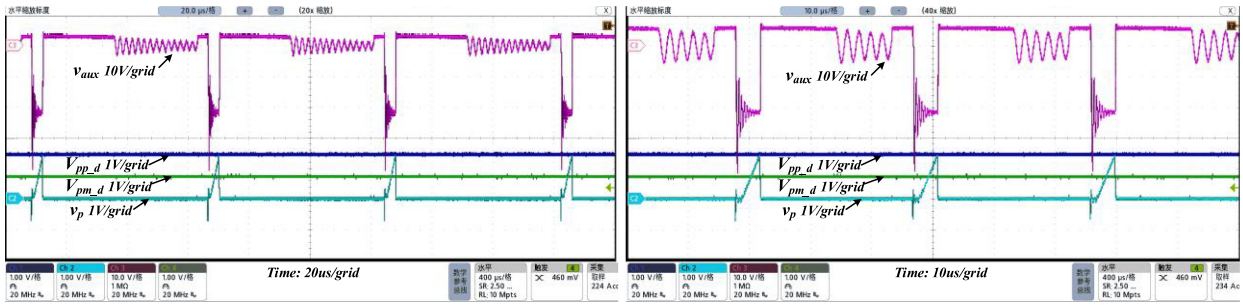
### B. Output Current Precision

The average diode current is calculated from (14) and it is kept unchanged with PID modulation method. The load current accuracy of the proposed control method is shown in Fig. 14(a). The output current varies from 1.778 to 1.819 A, and the accuracy is within 1.2%. Thus, high precision of the output current can be acquired with the proposed control method.

The average diode current can be simplified and calculated as in traditional PSR flyback converter from (15) and it is kept unchanged. The output current accuracy is shown in Fig. 14(b). As the calculated result of (15) is larger than the theoretical result, the actual output current will be lower than the target output current. When the load resistance increases, $t_{42}$ is reduced as the output voltage increases. As $t_{65}$ is nearly unchanged, referring to (15), the calculated diode current gets larger than the theoretical value. Thus, the output current decreases. The output current varies from 1.644 to 1.753 A, and the accuracy is within 8.7%. This traditional control method is simpler and it can only be used in applications which does not need high current accuracy.

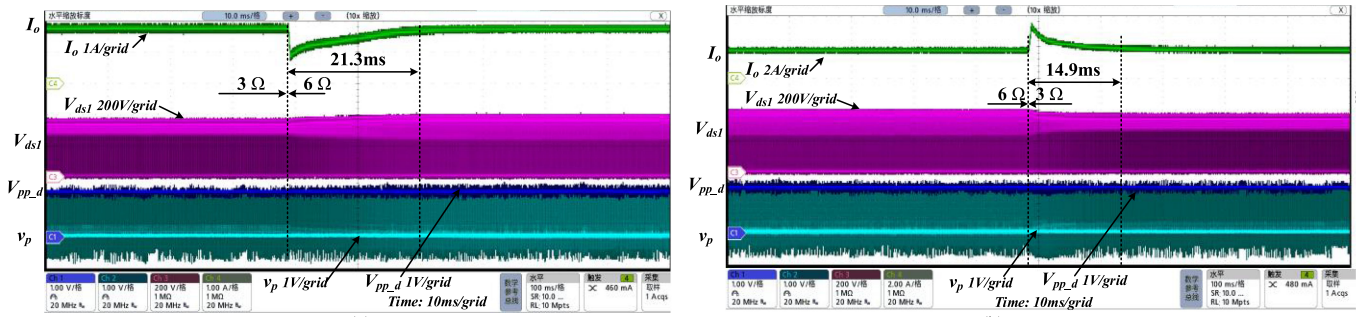
### C. Total Efficiency

A comparison has been made between the proposed PSRAC flyback converter and the traditional PSR flyback converter as in Fig. 15. The total efficiency of the proposed control method is shown in Fig. 15(a). Power efficiency is in the range of




(a) (b)

Fig. 12 Waveforms of $v_p$, $V_{pp\_d}$, $V_{pm\_d}$, and $v_{\rm aux}$. (a) 220 Vac input voltage with 3 Ω load. (b) 220 Vac input voltage with 6 Ω load.




(a) (b)

Fig. 13 Dynamic performance of the proposed control method. (a) Load changes from 3 to 6 Ω with 220 Vac input voltage. (b) Load changes from 6 to 3 Ω with 220 Vac input voltage.

TABLE II
CURRENT PRECISION COMPARISON WITH OTHER WORKS

| Symbol | [6] | [8] | [10] | [12] | [14] | This work | |
|---|---|---|---|---|---|---|---|
| | | | | | | (a) Traditional control | (b) Proposed control |
| Power | 3.2W | 8.4/60W | 9.5W | 60.8W | 10.5W | 19.44W | 19.44W |
| Output Current | 0.8A | 0.35/1.4A | 0.37A | 3.8A | 2.1A | 1.8A | 1.8A |
| CCM or DCM | DCM | DCM | DCM | CCM+DCM | DCM | DCM | DCM |
| Topology | PSR flyback | PSR flyback | PSR flyback | PSR flyback | PSR flyback | PSRAC flyback | PSRAC flyback |
| Current Precision | ±1.9% | ±2.0% | ±1.5% | ±1.8% | ±2% | ±8.7% | ±1.2% |

Illustration: (a) Traditional control method in constant current control PSR flyback converters; (b) The proposed accurate constant current control method for PSRAC flyback converter.

80.0%–86.5%. Replace the active-clamp circuit with traditional resistor-capacitor-diode (RCD) circuit and keep the parameters of the topology and the control loop unchanged. The total efficiency of traditional flyback converter is shown in Fig. 15(b). The efficiency is in the range of 77.0%–82.9%. Compared to traditional flyback converter, the peak efficiency of the PSRAC flyback converter is improved by 3.6%.

As in Fig. 16, power loss breakdown of the proposed active-clamp method and traditional RCD clamp circuit was committed using a combination of simulation, measurement, and calculation. The input voltage was 265Vac and the load resistance is 6 Ω. When active-clamp circuit is used, the power loss of the switches $P_{mos}$ are reduced. As in Fig. 17, the switching loss of the two switches $P_{sw}$ is reduced as soft-switching technique is realized, however the conduction loss $P_{\rm con}$ is improved as the conduction time is longer.

The power loss of the transformer $P_{Lm}$ increases as the core loss is improved with larger variation of magnetic flux density. The power loss of the external leakage inductance $P_{Lk}$ is smaller than the power loss of the RCD clamp circuit $P_{\rm RCD}$. $P_d$ is the power loss of the output diode which is nearly unchanged. $P_{\rm other}$ is the power loss of other devices including the input rectifier

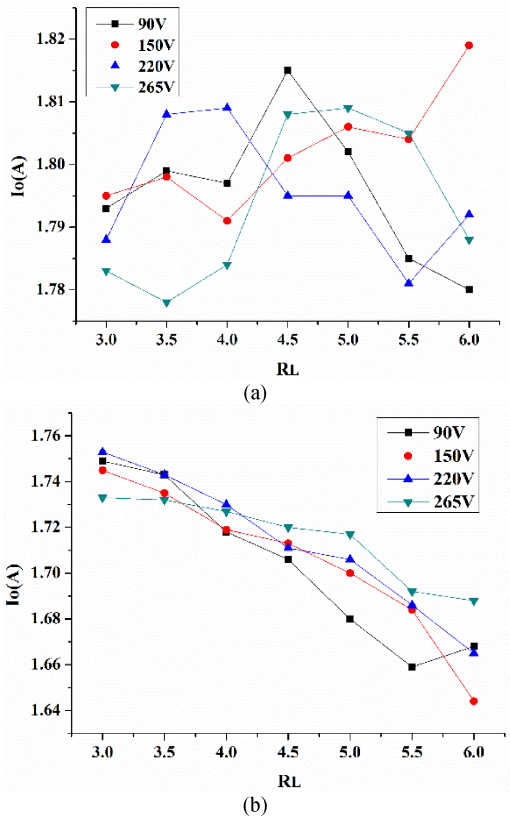



Fig. 14 Tested output current accuracy with different output current calculation methods. (a) Accurate output current calculation method. (b) Simplified output current calculation method.

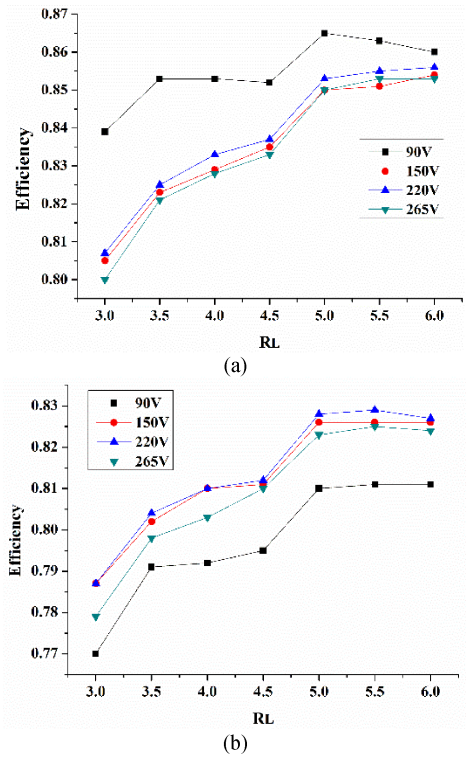



Fig. 15. Efficiency of the two converter topologies. (a) PSRAC flyback converter. (b) Traditional PSR flyback converter.

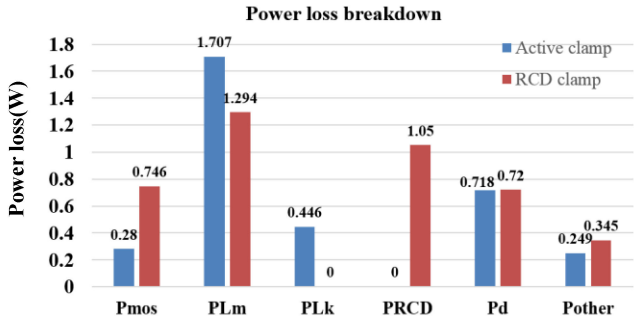



Fig. 16. Power loss breakdown of flyback converter with two clamp circuits.

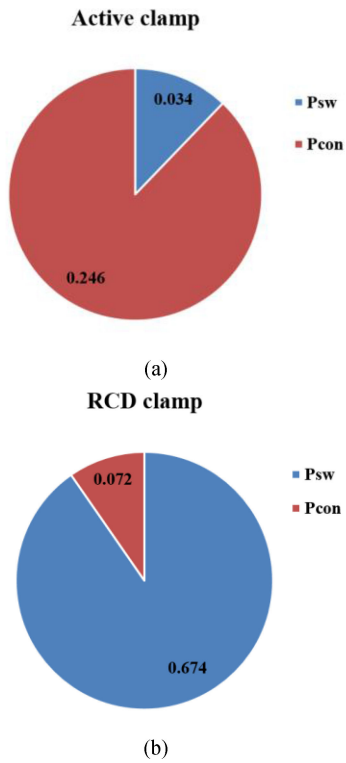



Fig. 17. Power loss of switches of flyback converter with two clamp circuits. (a) Active clamp. (b) RCD clamp.

bridge, the current sampling resistor, the input filter circuit, and the output capacitor.

### *D. Comparison With Other Works*

The current precision comparison with other work is shown in Table II. Compared to other PSR controlled flyback converters, active clamp technique and constant output current are realized in the proposed PSRAC flyback converter. The output current can be estimated accurately based on charge balance principle and the accuracy of the output current is within 1.2%. When the traditional control method is applied, the current accuracy is 8.7% which is much lower.

As analyzed, soft-switching technique is realized in PSRAC flyback converter with DCM mode. The output diode current can be predicted from primary parameters and the control parameters

given by the control loop. Constant output current is realized and high precision of the output current is also achieved.

## VI. Conclusion

Active-clamp flyback converter can realize soft-switching technique by adding an auxiliary switch compared to traditional flyback converter. However, optocoupler used in the feedback loop introduces problems like CTR degradation and temperature drift. To remove the optocoupler, a constant current controlled PSRAC flyback converter is proposed in this article. As the current that flows through the output diode is nonlinear when soft-switching technique is used, traditional constant current controlled method for PSR flyback converter cannot be used directly. Base on the charge balance principle, a new constant current digital control method is further proposed for PSRAC flyback converter. The average diode current can be predicted from the primary current and the auxiliary winding voltage. Peak current control is used in the control loop and it only contains a low-speed DAC, three comparators, and a digital controller. The proposed control scheme was verified by a FPGA controlled 5.4–10.8 V/1.80 A PSRACF converter. PFM mode is used and fully soft-switching of main switch is realized. The control is also stable during dynamic transition. The output current accuracy is high and is within 1.2% in different input and output condition. And, the peak efficiency is improved by 3.6% compared to traditional PSR flyback converter with RCD clamp circuit.

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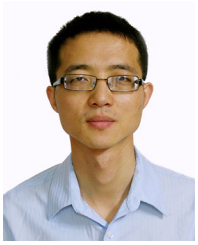

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