A Clamped and Harmonic Injected Class-E Converter With ZVS and Reduced Voltage Stress Over Wide Range of Distance in WPT System

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***Abstract*—The inherent frequency of magnetic coupling resonance based wireless power transfer system (MCR-WPT) is up to the level of kHz or even MHz. The class-E converter with zero-voltage switching (ZVS) could eliminate the considerable switching loss, however, the high voltage stress and sensitive ZVS condition to coils distance limit its application seriously in MCR-WPT. To solve the issues, a voltage-clamped class-E converter, consisting of an auxiliary clamped circuit to decrease the voltage stress and a harmonic circuit to realize ZVS against a wide range of coils position, is proposed for the WPT system. According to the harmonic analysis, the relationship among duty cycle, input voltage, amplitudes and phases of the harmonics is obtained. Then, the design strategy for system parameters, especially for the harmonic circuit is presented, so that, ZVS could be maintained over a wide range of coils distance. Meanwhile, the efficiency analysis is also carried out, suggesting a steady high efficiency further. Three design examples with disparate harmonic parameters and ZVS ranges are presented and one of the three examples is selected to make comparison with a typical Class-E WPT system. The experimental results agree with the theoretical analysis well.**

***Index Terms*—Class-E converter, harmonic injection, soft switching, voltage stress, wireless power transfer (WPT).**

NOMENCLATURE

V_{DD}	Input dc voltage.
L_C	Choke inductor.
C_C	Clamping capacitor.
C_S	Shunt capacitor.
S, Sa	Main and auxiliary switches.
L_n, C_n	Inductor and capacitor of the *n*th harmonic circuit.
L_1, C_1	Coil's inductance and capacitor of the primary side.
k	Coupling coefficient of the coils.
L_1, C_{11}	Coil's inductance and capacitor of the secondary side.
R	Real load.
C_O	Rectifier capacitor.
R_L	Equivalent load considering the voltage drop on the rectifier.
i_C	Current of L_C.
I_C	Average value of i_C
v_{Cc}	Voltage on C_C.
V_{Cc}	amplitude of v_{Cc}.
i_{CS}	Current flows through C_S.
v_{Cs}	Voltage on C_S.
V_{Cs}	Amplitude of v_{Cs}.
i_S	Current flows through *S*.
i_{Cc}	Current flows through C_C.
i_1	Current in the primary coil.
I_1	Amplitude of i_1.
i_n	Harmonic current.
I_n	Amplitude of i_n.
i_{11}	Current in the secondary coil.
V_{out}, I_o	Output voltage and current.
R_e	Equivalent resistance on the primary side.
R_{opt}	Optimal load when class-E realize ZVS/ZDS.
M	Mutual inductance.
v_{hn}	*n*th harmonic voltage in v_{Cs}.
V_{hn}	Amplitude of v_{hn}.
v_{fa}	Fundamental voltage in v_{Cs}.
V_{fa}	Amplitude of v_{fa}.
D	Conducting duty cycle of *S*.
T, ω	Period and angular frequency.
φ_1, φ_n	Initial phase of v_{fa} and v_{hn}.
θ_1,θ_n	Phase of v_{fa} and v_{hn} when *S* is turned ON.
α_n	Phase of i_{hn} when *S* is turned ON.
Z_1, Z_n	Reactance of the harmonic and resonant network.
Q_{Cs},	Charge stored in C_S.
Q_{IC}	Charge injected by I_C.
Q_{i1}	Charge injected by i_1.
Q_t	$Q_{IC} + Q_{i1} + Q_{Cs}$.
R_S	Conduction resistance of switches.
R_n	Parasitic resistance in harmonic circuit.
R_{s1}, R_{s11}	Parasitic resistances in resonant network.
V_F	Forward voltage drop of the diode.
P_{Rn}	Power loss on R_n.
P_S	Power loss on R_S.
P_{Rs1}	Power loss on R_{S1}.

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P_t	Total power loss $P_{Rn} + P_S + P_{Rs1}$.
η_p	Efficiency of the primary side.
η_p	System efficiency.

I. Introduction

STRONG coupled coils can achieve wireless power transfer (WPT) in a few millimeters [1]. However, the frequency and power transfer distance are seriously limited due to the leakage inductance, making it inapplicable in many occasions. Magnetic coupling resonance WPT (MCR-WPT) technology uses capacitor to compensate the leakage inductance, and can keep a high efficiency over a middle distance, up to now, it has been applied in electric vehicles, biomedical implanted devices, and household appliances [2]–[9]. In the MCR-WPT systems, the dc source needs to be transformed to high-frequency ac source, correspondingly, considerable switching loss will be introduced. Zero-voltage-switching (ZVS) is an effective technology to solve this issue [10]. Due to the inherent ZVS and zero-derivative-switching (ZDS) feature, the class-E converter becomes one of the most potential candidates for WPT systems [11]–[14]. Based on the traditional design strategy of the class-E converter, WPT systems could attain a high efficiency under the fixed distance and load. However, for the class-E converter-based WPT system, ZVS and ZDS are sensitive to the coils position and can hardly be maintained during the whole operation process, leading potential safety hazard and low efficiency [15]. To solve this issue, parameters tunable technologies, using dc-feed inductor or switched-capacitor matrixes, have been introduced [16], [17]. In these research works, the value of choke inductor or the parameters of matching network could be adaptively tuned, however, the structures are difficult to be implemented.

ZDS is to avoid the current being reversed before the switch is turned ON. In recent research works, unidirectional switches such as MOSFET have been widely used and ZDS becomes no longer necessary for high efficiency [13]. Correspondingly, many design strategies focus on ZVS operation in a wide range of distance and load have been proposed [18]–[20]. However, another drawback lies in that the voltage stress will be influenced by the coils distance and the load. An uncertain voltage stress may breakdown the switches.

In former research works, adding harmonic circuits is a common method to decrease voltage stress [21]–[27]. In [21] and [22], several of harmonic filters are connected in series with the resonant network and the voltage curve on the switch becomes flat, however, as each harmonic requires a filter, the system is complex. In [23]–[26], a second harmonic circuit with much simpler construction is connected in parallel with the switch and the voltage stress can also decrease to 2.6 times of the input voltage under the optimum condition. Furthermore, in [27], harmonic circuit consisting of two inductors and two capacitors were analyzed, similar to the class F and class E/F converter in [21],[22], the voltage stress can decrease to 2.2 times of the input voltage, but, less passive components are needed in the work.

Unfortunately, even though above research works are effective, following drawbacks are pendent for class-E WPT systems.

1) In above researchers, ZVS realization is still on the basis of the reactive current in the resonant network. Namely, there is always a phase difference between the voltage source and the resonant current during the power injection process [20]. This will weaken the power transfer efficiency of the WPT system. How to eliminate the phase difference remains to be solved.
2) R_e of the WPT system is sensitive to the coils distance (the meanings of the symbols are in the nomenclature). In former researchers, after the parameters are determined, ZVS could only be realized when R_e equals to $R_{\rm opt}$, or slightly smaller than $R_{\rm opt}$. Because a larger load leads to a smaller resonant current, namely, less charge can be extracted from the capacitor. On the contrary, when R_e is much smaller than $R_{\rm opt}$, the resonant current will become extremely large, and the shunt capacitor may be recharged.
3) When the resonant current and the choke current are changed due to the fluctuation of R_e, the charge injected in the shunt capacitor of the switch will also varies. As the shunt capacitor is small in typical and improved class-E converters, the drain–switch voltage of the switch will fluctuate seriously [28]. Namely, the voltage stress is still unfixed in former research works, leading system security issue [29].

Therefore, decreasing the voltage stress, decoupling the relationship between voltage stress and external factors, widening the ZVS range, and eliminating the phase difference during the power injection process are still pending issues for class-E converter based WPT systems.

In the article, a clamped and harmonic injected class-E converter with much looser ZVS condition, lower and steadier voltage stress, is employed for the WPT system. Compared with the method of reducing voltage stress using harmonic circuit, the clamped circuit in the proposed converter, consisting of an auxiliary switch and a relatively large capacitor, makes the switch voltage waveform become a quasi-square with a lower voltage amplitude. Meanwhile, because of the clamped capacitor, the amplitude of the clamped voltage could hardly be influenced by external factors, therefore, the system security could be enhanced. In the article, the harmonic circuit connected in parallel with the main switch is employed to provide a steady harmonic current to extract the charge of the shunt capacitor, correspondingly, ZVS could always be realized even when $R_e \geq R_{\rm opt}$. In addition, since ZVS is achieved through the harmonic current, the phase difference between the switch voltage (defined as v_{Cs}) and the main resonant current (defined as i_1) is unnecessary for the proposed topology to realize ZVS. Thus, reactive power in the proposed system can be eliminated and the power transfer efficiency can be enhanced.

The rest of the article is organized as follows. In Section II, the circuit is described, and then the principle and harmonic analysis is developed. The parameter design strategy and efficiency analysis are given in Section III. In Section IV, three design examples with different harmonics circuits and ZVS regions are built up to verify the harmonic analysis and the parameter design strategy, furthermore, one case is selected to make comparison with

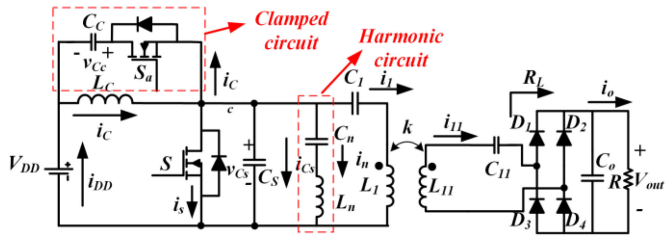

Fig. 1. Configuration of the proposed topology.

typical class-E converter under coils distance change. Finally, a summary is given in the final section.

II. Operation Principle Description and Harmonic Analysis

A. Circuit Description

The proposed topology is presented in Fig. 1 and the series compensation network is employed in the receiver.

V_{DD} is the dc supply voltage source. L_c denotes the choke inductor. S denotes the main switch, providing circuit path for L_c and the resonant network. C_s represents the shunt capacitor across S, which can ensure ZVS by reducing the climb rate of the voltage. L_1 and L_{11} represent the inductance of primary and secondary coils. Relying on the mutual inductance between the two coils, the energy can be transformed from the primary side to the secondary side without contact. The capacitors C_1 and C_{11}, which are placed in series with L_1 and L_{11}, respectively, are the compensation capacitors for the primary and secondary side of the WPT system.

If only the above components are utilized, a traditional class-E WPT system can be made up. Then, to decrease its voltage stress and realize ZVS, a voltage clamped circuit and a harmonic circuit are introduced. S_a is the auxiliary switch in voltage clamped circuit, and a relatively large capacitor C_C is connected in series with it to clamp the voltage on S. C_n and L_n are the capacitor and inductor of harmonic circuit. The nth harmonic current can flow throw the path to extract the charge from C_S. In addition, a rectifier bridge in parallel with a relatively large capacitor C_o is applied in the receiver to filter a dc output, and the relationship between equivalent load R_L and real R is as follows:

$$R_L = \frac{8R}{\pi^2} + \frac{2V_F}{I_O} \tag{1}$$

where V_F is the forward voltage drop on single diode and I_o is the average output current. When I_o is small, the voltage drop on the diode cannot be negligible.

B. Operation Principle

As the principle to achieve ZVS by different harmonics is similar, only the third harmonic is selected as an example to analyze. The typical waveform of the WPT system is shown in Fig. 2, and the current-flow path of each mode is shown in Fig. 3. There are six operating modes in one switching period, and they are described as follows.

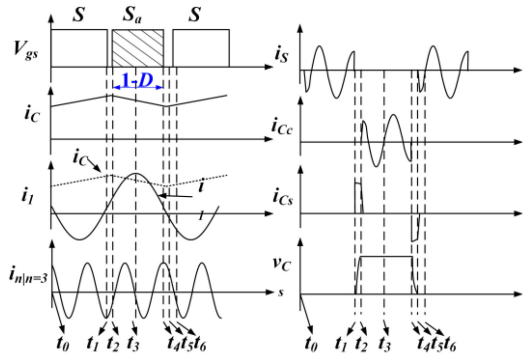

Fig. 2. Key waveform of the WPT system.

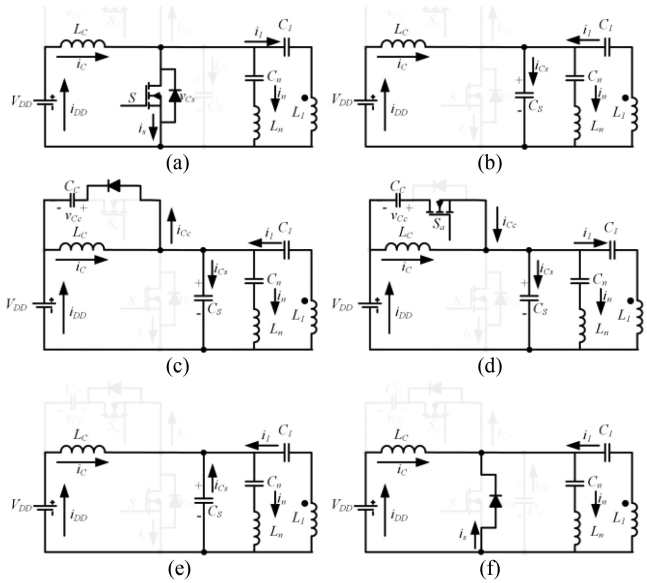

Fig. 3. Current loops of each operation mode for the proposed topology. (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6].

Mode 1 [t_0, t_1]: Before t_1, the S is turned ON and S_a is turned OFF. Choke inductor L_C is charged by the dc source V_{DD}, therefore, i_C increases linearly. Meanwhile, the main resonant current i_1 and the harmonic current i_n flow through S. During the mode, the capacitor C_C is never charged nor discharged.

Mode 2 [t_1, t_2]: During this mode, both S and S_a are OFF and i_s becomes zero. C_S is charged by i_{Cs}, which is the sum of i_C, i_n, and i_1. Due to the voltage clamping feature of C_S, v_{Cs} rises from zero slowly. Then, as both i_s and v_{Cs} are about zero at t_1, zero-voltage turn-OFF is realized on S. Meanwhile, the main resonant circuit consists of C_1 and L_1 begins to be charged.

Mode 3 [t_2, t_3]: At t_2, voltage v_{Cs} equals to the sum of v_{Cc} and V_{DD}. Thus, the body diode of the clamped switch S_a begins to conduct, then, C_C and C_S are charged together. Due to the large capacitance of C_C, most of the current goes through C_C and its voltage v_{Cc} barely changes, thus, v_{Cs} is clamped. As the body diode of S_a conducts, S_a can achieve ZVS during the mode.

Mode 4 [t_3, t_4]: Switch S is still OFF and S_a is ON. C_C and C_S are charged or discharged together. Similar to the mode 3, the main resonant circuit is still charged.

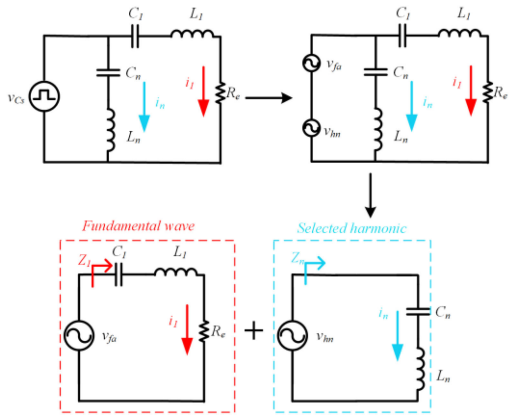

Fig. 4. Equivalent circuit of the proposed topology for harmonic analysis.

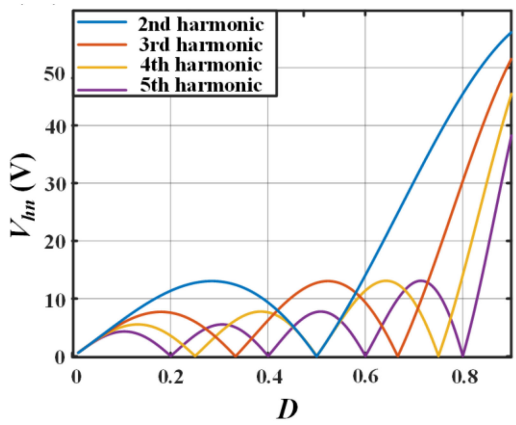

Fig. 5. Variation in V_{hn} with respect to D.

Mode 5 [t_4, t_5]: At t_4, the clamping switch S_a is turned OFF, C_C stops discharging and the harmonic current i_n continues to discharge C_S. However, due the voltage clamping feature of C_S and C_C, the drain–source voltage v_{Sa} of S_a rises from zero slowly and ZVS can be achieved on S_a.

Mode 6 [t_5, t_6]: At t_5, C_S finishes discharging. i_1, i_n and i_C flow through the body diode of S. As v_{Cs} is clamped to zero, ZVS can be achieved if S is turned ON during the mode.

C. Harmonic Analysis

Before analyzing, the proposed topology is simplified.

1) The series type receiver of the WPT system is considered as an equivalent resistance R_e on the primary side. It can be calculated by the following equation:

$$\begin{cases} R_e = \dfrac{\omega^2 M^2}{R_{s11} + R_L} \\ M = k\sqrt{L_1 L_{11}} \end{cases} \tag{2}$$

where ω is the operation angle frequency of the system, k is the coupling coefficient, M is the mutual inductance, and R_{s11} is the parasitic resistance of L_{11} and C_{11}.

1) In the primary side, only the resonant circuit is kept and the other part is replaced by the voltage source v_{Cs}.
2) As [t_1, t_2] and [t_4, t_5] shown in Fig. 2 are negligible, v_{Cs} is assumed as square voltage.

Fig. 4 shows the corresponding equivalent circuit of Fig. 1. According to FFT, the quasi-square waveform v_{Cs} contains different frequency sine components and the series resonant circuit provides the almost zero impedance for specific frequency. Hence, only v_{fa} (the fundamental element of v_{Cs}) and v_{hn} (the nth harmonic of v_{Cs}) are considerable in the proposed topology. Z_1 denotes the impedance of the main resonant circuit under the fundamental voltage v_{fa} and Z_n denotes the reactance of the harmonic circuit under the nth harmonic voltage v_{hn}

$$\begin{cases} v_{hn} = V_{hn} \sin(\omega n t + \phi_n)\ n = 1, 2, 3, \cdots \\ v_{fa} = v_{hn}\ n = 1 \end{cases} \tag{3}$$

$$\begin{cases} V_{hn} = \sqrt{A_n^2 + B_n^2} \\ A_n = -\dfrac{V_{Cs} \cdot \sin(2\pi n D)}{n\pi} \\ B_n = -\dfrac{V_{Cs} \cdot \cos(2\pi n D)}{n\pi} \end{cases} \tag{4}$$

$$\phi_n = \arctan\left(\frac{A_n}{B_n}\right) \tag{5}$$

where D is the conduction duty cycle of S, V_{hn} is the amplitude of the nth harmonic voltage v_{hn} and φ_n is the initial phase. V_{Cs} is the amplitude of the square voltage v_{Cs}. It can be calculated based on the relationship between V_{Cs} and V_{DD}, and voltage-second balance theory on L_C, which are shown in (6) and (7). The result is shown in the following:

$$V_{Cs} = V_{Cc} + V_{DD} \tag{6}$$

$$\int_0^{DT} V_{DD} dt = \int_0^{(1-D)T} V_{C_C} dt \tag{7}$$

$$V_{C_S} = \frac{V_{DD}}{1 - D} \tag{8}$$

Fig. 5 shows the relationship between D and V_{hn}. Obviously, the nth harmonic has (n–1) zero points when D ranges from 0 to 1. At the zero points, no harmonic current could be provided to release the charge in C_S. Therefore, to realize the ZVS condition, appropriate harmonic should be selected according to the duty cycle.

Theoretically, any harmonic could be employed for ZVS. However, there is less time for high-order harmonic to release the charge in C_S, namely, a larger harmonic current is required to achieve ZVS, leading to a higher loss on the parasitic resistance. Thus, the low-order harmonic is preferred.

In Fig. 5, the envelop line of the second and third harmonic can cover almost all the range of D, therefore, these two harmonics are the best candidate components for ZVS realization due to their low-order.

III. Parameters Design And Efficiency Analysis

The following assumptions are given before analysis.

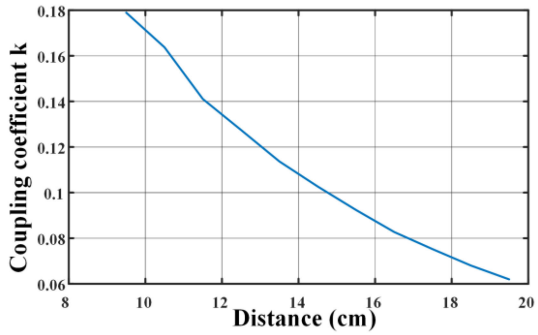

Fig. 6. Relationship between k and the coils distance in the proposed prototype.

1) The choke inductance L_C is large enough so that its current i_C is assumed to be the constant current I_C.
2) The clamped capacitor C_C is large enough and the clamped voltage v_{Cc} is considered to be constant value of V_{Cc}.
3) The resonant current i_1 and i_n are sinusoidal.
4) The parameters of S and S_a are assumed to be the same.
5) C_S is so small that [t_1, t_2] and [t_4, t_5] are neglected. In the other words, it is assumed that [t_1, t_5] approximately equals to [t_2, t_4]. Then, assume the operation period T, the conduction duty cycle D of the main switch S could be defined as follows:

$$D \approx \frac{T-(t_4-t_2)}{T} \tag{9}$$

6) As shown in Figs. 4 and 5, there are numerous of harmonics v_{hi} in v_{Cs}, and only the fundamental wave v_{fa} and the selected harmonic v_{hn} are considered in the article, because the resonant circuits exhibit large reactance under other harmonics.

Furthermore, following notes should also be noticed.

1) k demonstrates the coil distance. Fig. 6 shows the k-distance curve of the coils used in the proposed prototype. Where k between two coils is measured by the WK-6500B impedance analyzer. Seen from the curve, k is negatively correlated to the coils distance.
2) In the following content, R_e is contained in the equations, instead of k and R_L. Obviously in (2), the influence of coupling coefficient k and the load R_L to the system performance equals to the change of equivalent resistance R_e on the primary side. Therefore, the essence of realizing ZVS over a wide range of coils distance and load is to maintain ZVS under a variable R_e.

A. Parameters Design of Harmonic Circuit

I_1 and I_C can influence the released charge. In the section, they are assumed as known quantities and will be calculated in later section.

The harmonic current i_n is required to discharge the shunt capacitor C_s. As a large i_n will results in a high loss, while a small i_n may lose the ZVS condition, an appropriate i_n is needed to keep ZVS operation while introducing a relatively small loss. In this section, an optimal design strategy for the harmonic circuit to realize critical ZVS under the fixed k and R_L is proposed.

To determine the value of i_n, it is necessary to calculate how much charge should be discharged from shunt capacitor C_s. The charge is defined as Q_t. From Figs. 1 and 2, obviously, Q_t is consisted of three parts as follows:

$$Q_t = Q_{Cs} + Q_{Ic} + Q_{i1} \tag{10}$$

where Q_{Cs} is the charge stored in C_S, and it can be calculated out as follows:

$$Q_{Cs} = V_{C_S} C_S = \frac{V_{DD}}{1-D} C_S \tag{11}$$

Q_{Ic} is the charge injected by the choke current I_C, and it can be calculated out as follows:

$$Q_{Ic} = I_C \cdot t_r \tag{12}$$

where t_r is the required time to completely release Q_t, and it should be set based on the switching speed of the applied switch S. I_C will be solved when analyzing the efficiency.

Q_{i1} is the charge injected by the main resonant current i_1, and it can be calculated as follows:

$$Q_{i1} = \int_0^{t_r} I_1 \sin(\omega t + \theta_1)\, dt = \frac{I_1(\cos(\theta_1) - \cos(\omega t_r + \theta_1))}{\omega} \tag{13}$$

where θ_1 is the phase of the fundamental voltage v_{fa}. As the main resonant circuit works in resonant state and there is no phase difference between v_{fa} and i_1, θ_1 also represents the phase of i_1. As to the phase of v_{hn}, it is defined as θ_n. θ_1 and θ_n can be calculated by following equations:

$$\begin{cases} \theta_1 = \varphi_1 + 2\pi(1-D) \\ \theta_n = \varphi_n + 2\pi n(1-D) \end{cases} \tag{14}$$

After Q_t is obtained, the value of i_n to meet ZVS condition can be calculated by following equations:

$$\int_0^{t_r} I_n \sin(\omega n t + \alpha_n)\, dt \geq Q_t \tag{15}$$

$$I_n \geq \frac{Q_t \cdot \omega n}{\cos(\alpha_n) - \cos(\omega n t_r + \alpha_n)} \tag{16}$$

where α_n is the phase of i_n. Different from the main resonant circuit, there is a phase difference between v_{hn} and i_n. As the parasitic resistance of the harmonic circuit has much small weight in the harmonic impedance Z_n, it is negligible when considering the phase of i_n. Therefore, the relationship between α_n and θ_n is as follows:

$$\begin{cases} \alpha_n = \theta_n + \frac{\pi}{2} Z_n < 0 \\ \alpha_n = \theta_n - \frac{\pi}{2} Z_n > 0 \end{cases} \tag{17}$$

In (17), if Z_n is capacitive, the phase difference between i_n and v_{hn} is 90°. Reversely, if Z_n is inductive, it should be –90°. To illustrate the relationship among different phases more clearly, an example of second harmonic is illustrated in Fig. 7. Obviously, when S_a is turned OFF, α_n can influence the direction of i_{hn}, and only when the harmonic current i_{hn} is in positive direction, it can discharge C_S. Namely, when S_a is turned OFF,

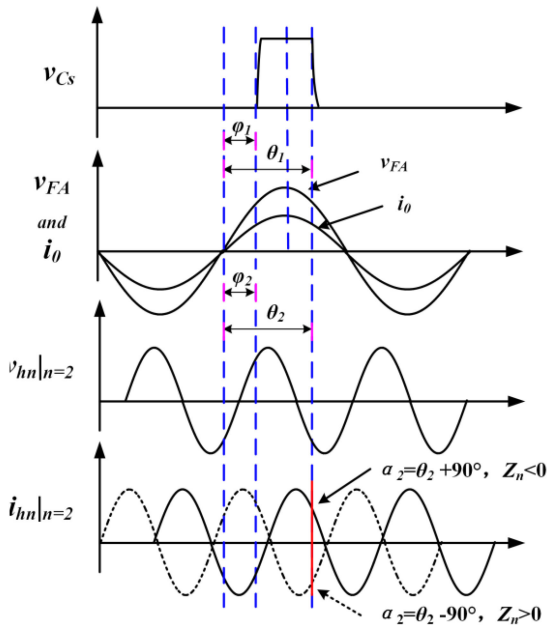

Fig. 7. Phase relationship between different waveforms.

the phase of i_n should in the range of $[0, \pi]$. Therefore, to achieve ZVS, α_n should satisfy the following:

$$\alpha_n \in [2\pi m, \pi + 2\pi m], m = 1, 2 \ldots \tag{18}$$

Based on the above analysis, the key point to design strategy is to set Z_n appropriately, and to satisfy (16) and (18) for ZVS condition. $|Z_n|$ can be calculated by (18), and its sign can be designed according to (17) and (18)

$$|Z_n| = \frac{V_{hn}}{I_n} \tag{19}$$

Then, the relationship between L_n and C_n can be calculated by (20). After one of the two parameters is selected, the other one can be obtained as well

$$L_n = \frac{Z_n}{\omega n} + \frac{1}{C_n \cdot (\omega n)^2} \tag{20}$$

The design strategy introduced above is under the fixed k and R_L (namely, the fixed R_e). In practical, k and R_L in the WPT system varies frequently and R_e can hardly be fixed. To illustrate the ZVS characteristics more clearly, Fig. 8 is given, where k is considered as the variable and R_L is fixed.

Three curves are shown in Fig. 8. The orange curve shows the amplitude of practical harmonic current I_n, it will be independent to k after the harmonic circuit is designed. The red curve denotes R_e calculated by (2). Notice, for the WPT system of SS type, there is positive relationship between k and R_e. Namely, a larger k means a larger R_e, and finally results in a smaller Q_t in shunt capacitor. Correspondingly, as the blue curve shows, a smaller harmonic current is required for ZVS. Therefore, ZVS could always be maintained at $R_e \geq R_{\text{opt}}$.

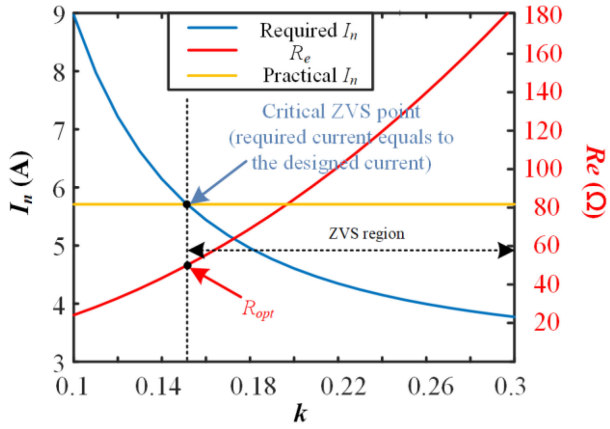

Fig. 8. Relationship among k, R_e and ZVS region ($f = 200$ kHz, $L_1 = L_{11} = 110$ μH, $C_1 = C_{11} = 5.918$ nF, $R_L = 10$ Ω).

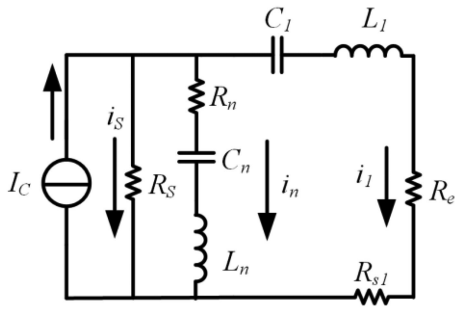

Fig. 9. Equivalent circuit of the proposed topology for efficiency analysis.

In Fig. 8, only k is considered as a variable to change R_e. Actually, if R_L, or both R_L and k are designed as variables, similar conclusion could also be obtained: when $R_e \geq R_{\text{opt}}$, ZVS could always be maintained.

B. Efficiency Analysis

While calculating the efficiency of the primary side, the parasitic resistance of L_1 and C_1 (named R_{s1}), the conduction resistances of S_a and S (named R_S), and the parasitic resistance of L_n and C_n (named R_n) are considered. Recalling in Fig. 2, there is only one switch turned ON at each moment, therefore, the equivalent circuit shown in Fig. 9 yields. The total power loss P_t can be expressed as follows:

$$P_t = P_S + P_{Rn} + P_{Rs1} \tag{21}$$

where P_S, P_{Rn}, and P_{Rs1} denote the power loss on R_S, R_n, and R_{S1}, respectively.

The power loss P_{Rs1} can be calculated by the following:

$$P_{Rs1} = \frac{{I_1}^2}{2} R_{s1} \tag{22}$$

where I_1 is the amplitude of i_1 and can be calculated by the following [30]:

$$I_1 = \frac{V_{fa}}{R_e + R_{S1}} = \frac{V_{DD}\sqrt{2\,(1 - \cos(2\pi D))}}{\pi\,(1-D)\,(R_e + R_{S1})} \tag{23}$$

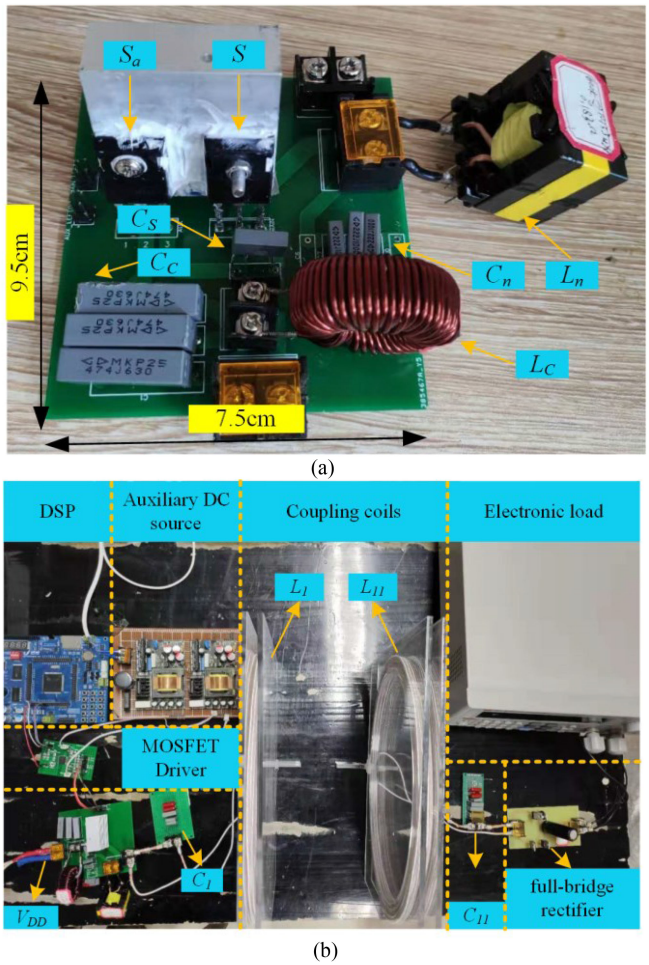

Fig. 10. Prototype of the proposed WPT system. (a) Proposed topology. (b) Entire WPT system.

The power loss P_{Rn} can be calculated by the following:

$$P_{Rn} = \frac{1}{T}\int_0^T i_n^2 R_n dt = \frac{(Q_t \omega n)^2}{2(\cos(\omega n t_r + \alpha_n) - \cos(\alpha_n))^2} R_n \tag{24}$$

The power loss P_S on R_S can be calculated by the following:

$$P_S = \int_0^T (i_n + i_1 + I_C)^2 R_S dt = \left(\frac{(I_n + I_1)^2}{2} + {I_C}^2\right) R_S \tag{25}$$

In (25), I_C and I_n are unknown variables, and to solve their values, according to the energy conservation balance, it yields the following:

$$V_{DD} I_C = P_t + \frac{I_1^2}{2} R_e \tag{26}$$

After V_{DD}, D, and t_r are fixed, I_C and I_n can be calculated by (15) and (26) in MATLAB. Then, the efficiency η_p of the primary side can be calculated by (27) and the efficiency η_w of the WPT system can be calculated by (28)

$$\eta_p = 1 - \frac{P_t}{V_{DD} I_C} \tag{27}$$

TABLE I
SPECIFICATIONS OF THE PROTOTYPE

Parameters	Value	Parameters	Value
f	200 kHZ	R_S	40mΩ
L_C	0.5 mH	R_n	0.33 Ω
L_1, L_{11}	110 μH	R_{s1}, R_{s11}	0.67 Ω
C_1, C_{11}	5.75 nF	R	37 Ω
Cs	3.3 nF	I_O	1.18 A
C_C	1.41 μF	V_F	2.1 V
k	0.068~0.178	Total output power	55 W
C_o	150 μF	V_{DD}	22-35V
D_1, D_2, D_3, D_4	RHRP3060	R_L	33.6 Ω
S, S_a	IRFP260NPbF		

TABLE II
THREE CASES OF SELECTED C_n AND L_n FOR ZVS VERIFICATION

	t_r (ns)	D	L_n (μH)	critical k	Harmonic order n	C_n (nF)	
						ideal	real
I	250	0.5	10.17	0.103	3	7.47	7.6
II	250	0.5	10.17	0.178	3	8.18	8.2
III	250	0.65	10.17	0.178	2	17.17	17.05

$$\eta_w = \eta_p \frac{R_L}{R_L + R_{s11}} \tag{28}$$

IV. EXPERIMENTAL RESULTS

As analyzed above, both k and R_L could influence ZVS through changing R_e. Due to the similar principle, in the experiments, only k (mirror the coils distance change) is employed as variable for verification.

A platform shown in Fig. 10, with the output power of 50 W, was implemented in the laboratory. The employed dc source and electronic load are FTP065-800-16 and RK8512, respectively. The switching frequency of S and S_a and the resonant frequency of the receiver were set to be 200 KHz. Specifications of the platform are listed in Table I. The CBB capacitors were utilized for resonant and harmonic circuits.

The real values of the components were measured based on the WK-6500B impedance analyzer. In addition, as shown in Table I, the input voltage V_{DD} is unfixed. This is because, in the comparative experiment, the coils distance can influence the output power. To ensure the output power to have a constant value of 55 W, V_{DD} is considered to be adjusted.

Based on the platform, three groups of harmonic circuits with different C_n and L_n, were first designed to verify the harmonic analysis and parameter design strategy. Corresponding parameters are listed in Table II. Then, one group of parameters was selected to make comparison with typical class-E converter on voltage stress, ZVS region and efficiency.

Ideally, under the three groups of the parameter, following phenomena will be observed in the experimental results.

1) Based on the cases I and II, the third harmonic was selected and the frequency of the current i_n should be $3f$ (600 kHz). At the falling edge of v_{Cs}, i_n should be positive, and its phase should be close to 90°. Furthermore, under the case I, the charge in C_S should be completely extracted after 250 ns when critical $k = 0.103$, and ZVS could

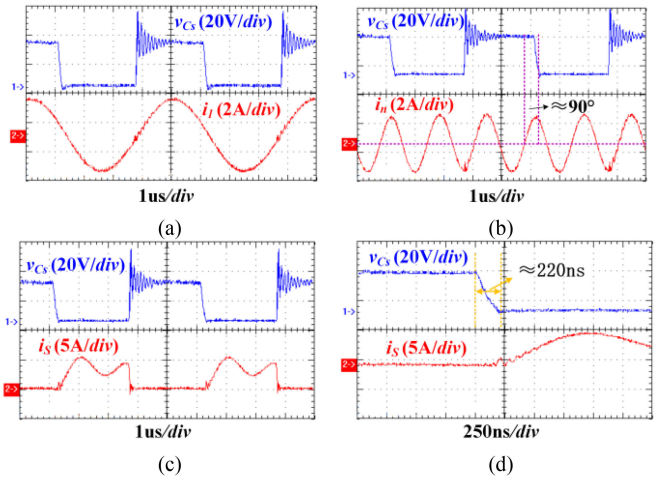

Fig. 11. Voltage/current curves at case I (L_n = 10.17 μH, C_n = 7.6 nF, D = 0.5 and critical k = 0.103). (a) v_{Cs} and i_1. (b) v_{Cs} and i_n. (c) v_{Cs} and i_S. (d) Zoomed-in v_{Cs} and i_S.

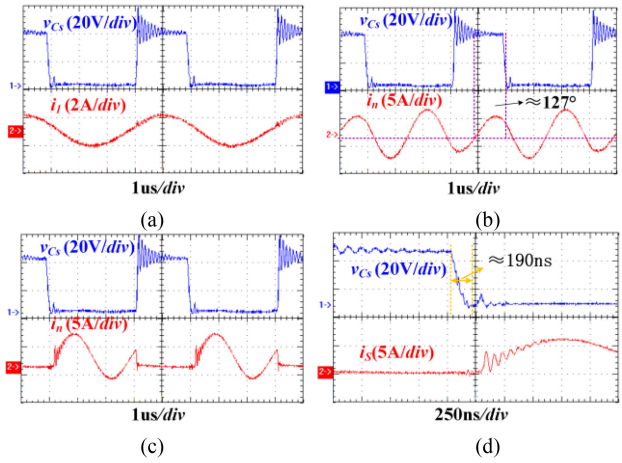

Fig. 13. Voltage/current curves at case III: L_n = 10.17 μH, C_n = 17.05 nF, D = 0.65 and critical k = 0.178. (a) v_{Cs} and i_1. (b) v_{Cs} and $i_{n—n=2}$ of. (c) v_{Cs} and i_S. (d) Zoomed-in v_{Cs} and i_S.

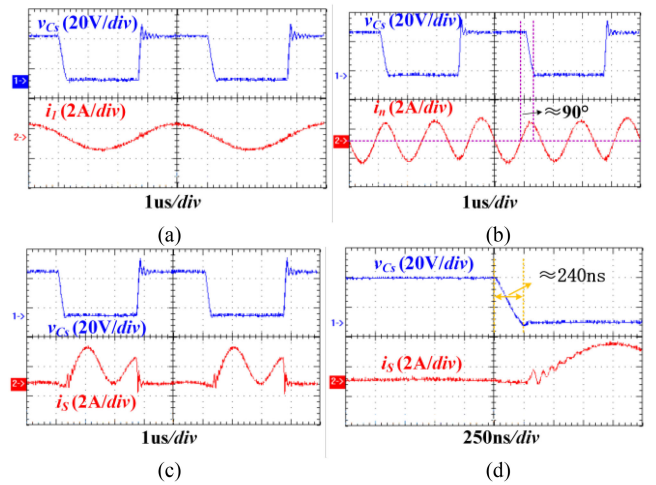

Fig. 12. Voltage/current curves at case II(L_n = 10.17 μH, C_n = 8.2 nF, D = 0.5 and critical k = 0.178). (a) v_{Cs} and i_1. (b) v_{Cs} and i_n of. (c) v_{Cs} and i_S. (d) zoomed-in v_{Cs} and i_S.

always be realized when k∈[0.103, 1]. Similarly, under the case II, C_S should be completely discharged after 250 ns when critical k = 0.178, and ZVS could always be realized when k∈[0.178, 1].

2) Based on case III, the second harmonic was selected, the frequency of the current i_n should be *2f* (400 kHz) and at the falling edge of v_{Cs}, the phase of i_n needs to be 127°. Furthermore, the charge in C_S should be completely extracted after 250 ns when critical k = 0.178, and ZVS could always be realized when k∈[0.178, 1].

Corresponding experimental results are shown in Figs. 11, 12, and 13, respectively. From Figs. 11(a), 12(a) and 13(a), obviously, the phase of i_1 is 90° at the center line of v_{Cs}. As the phase of v_{fa} is 90°at the center line of v_{Cs} as well, it suggests almost no phase difference between i_1 and v_{fa}. That is to say, different from the traditional class-E system, there is zero reactive power during the power injection process for the proposed topology.

In Figs. 11(b), 12(b), and 13(b), at the falling edge of v_{Cs}, the phase of i_n approaches to the analysis value. The small difference between the experimental value and theoretical value comes from that v_{Cs} is a quasi-square wave and its falling edge is much less steep than the square wave.

In Figs. 11(c) and (d), and 12(c) and (d), obviously, the duration of discharging process approaches to 250 ns, fitting well with the preset discharging time t_r. In Fig. 13(c) and (d), the discharging time is about 190 ns and smaller than t_r. In addition, *Cs* is recharged before *S* is turned ON. This may be caused by the distortion of $i_{n|n=2}$: the second harmonic has a lower quality factor than the third harmonic, correspondingly, the current distortion is more serious (as shown in Figs. 11(b), 12(b), and 13(b), $i_{n|n=3}$ more approaches sine wave than $i_{n|n=2}$). The distortion can be decreased by using a larger inductor L_n in the harmonic circuit.

To further verify the validity of the harmonic analysis, the curves under the duty cycle of D = 0.5 and D = 0.65 are given in Fig. 14. Obviously in Table II, when L_n = 10.17 μH and C_n = 17.05 nF, the harmonic circuit reveals small impedance for the second harmonic, however, as $i_{n|n=2}$ is zero in Fig. 14(a), it is verified that there is no second harmonic component in the square waveform v_{Cs} when D = 0.5. Similarly, it is also shown in Fig. 14(b) that there is negligible third harmonic component when D = 0.65. In addition, it is notable that when *S* is turned OFF, there are distinct oscillations of $i_{n|n=3}$ and $v_{Cn|n=3}$ in Fig. 14(b). This is caused by the zero-state response in the harmonic circuit. As shown in Fig. 14(c), when *S* is turned OFF, v_{Cs} begins to charge the harmonic circuit, L_n and C_n begins to store energy. However, at the moment when *S* is turned ON, both i_n and v_{Cn} return to zero and no energy is stored in the harmonic circuit.

Based on the above experimental results and discussion, the validity of harmonic analysis is verified.

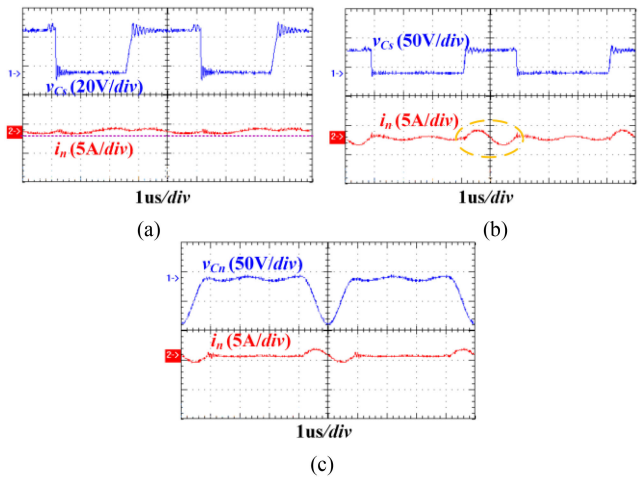

Fig. 14. Variation of the harmonic circuits voltage/current in respect to D. (a) v_{Cs} and $i_{n|n=2}$ when $L_n = 10.17\ \mu$H, $C_n = 17.05$ nF and $D = 0.5$. (b) v_{Cs} and $i_{n|n=3}$ when $L_n = 10.17\ \mu$H, $C_n = 7.6$ nF, $D = 0.65$. (c) v_{Cn} and $i_{n|n=3}$ when $L_n = 10.17\ \mu$H, $C_n = 7.6$ nF, $D = 0.65$.

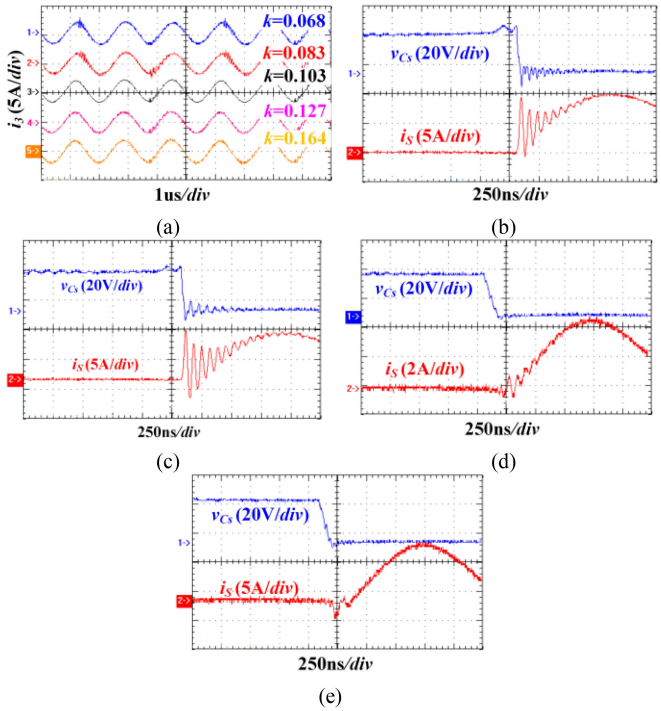

Fig. 15. Curves at case I ($L_n = 10.17\ \mu$H, $C_n = 7.6$ nF, $D = 0.5$) in respect to k. (a) $i_{n|n=3}$ under various k. (b) Zoomed-in v_{Cs} and $i_{n|n=3}$ ($k = 0.068$). (c) Zoomed-in v_{Cs} and $i_{n|n=3}$ ($k = 0.083$). (d) Zoomed-in v_{Cs} and $i_{n|n=3}$ ($k = 0.127$). (e) Zomed-in v_{Cs} and $i_{n|n=3}$ ($k = 0.164$).

The following-up experimental results focus on verifying low voltage stress, ZVS characteristic and efficiency of the proposed topology. The prototype, which could exactly realize ZVS under $k = 0.103$ and $D = 0.5$, were selected for experiments implementation ($L_n = 10.17\ \mu$H, $C_n = 7.6$ nF).

Fig. 15 shows the key waveforms of the proposed topology. Fig. 15(a) shows $i_{n|n=3}$ under different k, and it is obvious that the amplitude and phase of $i_{n|n=3}$ is never influenced by k. Fig. 15(b)–(e) show the zoomed-in waveforms of v_{Cs} and i_S under different k. When k is smaller than 0.103, ZVS will be lost, but if k is larger than 0.103, ZVS can be always achieved, fitting well with the preset ZVS region. Therefore, it is verified that the harmonic circuit can provide a stable current to extract charge, and ZVS could be realized over a wide range of coils distance.

Above experimental results have proved that ZVS turn-ON is realizable on S. Then, Fig. 16 gives the waveforms to further prove the ZVS feature of S and S_a. In Fig. 16(a), v_{Cs} rises slowly when S is OFF, therefore, the overlap of v_{Cs} and i_S can be effectively decreased comparing with hard switching. Fig. 16(b) and (c) are the curves of i_{Cc} and the drain–source voltage v_{Sa} of S_a. In Fig. 16(b), the current is negative after S is turned OFF, namely, i_{Cc} will flow through the body diode of S_a before S_a is turned ON. In Fig. 16(c), the overlap of i_{Cc} and v_{Sa} is negligible after S_a is OFF. To sum up, ZVS could always be realized on S and S_a due to the body diode of the switches and the voltage clamping feature of the shunt capacitor C_S.

A typical class-E converter based WPT system, which can exactly achieve ZVS when critical $k = 0.103$, is also designed for comparison, and the corresponding results are shown in Fig. 17. Obviously, when k becomes larger than 0.103, ZVS will be lost, leading to a lower efficiency. The efficiency curves of the proposed and typical class-E systems are shown in Fig. 18. It is notable that the power loss on the full-bridge rectifier (4.96 W) was also considered as a part of the output power, because the voltage drop V_F has also been considered when calculating R_L. As shown in Fig. 18, when $k = 0.103$, the efficiency of the WPT system based on typical class-E converter is 91.36%, about 2.91% higher than the proposed system due to additional loss on the harmonic circuit. However, when k increases, the efficiency of typical class-E system decreases rapidly. Instead, in the proposed topology, the efficiency could always be kept more than 87%, close to the calculation.

The power loss distribution under different k is calculated according to (21)–(28), and the pie charts are given in Fig. 19 to further analyze the changing trend of the power loss on each parasitic resistance. The conducting power losses P_{Rs1} on the primary coil and P_{Rn} on the harmonic circuit are the foremost in the WPT system. P_{Rs1} is much larger than P_{Rn} when k is small, then, P_{Rs1} will decrease and P_{Rn} will increase due to the incremental k. This is because a larger k will lead to a smaller i_1, namely, a lower conducting loss on R_{s1}. On the contrary, the harmonic current i_n will never be influenced by k, as a result, the weight of the loss caused by i_n is positively related to k. This is also the reason why the efficiency increases when $k < 0.14$ and decreases at $k > 0.14$.

The comparison of voltage stress is shown in Fig. 20(a). Notice the output power is maintained at 55 W. Obviously, the voltage stress of the proposed topology increases when k becomes larger. Recall the relationship between R_e and k, a higher input voltage is required to maintain the output power with R_e increasing, meaning a higher voltage stress. On the contrary, the voltage stress of typical class-E converter will decrease with k increasing. As shown in Fig. 17, when k becomes larger, the curve of v_{ds} more approaches square waveform, namely, the fundamental waveform v_{FA} of v_{ds}, will become larger and a

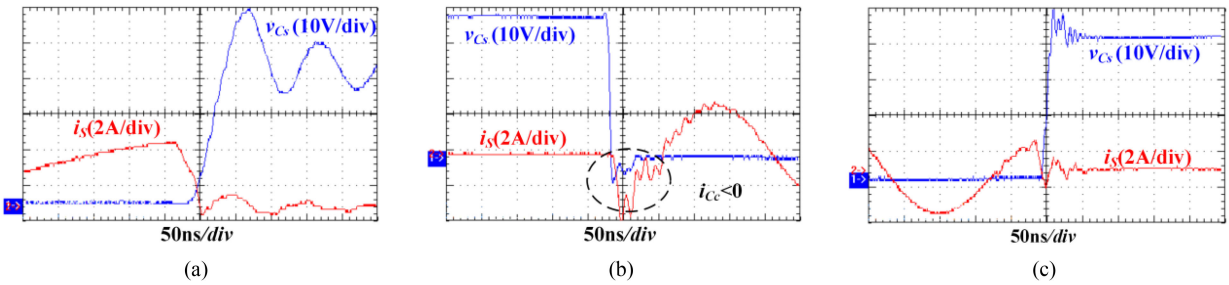

Fig. 16. Voltage and current curves of the switches at case I ($L_n = 10.17\ \mu$H, $C_n = 7.6$ nF, $D = 0.5$ and critical $k = 0.103$). (a) v_{Cs} and i_S when S is OFF. (b) v_{Sa} and i_{Cc} when S_a is ON. (c) v_{Sa} and i_{Cc} when S_a is OFF.

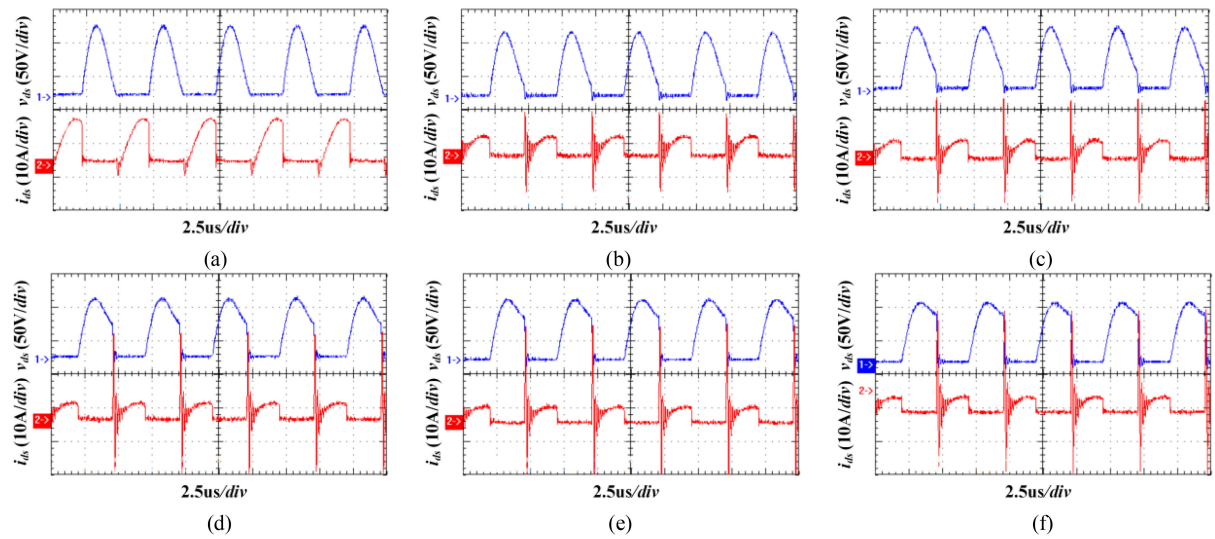

Fig. 17. Voltage and current curves of the switch in typical class-E WPT system ($C_S = 15.47$ nF, critical $k = 0.103$). (a) $k = 0.103$. (b) $k = 0.112$. (c) $k = 0.127$. (d) $k = 0.141$. (e) $k = 0.162$. (f) $k = 0.178$.

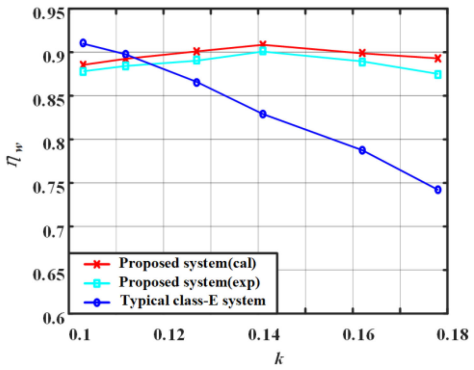

Fig. 18. Efficiency curves of the proposed and typical systems ($D = 0.5$).

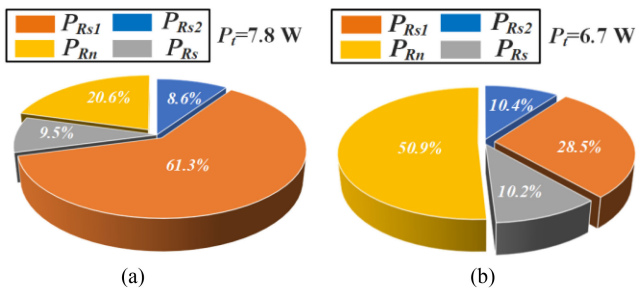

Fig. 19. Power loss distribution. (a) $k = 0.103$. (b) $k = 0.178$.

smaller input voltage can guarantee output power, resulting in a lower voltage stress. However, ZVS could never be realized in these cases.

Furthermore, observed from Fig. 20(a), when the converters are operated under optimum condition ($k = 0.103$), the voltage stress of switch in the proposed topology will reduce down to be 41.7% of that in the typical class-E converter if they have the same output power (with different V_{DD}). Theoretically, the voltage stress of switch in the proposed topology will be 55.6% of that in the typical class-E converter under the same input voltage. Therefore, after the phase difference between v_{Cs} and i_1 is eliminated, a lower input voltage could satisfy the same output power in the proposed system, meaning a lower voltage stress. Furthermore, the curves of V_{DD} and V_{out} are also given in Fig. 20(b) and (c). Comparing with Fig. 20(a) and (b), the voltage stress always doubles V_{DD} at D of 0.5, fitting will with (8). The validity of the theoretical analysis is further verified.

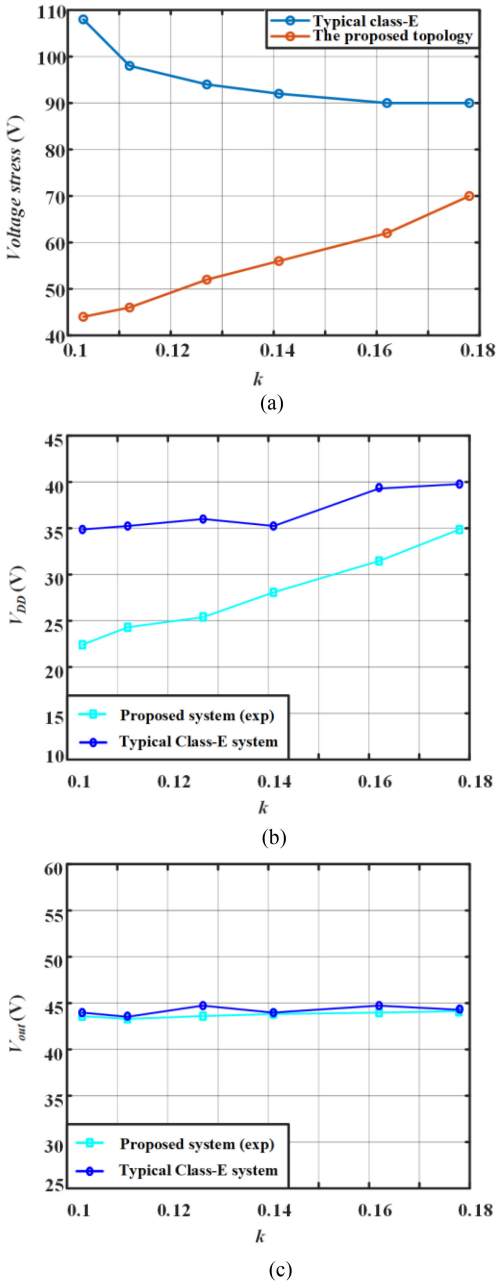

Fig. 20. Variation in voltage stress, V_{DD} and $V_{\rm out}$ with respect to k, under the same output power. (a) Voltage stress. (b) V_{DD}. (c) $V_{\rm out}$.

In addition, it is also notable that the harmonic circuit brings additional conducting loss. Therefore, the relationship between switching loss and conducting loss is given in Fig. 21. Obviously, by designing the parameters properly, the harmonic circuit is helpful in improving the efficiency.

The ringing on the voltage curves in Figs. 11–15 is caused by the resonance between C_S and the parasitic inductance in the circuit. In the article, the parasitic inductance is introduced by the loose layout (a loose layout is much easier for voltage/current measurement). Measured by the impedance analyzer TH2839, the parasitic inductance is about 90 nH. It can be weaken by optimizing the layout of the circuit further.

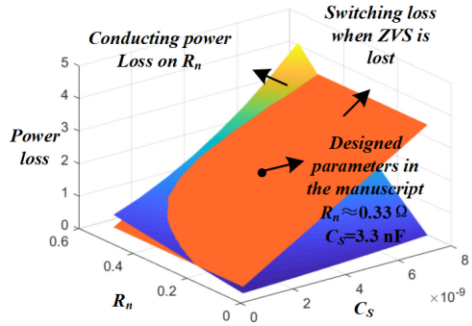

Fig. 21. Relationship among R_n, C_S, and power loss.

V. Conclusion

The article presents a clamped and harmonic injected class-E converter for WPT systems. The clamped circuit is employed to steadily decrease the voltage stress and the harmonic injection circuit is utilized to achieve ZVS over a wide range of coils distance. The prototype with three different critical conditions under given duty cycle was built. It has shown that the prototype can exactly satisfy ZVS at the preset critical coil distance, hence, ZVS could be realized when the coils distance is smaller than the critical coils distance. Furthermore, it could also be observed that when $D = 0.5$ and $D = 0.65$, there has no second harmonic and third harmonic, respectively, fitting well with the harmonic analysis. Then, one case of the proposed converter was compared with typical class-E converter. WPT system based on the proposed converter could maintain ZVS when k ranging from 0.103 to 0.178, as a result, a relatively steady efficiency ranging from 85% to 88% could be maintained. As to the typical class-E converter based WPT system, ZVS could only be realized when $k = 0.103$, correspondingly, the efficiency rapidly decreases from 88% to 72% due to the lost ZVS. Furthermore, when both the converters could realize ZVS, about 58.3% of the voltage stress could be decreased in the proposed converter.

In general, Class-E converter will be operated at a fixed duty cycle. Under given duty cycle, the article provides an effective method to steadily decrease the voltage stress while maintaining ZVS over a wide range of coils distance for class-E converter in WPT system. In the future, the authors will focus on realizing ZVS realization over a wide range of coils distance even at various duty cycles, and optimizing the system parameters for higher efficiency.

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