A CMOS Envelope Tracking Supply Converter for RF Power Amplifiers of 5G NR Mobile Terminals

Yu-Chen Lin and Yi-Jan Emery Chen, *Fellow, IEEE*

***Abstract*—An envelope tracking supply converter was presented for the RF power amplifiers of sub-6 GHz 5G NR mobile devices. The hybrid supply converter consisted of a linear, fast switching, and slow switching regulators connected in parallel. The two-phase hysteretic control was proposed for use in the fast switching regulator to track the fast-varying envelope of 40-MHz 5G NR signal. The 0.25-μm CMOS supply converter achieved a maximum efficiency of 79.1%. The power-added efficiency improvement of the RF power amplifier with the proposed supply converter was 3.1% when tested with a 40-MHz 256-QAM 5G NR signal.**

***Index Terms*—5G NR, envelope tracking (ET), mobile communication, power amplifier (PA), RF transmitter, supply converter.**

I. Introduction

MOBILE communication provides the unprecedented user experience to ignite overwhelming technology development and application innovation. The wireless communication standards evolve rapidly to facilitate higher data rate and shorter latency. Because of limited spectral resources, the RF signals of 4G systems and beyond, such as long-term evolution (LTE) and sub-6 GHz 5G NR (New Radio), have high value of peak-to-average power ratio (PAPR) caused by the highly spectral-efficient modulation schemes. The characteristic of high PAPR makes the power amplifiers (PAs), the most power-hungry blocks in RF transceivers, operate at a large backoff region to comply with the stringent linearity requirement. The RF PAs deliver high efficiency at the power level near saturation but their efficiencies degrade significantly at power back-off. In order to enhance the efficiency at backoff region, the techniques of envelope elimination and restoration (EER) [1], [2] and envelope tracking (ET) [3]–[5] were proposed to dynamically change the supply voltages of RF PAs. The EER technology needed a wideband and high-fidelity supply converter (SC) to restore the nonconstant envelope RF signal without severe distortion. It was extremely difficult to develop such a supply converter, so EER was rarely demonstrated for modern mobile communication until the modified EER which does not restore the modulated signal by varying the supply voltage was proposed [6]–[8]. The SC requirement for ET is much relaxed such that the technology has been widely adopted in many wireless communication devices.

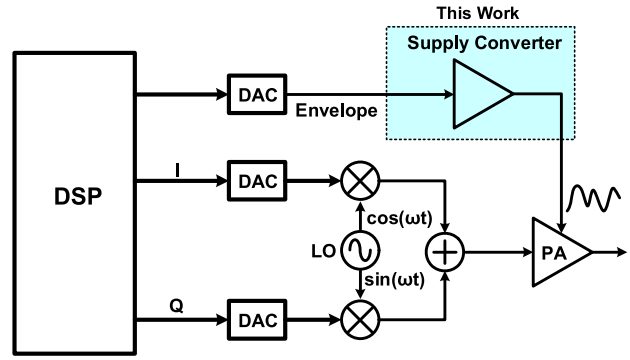

Fig. 1. Block diagram of envelope tracking RF transmitter.

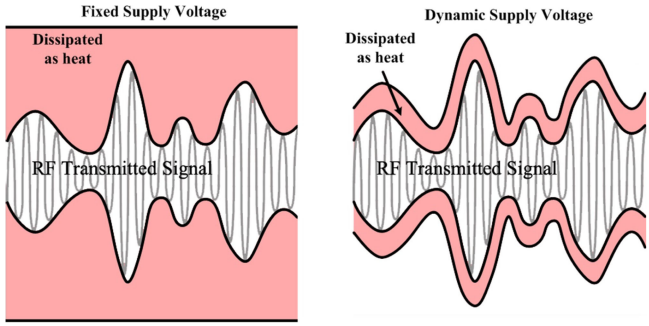

Fig. 2. Fixed supply voltage versus envelope tracking dynamic supply voltage.

Fig. 1 shows the block diagram of a typical envelope tracking RF transmitter. The supply voltage of the PA is dynamically changed by the SC. Fig. 2 illustrates the schemes of fixed supply voltage and envelope tracking dynamic supply voltage. ET reduces the supply voltage of the PA in accordance with the envelope of the modulated RF signal and keeps the modulated waveforms amplified in the linear region. Intuitively ET can enhance the PA's efficiency significantly but the overall efficiency of the ET PA should include the power consumption of the SC

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The authors are with the Department of Electrical Engineering, Graduate Institute of Electronics Engineering, and Graduate Institute of Communication Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: domainlin403@gmail.com; emerychen@ntu.edu.tw).

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as expressed

$$\eta_{\text{overall}} = \eta_{SC} \cdot \eta_{PA} \tag{1}$$

where η_{SC} and η_{PA} are the efficiencies of SC and PA, respectively. Therefore, the efficiency of the SC needs to be high enough to benefit from the power saving of ET.

Rapid output response is another critical design issue for the SC of ET. As the mobile communication standards evolve, the modulation channel bandwidth extends to convey more data. The 5G NR FR1 (sub-6 GHz) supports the channel bandwidth from 5 to 100 MHz while the maximum channel bandwidth of 4G LTE is 20 MHz without carrier aggregation. The wide modulation bandwidth causes fast variation of the time-domain envelope waveform. However, the transistors in the SC need to be large enough to power the RF PAs and the associated parasitics and passive components tend to slow down the output response.

The ET SC can be implemented in the form of a linear regulator, which has wide bandwidth and little output ripples to achieve excellent in-band and out-of-band spectral performance [9]. Nevertheless, the linear regulator suffers from poor efficiency when the output voltage is away from the fixed supply voltage, which is the case that the PAs operate more frequently for high PAPR modulated signals. The alternative option is using a switching regulator, which can achieve higher efficiency across a broad range of output voltages than a linear regulator [10], [11]. Nonetheless, there are several technical issues associated with the switching converters for ET application. To faithfully track the instantaneous envelope of a RF signal with wide modulation bandwidth, the switching frequency of the converter needs to be much higher than the modulation bandwidth. What raises the switching frequency even higher is that the envelope bandwidth expands beyond the modulation bandwidth because of nonlinear cartesian-to-polar transformation. The physical size of the power transistors in a SC is usually very large and it makes high frequency switching difficult. High switching frequency also results in low power efficiency for switching regulators due to significant switching loss and less ideal switching behavior.

Several hybrid SC architectures were proposed to combine the advantages of linear and switching regulators [12]–[14]. In the cascade hybrid SC, the supply voltage of the linear regulator was connected to the output of the switching regulator. The output of the linear regulator supplied the power for a RF PA. The switching regulator reduced the difference of the supply and output voltages of the linear regulator. Although the linear regulator's efficiency could be enhanced, the overall efficiency of the cascade hybrid SC was equal to the multiplication of the individual efficiency of the two regulators. Moreover, the switching regulator needed a modified envelope signal with proper offset to vary its output voltage. The other type of hybrid SCs connected the outputs of the linear and switching regulators together in parallel form [15]–[28]. The switching regulator was designed to provide the average power and the linear regulator was used to supply the fast-varying current and absorb the current ripples generated by the switching regulator. Since most of the power was provided by the high-efficiency switching regulator, the parallel hybrid SCs usually had higher overall efficiency than the cascade hybrid SCs. In conjunction with the parallel hybrid technique, Kanbe *et al.* [34] proposed the use of the fast and slow switching regulators of hysteretic control to extend the signal tracking bandwidth and improve efficiency.

This article presented the ET SC capable of supporting 40-MHz channel bandwidth for sub-6 GHz 5G NR RF PAs. The parallel hybrid SC consisted of a slow switching regulator, fast switching regulator, and linear regulator. Different from the hysteretic controlled fast and slow switching regulators shown in [34], the control mechanisms of the slow and fast switching regulators were pulsewidth modulation (PWM) and hysteretic control, respectively. In addition, a new two-phase hysteretic control was proposed to design the fast switching regulator and extend its tracking bandwidth. The current two-phase hysteretic technique limited the duty cycle of the control signal to below 50%. The proposed technique removed the hurdle of 50% duty cycle to enhance transient response. The 0.25-μm CMOS SC achieved the peak efficiency of 79.1% when tested with a 40-MHz 256-QAM 5G NR signal. The output power of the RF PA was 24.3 dBm and the adjacent channel leakage power ratio (ACLR) was -30.6 dBc without additional digital predistortion (DPD).

II. Hybrid Supply Converter Design

A. Supply Converter Architecture

The functional blocks of the presented SC, as shown in Fig. 3, can be divided into five parts: linear regulator, fast switching regulator, slow switching regulator, slew-rate (SR) enhancement circuit, and current control block. The linear regulator and the slow switching regulator are connected like the conventional parallel hybrid SC. The PWM frequency of the slow switching regulator is 5 MHz. The fast switching regulator is added to the conventional parallel hybrid SC architecture to enhance the overall converter efficiency. In a conventional hybrid SC, the switching regulator supplies the power for the envelope signal of the frequency span up to several kilohertz and the linear regulator supplies the power for the frequency span beyond the switching regulator's coverage. The power spectral density (PSD) of the envelope of a typical 5G NR signal with modulation bandwidth of 40 MHz is shown in Fig. 4. Although the majority of the envelope signal power falls below several kilohertz, the other signal components still have big impact on the overall SC efficiency. If the switching regulator is designed to cover higher frequency components, the efficiency of the switching regulator will drop because of the increased switching loss. The parasitics of the large power transistors also limit their switching frequency and output signal bandwidth.

The fast switching regulator utilizing the proposed two-phase hysteretic control mechanism is added in the SC to supply the envelope signal power beyond several kilohertz and below 40 MHz. In such arrangement, the low-efficient linear regulator only needs to supply less than 10% of the overall power and it helps enhance the overall SC efficiency. On the contrary, the inefficient linear regulator would supply nearly 20% of the power if the fast switching regulator is not deployed. Because the fast switching regulator provides far less power than the

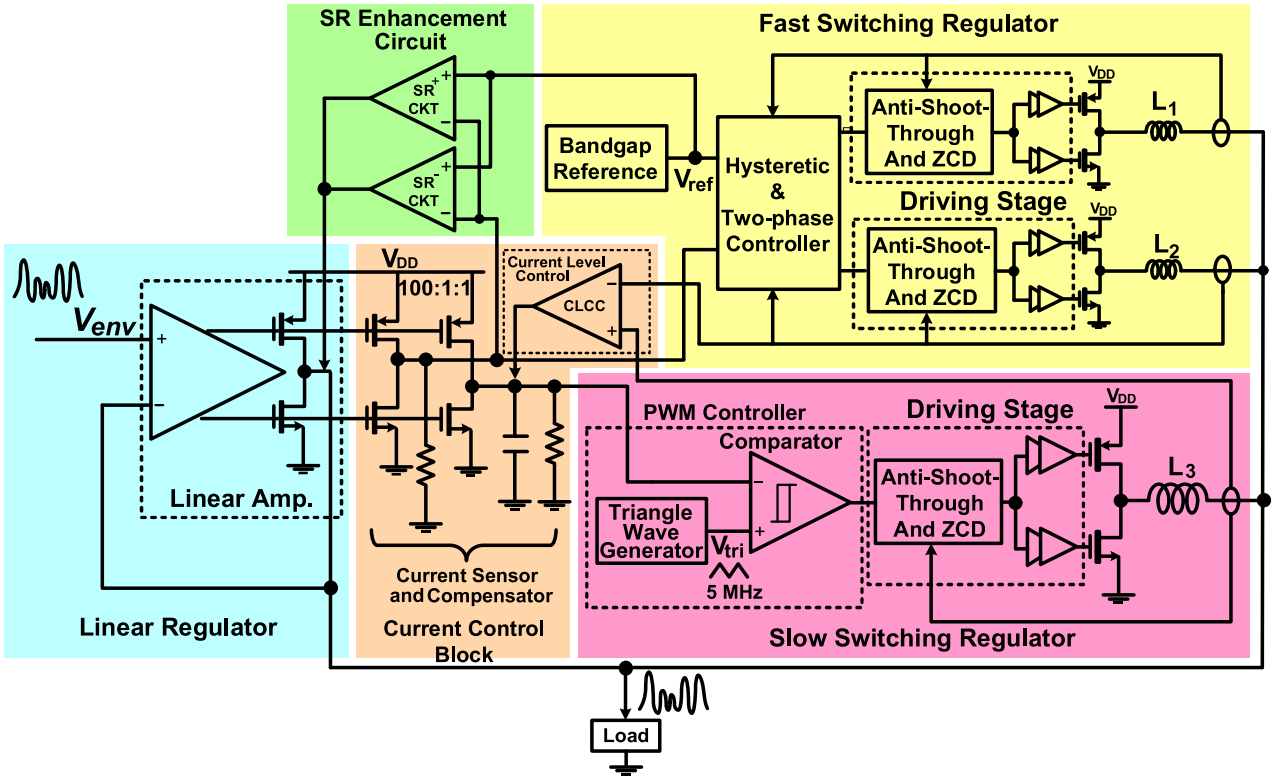

Fig. 3. Block diagram of proposed hybrid supply converter.

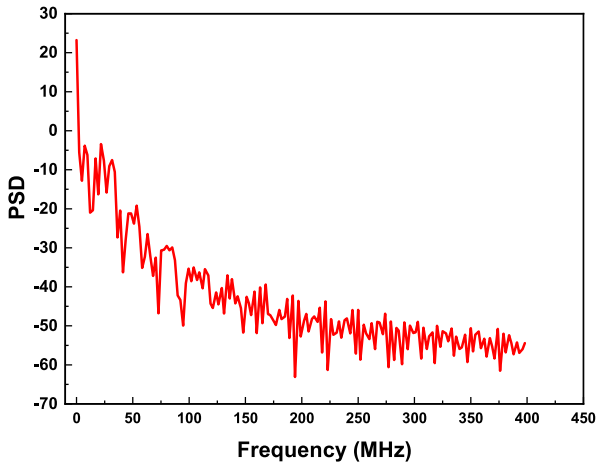

Fig. 4. PSD of the envelope of a typical 5G NR signal with modulation bandwidth of 40 MHz.

slow switching regulator, the power transistor size in the former can be much smaller than that in the latter and it facilitates faster switching frequency. The efficiency of the fast switching regulator is lower than that of the slow switching regulator due to more switching loss but it is still much higher than that of the linear regulator. Therefore, the overall efficiency of the proposed hybrid supply converter (HSC) is better than the conventional one. The comparison of the overall efficiency calculation between the conventional and proposed HSCs is shown in Table I. Using the typical regulator efficiency for calculation, adding the fast switching regulator to share the loading of the linear and switching regulators in the conventional parallel hybrid SC can enhance the overall efficiency. The currents supplied by the individual regulators in the proposed HSC are illustrated in Fig. 5.

TABLE I
OVERALL EFFICIENCY OF PROPOSED AND CONVENTIONAL PARALLEL HYBRID SUPPLY CONVERTERS

Proposed HSC (power/eff.)			Conventional HSC (power/eff.)		
Slow switching	0.60 W	90%	Switching regulator	0.8 W	90%
Fast switching	0.30 W	83%			
Linear regulator	0.1 W	45%	Linear regulator	0.2 W	45%
Overall efficiency	80%		Overall efficiency	75%	

Removing the slow switching regulator and leaving the fast switching regulator can be regarded as the kind of conventional hybrid supply converter. It is very difficult to design the switching regulator which supplies most of the power and covers the signal bandwidth up to 40 MHz. Even though it is doable, the efficiency of the switching converter is typically lower than the efficiency of the fast switching regulator shown in Table I because of more power needed to be delivered. Even if we use the same efficiency of the fast switching regulator shown in Table I to calculate the overall efficiency of the hybrid supply converter of which the slow switching regulator is removed, the

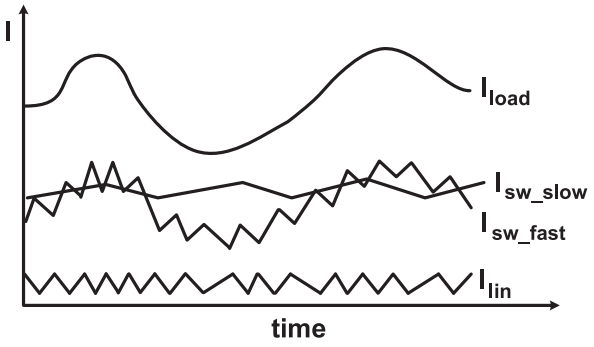

Fig. 5. Current supplied by the individual regulators in the proposed HSC.

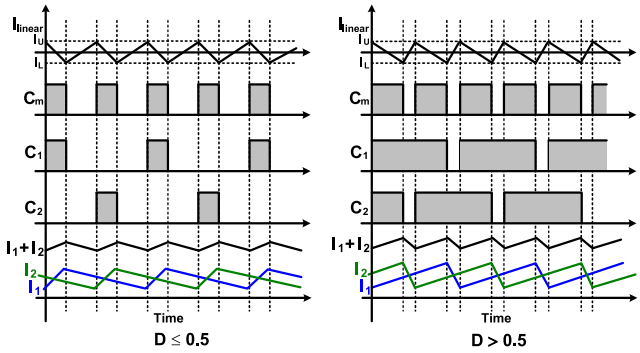

Fig. 6. Example waveforms of two-phase hysteretic control.

efficiency is 76.5%, higher than the conventional HSC but still lower than the proposed HSC.

The output currents of the fast switching and slow switching regulators are detected for multiple purposes. The sensed voltages of regulator currents are used in the zero current detectors (ZCD) to avoid the reverse current delivered by the other switching regulator. The sensed voltages of the fast switching regulator are also used to generate the two-phase hysteretic control signal. In addition, the sensed currents of the slow and fast switching regulators are fed into the current level control circuit (CLCC) to facilitate the output current distribution between the two regulators.

B. Two-Phase Hysteretic Control

Although the fast switching regulator has much smaller power transistors than those of the slow switching regulator, it is still very challenging to make the transistors switch fast enough to track an envelope signal with 40 MHz bandwidth. The hysteretic control features the advantages of fast response, no need of additional compensation circuit for stability, simple implementation, and small circuit area. In order to take the advantage of the conventional two-phase supply converter technique in terms of efficiency enhancement, ripple reduction, and fast load transient, the novel two-phase hysteretic control is proposed for the design of the fast switching regulator.

The prior work implemented the two-phase hysteretic control by alternating delivery of the hysteretic control signal to two different power stages [29]. The approach limited the duty cycle of each power stage to the maximum of 50% and the slew rate of the converter was constrained accordingly.

The proposed two-phase hysteretic control method, which removed the limitation of 50% duty cycle (D), detected the current variation of the linear regulator and utilized the designated algorithm to generate the hysteretic control signals for the power stages. Fig. 6 shows the example waveforms of the proposed two-phase hysteretic control. The left plot is for the case that the duty cycles of the two-phase power stages are less than or equal to 50%, and the right plot is for the case that the duty cycles are more than 50%. The hysteretic control is facilitated by detecting the ripples of the linear regulator current I_{linear}. The upper bound $\mathrm{I_U}$ and lower bound $\mathrm{I_L}$ of the linear regulator current are used to form the hysteretic window. $\mathrm{I_1}$ and $\mathrm{I_2}$ are the two-phase currents

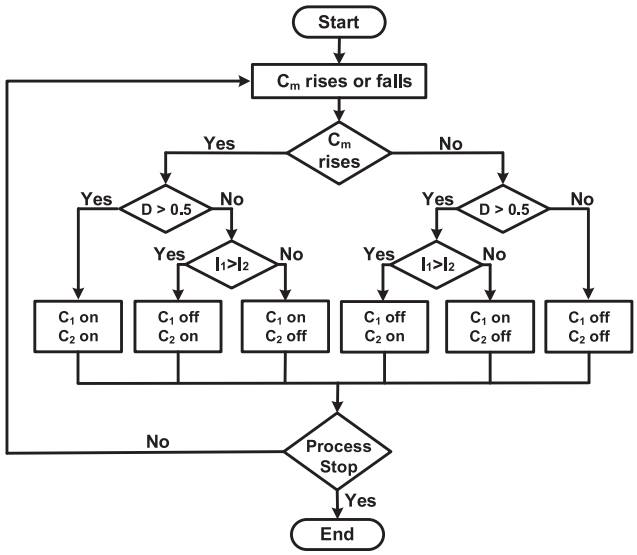

Fig. 7. Flowchart for generating $\mathrm{C_1}$ and $\mathrm{C_2}$ control signals.

delivered by the power stages of the hysteretic controlled fast switching regulator. The main hysteretic control signal $\mathrm{C_m}$ turns ON ($0\rightarrow1$) when the linear regulator current rises and reaches $\mathrm{I_U}$, meaning that the fast switching regulator needs to supply more current to reduce the linear regulator current. On the contrary, $\mathrm{C_m}$ turns OFF ($1\rightarrow0$) when the linear regulator current falls to $\mathrm{I_L}$, meaning that the fast switching regulator needs to reduce current to have the current return to the designated level. $\mathrm{C_1}$ and $\mathrm{C_2}$ are the control signals of the two-phase power stages. The summed current of the two-phase currents, $\mathrm{I_1 + I_2}$, rises when $\mathrm{C_m}$ is ON and falls when $\mathrm{C_m}$ is OFF. For the duty cycle less than 50%, $\mathrm{C_m}$ is alternately distributed to the two-phase regulator as $\mathrm{C_1}$ and $\mathrm{C_2}$. For the duty cycle larger than 50%, $\mathrm{C_1}$ and $\mathrm{C_2}$ turn ON alternately at the rising edge of $\mathrm{C_m}$ and turn OFF at the falling edge of the next $\mathrm{C_m}$ pulse.

The flowchart generating $\mathrm{C_1}$ and $\mathrm{C_2}$ for both duty-cycle cases is shown in Fig. 7. $\mathrm{C_1}$ and $\mathrm{C_2}$ make transition when $\mathrm{C_m}$ changes from 0 to 1 or from 1 to 0. For the case of $\mathrm{D \leq 50\%}$, $\mathrm{C_1}$ changes to 1 and $\mathrm{C_2}$ remains 0 at the rising edge of $\mathrm{C_m}$ if $\mathrm{I_1}$ is smaller than $\mathrm{I_2}$. Similarly, $\mathrm{C_2}$ changes to 1 and $\mathrm{C_1}$ remains 0 at the rising edge of $\mathrm{C_m}$ if $\mathrm{I_2}$ is smaller than $\mathrm{I_1}$. $\mathrm{C_1}$ and $\mathrm{C_2}$ change to 0 at

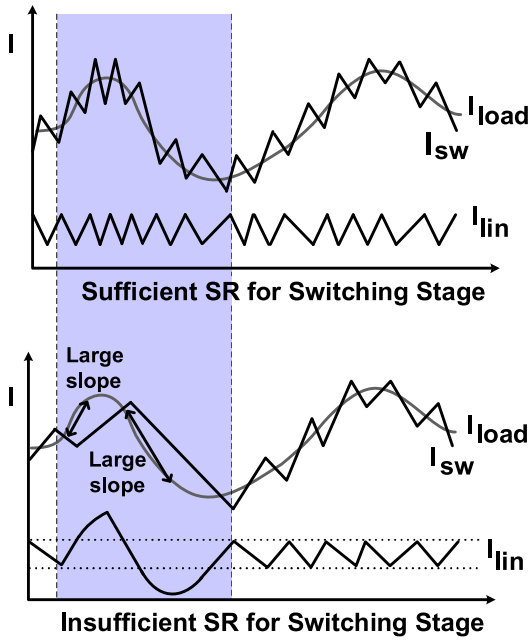

Fig. 8. Current waveforms of linear and switching regulators for sufficient and insufficient slew rates.

the falling edge of C_m. For the case of D $>$ 50%, C_1 and C_2 change to 1 at the rising edge of C_m if their current states are 0 and remain 1 if their current states are 1. C_1 changes from 1 to 0 at the falling edge of C_m if $I_1 > I_2$. Similarly, C_2 changes from 1 to 0 at the falling edge of C_m if $I_2 > I_1$.

C. Slew-Rate Enhancement

The envelope of the modulated signal of wide bandwidth sometimes varies drastically such that the slew rate of the fast switching regulator is not high enough to track on the variation [30]. The current waveforms of the linear and switching regulators for both cases of sufficient and insufficient slew rates are illustrated in Fig. 8. The linear regulator needs to source or sink more instantaneous current when the slope of the envelope signal exceeds the slew rate of the switching regulators. The current ripples delivered by the linear regulator are usually about a few tens of milliamperes but the instantaneous current sink and source can reach hundreds of milliamperes. The efficiency of the linear regulator would be severely degraded if it was designed to handle the need of occasional current surge.

The other option for responding to abrupt envelope signal change is increasing the slew rate of the fast switching regulator. However, it would need to increase the power transistor sizes. The excessive parasitics associated with the power transistors would limit the tracking response of the fast switching regulator.

The slew-rate enhancement circuit is developed to handle the occasional current surge. The SR enhancement circuit is composed of an SR^+ driver circuit and an SR^- driver circuit as shown in Fig. 3. The SR^+ driver sources current and SR^- driver sinks current rapidly when the rising and falling slopes of the switching regulator currents are not sufficient, respectively. While the current supply capability of the switching regulator is adequate, both of the SR driver circuits do not function so the impact to the overall efficiency degradation is little.

III. Circuit Design

A. Switching Regulators

The design of the slow switching regulator is similar to most conventional buck switching converters and its schematic diagram is shown in Fig. 3. The envelope signal is compared with a 5-MHz triangular waveform to generate the PWM pulses. The driving stage of the power transistors consists of driving buffers with exponentially scaled sizes, anti-shoot-through circuit, and ZCD will be shown later in this section. The slow switching regulator is designed to deliver around 60% of the output power because its efficiency can reach 90% or higher.

The fast switching regulator is designed to track the signal up to 40 MHz and deliver around 30% of the output power. The transfer function of the converter can be simplified as

$$H_{FS}(s) = \frac{G_M}{1 + \frac{s}{\omega_o \cdot Q} + \frac{s^2}{\omega_o^2}} \tag{2}$$

$$\omega_o = \frac{1}{\sqrt{LC_L}},\ Q = R_L \cdot \sqrt{\frac{C_L}{L}} \tag{3}$$

where R_L and C_L are equivalent load resistance and capacitance, respectively, L is the output inductor, and the inductance is selected to fulfill $\omega_o > 40$ MHz. Although small inductors can extend the bandwidth of the converters, the output current ripples are increased. The current ripples need to be compensated by the linear regulator to avoid the spurious spectrum at RF PA output. The low-efficiency linear regulator needs to supply more current for large current ripples and it leads to lower overall efficiency. The inductance value is chosen based on the amplitude limit of current ripples. The power transistors of the fast switching regulator need to switch several times faster than 40 MHz. Owing to the proposed two-phase hysteretic control technique, the required switching frequency can be lowered by half but it is still challenging for large power transistors. The power transistor size is determined mainly based upon the current to be delivered and small transistor parasitics. The optimization of conduction loss is secondary because the fast switching regulator supplies much less power than the slow switching regulator.

B. Two-Phase Hysteretic Controller

The circuit schematic diagram of the two-phase hysteretic controller is shown in Fig. 9. The process of determining whether the duty cycle is greater than 0.5 can be realized by comparing the output voltage (V_{out}) with the reference voltage V_{ref}, which is $0.5V_{DD}$. The relationship of V_{out}, V_{DD} and duty cycle (D) is derived as

$$\frac{V_{out}}{V_{DD}} = D\left(\frac{V_{DD} - V_{SDH} + V_{DSL}}{V_{DD}}\right) - \frac{V_{DSL}}{V_{DD}} \tag{4}$$

where V_{SDH} and V_{DSL} are the source–drain voltage of the high-side and drain–source voltage of the low-side power transistors of the fast switching regulator, respectively. The turn-ON resistance of the power transistors is usually small so the ratio

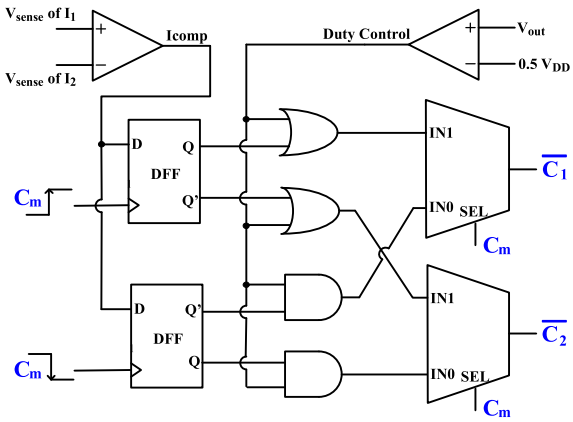

Fig. 9. Two-phase hysteretic controller.

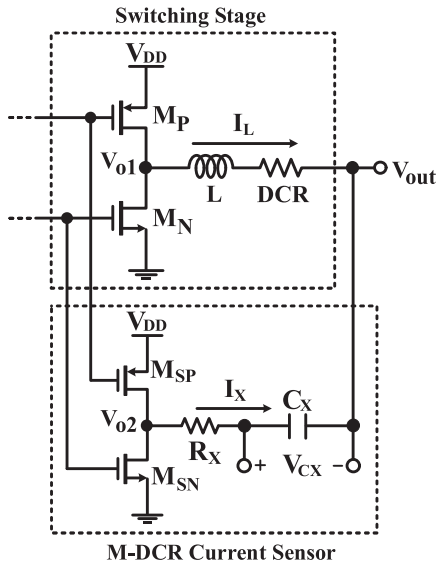

Fig. 10. Circuit schematic diagram of modified DCR current sensor.

of V_{out} and V_{DD} can be approximated as follows:

$$\frac{V_{out}}{V_{DD}} \approx D. \tag{5}$$

The inductor dc resistance (DCR) current sensing technique is widely used in the CPU voltage regulator application [31]. V_{CX} is the sensed voltage of I_L in the DCR technique, which is equal to the voltage across the inductor's dc resistance. The DCR technique has the advantage of lossless characteristic, but it is prone to noise agitation. The modified DCR (M-DCR) sensing technique [31], [32] shown in Fig. 10 is used to sense the fast switching regulator currents for the two-phase hysteretic control. The V_{CX} of the M-DCR sensing circuit is several times of the voltage that the DCR delivers such that the requirement of very fine comparator resolution for the conventional DCR sensing technique is relaxed.

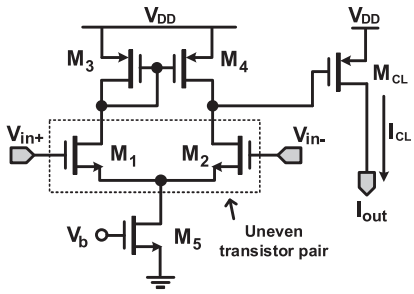

Fig. 11. Schematic diagram of CLCC.

The scaled replica of the output is used to make V_{o1} equal to V_{o2}. The voltage V_{CX} can be derived as

$$V_{CX} = I_L \cdot DCR \cdot \frac{1 + \frac{sL}{DCR}}{1 + sR_X C_X}. \tag{6}$$

By choosing the values R_x and C_x corresponding to L and DCR, V_{CX} can be simplified as

$$V_{CX} = I_L \cdot DCR. \tag{7}$$

The current I_L can be obtained by dividing V_{CX} by DCR.

C. Current Control Block

The current control block consists of current sensing circuits and a CLCC as shown in Fig. 3. The current sensing circuits use the transistor size ratio of 100:1 to detect the output current of the linear regulator. The CLCC is used to ensure that the slow switching regulator supplies more current than the fast switching regulator because the former has higher efficiency than the latter. Since the output terminals of the slow and fast switching regulators are connected together, current sensing needs to be used to achieve appropriate power distribution.

The schematic diagram of the CLCC is shown in Fig. 11. The two input terminals are connected to the voltages proportion to the sensed slow switching regulator current (I_{slow}) and fast switching regulator current (I_{fast}), respectively. The transistor size of input pair is uneven to create the internal voltage offset responding to the proper ratio of I_{slow} and I_{fast}. The ratio developed in this work is around 2:1. The overdrive voltage (V_{ov}) for the input transistor pair can be designed by

$$\frac{V_{OV1}}{V_{OV2}} = \frac{\sqrt{W_2/L}}{\sqrt{W_1/L}}. \tag{8}$$

When ratio of I_{slow} to I_{fast} is low, the uneven differential amplifier turns ON M_{CL}, and the CLCC starts to supply current to the compensator circuit. The output voltage of the compensator increases and enlarges the duty cycle of the slow switching, raising the output current of the slow switching regulator. The CLCC keeps supplying current until the ratio is restored.

D. SR Enhancement Circuit

The schematic diagram of the slew-rate (SR) enhancement circuit is shown in Fig. 12. The charge pump consisting of the transistors, M_{PC} and M_{NC}, is on standby when the slew rate

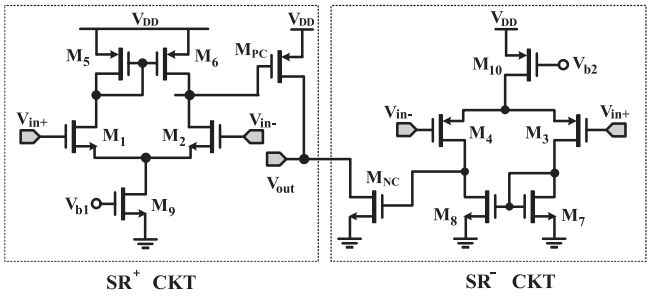

Fig. 12. Schematic diagram of slew-rate enhancement circuits.

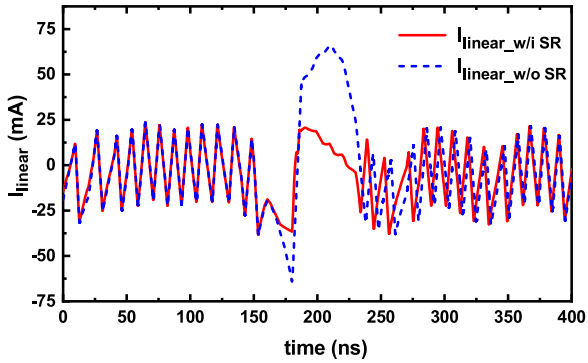

Fig. 13. Simulated linear regulator currents with and without SR enhancement circuit.

of the fast switching regulator is sufficient. On the contrary, the charge pump will source or sink additional current to avoid the need for the linear regulator to deliver excessive current. Therefore, the output stage of the linear regulator can operate at low quiescent current level to reduce its power consumption. Because the charge pump is inactive most of the time, its impact on overall efficiency degradation is very little.

M_{PC} and M_{NC} are controlled by the hysteretic window realized by the uneven differential pairs, M_1-M_2 and M_3-M_4. The uneven differential pairs present a voltage offset V_{os}. One of the input terminals is connected to the voltage that is proportional to the sensed linear regulator current (I_{linear}) and the other input terminal is connected to the reference voltage (V_{ref}). When the slew rate is sufficient, I_{linear} varies within the hysteretic window. When the slew rate is insufficient, I_{linear} exceeds the hysteretic window. The SR^+ driver is enabled to source extra current to the load when the sensed voltage of I_{linear} is larger than $V_{ref}+V_{os}$ and the SR^- driver is enabled when the sensed voltage is smaller than V_{ref}–V_{os}. The simulated linear regulator current with and without the SR enhancement circuit is shown in Fig. 13.

E. Driving Stage Circuits

The driving stage circuits for the switching regulators are basically the buffer chains with exponentially scaled transistors. The anti-shoot-through function is implemented by adding delay to the moment of turning ON the power transistors. The zero-current detector (ZCD) is incorporated in the delay inverter chain of the low-side switch. The schematic diagram of the driving stage circuits is shown in Fig. 14.

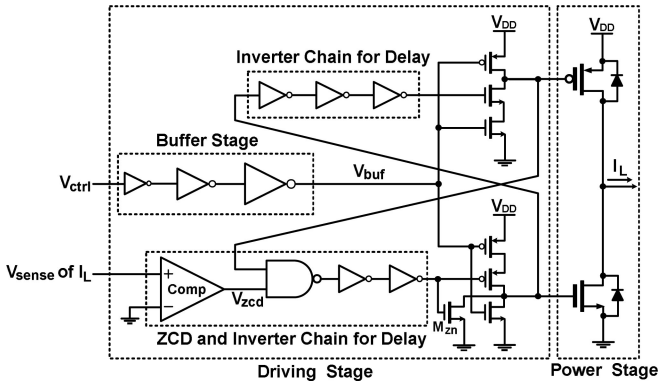

Fig. 14. Schematic diagram of driving stage circuits.

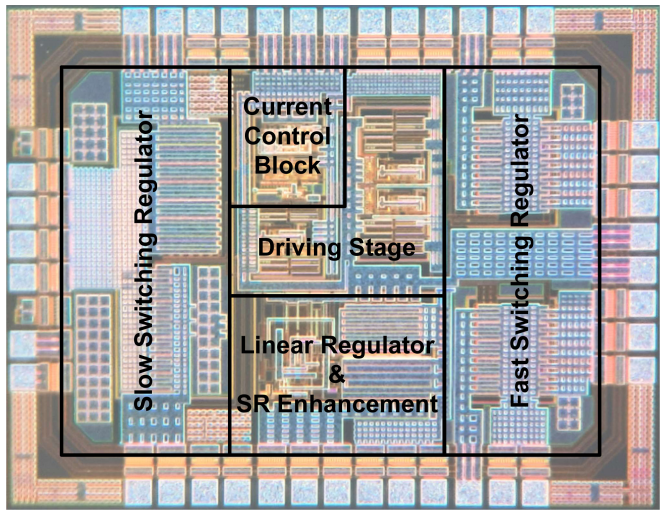

Fig. 15. Microphotograph of CMOS envelope tracking supply converter.

There are more than one regulators with their output terminals connected together in the parallel hybrid SCs. The reversed current may occur in the switching regulator when its low-side switch is turned ON and the currents of the other regulators flow through the switch [33]. It will cause significant power consumption and efficiency degradation. The ZCD is used in this article to avoid the issue of reversed current. V_{sense} is the sensed voltage of the inductor current I_L of the switching regulator. When I_L drops to zero, the low-side switch will be turned OFF to avoid reversed current.

IV. Measurement

The hybrid supply converter was implemented in a 0.25-μm CMOS technology and the die size including I/O pads was 1.94 mm $\times$ 1.49 mm. The microphotograph of the chip was shown in Fig. 15. The measurement setup of the envelope tracking SC was shown in Fig. 16. The test signal was the envelope of a 5G NR 40 MHz 256-QAM modulated signal, whose swing was from 0.5 to 4 V. The measured input and output signals of the

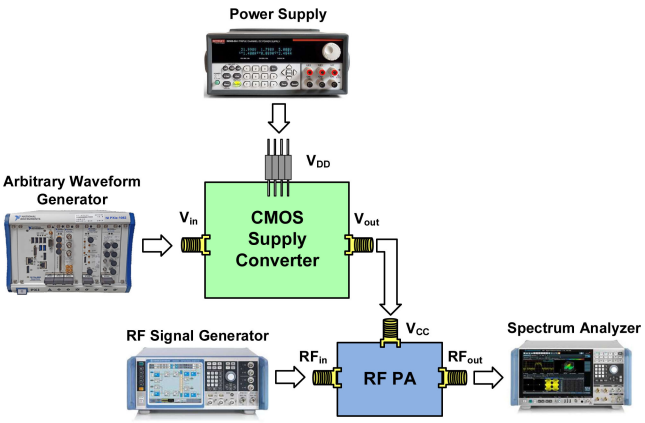

Fig. 16. Measurement setup.

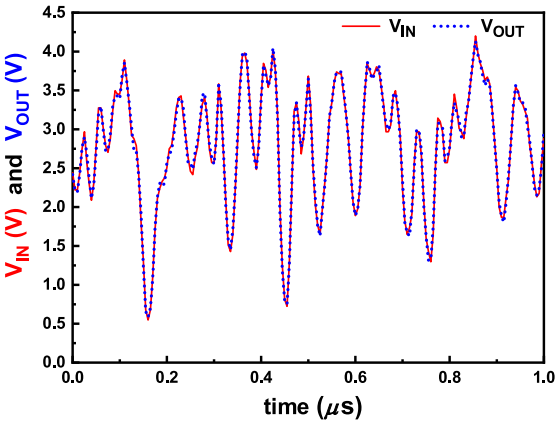

Fig. 17. Measured 40-MHz 5G NR input and output envelope signals of CMOS supply converter.

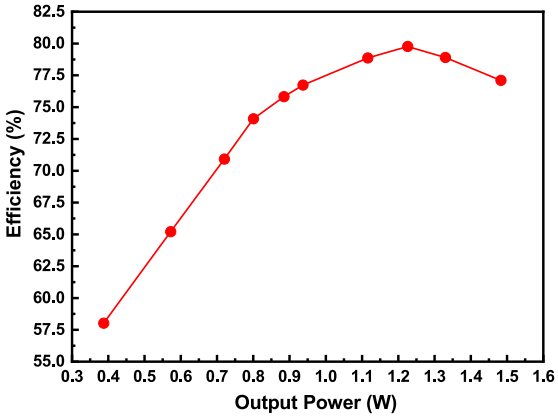

Fig. 18. Measured ET SC efficiency with respect to its output power.

hybrid SC were shown in Fig. 17 and the maximum difference was less than 200 mV. The maximum efficiency achieved by the CMOS hybrid SC was 79.1%. The measured efficiency with respect to the SC's output power was shown in Fig. 18.

The ET SC was also measured with an off-the-shelf RF PA, SKY66184-1 from Skyworks, operating at 2.14 GHz. The PAPR of the 5G NR 40 MHz 256 QAM test signal was 12 dB. The

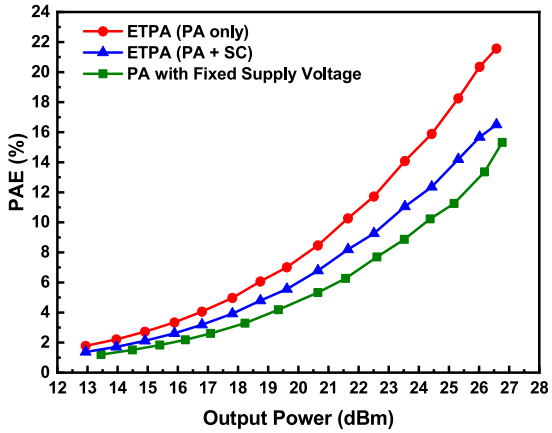

Fig. 19. Measured PAE of RF PA with fixed supply and envelope tracking supply.

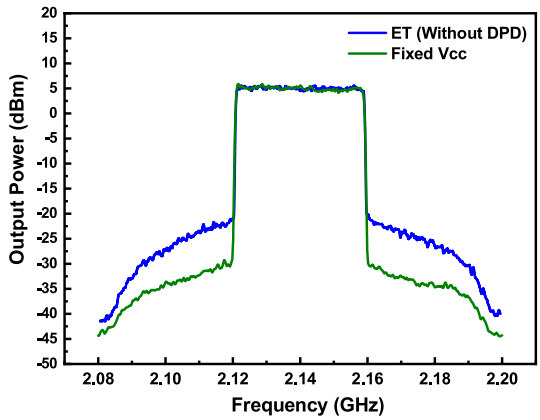

Fig. 20. Output spectrums of RF PA with fixed and envelope tracking supplies.

measured power-added efficiency (PAE) including the power consumption of RF PA and ET SC was 13.9% at the PA output power of 25 dBm. When the RF PA was measured with a fixed supply voltage, the PAE was only 10.8%. The envelope tracking technique with the presented SC achieved 3.1% improvement in PAE. The measured PAE with respect to PA output power for fixed supply and envelope tracking supply was shown in Fig. 19.

For mobile terminals tested with 5G NR 40-MHz 256-QAM signal, the ACLR and error vector magnitude (EVM) of the RF PA output needed to be lower than −30 dBc and 3.5%, respectively. The maximum output power of the ET PA able to pass the ACLR and EVM requirement without predistortion or calibration was 24.3 dBm with 17.2% of PAE. The measured ACLR and EVM were −30.6 dBc and 3.47%, respectively. For the RF PA with a fixed supply, the measured ACLR and EVM at the same output power were −38.4 dBc and 2.11%, respectively. The output signal spectrums for both fixed supply and ET PAs were shown in Fig. 20. Reducing the supply voltage of the fixed supply PA with a step-down converter could enhance the efficiency but degrade the linearity. The measured PAE is enhanced to 12.4% when lowering the supply voltage of the PA till the linearity becomes roughly the same as that of the ET PA.

TABLE II
SUMMARY OF CMOS SUPPLY CONVERTERS MEASURED WITH RF POWER AMPLIFIERS FOR MOBILE COMMUNICATIONS

	[17]	[18]	[19]	[20]	[21]	[22]	[23]	This Work
Technology	0.35-μm SiGe BiCMOS	0.35-μm BCD(2)	0.18-μm CMOS	0.32-μm SOI CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.25-μm CMOS
Supply (V)	4.2	5	5	3.9	3.45 ~ 5	4.7	3.6	5
Frequency (GHz)	2.4	0.7	1.85	0.85	1.71	1.7	1.95	2.14
PAPR (dB)	7	7.5	7.5	6.7	7.5	7.5	8.2	12
Mod. BW (MHz)	5	20	10	20	20	10	10	40
Modulation	LTE 16 QAM	LTE 16 QAM	LTE 16 QAM	LTE QPSK	LTE 16 QAM	LTE 16 QAM	LTE 64 QAM	5G NR 256 QAM
Converter Efficiency	N/A	78.4%	90%	74%	75.9%	81.5%	83%	79.1%
PAE Improvement	N/A	4 ~ 6 %	2.8%(1)	2.2%(1)	4.2%	3.6%	N/A	3.1%(1)
Supply Swing (V)	1.9 ~ 4.1	4.5	0.5 ~ 4.5	N/A	0.5 ~ 4.5	1.1 ~ 3	1.1 ~ 3.4	0.5 ~ 4
ACLR (dBc)	N/A	N/A	-34.2	-34	-33.6	-35.6	-35.6	-31.8
EVM (%)	5.0	5.6	2.8	N/A	3.2	3.0	6.0	3.0
Size (mm × mm)	1.1×1.5	4.03(4)	1.3×1.3	1.5×0.72	1.4×1.0	0.75×0.80	1.05×1.05(3)	1.94×1.49

(1) PAE calculation includes power consumption of supply converters.
(2) Bipolar-CMOS-DMOS.
(3) Core area.
(4) Unit is mm^2.

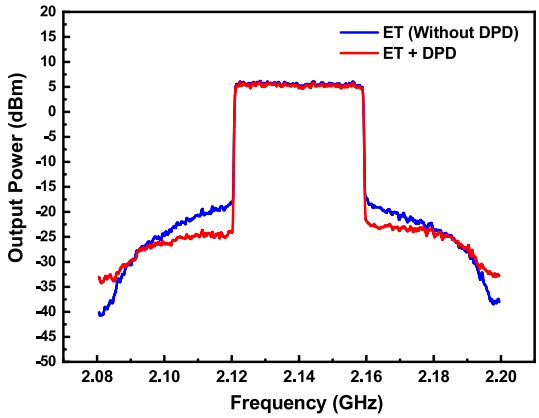

Fig. 21. Output spectrums of ET PA with and without using DPD.

The simple DPD technique could be used to linearize the ET PA for the output power above 25 dBm. With the lookup-table-based DPD, the ACLR of the ET PA was improved from −27.8 to −31.8 dBc at the output power of 25 dBm. The measured EVM with DPD was 3.0%. The output signal spectrums of the ET PA with and without DPD were shown in Fig. 21. The spectrum regrowth resulting from PA nonlinearity was diminished by DPD. Table II summarized the performance of the published CMOS supply converters that were measured with RF PAs for latest mobile communications. Although the PAPR of the 40-MHz 5G NR signal was several decibels higher than that of the 4G LTE signals, the measurement results demonstrated excellent performance potential of the proposed hybrid SC for sub-6 GHz 5G NR mobile applications.

V. CONCLUSION

A CMOS envelope tracking supply converter consisting of a linear, slow switching, and fast switching regulators was reported for the applications of 5G NR mobile terminals. In order to track the fast-varying signal envelope of 40-MHz modulation bandwidth, the two-phase hysteretic control method was proposed for the fast switching regulator. The slew-rate enhancement circuit was introduced in response to the high PAPR nature of sub-6 GHz 5G NR signal. The hybrid supply converter achieved a maximum efficiency of 79.1%. Compared to the RF PA without using envelope tracking supply, the PAE improvement of the RF PA with the proposed supply converter was 3.1% when tested with the 40-MHz 256-QAM 5G NR signal of which the PAPR is 12 dB.

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Yu-Chen Lin received the B.S. degree in electrical engineering from the National Taipei University of Technology, Taipei, Taiwan, in 2016, and the M.S. degree from the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, in 2019.

He is currently an Analog IC Design Engineer with Richtek Technology Corporation, Hsinchu, Taiwan. He is involved in architecture and IC implementation of various power management products.

Mr. Lin was a recipient of the Excellence Award by the 20th Macronix Golden Silicon Awards.

Yi-Jan Emery Chen (Fellow, IEEE) received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1987, the M.S. degree in electrical and computer engineering from the University of California at Santa Barbara, CA, USA, in 1991, and the Ph.D. degree in electrical engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2001.

From 1992 to 1993, he was a Software Engineer with Siemens Telecommunication, where he was involved with synchronous optical network (SONET) equipment development. From 1993 to 1996, he was with Tektronix, where he was responsible for electronic test and measurement solutions. From 2000 to 2002, he was with National Semiconductor, where he was involved with radio-frequency (RF) transceiver and RF power amplifier (PA) design. In 2002, he was with the Georgia Institute of Technology, as a member of the Research Faculty. Since 2003, he has been with the National Taiwan University, where he is currently a Professor. His recent research focuses on the design of RF integrated circuits (RFICs), RF power amplifiers, LCD/LED drivers, and power management ICs.

Dr. Chen served as an Associate Editor of the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2009 to 2015. He has been serving on the Technical Program Committees of the IEEE MTT-S International Microwave Symposium (IMS), and the IEEE Radio and Wireless Symposium (RWS) since 2008. He was the Chair of IEEE MTT-S Taipei Chapter from 2017 to 2018. He was the co-recipient of the 2000 IEEE MTT-S IMS Best Student Paper Award and also the 2008 University Team Award for Contribution to Industrial Economics from the Ministry of Economic Affairs, Taiwan. He has been the Advisor of several student award recipients including the Chi-Mei Award, Macronix Golden Silicon Award, FineTek Technology Award, Paper Award from the Institute of Chinese Electrical Engineering, and Master Thesis Award from Taiwan IC Design Society.