Two-Mode Controlled Single/Dual-Input DC–AC Inverter With Wide-Range DC Input

Xuefeng Chen, *Member, IEEE*, and Zhe Zhang, *Senior Member, IEEE*

***Abstract*—This article presents a two-mode controlled step-up inverter (TMCSI), which is capable of handling single or dual inputs with a wide range of dc input voltage. In comparison to traditional multistage dc/dc power conversion systems, the power conversion stage is reduced and the voltage/current stress of device is significantly alleviated without using high-voltage dc-bus capacitors. As a result, the reliability and overall conversion efficiency are improved accordingly. By combining the two working modes, the proposed inverter achieves uniform distribution of duty ratio under single/dual-input with a wide range of input voltage, and thereby is very suitable for systems having large input voltage variation. Moreover, based on the dual-input TMCSI, a novel power allocation method is also proposed to improve the system load-bearing ability. The power allocation method is controlled separately from two working modes that allows the two-input sources directly supply the ac load simultaneously. In this article, topology derivation, two-mode control strategy, characteristics of steady principle, and design criteria for the key circuit parameters are systematically analyzed, and important conclusions are obtained. Finally, the experimental results from the single/dual-input 500 VA 96–192 V_{dc} input and 220 V_{ac}/50 Hz output inverter prototype verify the effectiveness of the proposed TMCSI topology and its associated power regulation approach.**

***Index Terms*—Buck–boost converter, full bridge inverter, step-up inverter, two-mode control, wide range input voltage.**

NOMENCLATURE

D_{Ssn}	Duty ratio of selective switch S_{sn}.
d_1/d_{ST1}	Duty ratio of full-bridge inverter/ buck–boost converter.
u_{ab}	Output voltage of full bridge.
u_{i1}/u_{i2}	Output voltage of two input units.
U_{in}/ I_{in}	Output voltage/current of the input source n.
U_{os}	High-frequency switching voltage
$U_{os} =$	$(D_{Ss1}U_{i1} + D_{Ss2}U_{i2})$.
P_{i1M}	Maximum output power of PV cells.
U_{i1M}	PV's output voltage at maximum power point.
U_{il_ref}	Reference voltage for PV cells.
I_{il_ref}	Reference current for PV cells.
P_o	Output power of the inverter.
k	Output value of the voltage regulator.
K_m	Maximum value of k.
u_{sn}	Modulation signal of carrier waveform.
U_{cm}	Amplitude of carrier waveform.
p_{i1}/ p_{i2}	Output power of the two input sources U_{i1}/U_{i2}.
I_{L1avg}	Average current of inductor L_1.

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Xuefeng Chen is with the Department of Electrical Engineering, Fuzhou University, Fuzhou 350400, China (e-mail: cxf199401@163.com).

Zhe Zhang is with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark (e-mail: zz@elektro.dtu.dk).

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I. INTRODUCTION

NOWADAYS applying renewable energies to distributed generation, transportation, multienergy systems, etc., has become a key technology for future developments toward a fossil-free society. DC–AC inverters have significance of power transforming for ac load or grid, and thereby are critical in the application of solar energy, wind, and hydrogen.

Many research works have been done to pursue both high conversion efficiency and high ac quality in a hybrid system with multiple and various dc inputs, such as photovoltaics, fuel cells, and batteries [1]–[4]. Usually a step-up function is needed in such dc–ac power conversion systems [3], [4]. The traditional low-frequency link inverter proposed in [5] and [6] is cascaded by full/half-bridge inverter and a step-up line-frequency transformer. It inherits buck-type inverters' advantages, e.g., high efficiency, high reliability, simple modulation and control; however, an inverter system employing line-frequency (50/60 Hz) transformers, suffers from high cost, bulky size, and loud acoustic noise. Li and Wolfs [7] and Hu *et al.* [8] presented a multistage dc–ac power system, including the following:

1) the conventional two-stage dc–ac power system in [9] and [10], which consists of a boost converter as the front-end dc–dc step-up converter and a full/half-bridge inverter;
2) the multistage high-frequency link (HFL) inverter proposed in [11] and [12], which is configured by a dc–dc converter with a high-frequency transformer and a full-bridge inverter, in which bidirectional switches are normally adopted;
3) the differential-mode HFL inverter presented in [13] and [14], which connects the output of two identical HFL dc–dc converters in a differential output.

These cascade-connected conversion systems have a relatively high voltage boosting ability, but induce high conduction and switching losses, so that the overall efficiency suffers.

On the other hand, when these inverters are powered by renewable or clean energy sources that have varied output voltage due to the random and intermittent characteristics, e.g., photovoltaics or their inherent electrochemical features, e.g., fuel cells, the

overall power conversion efficiency suffers because the wide input voltage range causes a narrow or even extreme duty ratio regulating range under a ultrahigh or low-input voltage. The quasi-Z source inverter, as a single-stage converter, proposed in [15] and [16] can handle wide-range input voltage, and has less number of active switches and high-quality ac output waveform, but high current and voltage stresses over active switches, bulky passive components and complicated control make it difficult to achieve high efficiency and low cost for matching the demand of the large-scale usage in mass production. A new concept of dual-dc-port asymmetrical multilevel inverter (DP-AMI) is studied in [17]. Due to the asymmetrical multiple voltage levels generated in the inverter, the proposed DP-AMI can achieve reduced number of power stages as well as lower voltage/current stresses over switches. In [18] and [20], the promising multilevel inverters in medium and high power.

Applications are proposed, which can handle the series-connected separate dc-voltage source or regulated voltage from the conventional dc–dc converter for ac load supply, and generate high-quality staircase pseudo sinusoidal voltage waveform with low total harmonic distortion. These multilevel inverters allow use of less sizable output filters and offer robust, efficient, and fault-tolerant features.

The major contribution of this article is to propose a new family of a two-mode controlled step-up inverter (TMCSI) and its associated control strategy. The proposed dc–ac power system has following advantages.

1) Both the number of power conversion stages and the voltage/current stress of devices are reduced without using high-voltage bus capacitors that is beneficial for improving efficiency and reducing converter size/volume.
2) Using the two working modes, the proposed inverter can be effectively used in the application of wide-range input voltage for a uniform distribution of duty ratio under input voltage variation.
3) A TMCSI-based dual-input inverter with a power allocation control is proposed. This dual-input inverter allows two input dc sources to directly supply an ac load simultaneously, and also inherits the advantages of the two-mode control method, which help to achieve the uniform distribution of duty ratio under single- or dual-input operation. Therefore, semiconductors' current stress is reduced significantly.

The rest of this article is organized as follows. After the introduction, Section II presents the derivation of the proposed TMCSI and its topology family. Section III provides the analysis of two-mode control strategy and operation principle under single- and dual-input. Section IV discusses the proposed inverter's characteristics and its design considerations. Section V gives experimental results to verify the theoretical analysis and design. Finally, Section VI concludes this article.

II. Proposed TMCSI and Its Topology Family

The proposed TMCSI is shown in Fig. 1, which consists of n T-networks and a full-bridge inverter. The more the number of T-network is, the higher the voltage gain, i.e., the lower input voltage that the inverter can have. The T-network is actually a buck/boost dc circuit that is composed of inductor L_1, capacitor C_1, and power switches S_{T1}, S_{T2}. It can realize bidirectional power transforming as well as boost input voltage. It is noteworthy that the shoot through issue of H-bridges can be avoided due to the T-network circuit that results in high system reliability. Therefore, the proposed inverter based on buck/boost converter (BBC) can also be called as TMCSI-BBC. Taking $n = 1$ and positive cycle of output voltage u_o as an example, there are two working modes.

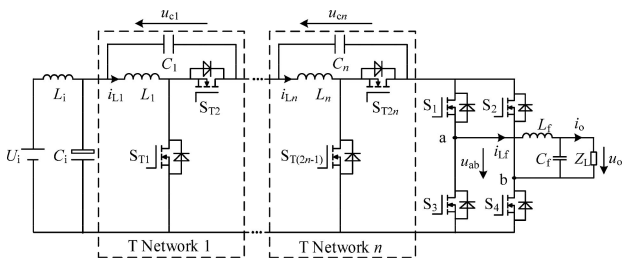

Fig. 1. Topology of TMCSI-BBC.

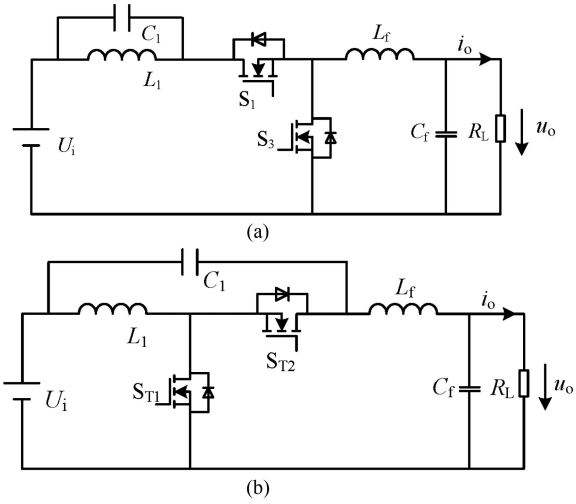

Fig. 2. Equivalent circuit of the proposed TMCSI-BBC. (a) Equivalent circuit under $U_i > |u_o|$. (b) Equivalent circuit under $U_i < |u_o|$.

Mode I: When $U_i >$ the absolute value $|u_o|$, S_{T1} keeps OFF and S_{T2} is ON. The full-bridge inverter is controlled by sinusoidal pulsewidth modulation (SPWM), and the output u_{ab} is a PWM waveform. Its equivalent circuit is plotted in Fig. 2(a). It can be seen that a new power flow path between the low-voltage input U_i and ac output side is constructed that allows U_i to supply the load directly due to the low impedance characteristic of the intermediate capacitive link under high frequency.

Mode II: When $U_i < |u_o|$, the T-network has complementary SPWM switching, U_i and C_1 supply the load in series, and at the same time the full-bridge inverter works in a low-frequency polar-inversion manner, as shown in Fig. 2(b).

Therefore, the regulation of ac output voltage can be realized by combing the two working modes and shifting between these two modes based upon the voltage relationship of U_i and $|u_o|$.

Besides the T-network structure, the proposed two-mode control can be extended further to the Z-source inverter and its

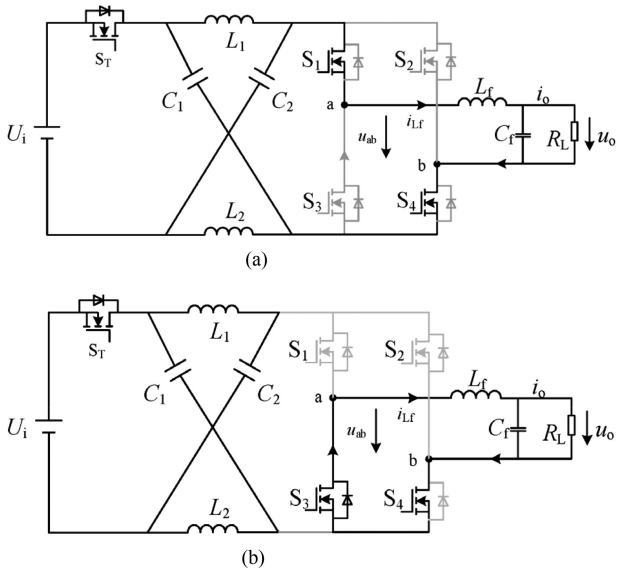

Fig. 3. Equivalent circuit of TMCSI-ZN under $U_i > |u_o|$. (a) Equivalent circuit I. (b) Equivalent circuit II.

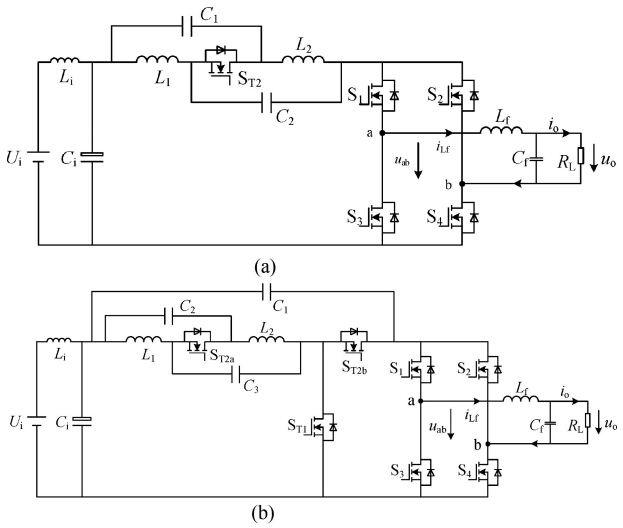

Fig. 4. Topology of the proposed TMCSI based on quasi-Z network. (a) Quasi-Z source inverter. (b) TMCSI-QZ.

derivatives. By replacing C_1 and C_2 with small film capacitors, the conventional Z-source inverter can be controlled by the same aforementioned two-mode control approach. As a result, the voltage and current stress on both L_1, L_2 and the power switches is reduced that can decrease component size and cost, as well as improve the overall converter efficiency. When $U_i > |u_o|$, the full-bridge inverter works with SPWM, as shown in Fig. 3. When $U_i < |u_o|$, the shoot-through duty ratio of the full-bridge inverter legs can be regulated to boost U_i. By combining these two working modes, the output voltage inversion is achieved. Therefore, this proposed TMCSI based on the simplified Z-network can be called TMCSI-ZN. The topology of quasi-Z source inverter is shown in Fig. 4(a), the two-mode control can also be used as TMCSI-ZN does. To obtain higher boost ability, the topology can be changed, as shown in Fig. 4(b), and this proposed TMCSI

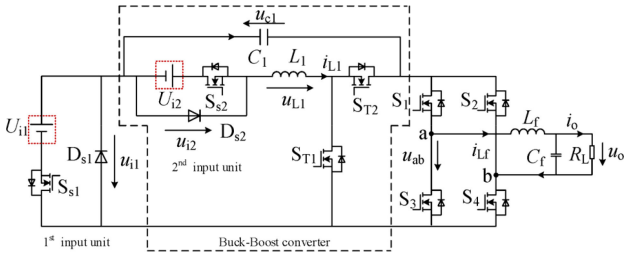

Fig. 5. Topology of the proposed dual-input inverter based on TMCSI-BBC.

based on the simplified quasi-Z-network can then be called as TMCSI-QZ.

Moreover, the proposed topology family can be extended to multiple-input inverters. Therefore, an additional input can be added to the proposed TMCSI-BBC, and forms a dual-input inverter, as shown in Fig. 5 and the second input is recommended to be connected in series with L_1. The two inputs of U_{i1} and U_{i2} can supply the ac load simultaneously.

More generally speaking, if the power allocation among n input sources is needed, each input source $U_{\rm in}$ should be equipped with a corresponding selective switch $S_{\rm sn}$ and a by-pass diode $D_{\rm sn}$. By regulating the duty ratio ($d_{\rm Ssn}$) of $S_{\rm sn}$ with the line frequency (LF) $f_{\rm o}$ of 50 Hz, and $f_{\rm o} \ll f_{\rm c}$ (PWM carrier frequency), the converter can realize power allocation between input sources.

III. Two-Mode Control Strategy and Operation Principle

The operation principle of two-mode control strategy under single input and dual inputs is the same. Nevertheless, power allocation control is needed for the two input sources in the dual-input case.

A. Two-Mode Control Strategy

Taking the proposed TMCSI-BBC with single input as an example, the typical waveforms of two-mode control strategy are shown in Fig. 6. Due to symmetry of an entire sinusoidal period of $u_{\rm o}$, only the positive half cycle is analyzed, where S_4 remains ON and S_2 is OFF. When $|u_{\rm o}|$ is lower than the switching voltage $U_{\rm os} = U_i$, $S_{\rm T1}$ and $S_{\rm T2}$ always keep OFF and ON, respectively. The full-bridge inverter is controlled by SPWM, and the output $u_{\rm ab}$ is a PWM waveform.

However, when $|u_{\rm o}| \geq U_{\rm os} = U_i$, S_1 and S_3 keep ON and OFF, respectively. $S_{\rm T1}$ and $S_{\rm T2}$ of buck/boost converter work with complementary SPWM driving signals, and $u_{\rm ab} = U_i + u_{c1}$ to realize boosting the input voltage. By combining these two operation modes, i.e., full-bridge mode and buck/boost mode, depending on $|u_{\rm o}|$ and $U_{\rm os} = U_i$, the inverter can output ac sinusoidal voltage.

B. Operation Principles for the Dual-Input System

For the dual-input operation, based on the proposed two-mode control strategy, power allocation for the two input sources is also needed by adjusting the duty ratio ($d_{\rm Ssn}$) of $S_{\rm sn}$. For example, if U_{i1} and U_{i2} employ photovoltaic (PV) cells and fuel cells as the

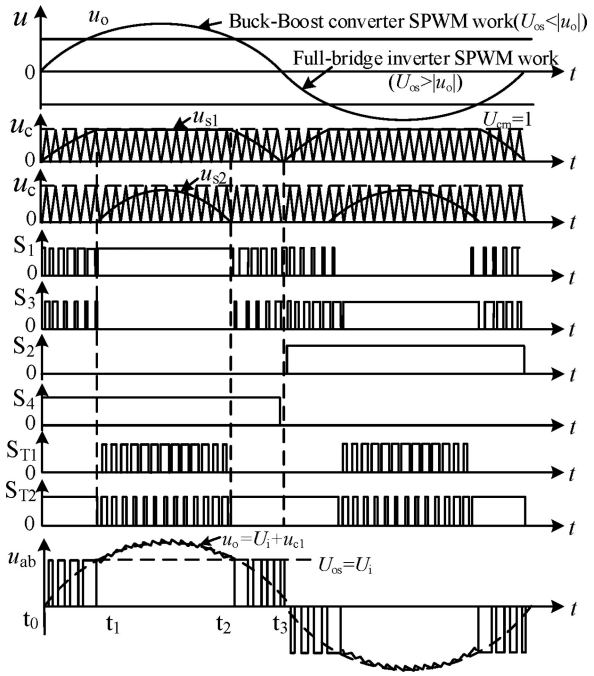

Fig. 6. Typical waveforms of two-mode control strategy.

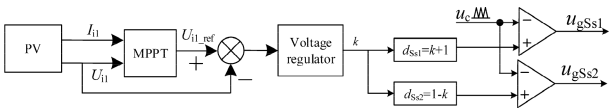

Fig. 7. MPPT control diagram with PWM modulation.

input sources, respectively, a master–slave energy management is adopted to achieve the full use of power generated from PV. Namely, the first input U_{i1} is chosen as the master power supply and need tracking its maximum power point (MPP), and the second input U_{i2} with adjustable output power supplements the power difference between the first input U_{i1} and the load in off-grid systems.

However, there is no power flow between the two input sources, and therefore the unidirectional renewable sources such as fuel cells, PVs, or wind hybrid system are preferably used as an input.

The MPPT control diagram with PWM modulation is shown in Fig. 7, PV's output voltage U_{i1} and current I_{i1} are sampled and its reference voltage $U_{\mathrm{il\_ref}}$ will be calculated by an MPPT algorithm. U_{i1} is controlled to follow $U_{\mathrm{il\_ref}}$ by a voltage regulator with an output of k. Then, the duty ratio (d_{Ssn}) of S_{sn} is obtained as $d_{\mathrm{Ss1}} = k + 1$ and $d_{\mathrm{Ss2}} = 1 - k$, the driver signal of S_{sn} is obtained by the PWM modulation. Power allocation between the two inputs is directly controlled by the voltage regulator for PV's MPPT, it makes the control system relatively simple and reliable [20]. Usually the MPPT control loop does not require high control bandwidth, which is set as $f_{\mathrm{o}} = 50$ Hz in this article, so d_{Ssn} can be considered as a constant value of D_{Ssn} in a LF period, as shown in Fig. 8. According to the relationship between the maximum power $P_{i1\mathrm{M}}$ provided by U_{i1} and the ac load P_{o}, the proposed dual-input inverter has two operating states, as shown in Fig. 8(a) and (b), respectively. Each operating state

TABLE I
TWO OPERATION STATES

Operating State	k	D_{Ss1}=k+1, D_{Ss2}=1-k	Two Working Modes		Typical Waveforms in Fig. 8
			Buck	Buck-Boost	
I	$K_m \geq k \geq 0$	D_{Ss1}=1, $1 \geq D_{\mathrm{Ss2}} \geq 0$	A	C	(a)
II	$0 > k \geq -K_m$	$1 \geq D_{\mathrm{Ss1}} \geq 0$, D_{Ss2}=1	B	D	(b)

consists of two working modes, and their equivalent circuits are shown in Fig. 9. $K_m > 1$ is the maximum value of $|k|$.

1) State I [see Fig. 8(a)]: If $P_{i1\mathrm{M}} > P_{\mathrm{o}}$, U_{i1} will supply the load alone. PV output voltage U_{i1} is larger than $U_{\mathrm{il\_ref}}$ and k is clamped at K_m by the voltage regulator. So ($D_{\mathrm{Ss1}} = 1 + k$) > 1 is clamped at $D_{\mathrm{Ss1}} = 1$, and then $D_{\mathrm{Ss2}} = 1 - k = 0$. Namely, S_{s1} keeps ON, and S_{s2} is OFF. Decreasing $P_{i1\mathrm{M}}$ to $P_{\mathrm{o}} \geq P_{i1\mathrm{M}} \geq P_{\mathrm{o}} U_{i1\mathrm{M}}/(U_{i1\mathrm{M}} + U_{i2})$, and U_{i1} is not sufficient to support the load alone, k will be regulated from 1 to 0 by the voltage regulator. While D_{Ss1} is still clamped at 1 and $1 \geq D_{\mathrm{Ss2}} \geq 0$, which means S_{s1} remains ON. The part of P_{o} provided by U_{i2} is adjusted by D_{Ss2}, which help U_{i1} to track its MPP. Since D_{Ssn} is almost a constant value in a LF period, U_{os} can be expressed as $U_{\mathrm{os}} = U_{i1} + D_{\mathrm{Ss2}} U_{i2}$ in State I.

Buck mode [Interval $t_0 - t_1$ and $t_2 - t_3$]: When $u_{\mathrm{o}} \leq U_{\mathrm{os}}$, in this mode, S_{T1} keeps OFF, S_{T2} ON, only the full-bridge inverter SPWM works, and its equivalent circuit A is shown in Fig. 9(a).

Buck–boost mode [Interval $t_1 - t_2$]: When $u_{\mathrm{o}} > U_{\mathrm{os}}$, S_1 keeps ON, S_3 is OFF, only the buck/boost converter works with complementary SPWM switching. U_{i1} and C_1 in series supply the load, shown as the equivalent circuit C in Fig. 9(b).

2) State II [see Fig. 8(b)]: If $P_{i1\mathrm{M}}$ provided by U_{i1} continues to decrease below $P_{\mathrm{o}} U_{\mathrm{ilM}}/(U_{\mathrm{ilM}} + U_{i2}) > P_{i1\mathrm{M}}$, k will be regulated from 0 to $-K_m$. Thus, $D_{\mathrm{Ss2}} = 1\text{-}k$ is clamped to $D_{\mathrm{Ss2}} = 1$, and $1 > D_{\mathrm{Ss1}} \geq 0$, which means S_{s2} keeps ON, the part of P_{o} provided by U_{i1} is regulated by D_{Ss1}, and makes U_{i1} track MPP, and U_{i2} supplements the power difference between $P_{i1\mathrm{M}}$ and P_{o}. U_{os} can be expressed as $U_{\mathrm{os}} = D_{\mathrm{Ss1}} U_{i1} + U_{i2}$ in State II.

Buck mode [Interval $t_{\mathrm{a}} - t_{\mathrm{b}}$ and $t_{\mathrm{c}} - t_{\mathrm{d}}$]: $u_{\mathrm{o}} \leq U_{\mathrm{os}}$, it is the same as in State I, i.e., the full-bridge inverter works, and its equivalent circuit B is shown in Fig. 9(a).

Buck–boost mode [Interval $t_{\mathrm{b}} - t_{\mathrm{c}}$]: $u_{\mathrm{o}} > U_{\mathrm{os}}$, the buck/boost converter works, $D_{\mathrm{Ss1}} U_{i1}$ and C_1 supply the load in series, and its equivalent circuit D is shown in Fig. 9(b).

In summary, when $P_{i1\mathrm{M}}$ decreases, k will decrease by the voltage regulator to reduce the output power of U_{i1} and make U_{i1} achieve MPPT, and vice versa. The dual-input system has two operating states, and each state consists of the two working modes, which have been listed in Table I. Combining the two working modes, the proposed inverter achieves voltage inversion under single/dual-input source.

The proposed control method is complex than the conventional multistage dc/ac power conversion system. However, it should be noted that at a certain time, only one pair of switches operate in high frequency that is in buck mode: S_1 and S_3 (zero voltage switching-ZVS), or S_2 (ZVS) and S_4 in the positive and negative half cycles, respectively; in buck–boost mode: S_{T1}

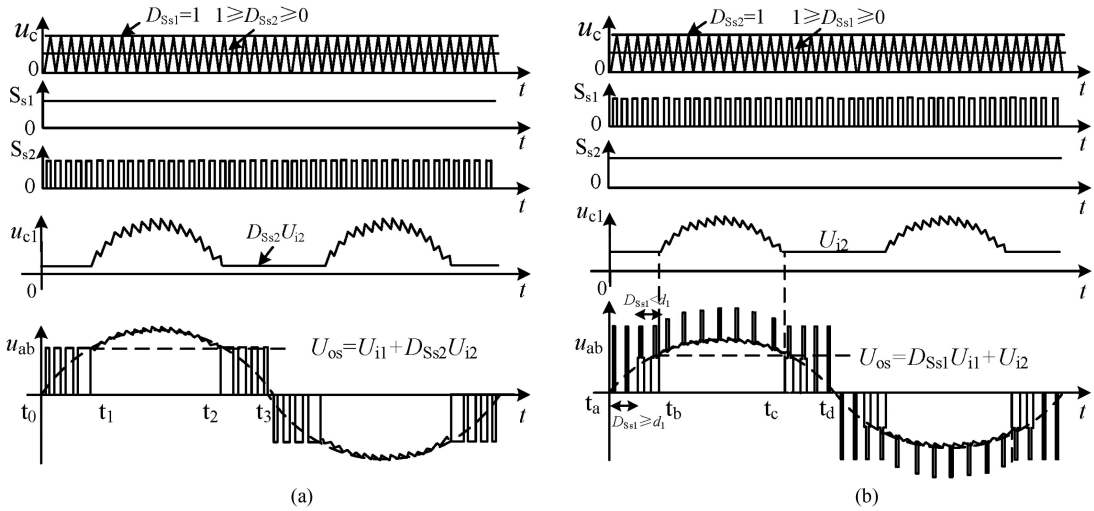

Fig. 8. Typical waveforms of two operating states in a LF period. (a) State I: $K_m \geq k \geq 0$. (b) State II: $0 > k \geq -K_m$.

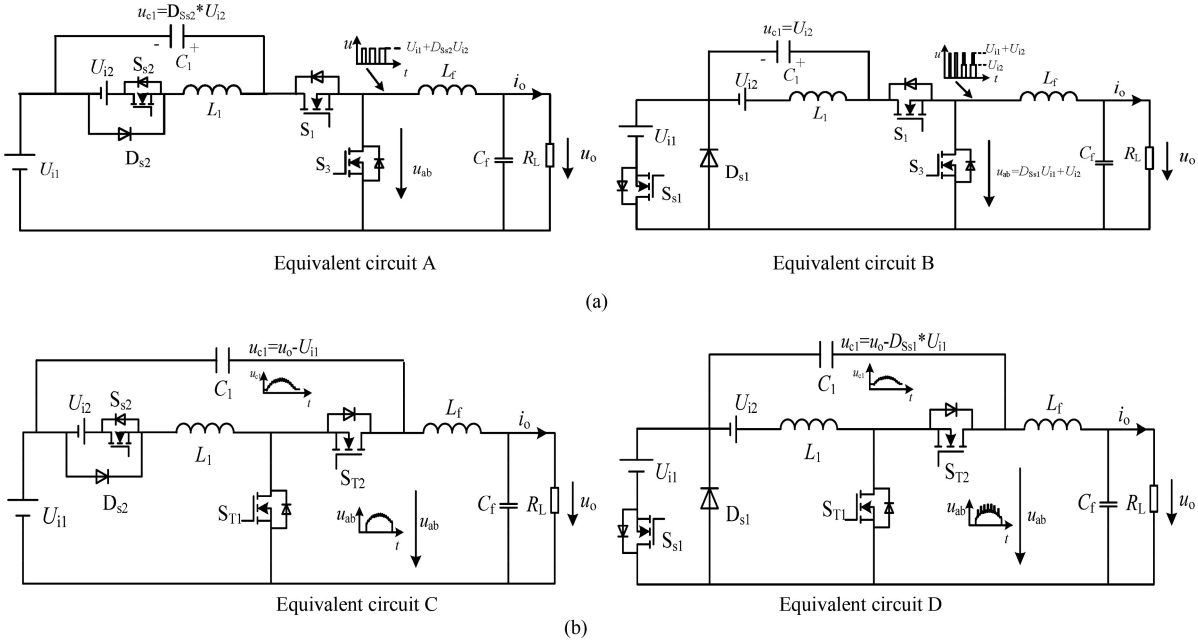

Fig. 9. Equivalent circuit of the proposed dual-input inverter. (a) Equivalent circuit in Buck mode. (b) Equivalent circuit in Buck-Boost mode.

and S_{T2} (ZVS) in high frequency, and S_1–S_4 operate in line frequency. The buck mode and buck–boost mode are controlled independently, which make the system have high reliability and simple control logic. Moreover, the proposed power allocation method for the two inputs is implemented separately from the two-mode control, therefore, in practice, this control under single-/dual-input can be easily realized using a digital signal processor.

IV. Characteristics and Design Consideration

A. Output Characteristics

When the full-bridge inverter operates in a steady state, the output voltage of u_o as a function of U_{i1} and U_{i2} can be expressed as follows:

$$u_o = \begin{cases} d_1(U_{i1} + D_{Ss2}U_{i2}) & D_{Ss1} \geq d_1 \\ D_{Ss1}U_{i1} + d_1 D_{Ss2}U_{i2} & D_{Ss1} < d_1 \end{cases} \quad (1)$$

where d_1 is the duty ratio of the full-bridge inverter. When the buck–boost converter operates, the output voltage is calculated by

$$u_o = \begin{cases} D_{Ss1}U_{i1} + \frac{d_{ST1}U_{i1} + D_{Ss2}U_{i2}}{1-d_{ST1}} & D_{Ss1} \geq d_{ST1} \\ D_{Ss1}U_{i1} + \frac{D_{Ss1}U_{i1} + D_{Ss2}U_{i2}}{1-d_{ST1}} & D_{Ss1} < d_{ST1} \end{cases} \quad (2)$$

where d_{ST1} is the duty ratio of the buck–boost converter.

Then, switching voltage U_{os} between the two working modes can be derived from (1) or (2), where $d_1 = 1$ or $d_{ST1} = 0$

$$U_{os} = D_{Ss1}U_{i1} + D_{Ss2}U_{i2}. \quad (3)$$

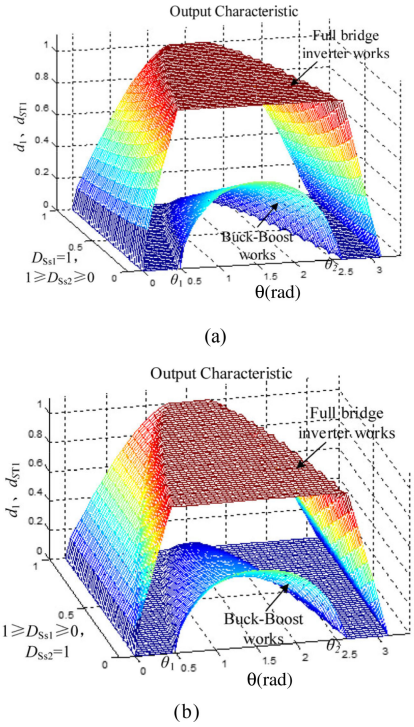

Fig. 10. Output characteristic of the proposed dual-input inverter. (a) $D_{\mathrm{Ss1}} = 1$, $1 \geq D_{\mathrm{Ss2}} \geq 0$. (b) $1 \geq D_{\mathrm{Ss1}} \geq 0$, $D_{\mathrm{Ss2}} = 1$.

The corresponding output characteristic curves, which are obtained from (1) and (2), can be plotted in Fig. 10. It shows that U_{os} increases with increasing D_{Ssn}, and the working time of full-bridge inverter becomes longer, and conversely the buck–boost's operation time is shorter. When $U_{\mathrm{os}} > \sqrt{2}U_{\mathrm{o}}$ (output voltage rms value), the buck–boost converter stops working. When $U_i < |u_{\mathrm{o}}|$, the voltage gain of the proposed TMCSI-BBC, the two mode controlled Z-source/Quasi-Z source inverter and TMCSI-QZ can be expressed in (4)–(6), respectively,

$$U_{o\_\mathrm{TMCSI-BBC}} = U_i / (1 - d_{\mathrm{ST1}}) \tag{4}$$

$$U_{o\_Z/\mathrm{QZ}} = U_i (1 - d_{\mathrm{ST1}}) / (1 - 2 \cdot d_{\mathrm{ST1}}) \tag{5}$$

$$U_{o\_\mathrm{TMCSI-QZ}} = U_i / (1 - 2 \cdot d_{\mathrm{ST1}}) . \tag{6}$$

B. Design Consideration

When the buck/boost converter works, the devices L_f and C_f act as an additional filters, so a smaller C_1/L_1 can be chosen with a larger high-frequency voltage/current ripple. Ignoring the current of C_1, in steady state, the average current of L_1 in one high-frequency period can be expressed as

$$I_{L1\mathrm{avg}} = \frac{u_{\mathrm{o}}}{R_{\mathrm{L}}(1 - d_{\mathrm{ST1}})} \tag{7}$$

where R_L is the load resistance.

Assuming the maximum current high-frequency ripple is about 60% of the maximum average current $I_{L1\mathrm{avgmax}}$, L_1 can be derived as (8). In the dual-input application, the equivalent

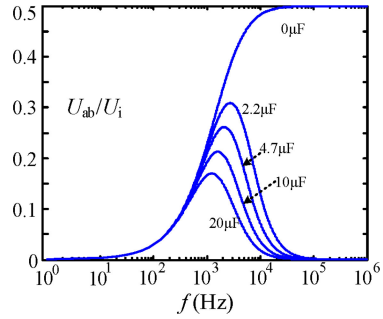

Fig. 11. Characteristic curves of U_{ab}/U_i to C_1 and f.

$$U_i = U_{i1} + U_{i2}$$

$$L_1 \geq \frac{U_{\mathrm{i}}(\sqrt{2}U_{\mathrm{o}} - U_{\mathrm{i}})U_{\mathrm{imin}}R_{\mathrm{Lmin}}T_{\mathrm{s}}}{60\%(\sqrt{2}U_{\mathrm{o}})^3} \tag{8}$$

where R_{Lmin} is the minimum load resistance and U_{imin} is the minimum input voltage.

In the same way, L_f can be derived in (9) based on 40% of the maximum average output current. When $u_{\mathrm{o}} = U_i/2$, L_f gets the minimum value

$$L_{\mathrm{f}} \geq \frac{u_{\mathrm{o}}(U_{\mathrm{i}} - u_{\mathrm{o}})R_{\mathrm{Lmin}}T_{\mathrm{s}}}{40\% * 2U_{\mathrm{i}}\sqrt{2}U_{\mathrm{o}}}. \tag{9}$$

When the full-bridge inverter works, L_1 is connected with C_1 in parallel, and the corresponding equivalent impedance is $Z_{\mathrm{L}} = sL_1/(1 + s^2L_1C_1)$, where s is the Laplace complex frequency. The impedance of LC-type output filter is $Z_{\mathrm{o}} = sL_f + R_{\mathrm{o}}/(1 + sC_fR_{\mathrm{o}})$. Assuming that $U_{\mathrm{ab}}/U_i = Z_{\mathrm{L}}/(Z_{\mathrm{L}} + Z_{\mathrm{o}})$, and the relationship between u_{ab}/U_i, C_1 and frequency f is plotted in Fig. 11. It can be seen that when $C_1 = 0$, U_{ab}/U_i is up to 0.5 in the intermediate and higher frequency range. With the increase of C_1, the band-stop frequency bands around the switching frequency get narrower. To obtain fast dynamic response and also reduce the reactive current, size/volume of the conversion system, $C_1 = 2.67\ \mu$F is selected for the experimental prototype.

C. Power Relationship Between the Two Inputs and Output

When the full-bridge inverter works, the load power P_{o} supplied by each inputs can be derived as

$$\begin{cases} P_{i1} = \frac{D_{\mathrm{Ss1}}U_{i1}}{D_{\mathrm{Ss1}}U_{i1} + D_{\mathrm{Ss2}}U_{i2}}P_{\mathrm{o}} \\ P_{i2} = \frac{D_{\mathrm{Ss2}}U_{i2}}{D_{\mathrm{Ss1}}U_{i1} + D_{\mathrm{Ss2}}U_{i2}}P_{\mathrm{o}}. \end{cases} \tag{10}$$

When the buck–boost converter works, the average input current i_{i2} of U_{i2} under can be expressed as

$$i_{\mathrm{i2}} = D_{\mathrm{Ss2}}I_{\mathrm{L1avg.}} \tag{11}$$

The instantaneous output power P_{o} provided by U_{i2} can be derived from (2), (7), and (11), and expressed as

$$P_{i2} = D_{\mathrm{Ss2}}U_{i2}I_{L1\mathrm{avg}} = D_{\mathrm{Ss2}}U_{i2}\frac{u_{\mathrm{o}}}{R_{\mathrm{L}}(1 - d_{\mathrm{ST1}})}. \tag{12}$$

In (12), P_{i2} is the function of D_{Ss2} and d_{ST1}. In operating State I, P_{i2} increases with increasing D_{Ss2}. In State II, $D_{Ss2} = 1$, as D_{Ss1} decreasing, d_{ST1} will increase and P_{i2} increase. Therefore, by adjusting D_{Ssn}, the control strategy can realize

TABLE II
PARAMETERS OF THE SINGLE/DUAL-INPUT PROTOTYPE

Parameter/Elements	Value
Rated Power	0.5kVA
$U_{\rm i}$ (Single input)	96-192VDC
U_{i1}/U_{i2} (Dual input)	96-148VDC
$u_{\rm o}$	220VAC50Hz
Switching Frequency	25kHz
L_1	500uH
C_1	2.2uF+0.47uF
$L_{\rm f}$	800uH
$C_{\rm f}$	2.2uF
S_{T1}, S_{T2} and S_1~S_4	IXFQ34N50P3
S_{s1}、S_{s2}	AP18N20GS/P-HF
D_{s1}、D_{s2}	MBR20H200CT
Control Circuit Chip	DSP TMS320F28335

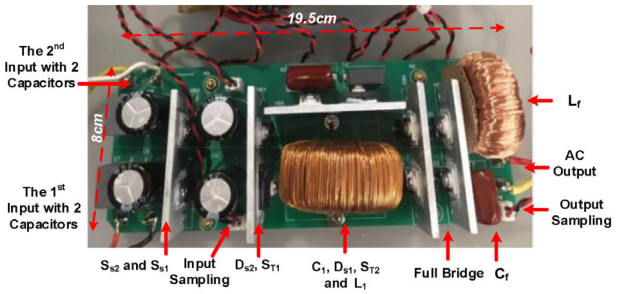

Fig. 12. Prototype of the proposed dual input inverter.

power allocation for the two input sources, and allow U_{i1} to track the MPP, and $P_{\rm o}$ supplied by U_{i1} can be expressed as $P_{i1} = P_{\rm o} - P_{i2}$.

V. EXPERIMENTAL RESULTS

The proposed dual-input inverter based on TMCSI-BBC with master–slave power distribution has been constructed in laboratory and the corresponding experimental test is carried out. The first input source U_{i1} uses a programmable solar simulator TC.P.16.800.400.S to simulate PV cells and the second input U_{i2} uses a power supply of 62012P-600-8 to supplement the load. The converter specifications as well as adopted components are listed in Table II. The prototype is shown in Fig. 12.

The maximum voltage stress over semiconductor devices of the proposed single-input TMCSI is $\sqrt{2}U_{\rm o}$. However, the voltage stress of the dual-input inverter based on TMCSI–BBC is $(1-D_{Ss1})U_{i1} + \sqrt{2}U_{\rm o}$ in buck–boost mode under operating State II, where the full-bridge inverter have no switching spike voltage. To lower the voltage stress, D_{Ss1} is limited at $1 \geq D_{Ss1} \geq 0.2$, which means the MPPT for U_{i1} stops working under some extremely low power conditions like partial shading or cold rainy weather, and IXFQ34N50P3 with rated voltage of 500 V is chosen for the proposed inverter. An *RC* snubber, placed in front of the full-bridge inverter and connected in parallel, can also be used.

The steady-state experimental waveforms of the off-grid dual-input system with the rated resistive load are shown in Fig. 13. The experimental results show that

1) S_4 remains ON in the positive half-cycle of $u_{\rm o}$. When $|u_{\rm o}| < U_{\rm os}$, $S_{\rm T1}$ keeps OFF and $S_{\rm T2}$ is ON, the full-bridge inverter works in high frequency and $u_{\rm ab}$ is a PWM wave. When $|u_{\rm o}| > U_{\rm os}$, S_1 keeps ON, $S_{\rm T1}$ and $S_{\rm T2}$ work in high frequency alternatively, and $u_{\rm ab} = D_{Ss1}U_{i1} + u_{c1}$.
2) When the full-bridge inverter works, the SPWM voltage is $U_{\rm os} = D_{Ss1}U_{i1} + D_{Ss2}U_{i2}$, as shown in Fig .13(a), when the buck–boost converter works, the maximum drain–source voltage of $S_{\rm T1}$ in State II is $u_{\rm dsT1} = D_{Ss1}U_{i1} + u_{c1}$.
3) By combining the two working modes, high-quality 220 V/50 Hz ac waveforms are obtained at output in each operating state by filtering $u_{\rm ab}$ with L_f, C_f.
4) The working time of the full-bridge inverter increases with increasing $U_{\rm os}$, and the operating time of the buck-boost converter decreases, as shown in Fig. 13(b)–(d).

The experimental waveforms are in accordance with the theoretical analysis.

The experimental waveforms under single input $U_{i1} = 148$ $\rm V_{dc}$ with the rated reactive load are shown in Fig. 14. The experimental results show that the proposed inverter can achieve bidirectional power flow under single-input source, and has high-quality waveform of $u_{\rm o}$.

The transient experimental waveforms with load abruptly changing from the rated resistive load to no load under single-input $U_{i1} = 96$ $\rm V_{dc}$ are shown in Fig. 15. The experimental results show that when the load abruptly changes, the system has fast dynamic response, and the response time is about 0.6 ms.

The dynamic experimental waveforms with single-input U_{i1} slowly changing between 96 to 192 V under rated resistive load are shown in Fig. 16. The results show that when U_{i1} changes with the maximum speed of 10 V/ms (restrained by the Chroma 62100H-600 Programmable dc source), the output $u_{\rm o}$ is unaffected, and the inverter achieves uniform distribution of duty ratio under the input voltage variation.

The transition experimental waveforms of the proposed off-grid system under the first input MPP (192 W, 96 V) and the second input $U_{i2} = 96$ V with the resistive load abruptly changing are shown in Fig. 17. In Fig. 17(a), first, the maximum output power of U_{i1} is $P_{i1\rm M} > P_{\rm o}$, U_{i1} supplies the light load alone. Once load increases to the rated, the first input source tracks to its MPP (96 V, 2 A, 192 W), and U_{i2} supplements the load. The system can smoothly change from State I to State II. Fig. 17(b) shows that the smooth transition can also be realized as load changing from the rated one to the light one.

The transition experimental waveforms under the rated resistive load, the first input MPP (576 W, 96 V) and the second $U_{i2} =$ 96 V with abrupt light intensity change are shown in Fig. 18. In Fig. 18(a), at first, $P_{i1\rm M} > P_{\rm o} = 0.5$ kW, and U_{i1} supplies the load alone. With the light intensity decrease, once the power supplied by U_{i1} is insufficient, U_{i2} starts supplying the load to help U_{i1} track its MPP, and the system can smoothly transits from State I to II. Fig. 18(b) shows that the transition can also be smooth as the light intensity increases from 400 to 1000 W/m^2.

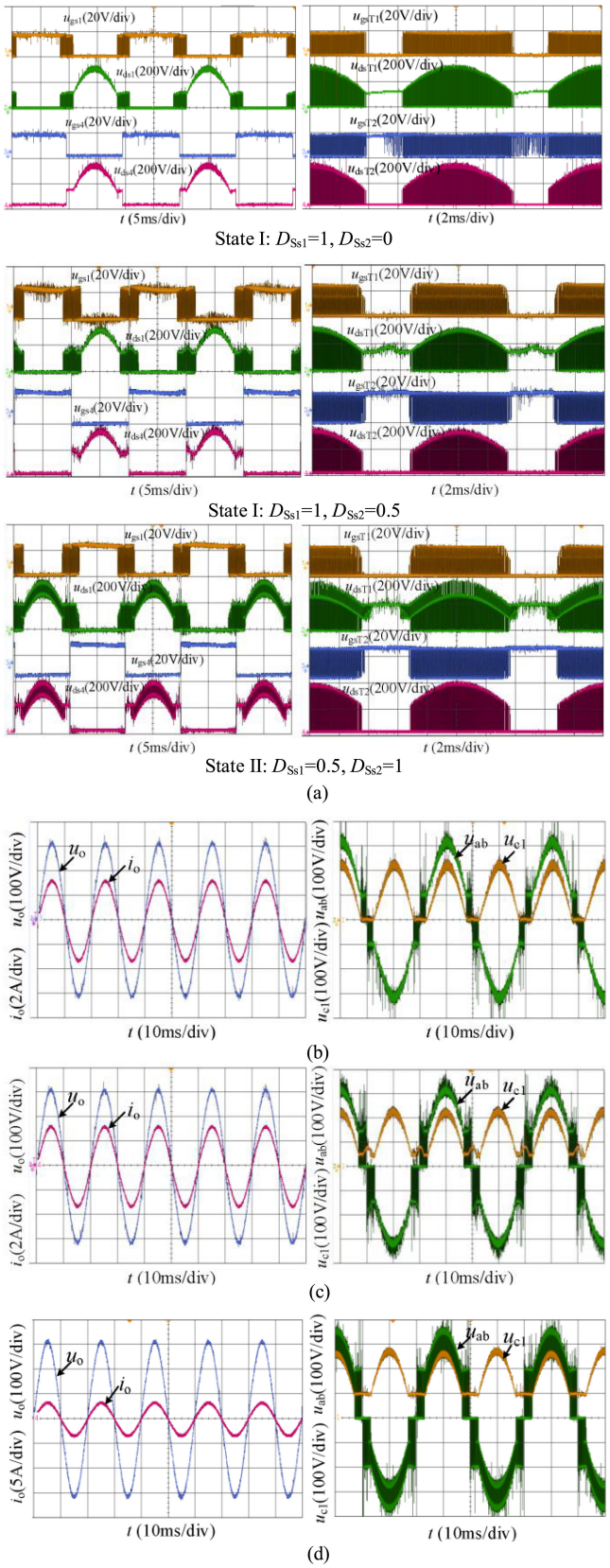

Fig. 13. Experimental waveforms of the proposed inverter with $U_{i1} = U_{i2} = 96$ V and output power of 500 W (rated load). (a) Driver voltage u_{gs1}, u_{gs4}, u_{gsT1}, u_{gsT2} and drain-source voltage u_{ds1}, u_{ds4}, u_{dsT1}, u_{dsT2} of the two states. (b) State I: $D_{Ss1} = 1$, $D_{Ss2} = 0$. (c) State I: $D_{Ss1} = 1$, $D_{Ss2} = 0.5$. (d) State II: $D_{Ss1} = 0.5$, $D_{Ss2} = 1$.

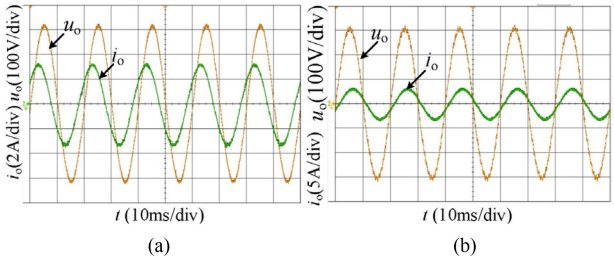

Fig. 14. Experimental waveforms of the proposed inverter under single input $U_{i1} = 148$ V_{dc} with reactive rated load. (a) Rated capacitive-resistive load cos $\phi = -0.75$. (b) Inductive-resistive load cos $\phi = 0.89$.

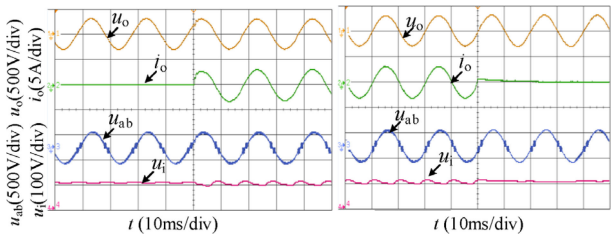

Fig. 15. Transient experimental waveforms with load abruptly changing from the rated resistive load to no load under single-input $U_{i1} = 96$ V_{dc}.

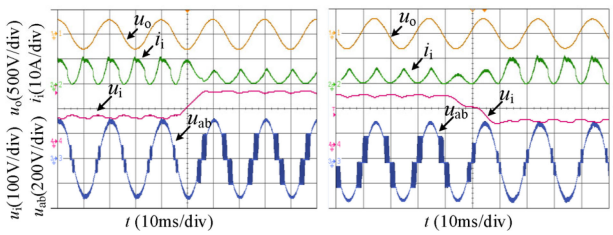

Fig. 16. Dynamic experimental waveforms with single-input U_{i1} slowly changing between 96 to 192 V under rated resistive load.

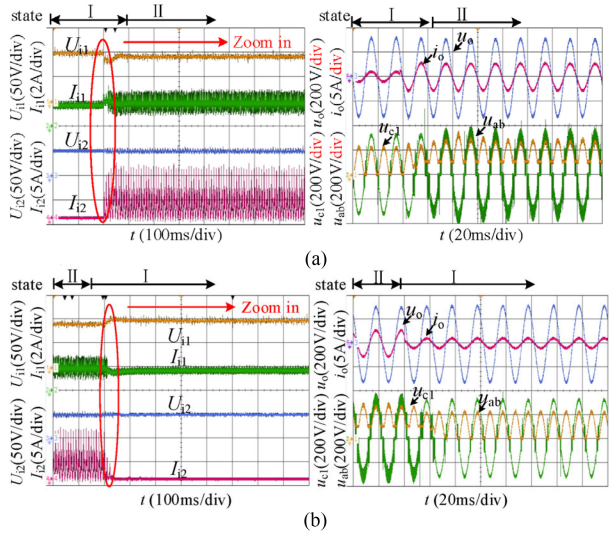

Fig. 17. Transition experimental waveforms of the proposed off-grid dual-input system with resistive load abruptly changing. (a) Load abruptly changes from the light load to the rated one. (b) Load abruptly changes from the rated load to the light one.

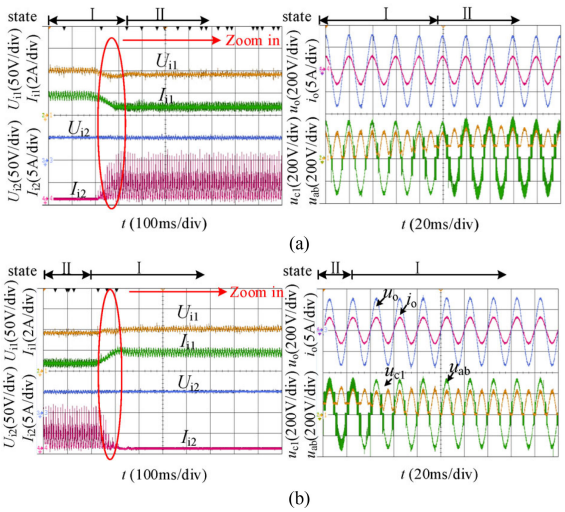

Fig. 18. Transition experimental waveforms among different operating states of the proposed off-grid system with abrupt light intensity change. (a) From 1000 to 400 W/m^2. (b) From 400 to 1000 W/m^2.

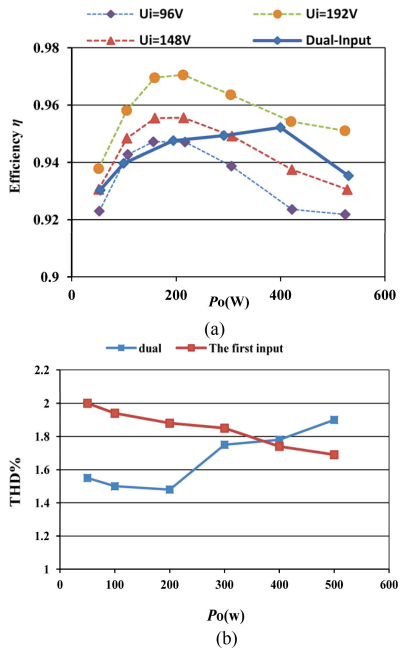

Fig. 19. Efficiency and THD measurement. (a) Measured efficiency. (b) Output voltage THD with resistive load.

The conversion efficiency and output voltage THD curves of the inverter prototype with different resistive load are measured and plotted in Fig. 19. In Fig. 19(a), the efficiency curves under different single-input voltage $U_i = 96$ V, 148 V, and 192 V and dual-input supply U_{i1} (192 W, 96 V)/U_{i2} (96V) are presented, respectively.

The following can be observed:

1) The conversion efficiency all increase first and then decrease with the load power increases, for the hard-switching loss of power switches at light load, and increasing conduction loss of devices under heavy load.

TABLE III
COMPARISON WITH OTHER INVERTERS

Configuration	Equivalent input voltage	Maximum efficiency	Type	Power allocation for the inputs ?
Proposed dual-input step-up inverter	U_i=192V	~97%	Buck-Boost	Yes
CTPS in [17]	U_i=190V	~95%	Buck-Boost	No
DP-AMI proposed in [17]	U_i=190V	~97%	Buck	No

2) With the input voltage increasing, the conversion efficiency increases, since the power loss of device caused by boosting input voltage of the buck–boost converter decreases.
3) The conversion efficiency under three different single-input voltage 96, 148, and 192 V with the rated load is 92.5%, 93%, and 95.5%, respectively, and the maximum efficiency is 94.5%, 95.7%, 97%, and respectively.
4) The maximum and full-load conversion efficiencies under dual inputs are 95.2% and 93.3%, respectively.

Fig. 19(b) shows the output voltage THD curves under the dual-input source U_{i1} (192 W, 96 V)/U_{i2} (96 V), it shows that: First, the output THD under the first input decreases with the load increasing, and THD under the dual inputs decreases first, and then increases, which is mainly because the effect of output filter is weakened in State II. Second, the minimum and full-load THD of u_o under dual-input supply is 1.48% and 1.9%, respectively, while under the first input is all 1.69%.

Combining the two working modes, the proposed inverter achieves uniform distribution of duty ratio under single/dual input with wide range varied input voltage. For S_{T1}, S_{T2}, and S_1–S_4, only a pair of switches operate in high frequency at a certain time as discussed in Section III-B, and therefore the inverter can achieve high average efficiency.

Compared with DP-AMI proposed in [17] and the conventional two-stage dc/ac power system (CTPS) under the same experimental conditions, the proposed inverter has better comprehensive performance, and comparison results are listed in Table III. The maximum conversion efficiency of CTPS (~95%) is lower than the proposed one (~97%). DP-AMI is just a buck-type inverter when powered by two input sources, and can also not realize power allocation between the two inputs. Its maximum efficiency is almost the same as the proposed under the same input voltage, but conversion efficiency under light load is relatively lower compared to the inverter in this article due to the inherent power loss caused by the front-end boost converter.

VI. CONCLUSION

A novel TMCSI with high efficiency was proposed and verified in this article. Based on low impedance of the intermediate capacitive link under high frequency, a new power flow path between the low-voltage input source and the ac output side is constructed. When the instantaneous value u_o is lower than input voltage U_i, the input source can supply the ac load directly. When $u_o > U_i$, the intermediate capacitive link boosts the input voltage, and supply the ac load with U_i directly. This solution

was realized by proposing a family of TMCSI. With the proposed TMCSI, the input power is processed without the front-end dc/dc setup converter, and the conversion stage is reduced, which is beneficial for the reducing current/voltage stress, switching losses, and size/volume of the conversion system.

The dual-input inverter based on TMCSI–BBC with a novel power allocation method is also studied to improve load capability. This power allocation method is controlled separately from the two-mode control strategy by adjusting $D_{S\mathrm{sn}}$ with line frequency, which can help to improve the dual-input system's reliability, since there is no overshoot issue anymore. The proposed dual-input setup inverter has two operating states, and each state consists of two working modes. The designed and developed 500 VA 96–192 V_{dc} input and 220-V 50-Hz ac inverter prototype has excellent comprehensive performance, and the experimental results are consistent with the theoretical analysis. The maximum achieved efficiency is 97% and the output voltage THD is lower than 2% over the entire power range.

REFERENCES

[1] X. Zhou, J. Xu, and S. Zhong, "Single-stage soft-switching low-distortion bipolar PWM modulation high-frequency-link DC–AC converter with clamping circuits," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7719–7729, Oct. 2018.

[2] E. Babaei, E. Asl Shokati, and M. Hasan Babayi, "Steady-state and small-signal analysis of high-voltage gain half-bridge switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3546–3553, Jun. 2016.

[3] Z Zhang, Z Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Analysis and design of a bidirectional isolated DC–DC converter for fuel cells and super capacitors hybrid system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 848–859, Feb. 2012.

[4] M. C Mira, Z. Zhang, A. Knott, and M. A. E. Andersen, "Analysis, design, modeling, and control of an interleaved-boost full-bridge three-port converter for hybrid renewable energy systems," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1138–1155, Feb. 2017.

[5] B. D. Reddy, M. P. Selvan, and S. Moorthi, "Design, operation, and control of S3 Inverter for single-phase microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5569–5577, Sep. 2015.

[6] G. Franceschini, E. Lorenzani, and G. Buticchi, "Saturation compensation strategy for grid connected converters based on line frequency transformers," *IEEE Trans. Energy Convers.*, vol. 27, no. 2, pp. 229–237, Jun. 2012.

[7] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[8] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A Review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[9] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC–DC converter photovoltaic systems: Power optimization issues," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 403–411, Feb. 2011.

[10] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[11] L. Diao, H. Du, Z. Shu, Y. Xue, M. Li, and S. M. Sharkh, "A comparative study between AI-HM and SPD-HM for railway auxiliary inverter with pulsating DC Link," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5816–5825, Jul. 2018.

[12] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback–forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012.

[13] J. Kan, S. Xie, Y. Wu, Y. Tang, Z. Yao, and R. Chen, "High-frequency-link inverter using combined synchronous rectifiers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6769–6777, Dec. 2014.

[14] D. Chen and S. Chen, "Combined bidirectional buck–boost DC-DC chopper-mode inverters with high-frequency link," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3961–3968, Aug. 2014.

[15] Z. Chen, Y. Chen, and B. Zhang, "An equivalent voltage source placement rule for impedance source network and performance assessment," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8382–8392, Oct. 2018.

[16] V. Jagan, J. Kotturu, and S. Das, "Enhanced-boost quasi-z-source inverters with two-switched impedance networks," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6885–6897, Sep. 2017.

[17] H. Wu, L. Zhu, F. Yang, T. Mu, and H. Ge, "Dual-DC-Port asymmetrical multilevel inverters with reduced conversion stages and enhanced conversion efficiency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2081–2091, Mar. 2017.

[18] A. Lashab, D. Sera, J. Martins, and J. M. Guerrero, "Multilevel DC-link converter-based photovoltaic system with integrated energy storage," in *Proc. 5th Int. Symp. Environ.-Friendly Energies Appl.*, Rome, Italy, 2018, pp. 1–6.

[19] A. Nazemi Babadi *et al.*, "Modified multilevel inverters with reduced structures based on PackedU-cell," *IEEE J. Emerg. Sel. Topics Power Electron.*., vol. 6, no. 2, pp. 874–887, Jun. 2018.

[20] A. Lashab *et al.*, "Cascaded multilevel PV inverter with improved harmonic performance during power imbalance between power cells," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2788–2798, May/Jun. 2020.

Xuefeng Chen (Member, IEEE) was born in Hubei Province, China, in 1994. He received the B.S. degree in electrical engineering and the M.S. degree in electrical engineering and power drives from Fuzhou University, Fuzhou, China, in 2015 and 2018, respectively.

He is currently working as an Application Engineer with MPS Integrated Circuit Application R&D Center, Hangzhou, China. His current research focuses on application of dc–dc and ac–dc converters.

Zhe Zhang (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2010.

He is currently an Associate Professor with the Department of Electrical Engineering, Technical University of Denmark (DTU), where he was an Assistant Professor from 2011 to 2014 Since January 2018, he has been the Head of Studies in charge of Electrical Engineering M.Sc. Programme at DTU. From 2005 to 2007, he was an Assistant Professor with Yanshan University. From June to August 2010, he was with the University of California, Irvine, CA, USA, as a Visiting Scholar. He has authored or coauthored more than 150 transactions and international conference papers and filed over ten patent applications. He has supervised over ten Ph.D. students since 2013. His current research interests include applications of wide bandgap devices, high frequency dc–dc converters, multiple-input dc–dc converters, soft-switching power converters, and multilevel dc–ac inverters, high-frequency magnetics for renewable energy systems, hybrid electric vehicles, and uninterruptable power supplies, piezoelectric-actuator and piezoelectric-transformer based power conversion systems.

Dr. Zhang has received several awards and honors including Best Paper Awards in IEEE ECCE, IFEEC, IGBSG, Best Teacher of the Semester, Chinese Government Award for Outstanding Students Abroad, etc. He is an Associate Editor in IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and IEEE Access, and the Guest Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS.