True Origin of Gate Ringing in Superjunction MOSFETs: Device View

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***Abstract*—As superjunction devices are scaled down to smaller dimensions, the gate ringing becomes more prominent in dynamic switching. The exact origin of superjunction MOSFET's gate ringing has not been so far identified as the conventional three-terminal measurement method cannot capture the dynamic behavior of the device, in particular the redistribution of charge between the different internal capacitive components in the superjunction structure. In this article, it is found that the gate ringing is highly related to the input capacitance. Specifically, by employing a TCAD model with a split gate method, the gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) current are investigated during the dynamic transitions. The gate ringing is highly dependent on sum of the input capacitances ($C_{GS} + C_{GD}$) for the turn-ON. In the case of the turn-OFF, however, the gate ringing is affected by the ratio of the input capacitances (C_{GD}/C_{GS}) and a lower C_{GS} is desirable for a low gate oscillation.**

***Index Terms*—Gate ringing, power MOSFET, superjunction.**

I. Introduction

THE gate ringing during the turn-OFF transition in power metal-oxide-semiconductor field-effect transistors (power MOSFETs), is an undesirable phenomenon leading to shoot-through in half-bridge systems [1]–[3]. The gate ringing mechanism during the turn-OFF is based on a resonant *RLC* feedback network. Based on a circuit analysis, several models accounting for the V_{DS} overshoot and the gate ringing have been developed [4]–[8].

However, the origin of the gate ringing is still unclear because the inticate flow of the current through different capacitive compnents within the devuce in dynamic conditions has not been investigated. Although the gate ringing could be significantly reduced by increasing the dynamic C_{GD}, the C_{GD} alone cannot explain the fundamental origin of the gate ringing.

According to a technical report [9], the ratio of the gate-to-source capacitance, C_{GS} to C_{GD} (C_{GS}/C_{GD}) should be as high as possible to minimize gate ringing. The approach of the technical report is logically correct in terms of the circuit analysis. However, a careful insight into the device physics of the power MOSFET and a thorough investigation into the intricate coupling between the device and the circuit bring us to a different conclusion. To start with, we note that the gate-to-channel capacitance, C_{CH}, in power MOSFETs has been disregarded, or assumed to be included in C_{GS} in most of the previous studies [3], [4], [10], [11]. By decoupling the gate-to-channel capacitance from the rest of C_{GS}, we can separately detect the displacement current into the MOS channel and assess its impact on the gate oscillations, as shown in Fig. 1. Note that the use of this TCAD method to decouple the transient currents in different regions does not infer that we propose the fabrication of a split-gate device. This method only allows us a detailed understanding of the phenomena involved in the gate-ringing by using different terminals in the TCAD setup.

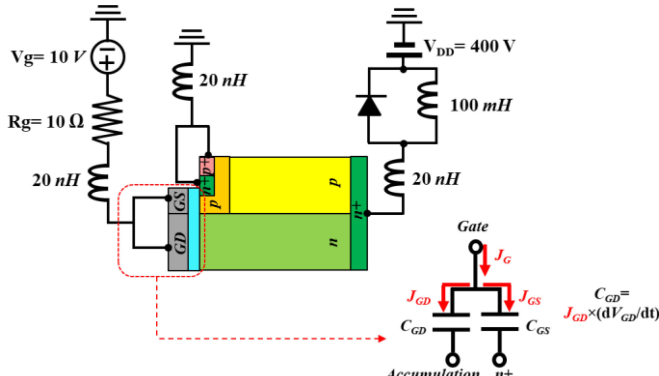

Fig. 1. Schematic illustration of the mix-mode inductive switching configuration. J_G, J_{GD}, and J_{GS} are the displacement current into gate, gate-to-drain terminal, and gate-to-source terminal, respectively.

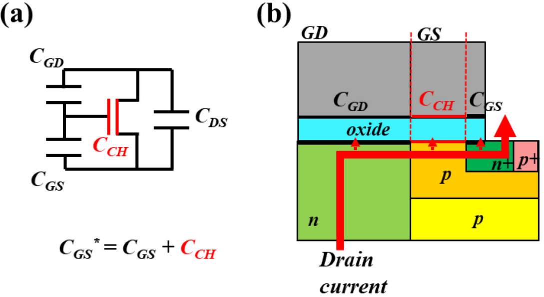

Fig. 2. Schematic illustration of gate-to-channel capacitance, C_{CH}, of a power MOSFET. C_{CH} is generally much higher than C_{GS}.

In advance, this report defines the $C_{GS}{}^{*}$ is equal to the sum of the C_{GS} and C_{CH}, as shown in Fig. 2

$$C_{GS}{}^{*} = C_{CH} + C_{GS} \tag{1}$$

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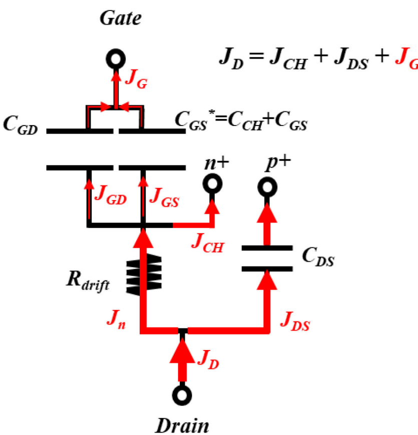


Fig. 3. Schematic illustration of the drain current, J_D, distribution in a superjunction MOSFET.

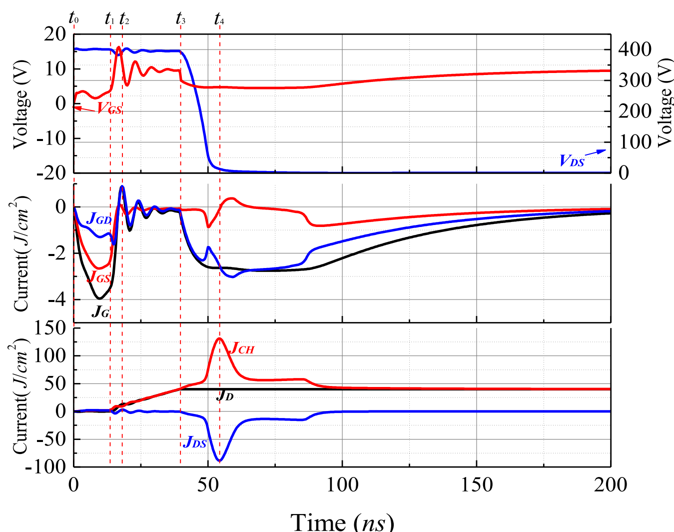


Fig. 4. Waveforms of inductive switching of the superjunction MOSFET during the turn-ON transition.

where C_{CH} is the gate to channel capacitance and C_{GS} is the gate to n+ overlap capacitance. It has been unclear whether the drain current charges the C_{GS} during the dynamic switching. According to the conventional circuit model given by Fig. 2(a), C_{GS} can be only charged by the displacement current crossing the C_{GD} [12]. However, considering the drain current path in a real device shown in Fig. 2(b), the drain current must pass through the channel, and the n$^+$ region and, therefore, some portion of the drain current must directly flow through C_{GD} and $C_{GS}{}^*$. For this reason, a circuit model for dynamic conditions in a power MOSFET can be drawn as shown in Fig. 3.

Where J_G, J_{GD}, and J_{GS} are gate, gate-to-drain, and gate-to-source current, respectively. J_{CH}, J_D, and J_{DS} are channel (n+ contact), drain, and drain-to-source (p+ contact) current, respectively. Using basic circuit analysis one can derive

$$J_D = J_{CH} + J_{DS} + J_{GD} + J_{GS} = J_{CH} + J_{DS} + J_G = J_S + J_G. \quad (2)$$

Simply, the drain current (J_D) is the sum of the gate current (J_G) and the source current (J_S). Equation (2) will be verified in the next section. The employed device is a superjunction (SJ) MOSFET because SJ MOSFETs have a smaller chip size than standard type (planar) MOSFETs, and therefore, they are prone to a significant gate ringing during the turn-OFF owing to the parasitic inductance. The goal of this study is to understand the real origin of the gate ringing in power MOSFETs and to verify the validity via detailed TCAD and mix-mode simulations.

II. Simulation Settings

A mixed-mode (device and circuit) simulation was employed for the inductive switching as shown in Fig. 1. The parasitic inductance of each terminal was 20 nH and the series gate resistance, R_g, was 10 Ω. The gap of the *GD* and the *GS* poly gates was 1 nm which does not affect the operation of the device. The parasitic inductance for each terminal of the device can be varied from at least 5 nH to around 50 nH depending on the package type and the circuit configuration. Therefore, 20 nH is not too large and not too small for seeing practical oscillation behavior. 10 *V* pulse was applied to the gate during the turn-ON and the gate was grounded during the turn-OFF.

The mobility model emolyed was doping dependent and high field saturation based on Masetti model [13], [14]. No hot carrier injection effects were considered. The half-cell pitch (*d*) of the device was 4.0 μm with the same pillar widths (n-pillar = p-pillar = 2.0 μm) and the length of the pillar was 40 μm. The doping concentration of the n-pillar and the p-pillar was the same: $N_D = N_A = 4.5 \times 10^{15}$ cm^{-3}. The thickness of the oxide was 0.1 μm.

The device's breakdown voltage is 730 V (650 V rating). The freewheeling diode was ideal without the reverse recovery current. The operating temperature was 300 K and the Joule heating (self-heating) was ignored. Nevertheless, we have checked that the gate ringing with/without Joule heating was virtually the same.

III. Turn-ON Analysis

Fig. 4 shows the waveforms of the superjunction MOSFET during the turn-ON transient period. It should be noted that during the turn-ON, the gate ringing occurs before the MOSFET enters the plateau period, and, during the turn-OFF, the ringing starts at the beginning of the Miller plateau.

$t_0 - t_1$*:* As soon as the gate voltage is applied at t_0, both of the C_{GD}, and the $C_{GS}{}^*$ start being charged by the inflow of the J_{GD}, and the J_{GS}. The inflow current rate dJ_G/dt causes a reverse gate potential, $L_G \times dJ_G/dt$, with a small oscillation (8 ns). When the channel of the MOSFET is activated (the inversion) with the threshold voltage, $V_{\rm th}$, at t_1, the drain current flows through the channel. Fig. 5 shows the schematic current flow during $t_0 \sim t_1$.

$t_1 - t_2$*:* When the MOS channel is turned-ON at t_1, the drain current, J_D, starts flowing into a channel current, J_{CH}, with a dJ_D/dt. The dJ_D/dt causes a temporary "potential shift" of the device. Specifically, the dJ_D/dt is multiplied by the parasitic source inductance ($L_S\times$ dJ_D/dt), and the parasitic drain inductance ($L_D\times$ dJ_D/dt), as shown in Fig. 6.

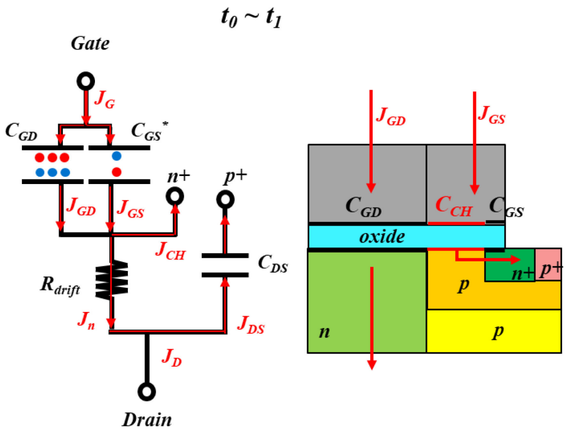
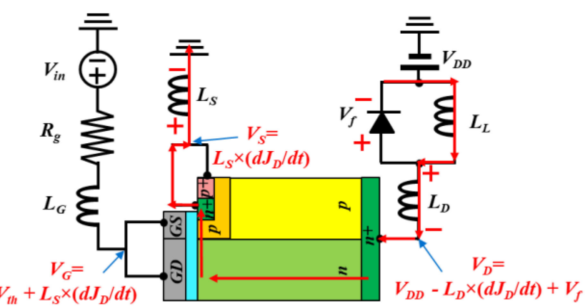


Fig. 5. Schematic illustration of the current flow during $t_0 - t_1$. Blue circle: hole, and red circle: electron.



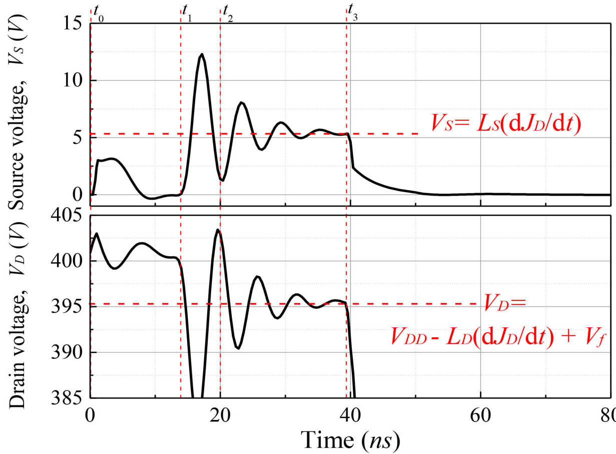


Fig. 6. "Potential shift" in the superjunction MOSFET when the channel current start flowing with dJ_D/dt during $t_1 \sim t_2$.

The potential shift of the drain and the source sides have been reported in several studies [15]–[17], but the gate terminal has not been examined in detail [11]. The potential on the source and drain terminal can be written as

$$V_S(t_1) = 0 \tag{3a}$$

$$V_S(t_2) = L_S \frac{dJ_D}{dt} \tag{3b}$$

$$V_D(t_1) = V_{DD} \tag{4a}$$

$$V_D(t_2) = V_{DD} - L_D \frac{dJ_D}{dt} + V_f. \tag{4b}$$

Owing to the increased source potential, the gate potential is suddenly shifted by the amount ($L_S \times dJ_D/dt$) without any gate charging current, as shown in Fig. 4. The gate potential can be written as

$$V_G(t_1) = V_{th} \tag{5a}$$

$$V_G(t_2) = V_{th} + V_S = V_{th} + L_S \frac{dJ_D}{dt}. \tag{5b}$$

The sudden shift of the gate potential lowers the inflow of gate current, J_G, sharply

$$J_G(t_1) = \frac{V_{in} - V_G}{R_g} = \frac{V_{in} - V_{th}}{R_g} \tag{6a}$$

$$J_G(t_2) = \frac{V_{in} - V_G}{R_g} = \frac{V_{in} - \left(V_{th} + L_S \frac{dJ_D}{dt}\right)}{R_g}. \tag{6b}$$

The change of gate current owing to the "potential shift" during $t_1 \sim t_2$

$$\frac{dJ_G}{dt} = \frac{J_G(t_2) - J_G(t_1)}{t_2 - t_1} = \frac{1}{t_2 - t_1} \frac{L_S}{R_g} \frac{dJ_D}{dt}. \tag{7}$$

It should be noted that relationships given by (3b), (4b), (5b), (6b), and (7) are the middle value of the oscillation. The rapid change of the gate current, dJ_G/dt, given by (7) finally produces a gate ringing by coupling with the parasitic gate inductance $L_G \times dJ_G/dt$ and the input capacitance, C_{iss} ($C_{GD} + C_{GS}^*$). Since the gate resistance, R_g, and the parasitic inductance, L_G, and the input capacitance C_{iss} are connected in series, the damping factor, ζ, can be calculated by a second-order differential equation [18]

$$\varsigma = \frac{R_g}{2} \sqrt{\frac{C_{iss}}{L_G}}. \tag{8}$$

The higher the damping factor is, the lower the gate ringing is. With given external components of the device, such as R_g and L_G, the only way for reducing the gate ringing is to increase the input capacitance.

$t_2 - t_3$: Since the drain current is increased with a constant rate, the "potential shift" lasts until the device supports the driving current. To sustain the increased drain current on the channel of the MOSFET, the gate should be charged continuously

$$V_G(t_2 \sim t_3) = V_{th} + \frac{J_D}{g_m} + V_S = V_{th} + \frac{J_D}{g_m} + L_S \frac{dJ_D}{dt} \tag{9}$$

$$J_G(t_2 \sim t_3) = \frac{V_{in} - V_G}{R_g} = \frac{V_{in} - \left(V_{th} + \frac{J_D}{g_m} + L_S \frac{dJ_D}{dt}\right)}{R_g} \tag{10}$$

where g_m is the transconductance of the MOSFET. Fig. 7 shows the schematic current flow in the device.

$t_3 - t_4$: As soon as the driving current is completely transferred into the device, the dJ_D/dt becomes zero and the "potential shift" is removed. The device enters the Miller plateau period to decrease the V_{DS}. As the V_{DS} decreases, the discharging current (J_{DS}) from the C_{DS} is directly transferred to the channel current (J_{CH}) causing a rapid increase in the channel current. The decrease in the V_{DS} continuously lowers the potential of

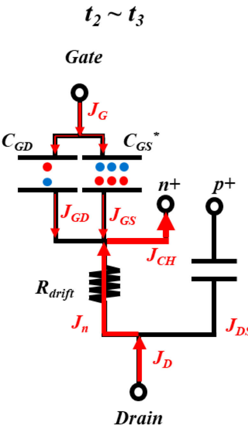


Fig. 7. Schematic illustration of the current flow during $t_2 - t_3$. Blue circle: hole. Red circle: electron.

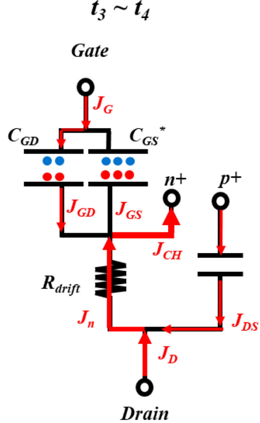


Fig. 8. Schematic illustration of the current flow during $t_3 - t_4$. Blue circle: hole. Red circle: electron.

the accumulation layer charging the C_{GD} ($J_G \approx J_{GD}$). Fig. 8 shows the schematic current flow.

After t_4: The C_{DS} is continuously discharged until the V_{DS} reaches the on-state voltage, and both the C_{GD} and the $C_{GS}{}^*$ are charged until the V_{GS} reaches V_{in}.

IV. Turn-off Analysis

Fig. 9 shows the typical waveforms of the turn-OFF transition of a superjunction MOSFET with the inductive switching circuit given by Fig. 1.

$t_0 - t_1$: This time is the transition period when both J_{GD} and J_{GS} are flowing out from the C_{GD} and the $C_{GS}{}^*$ (discharging of the gate). As suggested by (2), some amount of the drain current is flowing into the gate oxide, $J_D - J_{CH} - J_{DS} = J_G$. Fig. 10 shows the schematic current flow during $t_0 - t_1$. The blue and red circles are charged holes and electrons, respectively.

$t_1 - t_2$: During this period (Miller plateau), the drain current commutes from the channel (J_{CH}) into the C_{DS} charging current (J_{DS}) with increasing the V_{DS}. Most of the gate current is from the discharging of the C_{GD} because the increased V_{DS} raises the potential on the accumulation region continuously, i.e., the potential difference between the gate (or *GD* terminal) and the accumulation region becomes smaller. Since the C_{DS} is very

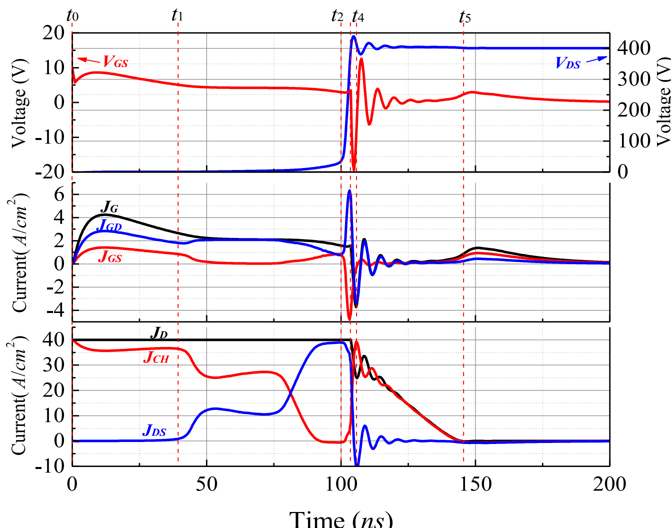


Fig. 9. Waveforms of inductive switching of the superjunction MOSFET during the turn-OFF transition.

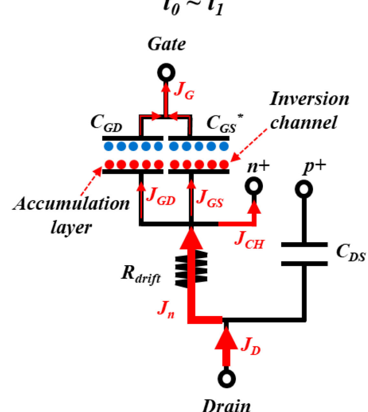


Fig. 10. Schematic current flow during $t_0 - t_1$. Blue circle: hole. Red circle: electron.

large in a superjunction MOSFET, most of the drain current is converted to the C_{DS} charging current [19]. At the same time, the channel current becomes zero and the channel of the MOSFET is depleted from inversion (temporary turn-OFF) with a slight decrease in V_{GS} below V_{th}. Fig. 11 shows the schematic current flow at t_2.

$t_2 - t_3$: As reported in previous studies, the superjunction C_{DS} decreases rapidly when the n-pillar and the p-pillar are fully depleted (pinch-off potential) [20], and, due to the small C_{DS}, the sharp increase in V_{DS} occurs until V_{DD} (400 V). The smaller C_{DS} does require less current to be charged, and, therefore, the drain current transfers to the channel current again. Meanwhile, the sharp increase in V_{DS} raises the potential on the accumulation region continuously causing a smaller potential drop across the C_{GD}, and a high current flow of the I_{GD}.

The displacement current across the C_{GD} (I_{GD}) during $t_2 - t_3$, mostly flows into the $C_{GS}{}^*$ rather than flowing out to the gate driver because the MOS channel should be turned-ON again (it was temporarily turned-OFF at t_2) to sustain the transferred channel current, J_{CH}, from, J_D. During the turn-ON

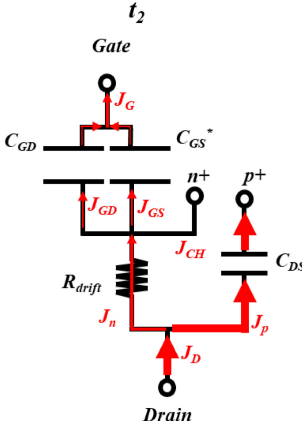


Fig. 11. Schematic illustration of the current flow at t_2.

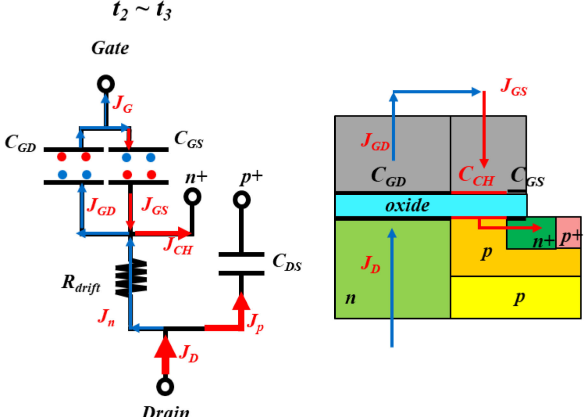


Fig. 12. Schematic illustration of the current flow during $t_2 - t_3$. Blue circle: hole. Red circle: electron.

transition, the gate current was directly converted into the J_{GD} while decreasing the V_{DS} rapidly. However, during the turn-OFF transition, the J_{GD} is not only flown out through the R_g, but also converted into J_{GS} to charge the $C_{GS}{}^*$.

In Fig. 9, there is a slight increase in J_{CH} while decreasing J_{DS} (100–103 ns). However, the increased channel current is not coming from the drain, but from the $C_{GS}{}^*$ charging electrons to form an inversion layer. Fig. 12 shows the schematic current flow during $t_2 - t_3$.

$t_3 - t_4$: After the V_{DS} reaches the V_{DD}, which is the moment when the C_{DS} charging is completed to sustain the V_{DD}, the J_{DS} is rapidly switched into the J_{CH} and the drain current starts decreasing. The current rate $-dJ_D/dt$ produces a "potential shift" as the way of the turn-ON case in the previous section. Specifically, the source voltage, V_S, formed by $-L_S \times dJ_D/dt$, and the gate potential is shifted by the amount of the source voltage without discharging of the gate as shown in Fig. 13.

$$V_S(t_3) = 0 \tag{11a}$$

$$V_S(t_4) = -L_S \frac{dJ_D}{dt} \tag{11b}$$

$$V_G(t_3) = V_{th} + \frac{J_D}{g_m} \tag{12a}$$

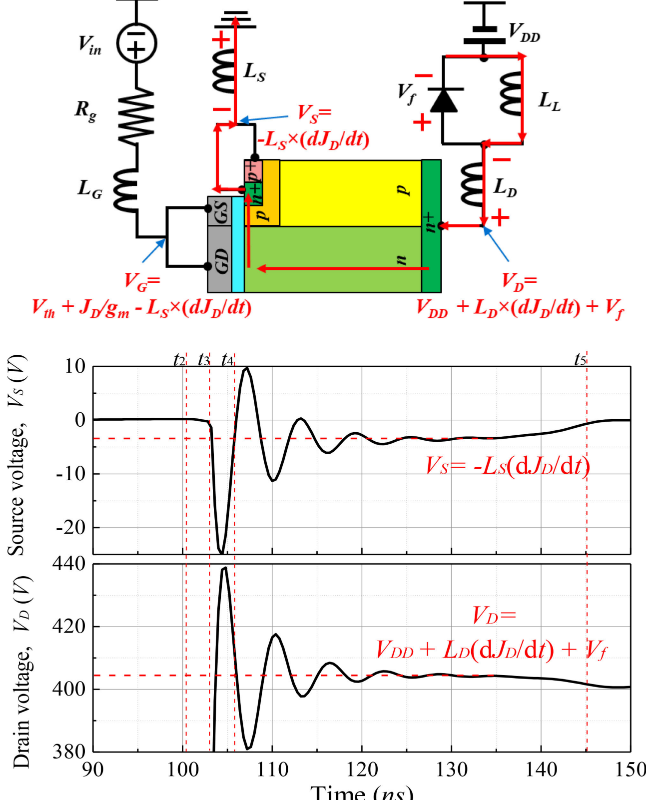


Fig. 13. "Potential shift" in the superjunction MOSFET when the channel current start flowing with dJ_D/dt during $t_3 - t_4$.

$$V_G(t_4) = V_{th} + \frac{J_D}{g_m} - V_S = V_{th} + \frac{J_D}{g_m} - L_S \frac{dJ_D}{dt}. \tag{12b}$$

The drain voltage is also shifted by the drain inductance

$$V_D(t_3) = V_{DD} \tag{13a}$$

$$V_D(t_4) = V_{DD} + L_D \frac{dJ_D}{dt} + V_f. \tag{13b}$$

It should be noted that the voltages given by (11)–(13) are the middle values of the oscillation. From the gate potential (V_G), the gate current (J_G) can be obtained as

$$J_G(t_3) = \frac{V_G(t_3)}{R_g} = \frac{V_{th} + \frac{J_D}{g_m}}{R_g} \tag{14a}$$

$$J_G(t_4) = \frac{V_G(t_4)}{R_g} = \frac{V_{th} + \frac{J_D}{g_m} - L_S \frac{dJ_D}{dt}}{R_g}. \tag{14b}$$

The rapid change of gate current owing to the "potential shift" during $t_3 \sim t_4$

$$\frac{dJ_G}{dt} = \frac{J_G(t_4) - J_G(t_3)}{t_4 - t_3} = -\frac{1}{t_4 - t_3} \frac{L_S}{R_g} \frac{dJ_D}{dt}. \tag{15}$$

The rapid change of the gate current, dJ_G/dt, given by (15) finally produces a gate ringing with the gate inductance $L_G \times dJ_G/dt$ by coupling with the input capacitance, C_{iss} ($C_{GD} + C_{GS}{}^*$).

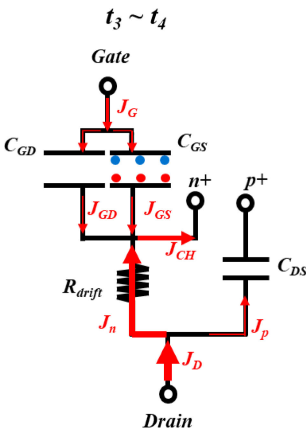


Fig. 14. Schematic illustration of the current flow during $t_3 - t_4$. Blue circle: hole. Red circle: electron.

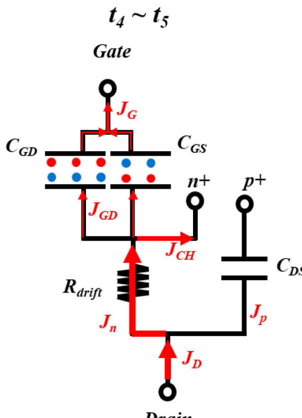


Fig. 15. Schematic illustration of the current flow during $t_4 - t_5$. Blue circle: hole. Red circle: electron.

However, during the turn-OFF transition of a superjunction MOSFET, there is one more mechanism in addition to the "potential shift." As already mentioned, the slight increase in the channel current during $t_2 - t_3$ is from the $C_{GS}{}^*$ charging to form an inversion (turn-ON the channel again, the channel was turned OFF at t_2), and the J_{GS} was directly supplied by the J_{GD} with the rapid increase in the V_{DS}. However, after the J_{GD} reaches the peak value at t_3, the J_{GD} starts decreasing because the C_{GD} is now supporting the V_{DD}. If the ratio, $C_{GD}/C_{GS}{}^*$, is large, the C_{GD} would be able to supply enough current to $C_{GS}{}^*$ to drive the current (40 A/cm^2). However, if the ratio, $C_{GD}/C_{GS}{}^*$, is small, the C_{GD} cannot supply enough current to $C_{GS}{}^*$ to drive the channel current. Therefore, the gate driver should supply additional current to $C_{GS}{}^*$. The sudden inflow through the gate, the gate inductance (L_G) produces the gate oscillation. Fig. 14 shows the schematic current flow during $t_3 \sim t_4$.

A conclusion that can be drawn is that the gate ringing is highly affected by the ratio of the input capacitances. A higher $C_{GD}/C_{GS}{}^*$ is desirable since the larger C_{GD} would be able to supply more current to charge the $C_{GS}*$, and the smaller $C_{GS}{}^*$ requires less external (gate drive) current to be turned on again to sustain the channel current. The validity of this mechanism will be proved in the next sessions with several case studies.

$t_4 - t_5$: The "potential shift" caused by the dJ_D/dt lasts until the drain current is fully transferred to the diode. Since the channel current is decreasing continuously, the input capacitance keeps discharging. When the drain current reaches zero at t_5, the current shift is removed, and the gate voltage is recovered to V_{th}. Fig. 15 shows the schematic current flow during this period.

After t_5: As soon as the "potential shift" is removed when the drain current drops zero at t_5, both the C_{GD} and the $C_{GS}{}^*$ discharge continuously, and the device is finally turned OFF.

V. Case 1: C^*_{GS} Control

In this section, the suggested mechanism of the gate ringing in a superjunction MOSFET will be verified with several case studies. The first case is the different channel length (L_{CH}) to see the effect of the $C_{GS}{}^*$. As shown in Fig. 16, while fixing other parameters, only the channel length is varied.

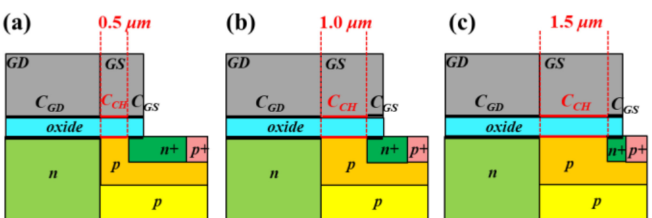


Fig. 16. Schematic illustrations of the channel length control. Other geometries are fixed except for the channel length.

Fig. 17 shows the turn-ON waveforms of the various channel lengths when the gate starts oscillating. As expected above, the shortest channel length condition, $L_{CH} = 0.5$ μm, shows the smallest gate ringing. Specifically, as explained in a previous section, the gate ringing is caused by the "potential shift" of the gate, and the rapid gate current change (J_G) which triggers the series $R_g L_G C_{iss}$ feedback loop on the gate. Therefore, a higher C_{iss} is desirable for less gate ringing given by (8).

Fig. 18 shows the turn-OFF waveforms with different channel lengths around when the gate starts ringing. Unlike the turn-ON case, the shortest channel length presents the lowest gate ringing. Specifically, as explained in the previous section, the origin of the gate oscillation during the turn-OFF is from the "potential shift" and the channel driving (the C^*_{GS} charging) by the C_{GD}. A larger channel length has a larger C^*_{GS}, and more C^*_{GS} charging current is required to support the same driving current. At the same C_{GD} condition, a larger C^*_{GS} should drag more external gate current from the gate driver, and the inflow rate of the external JG triggers the RgLGCiss oscillation loop. Therefore, a smaller channel length (a smaller C^*_{GS}) is desirable for a less gate ringing.

VI. Case 2: C_{GD} Control

The second case is to control the C_{GD} capacitance by changing the width of the n-pillar of the superjunction, as shown in Fig. 19. The channel length is fixed to secure the same $C_{GS}{}^*$. The doping concentrations for the asymmetrical pillar structures are calculated in order not to change the device specific on-state resistance (8 mΩcm^2). For example, for $\beta = 0.7$, since the n-pillar's width was increased by 0.7/0.5, the n-pillar's doping

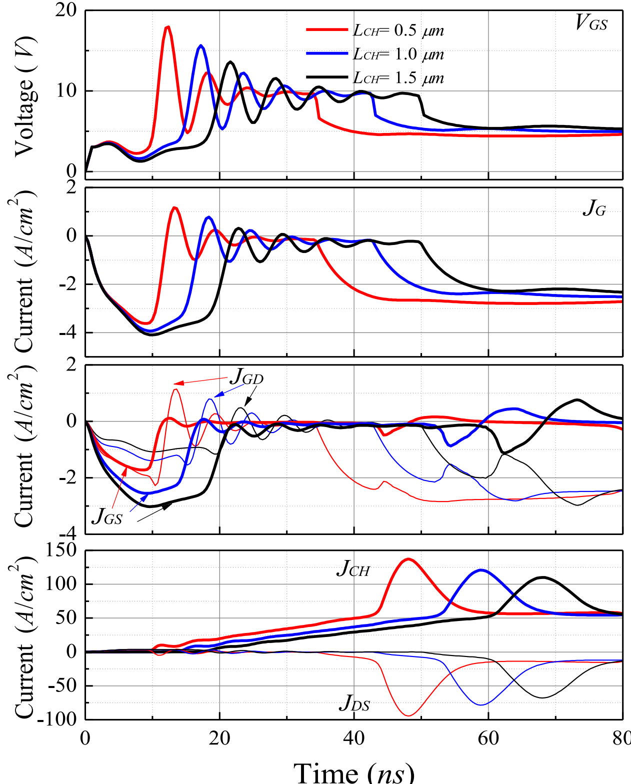


Fig. 17. Turn-ON gate ringing waveforms for the different channel lengths. Red lines: $L_{CH} = 0.5$ μm. Blue lines: $L_{CH} = 1.0$ μm. Black lines: $L_{CH} = 1.5$ μm.

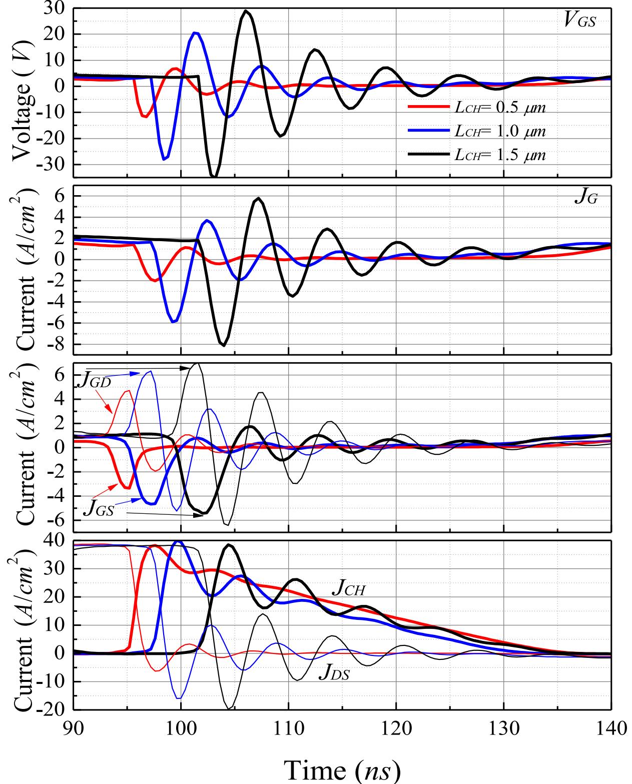


Fig. 18. Turn-OFF gate ringing waveforms for the different channel lengths. Red lines: $L_{CH} = 0.5$ μm. Blue lines: $L_{CH} = 1.0$ μm. Black lines: $L_{CH} = 1.5$ μm.

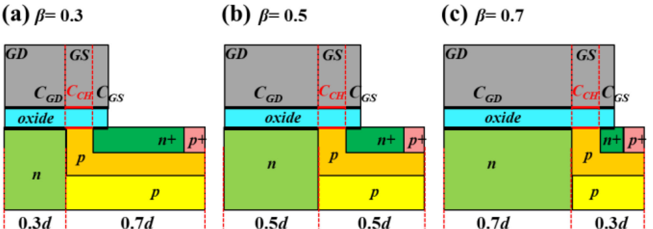


Fig. 19. Schematic illustrations of the C_{GD} control. Other geometries are fixed for the same $C_{GS}{}^*$. β is the n-pillar width ratio to the p-pillar. (a) $\beta = 0.3$, $N_D \times 0.3d = N_A \times 0.7d = 9.0 \times 10^{11}$ cm^{-2}. (b) $\beta = 0.5$, $N_D \times 0.5d = N_A \times 0.5d = 9.0 \times 10^{11}$ cm^{-2}. (c) $\beta = 0.7$, $N_D \times 0.7d = N_A \times 0.3d = 9.0 \times 10^{11}$ cm^{-2}.

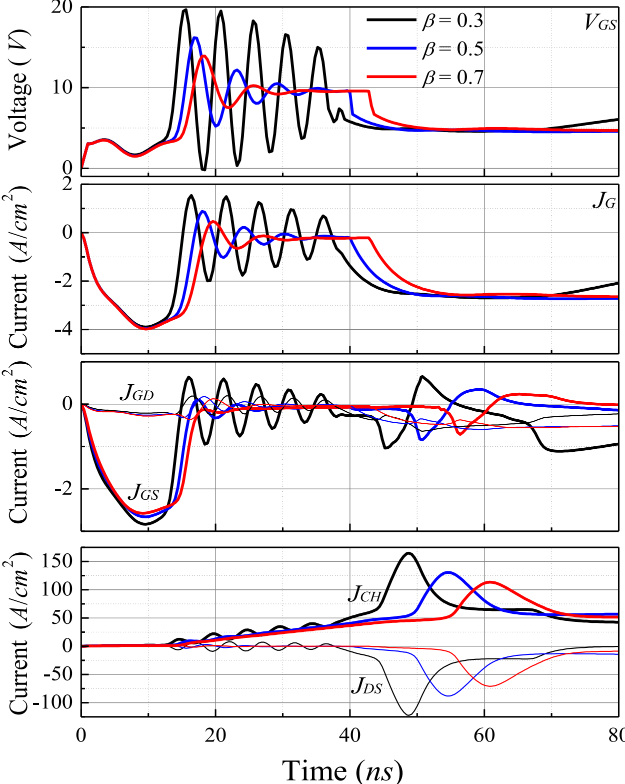


Fig. 20. Turn-ON gate ringing waveforms for the different n-pillar width ratio to the p-pillar (β). Red lines: $\beta = 0.7$. Blue lines: $\beta = 0.5$. Black lines: $\beta = 0.3$.

concentration was decreased by 0.5/0.7, $N_D(\beta = 0.7) = (0.5/0.7) \times 4.5\times10^{15}$ cm^{-3} $= 3.21\times10^{15}$ cm^{-3}. In other words, this approach will not change the sheet charge density (as well as the specific resistance) in the pillars as shown in the caption in Fig. 19 [21], [22].

Fig. 20 shows the turn-ON waveforms of the superjunction MOSFETs with different β.

As suggested in turn-ON analysis, the gate ringing during the turn-ON transition is dominated by the series $R_g L_G C_{iss}$ under the "potential shift." The higher β increases the C_{GD}, and C_{iss} as shown in Fig. 19. The higher C_{iss} finally presents a lower gate ringing with a slower gate voltage change.

Fig. 21 shows the turn-OFF waveforms for different β. In the case of the turn-OFF, a higher C_{GD} with a lower $C_{GS}{}^*$ is desirable for a lower gate ringing. $\beta = 0.7$ has the highest C_{GD},

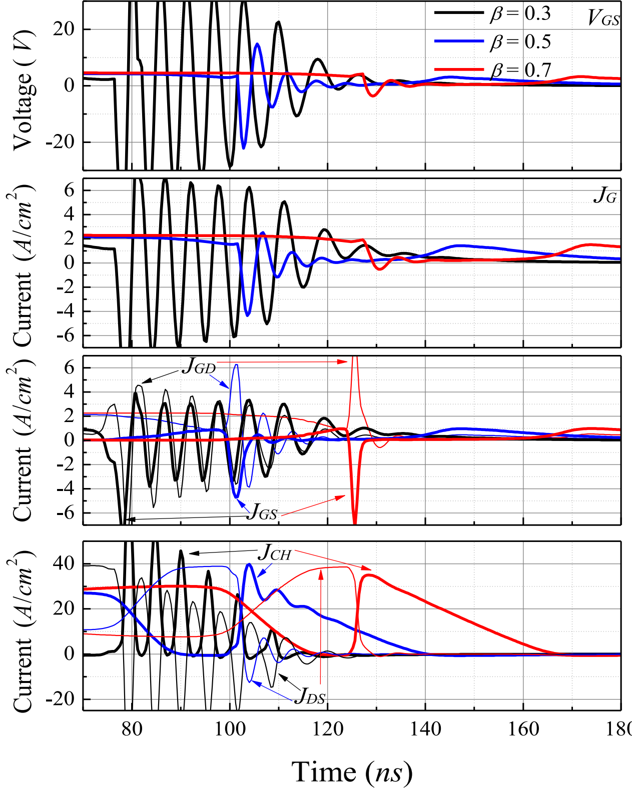


Fig. 21. Turn-OFF gate ringing waveforms for the different n-pillar width ratio to the p-pillar (β). Red lines: $\beta = 0.7$. Blue lines: $\beta = 0.5$. Black lines: $\beta = 0.3$.

and the gate ringing is the lowest securing the stable operation. More specifically, as the β increases from 0.3 to 0.7, the peak J_{GD}, which is directly converted to $C_{GS}{}^{*}$ charging current (J_{GS}), increases facilitating an easier turn-ON of the channel only by the J_{GD}. In other words, the $C_{GS}{}^{*}$ of $\beta = 0.3$ should be charged by the external current (gate driver) owing to the small C_{GD}, and the more inflow of the gate current from the external source accompanies a higher J_G/dt presenting a higher gate oscillation.

However, an asymmetrical pillar geometry may not be feasible for silicon devices. Due to the high diffusivity of the impurities in silicon, it is very challenging to change the n-pillar width to the p-pillar width ratio. In spite of the lack of practical feasibility, this example study provides a definite evidence that the gate ringing is highly dependent on the input capacitance ratio.

VII. Case 3: V_{th} Control

Fig. 22 shows the gate ringing waveforms for different threshold voltages ($V_{\rm th} = 3.5$, 4.0, and 4.5 V). During the turn-ON, since the potential shift of the gate occurs after the turn-ON of the channel ($V_{\rm th}$), a larger $V_{\rm th}$ condition suffers a smaller potential shift leading to a slightly smaller gate ringing. In the case of the turn-OFF shown in Fig. 23, the channel return-ON for a high $V_{\rm th}$ device requires very high gate-to-source current. Therefore, significant external gate current is supplied to the gate-to-source capacitance causing a large potential shift and the gate ringing.

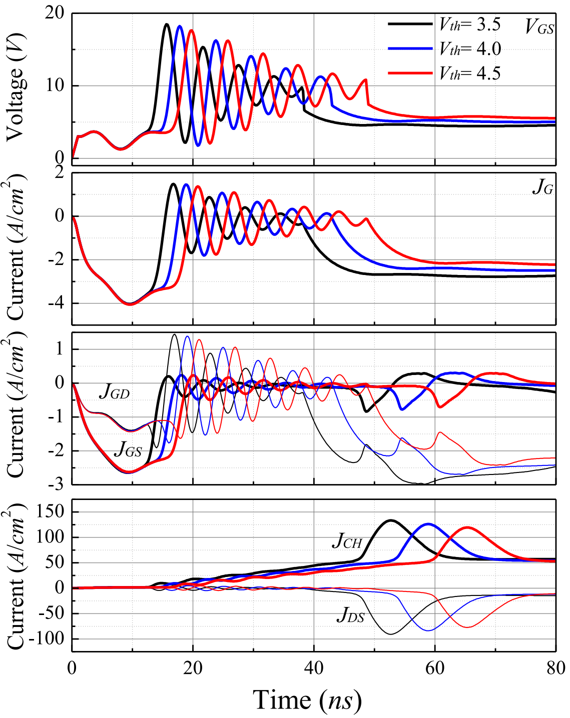


Fig. 22. Turn-ON gate ringing waveforms for $V_{\rm th} = 3.5$, 4.0, and 4.5.

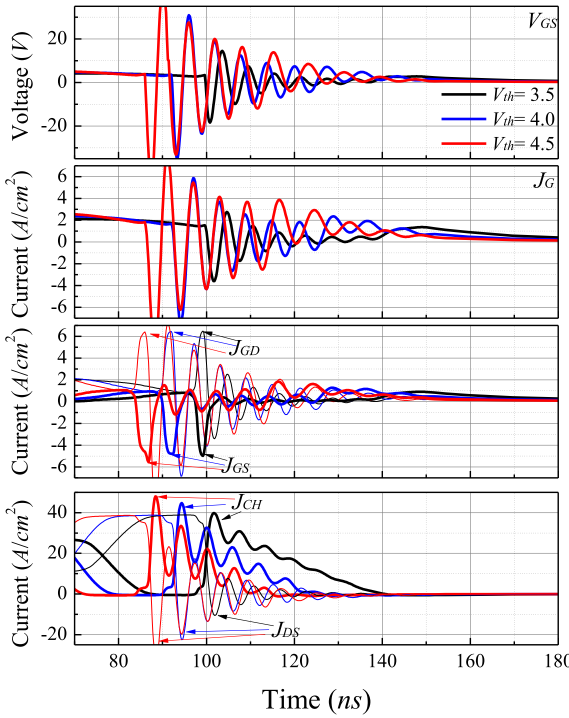


Fig. 23. Turn-OFF gate ringing waveforms for $V_{\rm th} = 3.5$, 4.0, and 4.5.

VIII. Conclusion

The fundamental origin of the gate ringing in a superjunction MOSFET has been investigated. By employing a split gate method, the gate-to-source and gate-to-drain current were extracted from a specifically-bulit TCAD model, respectively. It was proved that a component of the drain current is consumed for charging C_{GS}

and C_{CH}. In the case of the turn-ON, the gate ringing occurs when the gate voltage suffers a rapid "potential shift" owing to the source inductance multiplied by the J_D/dt. During the turn-OFF, the superjunction MOSFET channel was turned OFF when V_{DS} was rising because most of the drain current was consumed to charge the large C_{DS} (channel current is zero). Subsequently, after C_{DS} was charged enough, the drain current continued to flow through the MOS channel again. To return-ON the MOS channel, the I_{GS} was directly supplied by I_{GD} and the flow rate of I_{GD} determined the dV/dt. If the C_{GS*} was large (for example, a long channel length), the I_{GD} current would not be sufficient to return-ON the MOS channel and additional I_{GS} current is neded from the gate driver. The rapid change in the gate current finally triggered resonant oscillations sustained by the parasitic inductance in the gate.

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