Self-Aging-Prognostic GaN-Based Switching Power Converter Using T_J-Independent Online Condition Monitoring and Proactive Temperature Frequency Scaling

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***Abstract*—To mitigate unique aging and failure challenges encountered in GaN technology, this article develops the techniques that reinforce the reliability of GaN power circuits. In particular, an online condition monitoring scheme is developed to prognose the current collapse induced aging and failures in GaN power switches, using the devices' dynamic ON-resistance r_{DS_ON}, as the real-time precursor. As r_{DS_ON} is temperature-dependent in general, a gate-leakage based junction temperature T_J sensor is developed to assist in removing temperature effect from r_{DS_ON} reading, achieving T_J-independent condition monitoring. To improve the device longevity, a proactive temperature frequency scaling scheme is implemented to balance the power circuit performance and reliability. To validate the design concepts, a power converter IC prototype was designed and fabricated using an 180 nm high-voltage CMOS process. With all e-mode GaN power switches, it operates at 10 MHz switching frequency with a flexible input supply voltage ranging from 5 to 40 V and delivers a maximum power of 6 W. Experimental results demonstrate that the T_J-independent online condition monitoring reduces the false monitoring rate by 19 times over a temperature range from 0 to 125 °C. Meanwhile, the temperature frequency scaling engine reduces the T_J of the GaN switches by up to 16 °C, while striving for an optimal operation between performance and thermal stress.**

***Index Terms*—Current collapse, dynamic ON-resistance, GaN failure self-prognosis, online condition monitoring, proactive temperature frequency scaling.**

I. Introduction

OVER the past decades, silicon power transistor technology has advanced steadily, but gradually approaches its theoretical performance limits recently. As a promising alternative, gallium nitride (GaN) high-electron-mobility transistor (HEMT) technology demonstrates superior figure of merits [1], pushing switching power circuits to the high switching frequency regime above 10 MHz for higher power density and fast dynamic transient performance [2], [3]. However, before accomplishing large scale of commercialization and mass production, it still faces formidable reliability challenges [4]. In a typical power circuit, power devices handle vast majority of current and voltage stresses and face most significant electrical and thermomechanical failure risks. It is reported that the power devices account for 34% of power system failures in general power products [5]. Another study focusing on switching power converters reveals an even higher failure rate of 57.1% [6]. As for GaN power switch, as a new emerging power device, its aging and failure mechanisms are not as well-studied as the silicon counterparts. In the meantime, its unique structure and operation induce new aging and failure problems.

Use a classic half-bridge switching power converter as an example. As illustrated in Fig. 1, the high-side GaN switch M_H switch handles large switching current and high input voltage stress in charge phase. After repetitive switching actions, some electrons in the channel can be injected into the AlGaN barrier and the buffer layers, leading to the well-known *hot electron injection* effect. In discharge phase, M_H is OFF. The low-side switch M_L turns ON and ties the source of M_H to ground, creating high drain–source voltage (V_{DS}) stress on M_H. This induces charge traps in the insulator and the buffer layers, causing the so-called *charge trapping*. As a joint effect of both mechanisms, the trapped or/and injected electrons, in the insulator, the AlGaN barrier and the buffer layers, repel free electrons in the channel when M_H is ON, weakening the electron density at the heterojunction interface between the GaN region and the AlGaN barrier layer, which is referred as the two-dimensional electron gas layer (2DEG). This effect, known as current collapse or *i*-collapse in short, degrades the channel conductivity, increases the dynamic ON-resistance r_{DS_ON}, and is a major cause of GaN switch aging [4]. As the *i*-collapse induced aging develops, a GaN switch could fail eventually, incurring potential destructive breakdowns [7]–[9].

To avoid such catastrophic failures, power device condition monitoring is paramount. A straightforward approach of implementing such on IGBTs was reported in [10], in which collector–emitter voltage V_{CE} was chosen as the aging precursor. However, the condition monitoring can only be accomplished offline, inconveniently requiring frequent interruptions on operation. This could also be rather inaccurate and impractical since the

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Fig. 1. Device- and circuit-level *i*-collapse mechanism in a GaN power switch.

operation conditions of a power circuit between offline and online can differ significantly, leading to high false monitoring rate (FMR) [4]. Hence, online condition monitoring is highly preferable. In [11], an *in situ* condition monitoring was discussed by means of observing pole variations in the loop gain. However, the implementation of the pole location precursor is highly sophisticated, which is also noise-sensitive, and load- and line-dependent.

Another technical challenge for online condition monitoring lies in the fact that most aging precursors are sensitive to temperature. When the junction temperature T_J of a power switch varies, the aging assessment would be affected. As T_J is directly linked to the ambient temperature T_A and output current I_O (due to self-heating effect), T_J fluctuates frequently with T_A and I_O. As depicted in Fig. 2, when T_J rises from T_{J1} to T_{J2} due to T_A or I_O increase, the aging precursor (e.g., r_{DS_ON}) shifts to a higher level abruptly. This may cause r_{DS_ON} to surpass the specified aging threshold and thus trigger an aging event falsely even if the power switch works normally. In contrast, as T_J drops from T_{J2} to T_{J3} due to a decrease of T_A or I_O, r_{DS_ON} drops accordingly. In this case, r_{DS_ON} stays below the aging threshold even if the condition of the power switch has drifted away from the healthy state. Such an overlooked aging condition monitoring event would cause the power switch to further deteriorate. Hence, in

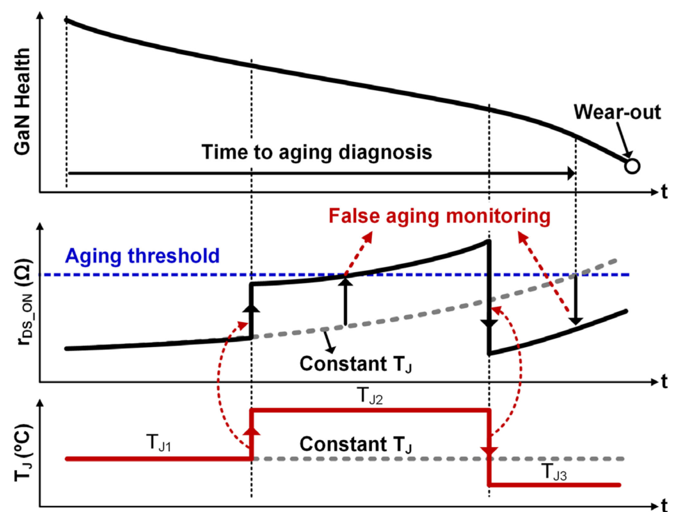


Fig. 2. False aging monitoring caused by temperature fluctuations.

order to assess the power switch's condition accurately, T_J effect on aging precursor must be removed, which makes the real-time T_J sensing essential. However, conventional temperature sensing circuits such as PTAT are not applicable in this scenario, because most GaN switches are not monolithically integrated

with silicon die, where the controller and other sensing blocks are built. Hence, the chip temperature fundamentally differs from the T_J of a GaN switch. To overcome it, the ON-resistance of power MOSFET is detected in [11] to determine the device's T_J. The main issue of this method is the aging dependence of ON-resistance, which degrades the sensing accuracy. Hence, a new T_J sensing approach is in urgent demand for GaN switch, which should be independent of aging and compatible with circuit integration.

In addition, another GaN power transistor reliability issue is the thermal effect. As illustrated in Fig. 1, to reduce the manufacture cost and improve the technology compatibility, it is common to fabricate GaN HEMTs on silicon substrate. Accordingly, in order to reduce the lattice mismatch, an AlGaN buffer layer is often inserted [12]. However, this increases the junction-to-ambient thermal resistance $R_{\theta JA}$ [13], [14]. Moreover, a GaN HEMT usually has much smaller die size over its silicon counterpart. This practically increases $R_{\theta JA}$ further. Consequently, combined with the r_{DS_ON} increase caused by the *i*-collapse effect, increased total resistance leads to higher power and heat generation, elevating T_J. According to Arrhenius' law, as T_J increases, the mean time to failure is shortened exponentially [15]. For even worse, the elevated T_J deteriorates the *i*-collapse effect with even higher r_{DS_ON}, significantly reducing the device lifetime. To alleviate such thermal-aging effect and extend a GaN HEMT's lifetime, thermal management becomes vital in GaN power circuits. The design in [16] used an electrothermal model to monitor and adjust the power distribution among parallel-connected power converters. However, this method requires a system to equip a highly powerful computing ability and is merely valid for multiphase converters. In [14], a smart gate driver was proposed to control power loss generation. However, it highly relies on power device parameters, which are sensitive to process, voltage, and temperature variations. An active thermal control was reported in [17] to adapt the switching frequency of a power converter to T_J. However, the T_J in this case is indirectly determined through power loss estimation, thus limiting the accuracy of the control.

To address the aforementioned challenges, this article presents three joint research efforts. First, a dynamic ON-resistance r_{DS_ON}-based online condition monitor is designed to prognose the *i*-collapse caused failure in GaN HEMTs. Second, to effectively eliminate the temperature effect on r_{DS_ON}, a gate leakage I_{GSS}-based, aging-independent, cross-die T_J sensor is integrated on-chip, which effectively reduces the FMR. Third, a proactive temperature frequency scaling scheme is developed to slow down the aging process in GaN HEMT without significant compromise on the power circuits performance. All the aforementioned techniques and circuits are built in a GaN-based half-bridge converter for demonstration. The remainder of this article is organized as follows. In Section II, we focus on our first design effort to introduce the r_{DS_ON}-based online condition monitoring. Section III elaborates the sensing scheme and circuit design of the I_{GSS}-based T_J sensing. Section IV details the temperature frequency scaling scheme and the proposed GaN power system, followed by the experimental results in Section V. Finally, this article is concluded in Section VI.

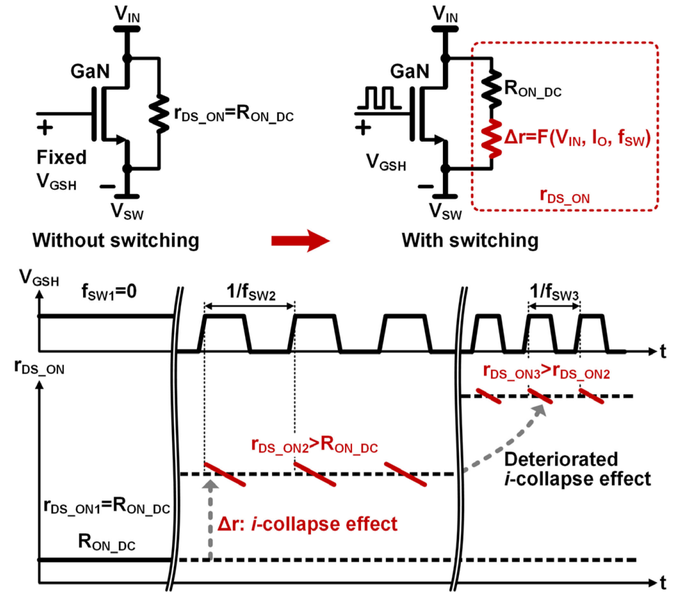


Fig. 3. Illustration of switching condition dependence of the dynamic on-resistance in a GaN HEMT.

II. Online Condition Monitoring Precursor: Dynamic ON-Resistance

A. Switching Condition Dependence of r_{DS_ON} Aging Precursor

In order to create a credible condition monitoring scheme, the first step is to define an appropriate aging precursor, which should change monolithically over the device degradation and signify gradual aging course rather than abrupt failure. Based on these considerations, the dynamic ON-resistance r_{DS_ON} is identified as the precursor to characterize the *i*-collapse caused aging. To implement such, r_{DS_ON} must be measured correctly with special consideration on the unique mechanisms of *i*-collapse effect. As shown in Fig. 3, when a GaN HEMT is constantly conductive ($f_{\mathrm{SW1}} = 0$), it faces no dynamic voltage or current stress. Thus, it is free from the *i*-collapse effect. In this case, its dynamic ON-resistance r_{DS_ON1} is equal to the static value $R_{\mathrm{ON_DC}}$. Once it switches between ON and OFF states at a switching frequency f_{SW2}, it faces repetitive voltage and current stresses and suffers from the *i*-collapse effect. Accordingly, r_{DS_ON} rises, making it larger than the $R_{\mathrm{ON_DC}}$ ($r_{DS_\mathrm{ON2}} > R_{\mathrm{ON_DC}}$). The elevation magnitude Δr is highly influenced by the input power source voltage V_{IN} and the load current I_O. Apparently, higher V_{IN} and larger I_O result in larger Δr due to more severe electrical stresses. In addition, recent device studies [18]–[21] also confirm the impact by the level of a switching frequency on r_{DS_ON}. As depicted in Fig. 3, when a switching frequency rises from f_{SW2} to f_{SW3}, the number of switching transitions increases within a fixed time interval. Consequently, the accumulation effect of the electrical stresses on a GaN power switch becomes more significant, intensifying the *i*-collapse effect and thus resulting in an even higher r_{DS_ON3}. In conclusion, because the dynamic ON-resistance r_{DS_ON} is highly influenced by instantaneous power and switching conditions such as V_{IN}, I_O, and f_{SW}, online

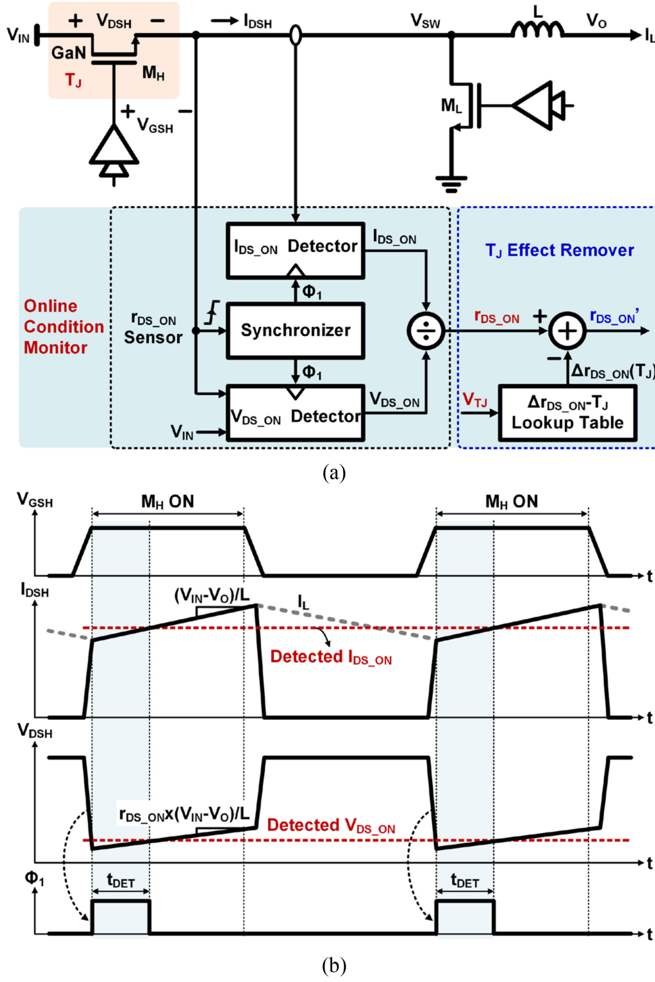


Fig. 4. (a) Circuit block diagram and (b) timing diagram of the r_{DS_ON}-based online condition monitor.

real-time measurement on r_{DS_ON} is essential to accurately evaluate the GaN switch's aging status.

B. Proposed Online r_{DS_ON} Condition Monitor

Fig. 4(a) depicts the block diagram of the proposed online r_{DS_ON} condition monitor. To sense the precursor r_{DS_ON} online, both V_{DS_ON} and I_{DS_ON} are measured on the high switch M_H simultaneously, during its ON states. As in Fig. 4(b), in the ON states, M_H is conductive to short V_{IN} to the switching node V_{SW}, energizing the inductor L. As a result, the high-side current I_{DSH}, which matches the inductor current I_L in this period, ramps up with a rate of $(V_{\mathrm{IN}}-V_O)/L$. Correspondingly, the high-side drain–source voltage V_{DSH} rises with a rate of $r_{DS_ON}\times(V_{\mathrm{IN}}-V_O)/L$. Both I_{DSH} and V_{DSH} require instant measurement simultaneously to determine the instant r_{DS_ON}. To achieve such, a time synchronizer is designed to synchronize the two detectors. As shown in Fig. 4(b), when V_{SW} rises rapidly from near ground to a high voltage due to a M_H switching-ON, the synchronizer captures this sharp rising edge to trigger the enable signal Φ_1, thus initializing the detections of I_{DSH} and V_{DSH}. After a sensing period t_{DET}, Φ_1 resets, commanding the two detectors to hold the instant values of I_{DSH} and V_{DSH} as the I_{DS_ON} and V_{DS_ON}, respectively. The synchronized I_{DS_ON} and V_{DS_ON} are fed into a divider for r_{DS_ON} computing. Successively, a T_J effect remover processes the r_{DS_ON} further, by eliminating the T_J influence on r_{DS_ON}. As shown in Fig. 4(a), the T_J of M_H is sensed and converted into a voltage signal V_{TJ} by the proposed I_{GSS}-based T_J sensor, which would be addressed in the next section. With such T_J information, the r_{DS_ON} variation ($\Delta r_{DS_ON}(T_J)$) due to T_J is determined. The $\Delta r_{DS_ON}(T_J)$ is then subtracted from the readout of r_{DS_ON}, obtaining a T_J-independent r_{DS_ON}'.

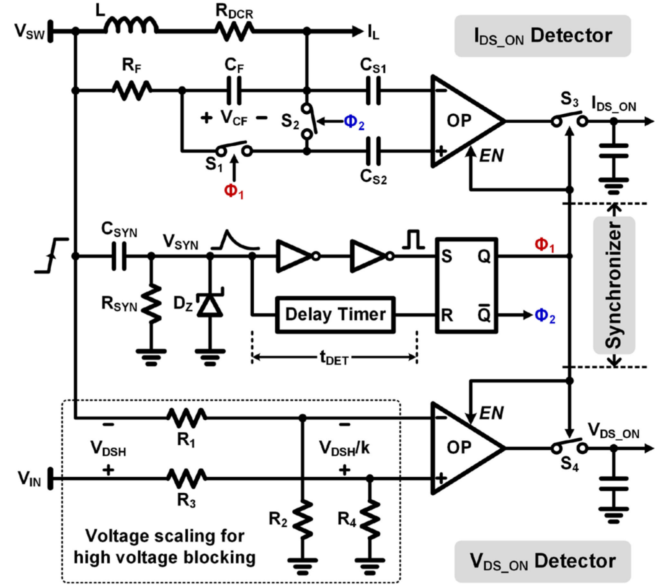


Fig. 5. Circuit schematic of the r_{DS_ON} sensor.

It should be noted that the dynamic ON-resistance r_{DS_ON} continuously varies during its ON states [4], [18], which certainly affects the measurement accuracy. However, the time constant of r_{DS_ON} decay during ON states is in the order of hundreds of microseconds [18], [19]. In this work, one switching period only lasts 100 ns, which is three orders shorter, indicating a negligible change on r_{DS_ON} during each ON state of M_H.

Fig. 5 details the circuit schematic of the r_{DS_ON} sensor. To implement the I_{DS_ON} detection, a direct current resistance (DCR) current sensor is utilized. Specifically, an RC filter consisting of R_F and C_F is connected in parallel with L to replicate the voltage drop across the direct-current resistance R_{DCR} of the inductor L. By letting the time constant $R_F\times C_F$ equal to L/R_{DCR}, V_{CF} has the same voltage as that across R_{DCR}. Note that V_{CF} is proportional to I_{DSH} during each ON state of M_H. To capture V_{CF}, a capacitive-coupled sensing stage is designed using two capacitors, C_{S1} and C_{S2}, combined with two switches, S_1 and S_2 [22], [23]. During the detection period, the switch S_1 is ON while S_2 is OFF. The increase of V_{CF} due to the I_L increase is coupled to an operational amplifier by C_{S1} and C_{S2}. At the end of the detection process, the output voltage of the operational amplifier is sampled, which carries the information of I_{DS_ON}. For V_{DS_ON} detection, both V_{IN} and V_{SW} are largely scaled down to isolate the high voltage from the sensing circuits.

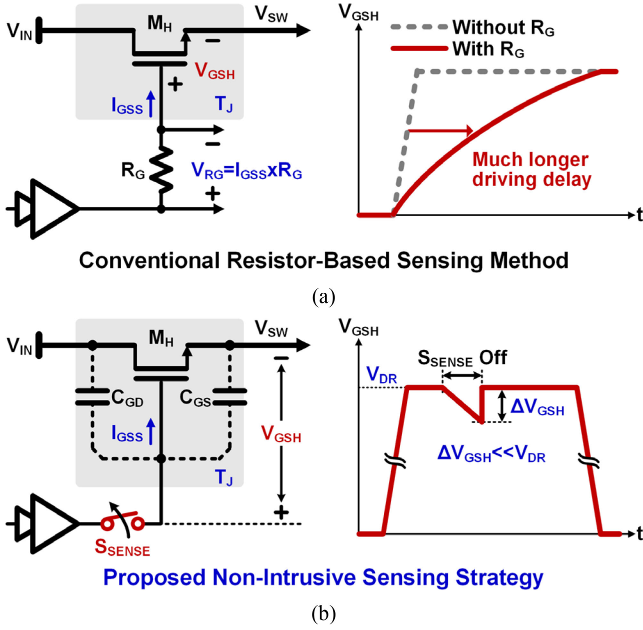


Fig. 6. (a) Conventional gate resistor-based I_{GSS} sensing. (b) Proposed non-intrusive I_{GSS} sensing.

The scaled voltage, V_{DSH}/k, is amplified and then sampled as V_{DS_ON} through the switch S_4. To synchronize these two detection processes, the synchronizer employs a capacitor C_{SYN} to sense the sharp rising edge of V_{SW} during the switching-ON of M_H. Accordingly, the signal Φ_1 is enabled, triggering the delay timer t_{DET}. After t_{DET} expires, Φ_1 is reset to terminate the detection processes. In the synchronizer, a pull-down resistor R_{SYN} is employed to reset V_{SYN} in every detection cycle, ensuring the proper detection logic. A Zener diode D_Z is connected to clamp the voltage swing range at the node V_{SYN}, preventing high voltage stresses on the low-voltage devices.

III. Gate Leakage Based Junction Temperature Sensing

A. I_{GSS} Based Nonintrusive Temperature Sensing

As the T_J fluctuation causes large errors on the proposed aging precursor r_{DS_ON}, its influence must be calibrated. However, GaN HEMTs are commonly available as discrete devices, making it challenging to determine the T_J remotely from an on-die controller. To overcome this, this article proposes a cross-die sensing mechanism, which characterizes a GaN switch's T_J by measuring its gate leakage I_{GSS}.

Studies show that the I_{GSS} of a GaN HEMT is temperature sensitive, but aging independent [24], [25], making it a perfect calibration parameter in this scenario. As I_{GSS} can be accurately measured on the board level [26], T_J of a GaN switch is thus successfully obtained regardless of its placement to the die. The main challenge is that the magnitude of I_{GSS} is usually very low and difficult to make accurate measurement. To overcome this, in Fig. 6(a), a series gate resistor R_G is used to magnify I_{GSS} linearly as a voltage V_{RG}. However, to reach reasonable sensing resolution, R_G has to be large. For a typical I_{GSS} of 100 μA [24]–[26], R_G should be at least 100 Ω to make V_{RG} higher than 10 mV. Such a large R_G would drastically increase the gate drive delay, restricting the minimum ON-time and increasing I–V switching power loss.

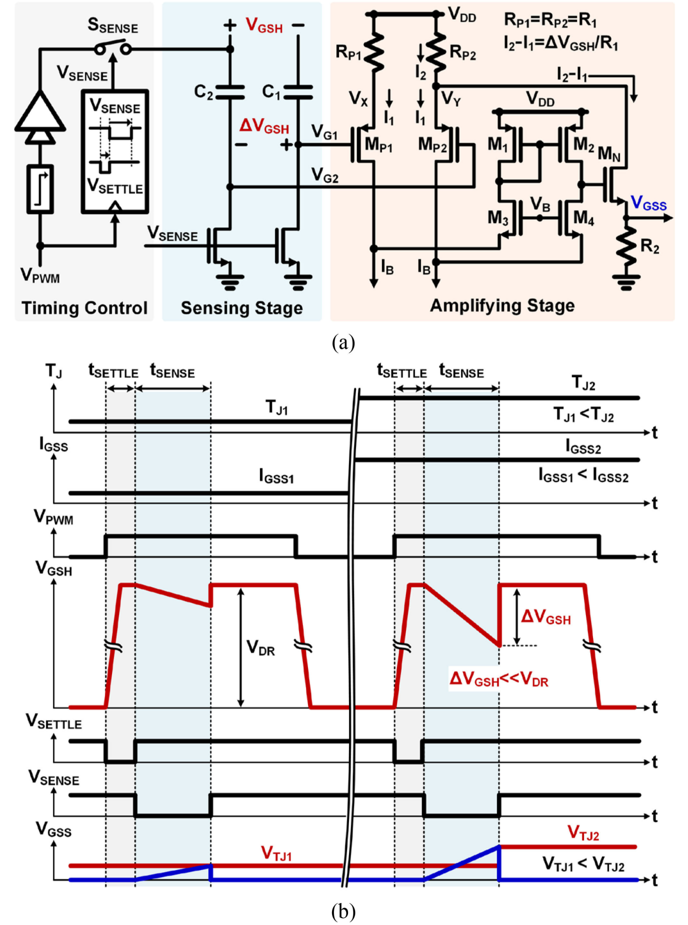


Fig. 7. (a) Circuit schematic and (b) timing diagram of the I_{GSS}-based T_J sensor.

In this article, a nonintrusive I_{GSS} sensing strategy is developed, which can be explained using Fig. 6(b). Compared to the regular gate driver, only one extra sensing switch S_{SENSE} is used. During the switching-ON of M_H, S_{SENSE} stays on without influencing the gate driving. After the gate voltage V_{GSH} settles at V_{DR}, S_{SENSE} is intentionally switched OFF for a short period of time. In this period, the gate capacitors C_{GS} and C_{GD} are discharged by I_{GSS}, causing a voltage drop ΔV_{GSH}, which can be calculated as follows

$$\Delta V_{GSH} = t_{SENSE} \times I_{GSS}/(C_{GS} + C_{GD}). \quad (1)$$

According to (1), I_{GSS} can be directly sensed by ΔV_{GSH}, which carries the information of T_J. Note that t_{SENSE} should be carefully controlled so that ΔV_{GSH} is much smaller than V_{DR}, in order to minimize the operation of the gate driver. After t_{SENSE} expires, S_{SENSE} is switched back on to retain the level of V_{GSH}.

B. Sensor Implementation

Fig. 7(a) shows the circuit schematic of the I_{GSS}-based, cross-die, nonintrusive T_J sensor. It consists of a timing control stage,

a sensing stage, and an amplifying stage. The timing diagram of the circuit is shown in Fig. 7(b).

At the beginning of each ON state, the feedback control signal V_{PWM} triggers the gate driver to turn on M_H, which also turns ON the sensing timer. After a time of t_{SETTLE}, the timer turns OFF S_{SENSE} to initialize the I_{GSS} sensing. At this instant, the gate of M_H is disconnected from the gate driver. I_{GSS} discharges the gate capacitor C_G (=C_{GS} + C_{GD}) at a rate of I_{GSS}/C_G, causing a gate voltage drop ΔV_{GSH}. ΔV_{GSH} is then coupled to the amplifying stage for further processing. To improve the dc gain and hence the processing accuracy, the amplifying stage is designed using a cascode voltage amplifier. V_B is controlled by a dc biasing circuit to provide proper gate voltage biasing at M_3 and M_4. The identical transistors M_{P1} and M_{P2} perform as source followers, which conduct the identical current I_1. Hence, the two transistors have the same gate–source voltage, leading to

$$V_{G1} - V_X = V_{G2} - V_Y. \tag{2}$$

Here, V_{G1} and V_X are the gate and source voltage of M_{P1}. V_{G2} and V_Y are those of M_{P2}. Derived from (2), we have

$$V_X - V_Y = V_{G1} - V_{G2} = \Delta V_{GSH}. \tag{3}$$

In the meantime

$$I_2 - I_1 = \frac{V_X - V_Y}{R_1} = \frac{\Delta V_{GSH}}{R_1}. \tag{4}$$

$I_2 - I_1$ is carried by M_N through a resistor R_2, generating the sensing voltage V_{GSS} as

$$V_{GSS} = \frac{R_2}{R_1} \times \Delta V_{GSH}. \tag{5}$$

At the end of t_{SENSE}, V_{GSS} is detected as the sensing signal V_{TJ}. By inserting (1) into (5), a linear relationship between V_{TJ} and I_{GSS} is obtained as follows:

$$V_{TJ} = \frac{R_2}{R_1} \times t_{\mathrm{SENSE}} \times I_{GSS}/\left(C_{GS} + C_{GD}\right). \tag{6}$$

After t_{SENSE} expires, S_{SENSE} switches ON to resume the normal gate driving. Since the sensing procedure takes place cycle-by-cycle, the change of the junction temperature T_J would be detected accurately in real time.

IV. Proactive Temperature Frequency Scaling

The proposed online condition monitoring and T_J sensing techniques facilitate a proactive measure for device longevity improvement through a temperature frequency scaling scheme. The essential principle is to adaptively manage the operation speed and thus heat generation of power circuits with an ultimate goal of achieving optimal performance (based on load current, transient speed and efficiency) and the aging status (based on T_J).

To illustrate the scheme, Fig. 8(a) shows the proposed circuit block diagram, with reference to the key operation timing diagram in Fig. 8(b). Conventionally, it is believed that, when a power converter operates at high f_{SW}, it has performance advantages of fast dynamic transient response and small inductor current and output voltage ripples. However, as the power

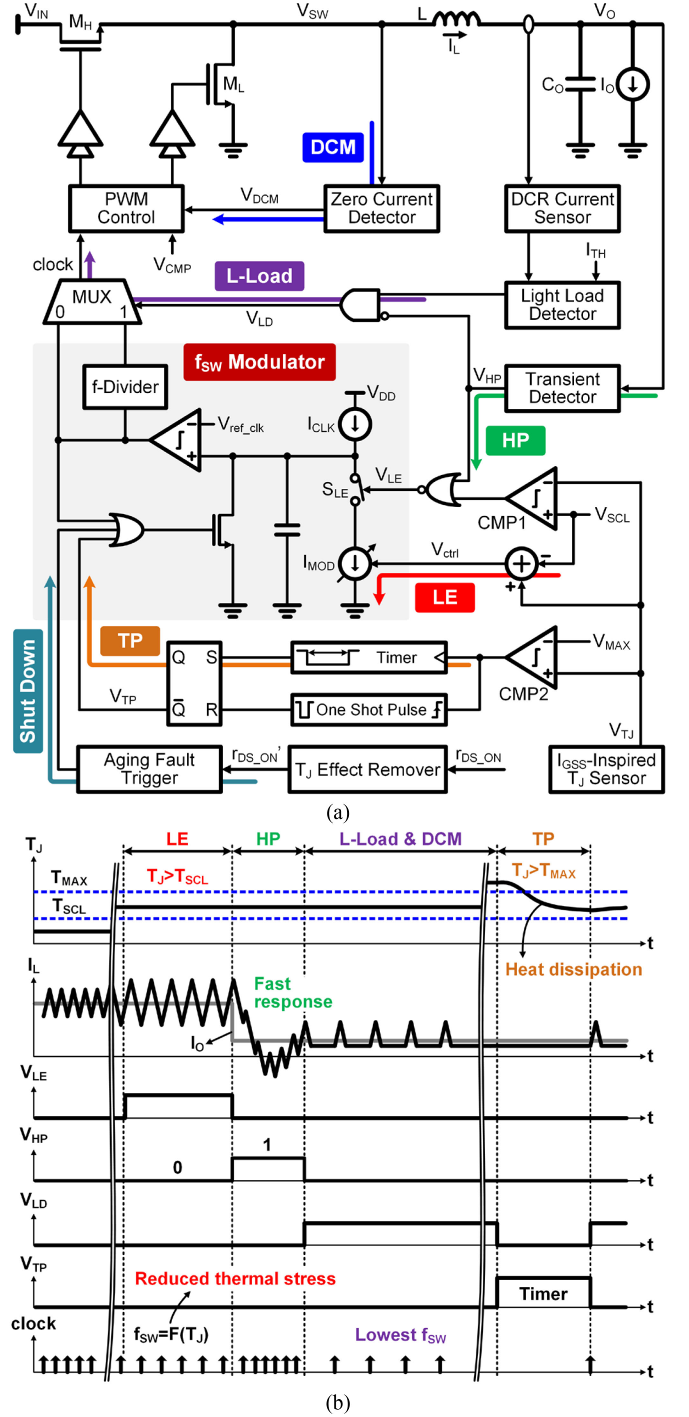


Fig. 8. (a) Circuit schematic and (b) operation principle of the proactive temperature frequency scaling scheme.

transistors have to switch faster at high f_{SW}, they consume more power and generate more heat, elevating T_J. If T_J is still at relatively low level, aging stress is the least significant and thus the power converter retains regular operation. However, if T_J rises beyond a predefined threshold T_{SCL}, the comparator CMP1 in Fig. 8(a) triggers the mode signal V_{LE} to high. S_{LE} then switches ON, activating the longevity enhancement (LE) mode. In the LE mode, a current source I_{CLK} in the f_{SW} modulator

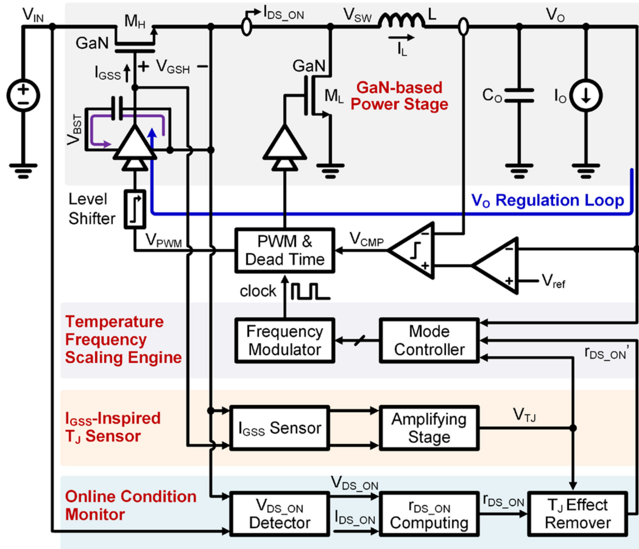


Fig. 9. System block diagram of the proposed power converter.

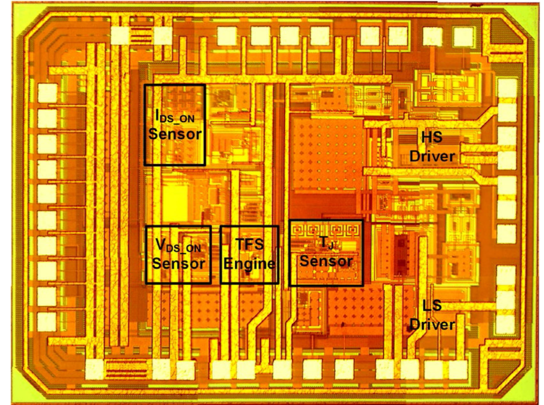


Fig. 10. Chip micrograph.

is tuned by a voltage-controlled modulation current I_{MOD}. As I_{MOD} is proportional to the difference of V_{TJ} to V_{SCL}, the f_{SW} is thus modulated inversely against the T_J. As such, thermal related aging stress is counteracted to a certain degree, owing to the switching power loss reduction, alleviating the positive interaction between thermal effect and aging, thereby enhancing the GaN longevity. Meanwhile, in order to achieve optimal operation between performance and thermal aging, load condition is monitored instantly by a transient detector in Fig. 8(a). When the load current I_O changes, fast transient response is required to avoid V_O overshoot/undershoot, which cause potential malfunctions on load modules. In this situation, the transient detector captures the event of V_O's abrupt change to set the mode signal V_{HP}, triggering the high-performance (HP) mode. S_{LE} is thus forced OFF, recovering f_{SW} to the maximum. On the other hand, when the power level drops, f_{SW} drops accordingly and the power converter enters the discontinuous conduction mode to retain high efficiency. To the other extreme, when T_J exceeds the allowed operation limit T_{MAX}, the comparator CMP2 sets high, triggering the one shot pulse generator and enabling the thermal protection (TP) signal V_{TP} to shut down the power converter. Once T_J drops below T_{MAX}, the normal operation resumes. Furthermore, along with the course of operation, if the aging precursor, namely the calibrated ON-resistance r_{DS_ON}', rises beyond its aging threshold value, alert signal would be triggered to shut down the converter, preventing it from permanent damage.

V. Experimental Verification

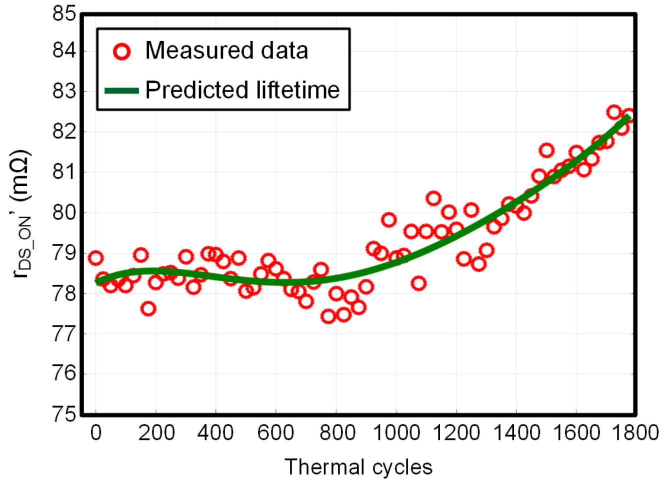
A. System Implementation

In order to demonstrate the effectiveness of reliability improvement, all the proposed techniques are incorporated into a GaN-based half-bridge converter, shown in Fig. 9. By sensing the dynamic ON-resistance r_{DS_ON} of GaN switch as the real-time precursor, the proposed online condition monitoring prognoses the *i*-collapse caused aging status of GaN switch, superior to the offline and *in situ* approaches in general. The gate-leakage I_{GSS} based T_J sensor acquires the instant T_J, which is crucial in the process of removing temperature effect on r_{DS_ON}. These successfully facilitate the T_J-independent online condition monitoring and largely reduce the FMR. On the other hand, the temperature frequency scaling engine slows down the aging process in GaN switches whenever possible, while minimizing the negative impacts on system performance. Rather than board-level implementation, all these three techniques are integrated into the monolithic silicon controller with a pulsewidth modulator for compact and energy efficient system integration. Overall, these techniques require no interruption on conventional closed-loop voltage regulation and are completely nonintrusive for a switching power circuit.

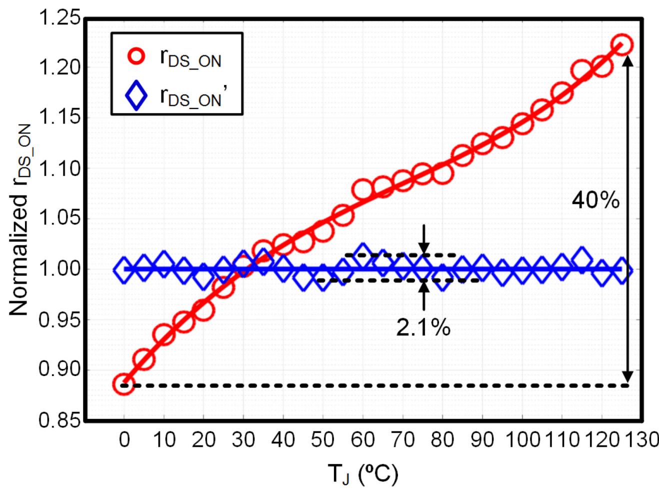
B. Experimental Results

An IC prototype of this design was fabricated in a 0.18 μm high-voltage CMOS process [27]. The chip micrograph is shown in Fig. 10 with an active die area of 1.56 mm^2, fully integrating the sensing circuits and proactive temperature frequency scaling engine. Operating at 10 MHz, the converter delivers a maximum power of 6 W over an input range of 5 to 40 V and a regulated output voltage programmable from 3.3 to 5 V.

To validate the online condition monitoring scheme, accelerated thermal stress test is carried out. Under the test, the GaN-based power converter operates at 10 MHz normally with 12 V input, 5 V output, and 1 A load current. To accelerate the aging process, the converter is placed in a temperature chamber and the chamber temperature is cycled between 0 and 125 °C periodically. As shown in Fig. 1, because of different lattice constants and thermal expansion coefficients [12], the interfaces between different layers suffer from thermomechanical stress during temperature cycling. Consequently, together with the electrical field imposed by the normal switching behaviors, it induces more charge traps in the insulator and buffer layers, accelerating the *i*-collapse effect in GaN HEMT [28], [29]. In this experiment, after each 25 thermal cycles, the ON-resistance

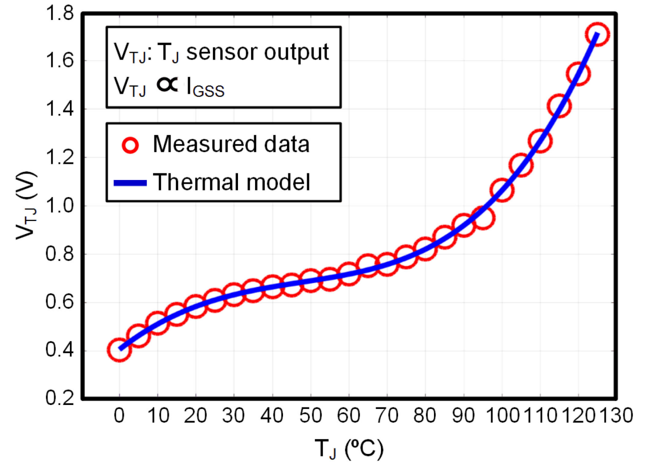


(a)

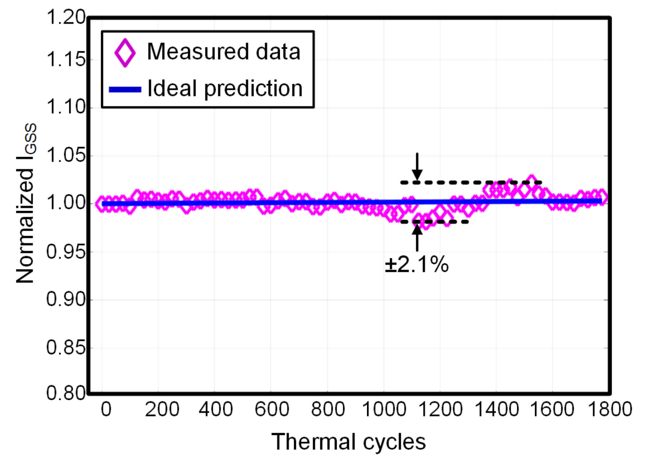


(b)

Fig. 11. Measured results on aging precursor. (a) Thermal stress test of r_{DS_ON}'. (b) Temperature dependence calibration on r_{DS_ON}.



(a)



(b)

Fig. 12. Measured results on the gate leakage I_{GSS}-inspired T_J sensing. (a) On-chip sensed voltage V_{TJ} versus T_J. (b) I_{GSS} versus thermal cycles.

of the GaN switch is measured at a reference temperature of 25 °C. On the other hand, with the ball grid array package [12], the GaN HEMTs used in this work rarely suffer from conventional solder crack and bond-wire lift-off degradation below 300 °C [30]. Instead, the aging process of GaN HEMT is mainly due to *i*-collapse effect [30], resulting in the gradual increase of the ON-resistance. Fig. 11(a) reveals that the r_{DS_ON}' increases gradually after a certain number of thermal cycles, offering clear and accurate tracking on the process of aging. In Fig. 11(b), with the sensed junction temperature T_J, the T_J effect on r_{DS_ON} is calibrated, eliminating the T_J-dependence of r_{DS_ON} from 40% to 2.1% between 0 and 125 °C. Accordingly, the false monitoring rate is suppressed by 19 times.

The performance of the I_{GSS}-based T_J sensor is shown in Fig. 12(a). The ON-chip sensed voltage V_{TJ} increases as T_J rises. The measurement data coincide well with the thermal model, which is used by T_J effect remover to perform T_J effect calibration on sensed r_{DS_ON}. On the other hand, as shown in Fig. 12(b), the I_{GSS} versus thermal cycles test proves that I_{GSS} aging dependence is below ±2.1%, much lower than conventional precursors.

To validate the operation principle of the T_J sensor, Fig. 13 shows the transient measurements on V_{GSH} at various temperatures. V_{GSH} drops during a constant 20 ns sensing period, in which the gate capacitor C_G is discharged by I_{GSS}. At 25, 55, and 75 °C, the voltage drops are 35, 70, and 120 mV, respectively. Apparently, ΔV_{GSH} gets larger as temperature rises, but is still much smaller than the gate drive voltage, which is about 5 V.

To validate the proactive temperature frequency scaling scheme, the switching frequency f_{SW}–T_J correlation test is given in Fig. 14. As T_J increases, f_{SW} scales across operation zones to reach an optimal operation between performance and aging. Furthermore, the power loss P_{LOSS} measurements reveal that the LE mode reduces P_{LOSS} by 200 mW in maximum and T_J by 16 °C with a typical $R_{\theta JA}$ of GaN switch as 82 °C/W. It greatly lowers the aging risk. As addressed in the design, HP mode is enabled during load transient to optimize the system performance.

Fig. 15 compares the dynamic response between the LE mode and the HP mode. The comparison is conducted with a supply voltage of 12 V and the output voltage of 5 V. In response to

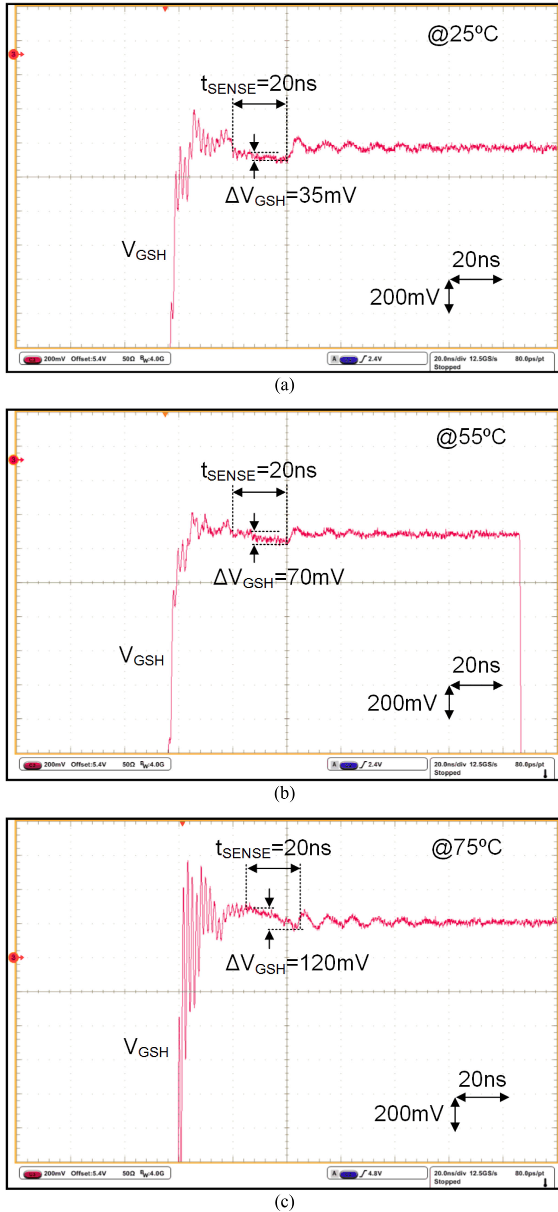


Fig. 13. Measured gate driving voltage V_{GSH} of M_H, with I_{GSS}-based T_J sensing at (a) 25 °C, (b) 55 °C, and (c) 75 °C.

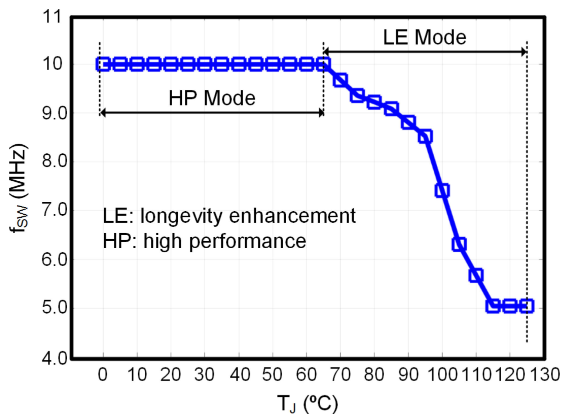


Fig. 14. Measured $f_{\rm SW}$-T_J correlation in the temperature frequency scaling scheme.

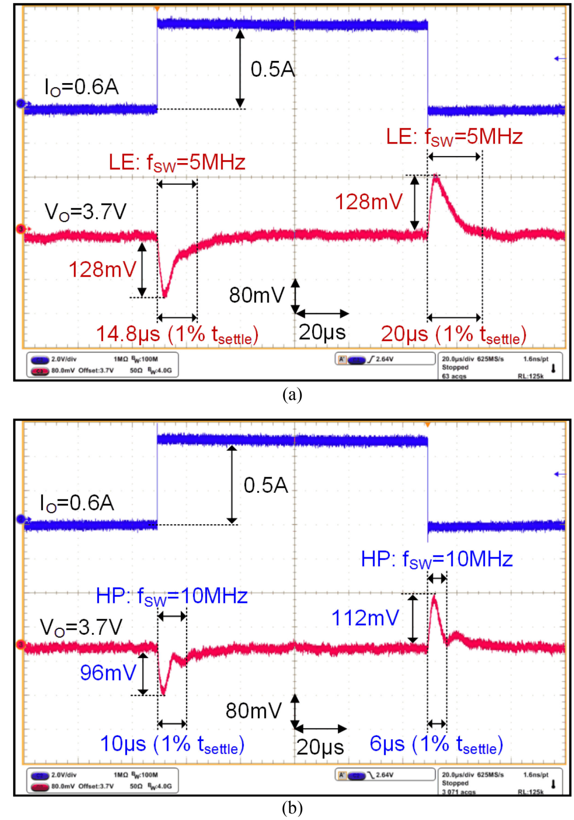


Fig. 15. Measured load transient response under (a) the longevity-enhancement (LE) mode, and (b) the high-performance (HP) mode.

500 mA I_O step-up change, the converter achieves a 1% settling time $t_{\rm settle}$ of 14.8 μs under the LE mode. By enabling the HP mode, $t_{\rm settle}$ reduces to 10 μs, improving the transient response by 50%. For the I_O step-down, the 1% settling time reduces from 20 to 6 μs by switching from the LE to the HP mode, improving the transient response by 70%.

VI. Conclusion

A self-aging-prognostic GaN-based dc–dc power converter is presented in this article. Particularly, an online condition monitoring is designed by sensing dynamic ON-resistance $r_{DS_\rm ON}$ of GaN switch as the precursor, capable of prognosing the i-collapse caused GaN device failure. In addition, a gate leakage-inspired junction temperature sensing is developed to calibrate the temperature effect on $r_{DS_\rm ON}$, improving the prognosis accuracy. Furthermore, a proactive temperature frequency scaling scheme is accomplished to enhance the system longevity. The design is successfully validated by experimental results.

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