Research on a Novel High-Efficiency Three-Phase Resonant Pole Soft-Switching Inverter

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***Abstract*—A high-efficiency three-phase resonant inverter is presented to optimize the performance of the inverter. When the auxiliary resonant circuit on each phase bridge arm works in the commutation process of the inverter, the voltage across resonant capacitors in parallel with main switches will form zero state periodically. In this case, main switches can achieve zero-voltage soft-switching. Meanwhile, auxiliary switches can achieve zero-current turn ON and zero-voltage turn OFF during the operation of the auxiliary resonant circuit. Soft-switching can reduce switching loss and make the inverter work efficiently. The novelty of the inverter mainly reflects in the simple structure of the auxiliary circuit and the simple control method of auxiliary switches. This article analyzes the working mode of the circuit and the realization condition of soft-switching. Meanwhile, it discusses theoretical calculation of the power loss of the auxiliary circuit. The experimental results on the 3-kW prototype show that switching devices work in the soft-switching state. The efficiency of the prototype under the rated output power reaches 98.7%, which is higher than that of the same type of other soft-switching inverter. Therefore, the topology is valuable for the research and development of the high-performance three-phase inverter.**

***Index Terms*—Inverter, high efficiency, resonant, soft-switching, switching loss.**

I. Introduction

INDUSTRIAL development has increasingly strict requirement on the switching frequency of the inverter. Besides high-frequency, high-efficiency, and high-power, inverters are also expected to have smaller size and lower cost [1]. When the switching device in the hard-switching inverter is in the switching state, the voltage across the switching device and the current flowing through the switching device will overlap in the switching process, which inevitably leads to switching loss. The switching loss of the hard-switching inverter will increase obviously at high switching frequency, which prevents the inverter from realizing high frequency. However, soft-switching technology applied in the inverter can reduce switching loss and improve the efficiency.

Soft-switching inverters mainly include the resonant dc-link inverter and the resonant pole inverter. The auxiliary resonant circuit of the resonant dc-link inverter is located between the dc power supply and the bridge arm. DC-link voltage periodically drops to zero to make main switches of the inverter achieve soft-switching [2]–[6]. However, the zero-state of dc-link voltage, which is formed periodically, has a negative impact on the dc voltage utilization of the inverter. The auxiliary circuit of the resonant pole inverter is located in the bridge arm of each phase [7]–[21], and the work of the auxiliary circuit has no adverse effect on the dc-link voltage, so the resonant pole inverter has gradually become a research hotspot in recent years. A variety of resonant pole inverters have been presented in relevant literatures. However, there are still some problems to be optimized. The auxiliary circuits of each phase presented in [7] and [8] both contain four auxiliary switches. More auxiliary switches will lead to the complexity of the auxiliary circuit, which is not conducive to reducing the hardware cost of the auxiliary circuit. Two auxiliary switches are arranged in the auxiliary circuits of each bridge arm in [9] and [10]. Although the number of auxiliary switches is small, four resonant inductors, six resonant capacitors, and eight auxiliary diodes are needed for the auxiliary circuit of each phase. Excessive passive components will also lead to the complexity of auxiliary circuit. The number of auxiliary switches in the topology presented in [11] is only one, but the maximum voltage across main switches is twice as much as the input dc voltage of the inverter, which will affect the reliability of main switches. There are no auxiliary switches in the proposed circuits in [12], which is beneficial to the simplification of the control method in the inverter. Nevertheless, the high loss of coupled inductors in series with bridge arms will hinder efficiency optimization. In [13], two storage capacitors are arranged between the dc buses and the high-frequency operation of the inverter may cause unequal voltage across the two storage capacitors, which will affect the reliability of the inverter. A transformer is installed in the auxiliary circuit of each phase in [14]–[16]. The accumulation of residual magnetism will cause the saturation of the transformer and the failure of the auxiliary circuit. In [17], the maximum voltage across auxiliary switches and auxiliary diodes is all no less than 1.5 times as much as the input dc voltage of the inverter, which is not conductive to reducing hardware cost. Furthermore, the load current still flows through resonant inductors after the resonance process ends, which leads to the

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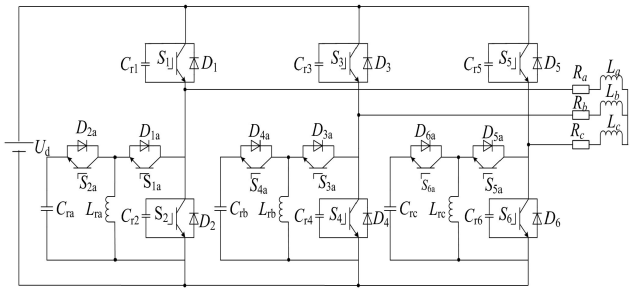

Fig. 1. Main circuit of the high-efficiency three-phase resonant pole inverter.

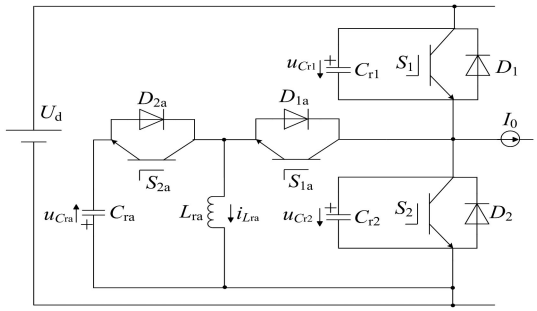

Fig. 2. One phase equivalent circuit of a high-efficiency three-phase resonant pole inverter.

increase of the power loss in the auxiliary circuit. In [18]–[21], the duty cycle of the trigger pulse of the auxiliary switch depends on the instantaneous value of the load current in each switching period. The accuracy of the load current detection must be high enough to ensure that the auxiliary circuit can operate normally, leading to the complexity of the control method. Moreover, the above-mentioned literatures concerning resonant pole inverters have no theoretical analysis on the power loss of the auxiliary circuit.

To overcome the above-mentioned shortcomings, this article presents a high-efficiency three-phase resonant pole inverter. Its advantages are as follows.

1) The auxiliary circuit is in parallel with each bridge arm, which limits the conduction loss of the auxiliary circuit. Besides, the structure of the auxiliary circuit on each bridge arm is relatively simple, containing only two auxiliary switches, a resonant inductor, and three resonant capacitors. Moreover, there are no storage capacitors and transformers in the auxiliary circuit, which improves the reliability of the inverter.
2) The maximum voltage across the switching devices is no higher than dc power supply voltage, which avoids the use of switching devices withstanding higher voltage, so as to reduce the hardware cost.
3) The duty cycle of the trigger pulse of the auxiliary switch can be designed as a fixed value.

The control process of the auxiliary circuit has no need for real-time detection of the load current, which simplifies the control of the auxiliary circuit. In addition, the presented inverter can be applied as the efficient variable frequency power supply of the electric drive system. To the author's knowledge, the efficiency of corresponding industry products in the electric drive system is usually about 98%. This article analyzes the working modes of the inverter and the conditions of soft-switching in detail. Meanwhile, it deduces the theoretical expression of the power loss of the auxiliary circuit. Finally, the experimental results on the 3-kW prototype verify the performance of the novel inverter.

II. Analysis on Working Process of the Circuit

A. Structure of the Circuit and Implementation Principle of Soft-Switching

Fig. 1 shows the main circuit of the inverter in which the auxiliary circuits are arranged on the bridge arm of each phase. As shown in Fig. 1, for the example of the auxiliary circuit on the a-phase bridge arm, it comprises resonant capacitors $C_{\rm r1}$, $C_{\rm r2}$, and $C_{\rm ra}$, resonant inductors $L_{\rm ra}$ and auxiliary switches $S_{1\rm a}$ and $S_{2\rm a}$, and their antiparallel diodes $D_{1\rm a}$ and $D_{2\rm a}$. The structures of the auxiliary circuits on the other two bridge arms are the same with that on the a-phase bridge arm. The auxiliary resonant circuits on the three phase bridge arms are independent of each other.

Before the main switches S_1–S_6 on the bridge arms is turned ON, the voltages across the resonant capacitors $C_{\rm r1}$–$C_{\rm r6}$ in parallel with S_1–S_6 decrease to zero in advance under the function of the auxiliary resonant circuits, so that S_1–S_6 can achieve zero-voltage turn ON. At the moment, when the auxiliary switches $S_{1\rm a}$–$S_{6\rm a}$ are turned ON, the resonant inductors $L_{\rm ra}$, $L_{\rm rb}$, and $L_{\rm rc}$ restrict the change rate of the current flowing through $S_{1\rm a}$–$S_{6\rm a}$ to reduce turn-ON loss, so that $S_{1\rm a}$–$S_{6\rm a}$ can achieve zero-current turn ON. During the turn-OFF transient of S_1–S_6 and $S_{1\rm a}$–$S_{6\rm a}$, resonant capacitors $C_{\rm r1}$–$C_{\rm r6}$ and $C_{\rm ra}$–$C_{\rm rc}$ restrict the change rate of the voltage across S_1–S_6 and $S_{1\rm a}$–$S_{6\rm a}$ to reduce turn-OFF loss, so that S_1–S_6 and $S_{1\rm a}$–$S_{6\rm a}$ can achieve zero-voltage turn OFF.

B. Working Mode of the Circuit

For the sake of the simplification of the following analysis, it can be assumed that: each device works in the ideal state; and because the load inductor is much higher than the resonant inductor, the load current I_0 remains constant in a switching cycle and the load can be regarded as a constant current source. Because the three-phase auxiliary resonant circuits in Fig. 1 are independently controlled, this article will analyze the working mode of the a-phase auxiliary resonant circuit in one switching cycle. Fig. 2 shows the single-phase equivalent circuit of the inverter and the positive direction of the physical quantity. The working process of the circuit in each switching cycle contains ten modes. Fig. 3 shows the characteristic waveforms of the circuit. Fig. 4 shows the equivalent circuit under each working mode. Fig. 5 shows a gate-pulse generation circuit of phase-a, in which Δ denotes dead time of the inverter, T denotes switching cycle, T_2 denotes the duration of Mode 2. $T_{S1\,a}$ and $T_{S2\,a}$ denote the fixed time that gate pulses of $S_{1\rm a}$ and $S_{2\rm a}$ are in the high level, respectively. The gate-pulse (v_{gS1} and v_{gS2}) generation strategy of S_1 and S_2 is bipolar sinusoidal pulsewidth modulation (SPWM). v_{g1} and v_{g2} can be derived by the comparison of a triangular wave $v_{\rm tri}$ with a reference sine wave $v_{a\text{-ref}}$. v_{g1} and v_{g2} pass through a rising-edge delay (named as turn-ON delay,

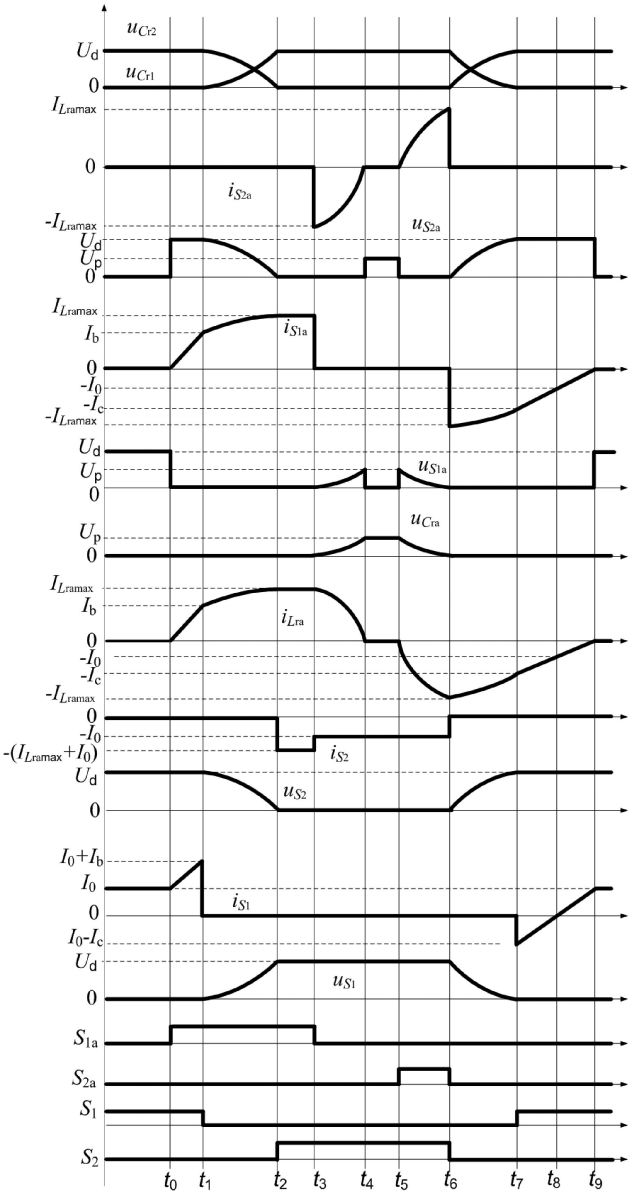

Fig. 3. Theoretical waveforms in resonant commutation.

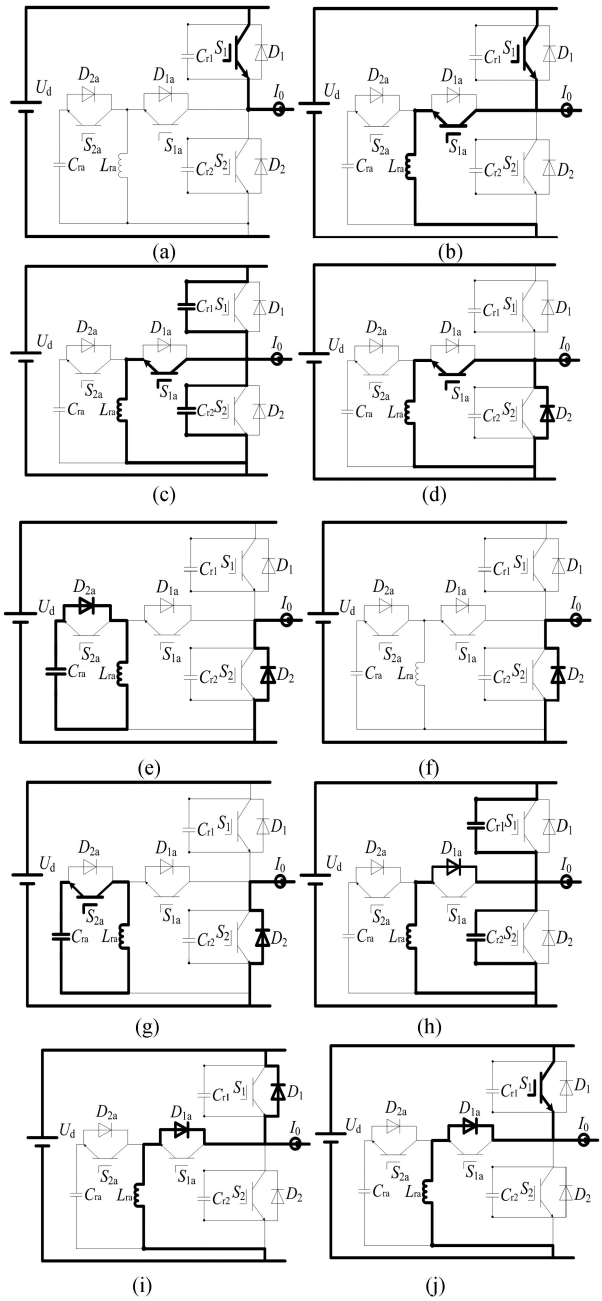

Fig. 4. Equivalent circuits in each working mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10.

delay time is Δ), which produces v_{gS1} and v_{gS2}. The gate-pulse ($v_{gS1\,a}$) generation of $S_{1\mathrm{a}}$ rests with v_{gS1} and v_{gS2}. First, v_{gS2} passes through a rising-edge delay (named as turn-ON delay, delay time is T–T_2–Δ), which produces v_{g3}. Next, v_{g3} and v_{gS1} pass through a logical AND, which produces v_{g4}. Finally, v_{g4} passes through a falling-edge delay (named as turn-OFF delay, delay time is $T_{S1\,a}$–T_2), which produces $v_{gS1\,a}$. The gate-pulse ($v_{gS2\,a}$) generation of $S_{2\mathrm{a}}$ also rests with v_{gS1} and v_{gS2}. First, v_{gS1} pass through a rising-edge delay (named as turn-ON delay, delay time is T–$T_{S2\,a}$–Δ), which produces v_{g5}. Finally, v_{g5} and v_{gS2} pass through a logical AND, which produces $v_{gS2\,a}$. v_{gS1}, v_{gS2}, $v_{gS1\,a}$, and $v_{gS2\,a}$ can pass through drive circuits to trigger S_1, S_2, $S_{1\mathrm{a}}$, and $S_{2\mathrm{a}}$.

Working Modes

Mode 1 (t–t_0). The current flows through S_1 and no current flows through the other switching devices. The voltages $u_{C\mathrm{ra}}$ and $u_{C\mathrm{r1}}$ across C_{ra} and C_{r1} are equal to zero. The voltage $u_{C\mathrm{r2}}$ across C_{r2} is equal to U_{d}. The current $i_{L\mathrm{ra}}$ flowing through L_{ra} is equal to zero. The current i_{S1} flowing through S_1 is equal to the load current I_0. The circuit works in the steady state.

Mode 2 (t_0–t_1). After $S_{1\mathrm{a}}$ is switched ON at t_0, L_{ra} starts to absorb electric energy. Meanwhile, $i_{L\mathrm{ra}}$ and i_{S1} start to increase linearly. At the end of Mode 2, $i_{L\mathrm{ra}}$ increases to I_{b} and i_{S1} increases to $I_0 + I_{\mathrm{b}}$.

$i_{L\mathrm{ra}}(t)$ can be presented by the following formula:

$$i_{L_{\mathrm{ra}}}(t) = \frac{U_{\mathrm{d}}}{L_{\mathrm{ra}}}(t - t_0) \tag{1}$$

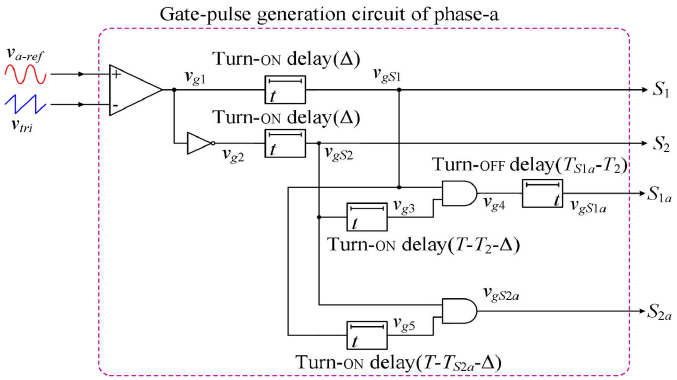

Fig. 5. Gate-pulse generation circuit of phase-a.

The duration of this mode can be expressed as follows:

$$T_2 = t_1 - t_0 = \frac{I_{\rm b} L_{\rm ra}}{U_{\rm d}} \tag{2}$$

Mode 3 (t_1–t_2). After S_1 is switched OFF at t_1, $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ work in the resonant state. $C_{\rm r2}$ releases electric energy. $C_{\rm r1}$ and $L_{\rm ra}$ absorb electric energy. i_{Lra} continues to increase in the positive direction. When i_{Lra} reaches the positive maximum value I_{Lramax}, u_{Cr1} increases to U_d and Mode 3 ends.

$i_{Lra}(t)$, $u_{Cr1}(t)$, $u_{Cr2}(t)$, and I_{Lramax} can be expressed as follows:

$$i_{Lra}(t) = \frac{U_{\rm d}}{Z}\sin\left[\omega\left(t-t_1\right)\right] + \left(I_0 + I_{\rm b}\right)\cos\left[\omega\left(t-t_1\right)\right] - I_0 \tag{3}$$

$$u_{Cr1}(t) = Z\left(I_0 + I_{\rm b}\right)\sin[\omega(t-t_1)] - U_{\rm d}\cos[\omega(t-t_1)] + U_{\rm d} \tag{4}$$

$$u_{Cr2}(t) = -Z\left(I_0 + I_{\rm b}\right)\sin\left[\omega\left(t-t_1\right)\right] + U_{\rm d}\cos\left[\omega\left(t-t_1\right)\right] \tag{5}$$

$$I_{Lramax} = \sqrt{\left(\frac{U_{\rm d}}{Z}\right)^2 + \left(I_0 + I_{\rm b}\right)^2} - I_0 \tag{6}$$

where $Z = \sqrt{L_{\rm ra}/(C_{\rm r1}+C_{\rm r2})}$ and $\omega = 1/\sqrt{L_{\rm ra}(C_{\rm r1}+C_{\rm r2})}$.

The duration of this mode can be shown as follows:

$$T_3 = t_2 - t_1 = \frac{1}{\omega}\arcsin\frac{U_{\rm d}}{\sqrt{U_{\rm d}^2 + Z^2\left(I_0 + I_{\rm b}\right)^2}} \tag{7}$$

Mode 4 (t_2–t_3). D_2 begins to work in conducting state at t_2. At the same time, the resonant state of $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ ends. In this mode, u_{Cr1} is maintained as U_d. u_{Cra} and u_{Cr2} are maintained as zero. i_{Lra} is maintained as I_{Lramax}. The circuit works in the steady state.

The duration of Mode 4 can be shown as follows:

$$\begin{aligned} T_4 &= T_{S1a} - T_2 - T_3 \\ &= T_{S1a} - \frac{I_{\rm b} L_{\rm ra}}{U_{\rm d}} - \frac{1}{\omega}\arcsin\frac{U_{\rm d}}{\sqrt{U_{\rm d}^2 + Z^2\left(I_0 + I_{\rm b}\right)^2}} \end{aligned} \tag{8}$$

where T_{S1a} denotes the fixed time when S_{1a} is in conducting state in each switching cycle.

According to (8), it can be concluded that T_4 is mainly determined by I_0 varying in sinusoidal waveform when other parameters are constant. When I_0 increases, T_4 also increases.

Mode 5 (t_3–t_4). After S_{1a} is switched OFF at t_3, $C_{\rm ra}$ and $L_{\rm ra}$ work in the resonant state. $L_{\rm ra}$ releases electric energy and $C_{\rm ra}$ absorbs electric energy. When i_{Lra} decreases to zero, u_{Cra} increases to the positive maximum value $U_{\rm p}$ and Mode 5 ends.

$i_{Lra}(t)$, $u_{Cra}(t)$, and $U_{\rm p}$ can be expressed as follows:

$$i_{Lra}(t) = \frac{U_{\rm p}}{Z_0}\cos\left[\omega_0\left(t-t_3\right)\right] \tag{9}$$

$$u_{Cra}(t) = U_{\rm p}\sin\left[\omega_0\left(t-t_3\right)\right] \tag{10}$$

$$U_{\rm p} = Z_0 I_{Lra\,max} = Z_0\sqrt{\left(\frac{U_{\rm d}}{Z}\right)^2 + \left(I_0 + I_{\rm b}\right)^2} - I_0 Z_0 \tag{11}$$

where $Z_0 = \sqrt{L_{\rm ra}/C_{\rm ra}}$ and $\omega_0 = \sqrt{1/(L_{\rm ra}C_{\rm ra})}$.

The duration of this mode can be shown as follows:

$$T_5 = t_4 - t_3 = \frac{\pi}{2\omega_0} \tag{12}$$

Mode 6 (t_4–t_5). No current flows through auxiliary circuits. Meanwhile, the inverter operates in the steady state during this mode.

Mode 7 (t_5–t_6). After S_{2a} is switched ON at t_5, $C_{\rm ra}$ and $L_{\rm ra}$ work in the resonant state. $C_{\rm ra}$ releases electric energy and $L_{\rm ra}$ absorbs electric energy. When u_{Cra} decreases to zero, i_{Lra} increases to the negative maximum value I_{Lramax} and Mode 7 ends.

$i_{Lra}(t)$ and $u_{Cra}(t)$ can be expressed as follows:

$$i_{Lra}(t) = -\frac{U_{\rm P}}{Z_0}\sin\left[\omega_0\left(t-t_5\right)\right] \tag{13}$$

$$u_{Cra}(t) = U_{\rm P}\cos\left[\omega_0\left(t-t_5\right)\right] \tag{14}$$

The duration of this mode can be shown as follows:

$$T_7 = t_6 - t_5 = \frac{\pi}{2\omega_0} \tag{15}$$

Mode 8 (t_6–t_7). After S_{2a} is switched OFF at t_6, $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ work in the resonant state. $C_{\rm r1}$ and $L_{\rm ra}$ release electric energy while $C_{\rm r2}$ absorbs electric energy. When u_{Cr1} decreases to zero, i_{Lra} changes to $-I_{\rm C}$ and Mode 8 ends.

$i_{Lra}(t)$, $u_{Cr1}(t)$, $u_{Cr2}(t)$, and $I_{\rm C}$ can be expressed as follows:

$$i_{Lra}(t) = \left(I_0 - I_{Lramax}\right)\cos\left[\omega\left(t-t_6\right)\right] - I_0 \tag{16}$$

$$u_{Cr1}(t) = Z\left(I_0 - I_{Lramax}\right)\sin\left[\omega\left(t-t_6\right)\right] + U_{\rm d} \tag{17}$$

$$u_{Cr2}(t) = Z\left(I_{Lramax} - I_0\right)\sin\left[\omega\left(t-t_6\right)\right] \tag{18}$$

$$I_{\rm c} = I_0 + \sqrt{\left(I_0 - I_{Lramax}\right)^2 - \left(\frac{U_{\rm d}}{Z}\right)^2} \tag{19}$$

The duration of this mode can be shown as follows:

$$T_8 = t_7 - t_6 = \frac{1}{\omega}\arcsin\frac{U_{\rm d}}{\left(I_{Lramax} - I_0\right)Z} \tag{20}$$

Mode 9 (t_7–t_8). The current starts to flow through D_1 at t_7. At the same time, the resonant state of $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ ends. During this mode, the voltage across $L_{\rm ra}$ is equal to $U_{\rm d}$ and

$L_{\rm ra}$ releases electric energy, leading to the linear decrease of i_{Lra}. When i_{Lra} decreases to $-I_0$, the current flowing through D_1 decreases to zero and Mode 9 ends.

$i_{Lra}(t)$ can be expressed as follows:

$$i_{L_{\rm ra}}(t) = \frac{U_{\rm d}}{L_{\rm ra}}(t - t_7) - I_{\rm c} \tag{21}$$

The duration of this mode can be shown as follows:

$$T_9 = t_8 - t_7 = \frac{(I_{\rm c} - I_0)\, L_{\rm ra}}{U_{\rm d}} \tag{22}$$

Mode 10 (t_8–t_9). After S_1 is switched ON at t_8, i_{Lra} is still in the state of linear decrease. Meanwhile, the current flowing through S_1 is in the state of linear increase. When i_{Lra} decreases to zero, Mode 10 ends.

$i_{Lra}(t)$ can be expressed as follows:

$$i_{Lra}(t) = \frac{U_{\rm d}}{L_{\rm ra}}(t - t_8) - I_0 \tag{23}$$

The duration of this mode can be shown as follows:

$$T_{10} = t_9 - t_8 = \frac{I_0 L_{\rm ra}}{U_{\rm d}} \tag{24}$$

At this point, the working mode analysis of the circuit within a switching cycle ends, and then the circuit returns to Mode 1 and enters the work of the next switching cycle.

C. Design Principles

1) In order to accomplish zero-current turn-ON of S_{1a} and S_{2a} at whole load range, when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$, the maximum current rate of change at the moment when S_{1a} and S_{2a} are switched ON should be no more than the set value $(di/dt)_{\rm r}$. $(di/dt)_{\rm r}$ is less than the rated current rate of change, which switching devices can withstand. The rated current rate of change can be consulted in the technical manual of corresponding switching devices. Specific design principles are as follows:

$$\frac{{\rm d}i_{\rm S_{1a}}}{{\rm d}t}\,|_{t=t_0} = \frac{U_{\rm d}}{L_{\rm ra}} \le \left(\frac{{\rm d}i}{{\rm d}t}\right)_{\rm r} \tag{25}$$

$$\frac{{\rm d}i_{\rm S_{2a}}}{{\rm d}t}\,|_{t=t_5} = \frac{U_{\rm p}}{L_{\rm ra}}\,|_{I_0=-I_{0\max}} \le \left(\frac{{\rm d}i}{{\rm d}t}\right)_{\rm r} \tag{26}$$

where $I_{0\max}$ denotes the maximum value of load current.

In Mode 2, the current i_{S1a} flowing through S_{1a} is equal to i_{Lra}. Therefore, the changing rate of i_{S1a} at the moment (t_0) when S_{1a} is switched ON can be derived on the basis of formula (1). Finally, (25) can be derived. In Mode 7, the current i_{S2a} flowing through S_{2a} is equal to i_{Lra}. Hence, the maximum changing rate of i_{S2a} at the moment (t_5) when S_{2a} is switched ON can be derived on the basis of (13). Finally, (26) can be derived. It should be noted that $U_{\rm p}$ is maximum when I_0 is equal to $-I_{0\max}$.

2) In order to accomplish zero-voltage turn-OFF of S_1, S_{1a}, and S_{2a} at whole load range, when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$, the maximum voltage rate of change at the moment when S_1, S_{1a}, and S_{2a} are switched OFF should be no more than the set value $(du/dt)_{\rm r}$. $(du/dt)_{\rm r}$ is less than the rated voltage rate of change, which switching devices can withstand. The rated voltage rate of change can be consulted in the technical manual of corresponding switching devices. Specific design principles are as follows:

$$\left.\frac{{\rm d}u_{\rm S_1}}{{\rm d}t}\right|_{t=t_1} = \frac{I_0 + I_{\rm b}}{2C_{\rm r1}}\,|_{I_0=I_{0\max}} \le \left(\frac{{\rm d}u}{{\rm d}t}\right)_{\rm r} \tag{27}$$

$$\left.\frac{{\rm d}u_{\rm S_{1a}}}{{\rm d}t}\right|_{t=t_3} = U_{\rm p}\omega_0\,|_{I_0=-I_{0\max}} \le \left(\frac{{\rm d}u}{{\rm d}t}\right)_{\rm r} \tag{28}$$

$$\left.\frac{{\rm d}u_{\rm S_{2a}}}{{\rm d}t}\right|_{t=t_6} = \frac{I_{L\rm ramax} - I_0}{2C_{\rm r2}}\,|_{I_0=-I_{0\max}} \le \left(\frac{{\rm d}u}{{\rm d}t}\right)_{\rm r} \tag{29}$$

where $I_{0\max}$ denotes the maximum value of load current.

In Mode 3, the voltage u_{S1} across S_1 is equal to u_{Cr1}. Therefore, the maximum changing rate of u_{S1} at the moment (t_1) when S_1 is switched OFF can be derived on the basis of (4). Finally, (27) can be derived. In Mode 5, the voltage u_{S1a} across S_{1a} is equal to u_{Cra}. Hence, the maximum changing rate of u_{S1a} at the moment (t_3) when S_{1a} is switched OFF can be derived on the basis of (10). Finally, (28) can be derived. In Mode 8, the voltage u_{S2a} across S_{2a} is equal to u_{Cr2}. Hence, the maximum changing rate of u_{S2a} at the moment (t_6) when S_{2a} is switched OFF can be derived on the basis of formula (18). Finally, (29) can be derived. It should be noted that $I_{L\rm ramax}$–I_0 is maximum when I_0 is equal to $-I_{0\max}$.

In addition, in order to accomplish zero-voltage turn-OFF of S_{1a} at whole load range, gate pulse of S_{1a} should become low level after u_{Cr2} decrease to zero in Mode 3. If gate pulse of S_{1a} becomes low level before u_{Cr2} decrease to zero in Mode 3, u_{S1a} will suddenly rise to u_{Cr2} during turn-OFF transient, resulting in the failure of zero-voltage turn-OFF of S_{1a}. Therefore, when the duration of conduction state of S_{1a} is no less than the maximum sum of T_2 and T_3 in every switching cycle, zero-voltage turn-OFF of S_{1a} will come true at whole load range. Because maximum T_3 is less than $\pi/(2\omega)$ according to (7), the duration of conduction state of S_{1a} can be equal to the sum of T_2 and $\pi/(2\omega)$.

Besides, in order to accomplish zero-voltage turn-OFF of S_{2a} at whole load range, gate pulse of S_{2a} should become low level when u_{Cra} decrease to zero at the end of Mode 7. If gate pulse of S_{2a} becomes low level before u_{Cra} decrease to zero in Mode 7, u_{S2a} will suddenly rise to u_{Cra} during turn-OFF transient, resulting in the failure of zero-voltage turn-OFF of S_{2a}. Therefore, when the duration of conduction state of S_{2a} is equal to T_7 in every switching cycle, zero-voltage turn-OFF of S_{2a} will come true at whole load range.

Above all, the duration of conduction state of S_{1a} and S_{2a} can be constant in every switching cycle and independent of instantaneous value of load current. The duty cycle of gate pulse of S_{1a} and S_{2a} is as follows:

$$\rho_{\rm S1a} = \frac{1}{T}\left(\frac{I_{\rm b} L_{\rm ra}}{U_{\rm d}} + \frac{\pi}{2\omega}\right) \tag{30}$$

$$\rho_{\rm S2a} = \frac{\pi}{2\omega_0 T} \tag{31}$$

Because the duty cycle of gate pulse of S_{1a} and S_{2a} must be less than one and the maximum ballpark dead time ratio can be set at B, the allowable range of switching frequency $f_{\rm c}$ satisfying

design principles is demonstrated as follows:

$$f_{\rm c} < \min\left\{\frac{1}{\frac{I_{\rm b}L_{\rm ra}}{U_{\rm d}}+\frac{\pi}{2\omega}}, \frac{1}{\frac{\pi}{2\omega_0}}, \frac{1}{2\Delta/{\rm B}}\right\} \tag{32}$$

where Δ means the dead time of the inverter.

3) In order to accomplish zero-voltage turn-ON of S_2 at whole load range, u_{Cr2} must reduce to zero before gate pulse of S_2 becomes high level. Therefore, when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$, the maximum duration of Mode 3 should be no more than Δ. Based on the above explanations, the following can be derived:

$$T_3\,|_{I_0=-I_{0\max}} \le \Delta \tag{33}$$

It should be noted that T_3 is maximum when I_0 is equal to $-I_{0\max}$. According to (7), the maximum value of T_3 must be less than $\pi/(2\omega)$. Therefore, if the following is satisfied, (33) will also be satisfied:

$$\pi/(2\omega) \le \Delta \tag{34}$$

When (34) is satisfied, zero-voltage turn-ON of S_2 can be accomplished at whole load range.

4) In order to accomplish zero-voltage turn-ON of S_1 at whole load range, the following three conditions should be satisfied.

First, according to Fig. 4(h), $I_{L\mathrm{ramax}}$, which is the value of the current flowing through $L_{\rm ra}$ at the beginning of Mode 8, must be more than $I_{0\max}$ in order that the resonance can happen normally when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$. Based on (6), it can be concluded that $I_{L\mathrm{ramax}}$ will be more than $I_{0\max}$ when the following is satisfied:

$$I_{\rm b} \ge I_{0\,\max} \tag{35}$$

Second, u_{Cr1} must decrease to zero before gate pulse of S_1 becomes high level. Therefore, when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$, the maximum duration of Mode 8 should be no more than dead time Δ of the inverter. Based on the above explanations, the following can be derived

$$T_8\,|_{I_0=I_{0\max}} \le \Delta. \tag{36}$$

It should be noted that T_8 is maximum when I_0 is equal to $I_{0\max}$. According to (20), the maximum value of T_8 must be less than $\pi/(2\omega)$. Therefore, if (34) is satisfied, (36) will also be satisfied.

Third, gate pulse of S_1 must become high level before the current flowing through D_1 decreases to zero in Mode 9. If gate pulse of S_1 does not become high level before no current flows through D_1 in Mode 9, resonance will happen again at the end of Mode 9 so that u_{Cr1} starts to increase, which leads to the failure of zero-voltage turn-ON of S_1. Therefore, when I_0 is in the range of $-I_{0\max}$ to $I_{0\max}$, the minimum sum of T_8 and T_9 should be no less than dead time Δ of the inverter. Hence, (37) can be derived as follows:

$$\Delta \le \min\{T_8 + T_9\}. \tag{37}$$

Because the minimum sum of T_8 and T_9 is no less than the sum of minimum T_8 and minimum T_9, the following can be substituted for (37):

$$\Delta \le T_8\,|_{I_0=-I_{0\,\max}} + T_9\,|_{I_0=I_{0\max}}\,. \tag{38}$$

It should be noted that T_8 is minimum when I_0 is equal to $-I_{0\max}$ and T_9 is minimum when I_0 is equal to $I_{0\max}$. Therefore, if (38) is satisfied, (37) will also be satisfied.

In summary, when (34), (35) and (38) are satisfied, zero-voltage turn-ON of S_1 can be accomplished at whole load range.

5) To ensure that the switching devices and diodes are not damaged at whole load range, the maximum value of resonant current, $I_{L\mathrm{ramax}}$, should not exceed the maximum allowable current value of the switching devices and diodes, $I_{\rm Dmax}$. Besides, at whole load range, the maximum value of i_{S1} at the end of Mode 2 is equal to $I_{0\max}+I_{\rm b}$, which should also be no more than $I_{\rm Dmax}$. It should be noted that $I_{L\mathrm{ramax}}$ is maximum when I_0 is equal to $-I_{0\max}$. Hence, design principles are as follows:

$$\left(\sqrt{\left(\frac{U_{\rm d}}{Z}\right)^2 + (I_0+I_{\rm b})^2} - I_0\right)|_{I_0=-I_{0\,\max}} \le I_{\rm Dmax} \tag{39}$$

$$I_{0\,\max} + I_{\rm b} \le I_{\rm D\,max}. \tag{40}$$

In summary, soft-switching can be achieved at whole load range when the above design principles are all satisfied. Soft-switching will still be maintained in no-load condition. However, the realization of soft-switching in no-load condition will lead to the penalty that the loss of the auxiliary circuits is more than the reduced switching loss of main switches. The penalty is adverse to the improvement of the efficiency at light load, resulting in lower efficiency compared with the hard-switching inverter. In other words, the penalty restricts the range of output power in which the efficiency can be improved by soft-switching. In addition, because the voltage across the capacitors in parallel with main switches is required to complete change in dead time, enough dead time is needed to achieve soft-switching. Moreover, the larger values of $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ is often required to reduce *di/dt* during turn-ON transient and *du/dt* during turn-OFF transient, which is beneficial to reducing switching loss effectively. However, the larger values of $C_{\rm r1}$, $C_{\rm r2}$, and $L_{\rm ra}$ can bring about more dead time according to (34). More dead time may reduce the allowable range of switching frequency according to (32), which will make against the application of the novel inverter in the field of very high switching frequency. In summary, more dead time, which is mandatory for obtaining the soft-switching, can result in a problem that the novel inverter is not suitable for very high switching frequency applications. The problem needs to be solved in future studies.

D. Maximum Voltage and Current of the Components in the Inverter

The maximum voltage across each component is no more than $U_{\rm d}$.

The maximum current flowing through $L_{\rm ra}$, $D_{1\rm a}$, $D_{2\rm a}$, $S_{1\rm a}$, and $S_{2\rm a}$ can be indicated as follows:

$$i_{L_{\rm ramax}} = i_{D_{1\rm amax}} = i_{D_{2\rm amax}} = i_{S_{1\rm amax}}$$

$$= i_{S_{2\mathrm{amax}}} = \left(\sqrt{\left(\frac{U_\mathrm{d}}{Z}\right)^2 + (I_0 + I_\mathrm{b})^2} - I_0 \right) |_{I_0 = -I_{0\max}} \tag{41}$$

The maximum current flowing through D_1 and D_2 can be indicated as follows:

$$i_{D_{1\max}} = (I_\mathrm{c} - I_0)\,|_{I_0 = -I_{0\max}} \tag{42}$$

$$i_{D_{2\max}} = (I_{L\mathrm{ramax}} + I_0)\,|_{I_0 = I_{0\max}}\ . \tag{43}$$

The maximum current flowing through S_1 can be indicated as follows:

$$i_{S_{1\max}} = (I_0 + I_\mathrm{b})\,|_{I_0 = I_{0\max}}\ . \tag{44}$$

It should be noted that $i_{S1\max}$ will be more than $2I_{0\max}$ at whole load range according to (35) and (44). Hence, the main switching device that can withstand high current should be selected in the inverter. Furthermore, the high current flowing through the main switching device can result in more conduction loss of the main switching device with the increase of the output power, which makes against the improvement of the efficiency in the field of high power. The inadequacy still needs further improvement in the future work. Hence, the presented inverter is more suitable for small and medium power applications on account of the inadequacy.

III. Theoretical Expression on the Power Loss of the Auxiliary Circuit

$S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ operate in the soft-switching state, and the switching loss can be considered to be zero. However, when the current flows through the devices, conduction loss will exist in the devices. The voltage across the switching device, which is in the conduction state, is labeled as V_{CE}. The voltage across the diode, which is in the conduction state, is labeled as V_{EC}. The switching frequency is labeled as f_c. The internal resistances of C_{ra}, C_{r1}, C_{r2}, and L_{ra} are labeled as $R_{C\mathrm{ra}}$, $R_{C\mathrm{r1}}$, $R_{C\mathrm{r2}}$, and $R_{L\mathrm{ra}}$, respectively.

The calculation formulas of the loss existing in $S_{1\mathrm{a}}$, $S_{2\mathrm{a}}$, $D_{1\mathrm{a}}$, $D_{2\mathrm{a}}$, C_{ra}, C_{r1}, C_{r2}, and L_{ra} are shown, respectively, as follows:

$$P_{\mathrm{S1a}} = V_{\mathrm{CE}} \left[\int_{t_0}^{t_1} i_{L\mathrm{ra}}(t)\mathrm{d}t + \int_{t_1}^{t_2} i_{L\mathrm{ra}}(t)\mathrm{d}t \right] f_\mathrm{c} \tag{45}$$

$$P_{\mathrm{S2a}} = -V_{\mathrm{CE}} \left[\int_{t_5}^{t_6} i_{L\mathrm{ra}}(t)\mathrm{d}t \right] f_\mathrm{c} \tag{46}$$

$$P_{\mathrm{D1a}} = V_{\mathrm{CE}} \left[\int_{t_3}^{t_4} i_{L\mathrm{ra}}(t)\mathrm{d}t \right] f_\mathrm{c} \tag{47}$$

$$P_{\mathrm{D2a}} = -V_{\mathrm{EC}} \left[\int_{t_6}^{t_7} i_{L\mathrm{ra}}(t)\mathrm{d}t + \int_{t_7}^{t_8} i_{L\mathrm{ra}}(t)\mathrm{d}t + \int_{t_8}^{t_9} i_{L\mathrm{ra}}(t)\mathrm{d}t \right] f_\mathrm{c} \tag{48}$$

$$P_{C\mathrm{ra}} = f_\mathrm{c} \left[\int_{t_3}^{t_4} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_5}^{t_6} i_{L\mathrm{ra}}^2(t)\mathrm{d}t \right] R_{C\mathrm{ra}} \tag{49}$$

$$P_{C\mathrm{r1}} = f_\mathrm{c} \left[\int_{t_1}^{t_2} \left(\frac{i_{L\mathrm{ra}}(t) + I_0}{2} \right)^2 \mathrm{d}t + \int_{t_6}^{t_7} \left[\left(\frac{i_{L\mathrm{ra}}(t) + I_0}{2} \right) \right]^2 \mathrm{d}t \right] R_{C\mathrm{r1}} \tag{50}$$

$$P_{C\mathrm{r2}} = f_\mathrm{c} \left[\int_{t_1}^{t_2} \left(\frac{i_{L\mathrm{ra}}(t) + I_0}{2} \right)^2 \mathrm{d}t + \int_{t_6}^{t_7} \left[\left(\frac{i_{L\mathrm{ra}}(t) + I_0}{2} \right) \right]^2 \mathrm{d}t \right] R_{C\mathrm{r2}} \tag{51}$$

$$P_{L\mathrm{ra}} = f_\mathrm{c} \left[\int_{t_0}^{t_1} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_1}^{t_2} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_3}^{t_4} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_5}^{t_6} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_6}^{t_7} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_7}^{t_8} i_{L\mathrm{ra}}^2(t)\mathrm{d}t + \int_{t_8}^{t_9} i_{L\mathrm{ra}}^2(t)\mathrm{d}t \right] R_{L\mathrm{ra}}. \tag{52}$$

To simplify calculation, I_0 in the above formulas can be equal to the effective value of the load current.

The calculation formula of the power loss existing in the three-phase auxiliary circuits is shown as follows:

$$P_{\mathrm{add}} = 3(P_{\mathrm{S1a}} + P_{\mathrm{S2a}} + P_{\mathrm{D1a}} + P_{\mathrm{D2a}} + P_{L\mathrm{ra}} + P_{C\mathrm{ra}} + P_{C\mathrm{r1}} + P_{C\mathrm{r2}}). \tag{53}$$

IV. Specific Parameter Design

The general design idea is as follows. First, the numerical value of L_{ra} can be obtained on the basis of (25). Second, the numerical value of C_{r2} can be obtained on the basis of (34) and the obtained numerical value of L_{ra}. Third, the numerical value of I_b can be obtained on the basis of (35), (38), and the obtained numerical values of L_{ra} and C_{r2}. Fourth, the numerical value of C_{r1} can be obtained on the basis of (27) and the obtained numerical value of I_b. Fifth, the numerical value of C_{ra} can be obtained on the basis of (26) and the obtained numerical values of L_{ra}, C_{r2}, and I_b. Sixth, the duty cycles of gate pulses of $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$, including the allowable range of switching frequency, are calculated on the basis of the obtained numerical values of parameters. Seventh, the obtained numerical values of parameters are plugged into (28) and (29) to verify whether the obtained numerical values can satisfy the conditions of zero-voltage turn OFF of auxiliary switches. Eighth, the numerical values of the maximum current flowing through each device at whole load range are calculated on the basis of (41)–(44) to offer reasons for choice in devices.

The known parameters are as follows: $P_0 = 3$ kW, $U_\mathrm{d} = 300$ V, $(di/dt)_\mathrm{r} = 15$ A/μs, $(du/dt)_\mathrm{r} = 2000$ V/μs, $f_c = 20$ kHz, $T = 50$ μs, $\Delta = 1.2$ μs, $I_{0\max} = 13$ A, and $B = 10\%$.

Specific Design Process

1) For the realization of zero-current turn ON of $S_{1\mathrm{a}}$ at whole load range, the range of L_{ra} shown by following can be

derived according to (25):

$$L_{\mathrm{ra}} \geq 15\ \mu\mathrm{H}. \tag{54}$$

On account of manufacturing tolerances and temperature change, $L_{\mathrm{ra}} = 20\ \mu$H is selected in fact.

2) For the realization of zero-voltage turn ON of S_1 and S_2 at whole load range, the range of C_{r2} shown by the following can be derived according to formula (34) where $L_{\mathrm{ra}} = 20\ \mu$H:

$$C_{\mathrm{r2}} \leq 0.0146\ \mu\mathrm{F}. \tag{55}$$

On account of manufacturing tolerances and temperature change, $C_{\mathrm{r2}} = 0.01\ \mu$F is selected in fact.

3) For the realization of zero-voltage turn ON of S_1 at whole load range, the range of I_{b} shown by the following can be derived according to formula (38) where $L_{\mathrm{ra}} = 20\ \mu$H and $C_{\mathrm{r2}} = 0.01\ \mu$F:

$$I_{\mathrm{b}} \geq 18\ \mathrm{A} \tag{56}$$

Meanwhile, (56) can satisfy (35). On account of current margin, $I_{\mathrm{b}} = 22$ A is selected in fact.

4) For the realization of zero-voltage turn OFF of S_1 at whole load range, the range of C_{r2} shown by the following can be derived according to formula (27) where $I_{\mathrm{b}} = 22$ A:

$$C_{\mathrm{r1}} \geq 0.0097\ \mu\mathrm{F}. \tag{57}$$

Hence, $C_{\mathrm{r1}} = C_{\mathrm{r2}} = 0.01\ \mu$F can satisfy (55) and (57).

5) For the realization of zero-current turn ON of $S_{2\mathrm{a}}$ at whole load range, the range of C_{ra} shown by the following can be derived according to formula (26) where $L_{\mathrm{ra}} = 20\ \mu$H, $C_{\mathrm{r2}} = 0.01\ \mu$F, and $I_{\mathrm{b}} = 22$ A:

$$C_{\mathrm{ra}} \geq 0.1275\ \mu\mathrm{F}. \tag{58}$$

On account of manufacturing tolerances and temperature change, $C_{\mathrm{ra}} = 0.15\ \mu$F is selected in fact.

6) For the realization of zero-voltage turn OFF of $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ at whole load range, $U_{\mathrm{d}} = 300$ V, $T = 50\ \mu$s, $L_{\mathrm{ra}} = 20\ \mu$H, $C_{\mathrm{r2}} = 0.01\ \mu$F, $C_{\mathrm{ra}} = 0.15\ \mu$F, and $I_{\mathrm{b}} = 22$ A are plugged into (30) and (31) to calculate the duty cycle of gate pulse of $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$

$$\rho_{S1\mathrm{a}} = \frac{1}{T}\left(\frac{I_{\mathrm{b}} L_{\mathrm{ra}}}{U_{\mathrm{d}}} + \frac{\pi}{2\omega}\right) = 0.049 \tag{59}$$

$$\rho_{S2\mathrm{a}} = \frac{\pi}{2\omega_0 T} = 0.054. \tag{60}$$

According to (32), the allowable range of switching frequency f_c satisfying design principles is demonstrated as follows:

$$f_c < 41.6\ \mathrm{kHz}. \tag{61}$$

Hence, $f_c = 20$ kHz satisfies design principles.

7) To verify whether $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ accomplish zero-voltage turn OFF at whole load range, $L_{\mathrm{ra}} = 20\ \mu$H, $C_{\mathrm{ra}} = 0.15\ \mu$F, $I_{\mathrm{b}} = 22$ A, $C_{\mathrm{r2}} = 0.01\ \mu$F, and $U_{\mathrm{d}} = 300$ V are plugged into (28) and (29). The following formulas can be derived:

$$\left.\frac{\mathrm{d}u_{\mathrm{S_{1a}}}}{\mathrm{d}t}\right|_{t=t_3} = U_{\mathrm{P}}\omega_0\,|_{I_0=-I_{0\max}} = 173.84\mathrm{V}/\mu\mathrm{s} \leq \left(\frac{\mathrm{d}u}{\mathrm{d}t}\right)_{\mathrm{r}} \tag{62}$$

$$\left.\frac{du_{\mathrm{S_{2a}}}}{dt}\right|_{t=t_6} = \frac{I_{L\mathrm{ramax}} - I_0}{2C_{\mathrm{r2}}}\,|_{I_0=-I_{0\max}} = 1953.8\ \mathrm{V}/\mu\mathrm{s} \leq \left(\frac{du}{dt}\right)_{\mathrm{r}}. \tag{63}$$

According to (62) and (63), it can be concluded that $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ can accomplish zero-voltage turn OFF at whole load range.

8) The maximum current flowing through devices at whole load range should be calculated to provide the basis for the selection of devices. The above-mentioned parameters are plugged into (41)–(44) and the following formulas can be derived:

$$i_{L_{\mathrm{ra}\max}} = i_{D_{1\mathrm{amax}}} = i_{D_{2\mathrm{amax}}} = i_{S_{1\mathrm{amax}}} = i_{S_{2\mathrm{amax}}} = \left(\sqrt{\left(\frac{U_{\mathrm{d}}}{Z}\right)^2 + (I_0 + I_{\mathrm{b}})^2} - I_0\right)|_{I_0=-I_{0\max}} = 26.08\ \mathrm{A} \tag{64}$$

$$i_{D_{1\max}} = (I_{\mathrm{c}} - I_0)\,|_{I_0=-I_{0\max}} = 37.9\ \mathrm{A} \tag{65}$$

$$i_{D_{2\max}} = (I_{L\mathrm{ramax}} + I_0)\,|_{I_0=I_{0\max}} = 36.26\ \mathrm{A} \tag{66}$$

$$i_{S_{1\max}} = (I_0 + I_{\mathrm{b}})\,|_{I_0=I_{0\max}} = 35\ \mathrm{A}. \tag{67}$$

According the above formulas, the rated current of the switching device and fast soft recovery diode we should select can be equal to 50 A. Hence, the model number of the main switching devices (S_1–S_6) is 1MBH50D-060, which include antiparallel freewheeling diodes (D_1–D_6). The model number of the auxiliary switching devices ($S_{1\mathrm{a}}$–$S_{6\mathrm{a}}$) is 1MBH50-060, which does not include antiparallel freewheeling diodes. The model number of fast soft recovery diode ($D_{1\mathrm{a}}$–$D_{6\mathrm{a}}$) is RHRG5060. The rated voltage and current of the above models are equal to 600 V and 50 A, corresponding to the fifth item in the design principles.

In summary, the above-mentioned parameters can make the switching devices accomplish soft-switching when I_0 is in the range of –13 to 13 A. In other words, soft-switching can be obtained at whole load range.

V. Experimental Verification

The novel three-phase experimental prototype is developed according to the main circuit shown in Fig. 1. Fig. 6 exhibits the image of the prototype. The parameters and devices of the prototype are shown in Table I. It should be noted that the size of the auxiliary circuit is comparable with the size of the three-phase inverter circuit in Fig. 6. Although the large size of the auxiliary circuit can lead to the sacrifice of the power density and the auxiliary circuit can also result in additional loss, the efficiency of the inverter can be improved when switching loss, which is reduced by soft-switching, is more than the additional loss caused by the auxiliary circuit. From the perspective of long-term operation of the inverter, economic benefits can be produced when the saved electricity cost caused by the improvement of the efficiency is more than the cost of the auxiliary

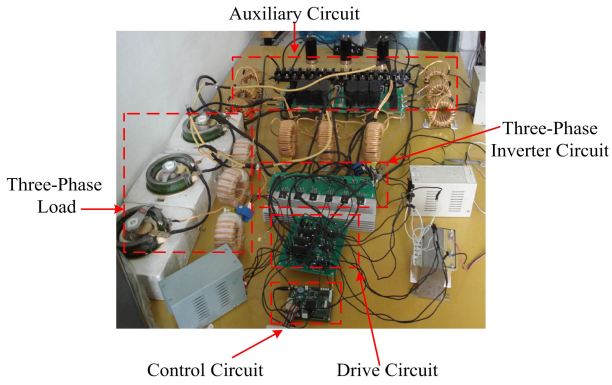

Fig. 6. Photograph of a three-phase experimental prototype.

TABLE I
PARAMETERS AND DEVICES OF THE PROTOTYPE

Components	Parameters
Control board	DSP TMS320F2812
Driving chip	EXB841
Rated output power(P_0)	3kW
DC power supply (U_d)	300V
Maximum load current (I_{0max})	13A
Switching frequency (f_c)	20kHz
Output frequency (f_0)	50Hz
Dead time(Δ)	1.2μs
The duty cycle of trigger pulse of S_{1a}, S_{3a}, S_{5a} (ρ_{S1a}, ρ_{S3a}, ρ_{S5a})	0.049
The duty cycle of trigger pulse of S_{2a}, S_{4a}, S_{6a} (ρ_{S2a}, ρ_{S4a}, ρ_{S6a})	0.054
S_1~S_6	1MBH50D-060 (600V, 50A)
S_{1a}~S_{6a}	1MBH50-060 (600V, 50A)
D_{1a}~D_{6a}	RHRG5060(600V, 50A)
C_{r1}~C_{r6}	0.01μF
C_{ra}~C_{rc}	0.15μF
L_{ra}~L_{rc}	20μH
Load inductor L_a, L_b and L_c	0.8mH
Load resistance R_a, R_b and R_c	11Ω

circuit. Therefore, it is worthwhile to achieve soft-switching at the cost of adding auxiliary circuits. However, the size of the auxiliary circuit still needs further optimization for the promotion and application of soft-switching inverters.

The experimental waveforms are exhibited in Fig. 7. The positive direction of voltage and current in Fig. 7 is consistent with the annotation in Fig. 2. Fig. 7(a) exhibits the waveforms of u_{Cr1}, u_{Cr2}, and i_{Lra} in a switching cycle. It can be seen that the experimental waveforms are basically consistent with the variation trend of theoretical waveforms exhibited in Fig. 3. The waveforms of u_{S1} and i_{S1} at the switching moment of S_1 under full load, light load, and no load are exhibited, respectively, in Fig. 7(b)–(d). It can be seen that u_{S1} increases at a relatively low rate when S_1 is switched to OFF-state so that zero-voltage turn-OFF of S_1 comes true under full load, light load, and no load. It can also be seen that u_{S1} has changed to zero before i_{S1} increases from zero so that zero-voltage turn-ON of S_1 comes true under full load, light load, and no load. Fig. 7(e) and (f) exhibits the experimental waveforms of u_{S1a}, i_{S1a}, u_{S2a}, and i_{S2a} at the switching moments of S_{1a} and S_{2a}. It can be seen that i_{S1a} and i_{S2a} increase at a relatively low rate so that zero-current turn-ON of S_{1a} and S_{2a} comes true. It can also be seen that u_{S1a} and u_{S2a} increase at a relatively low rate when S_{1a} and S_{2a} are switched to OFF-state so that zero-voltage turn-OFF of S_{1a} and S_{2a} comes true. Fig. 7(g) and (h) exhibits the experimental waveforms of the output line voltage and the output phase current of the prototype under the condition that the output frequency is equal to 50 Hz. It can be seen that the output three-phase current waveforms have no significant distortion and the inverter is in the stable operation. Fig. 7(i) exhibits the dynamic experimental waveforms of the output phase current when output power reduces from 3 to 1.5 kW. Fig. 7(j) exhibits the dynamic experimental waveforms of the output phase current when U_d reduces from 300 to 150 V. Fig. 7(i) and (j) exhibits that the dynamic change of the output phase current, caused by the change of output power and dc supply voltage, is relatively stable. Hence, auxiliary circuits on the bridge arms have no significant adverse effect on the dynamic response of the inverter.

For verification of better performance of this new topology in terms of total harmonic distortion (THD) and efficiency, we have made another four prototypes including a three-phase hard-switching inverter and three-phase soft-switching inverters in [7], [8], and [12]. The rated power of them is also equal to 3 kW. For a fair comparison among five different prototypes, the model number of the main switching devices in the three-phase inverter circuits of all the prototypes is 1MBH50D-060; the model number of the switching devices and diodes in the auxiliary circuits of all the soft-switching prototypes is 1MBH50-060 and RHRG5060, respectively; in terms of numerical values and material, resonant inductors, resonant capacitors, load resistance, and load inductor in each soft-switching prototype are the same to each other, respectively; and the sizes of an auxiliary circuit and a three-phase inverter circuit in each prototype are also the same to each other, respectively. Although the numerical values of resonant inductors and resonant capacitors in each soft-switching inverter are the same to each other, they all satisfy respective design principle. Bipolar SPWM is used as the control method in each prototype. In summary, the consistency of hardware selection and a control method in different prototypes can make for a fair comparison in the experiment to verify that the simple structure of auxiliary circuits is in favor of the improvement of the performance.

Fig. 8 exhibits the THD contrast of A-phase current. In the THD experiment, each prototype works in the same condition including $U_d = 300$ V, $\Delta = 1.2$ μs, and $P_0 = 3$ kW. Furthermore, dead-time compensation is not used in the software of each prototype. Besides, the filter is not added at the output of each prototype. Output frequency in each prototype can be changed by adjusting the frequency of a reference sine wave in SPWM. When output frequency is equal to 20, 30, 40, 50, and 60 Hz, the THD of A-phase current in each prototype can be obtained. As exhibited in Fig. 8, when output frequency is in the range of 20–60 Hz, the THD of A-phase current in the novel inverter of this article is lower than that in other resonant pole inverters and the THD of A-phase current in the hard-switching inverter is higher than that of other resonant pole inverters. Compared

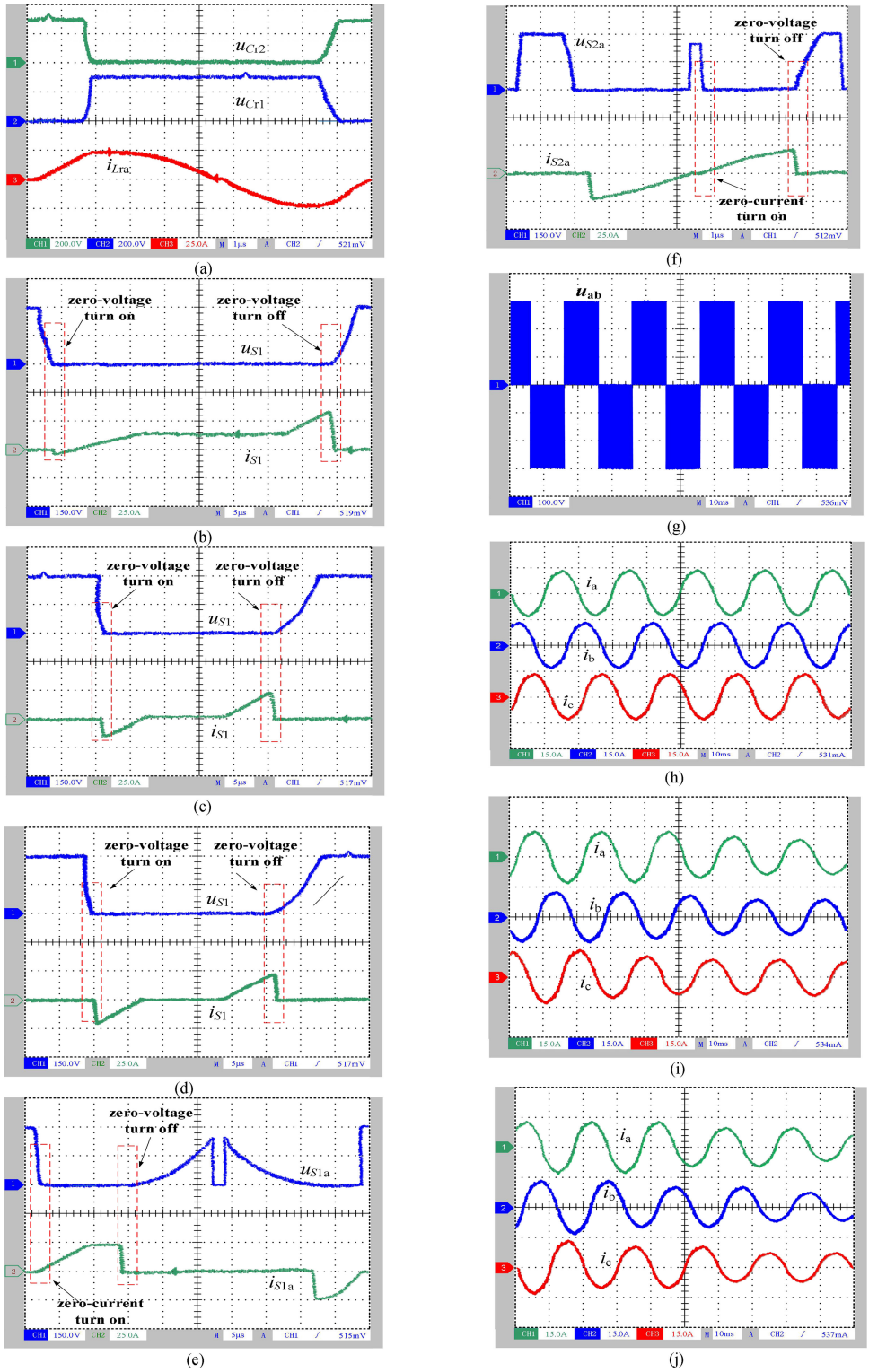

Fig. 7. Experimental waveforms. (a) Waveforms of the resonant current i_{Lra}, the resonant voltage u_{Cr1} and u_{Cr2} (scales: 200 V/div, 25 A/div, 1 μs/div). (b) Waveforms of the terminal voltage u_{S1} and the current i_{S1} when the main switch S_1 is switched (at full load, $I_0 = 13$ A during the exhibited switching cycle) (scales: 150 V/div, 25 A/div, 5 μs/div). (c) Waveforms of the terminal voltage u_{S1} and the current i_{S1} when the main switch S_1 is switched (at light load, $I_0 = 3$ A during the exhibited switching cycle) (scales: 150 V/div, 25 A/div, 5 μs/div). (d) Waveforms of the terminal voltage u_{S1} and the current i_{S1} when the main switch S_1 is switched (at no load, $I_0 = 0$ A during the exhibited switching cycle) (scales: 150 V/div, 25 A/div, 5 μs/div). (e) Waveforms of the terminal voltage u_{S1a} and the current i_{S1a} when the auxiliary switch S_{1a} is switched (scales: 150 V/div, 25 A/div, 5 μs/div). (f) Waveforms of the terminal voltage u_{S2a} and the current i_{S2a} when the auxiliary switch S_{2a} is switched (scales: 150 V/div, 25 A/div, 5 μs/div). (g) Waveforms of output line voltage u_{ab} of the inverter (scales: 100 V/div, 10 ms/div). (h) Waveforms of phase currents i_a, i_b, and i_c flowing through the three-phase load of the inverter (scales: 15 A/div, 10 ms/div). (i) Dynamic waveforms of phase currents i_a, i_b, and i_c flowing through the three-phase load of the inverter when output power reduces from 3 to 1.5 kW (scales: 15 A/div, 10 ms/div). (j) dynamic waveforms of phase currents i_a, i_b, and i_c flowing through the three-phase load of the inverter when U_d reduces from 300 to 150 V(scales: 15 A/div, 10 ms/div).

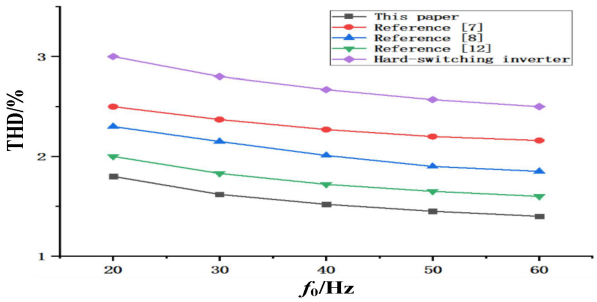

Fig. 8. Curve of the changing relationship between output frequency and THD of A-phase current in different inverters.

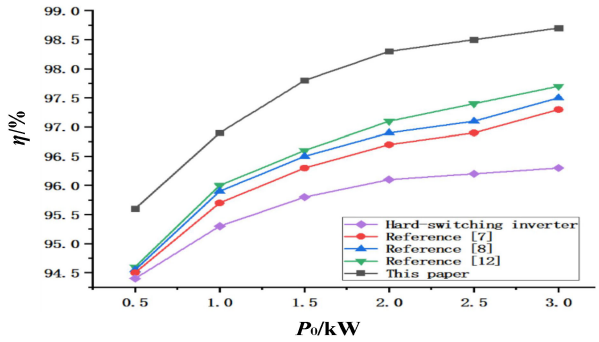

Fig. 9. Curve of the changing relationship between efficiency and output power when output power is in the range of 0.5–3 kW.

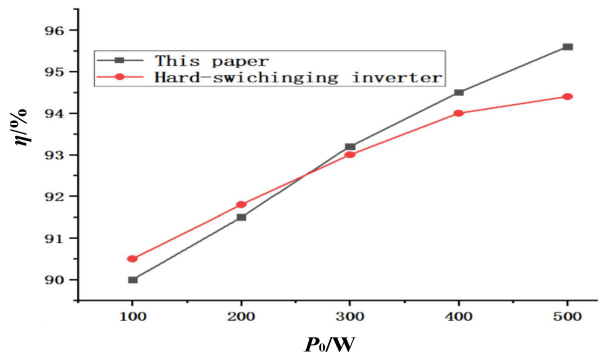

Fig. 10. Curve of the changing relationship between efficiency and output power when the output power is in the range of 100–500 W.

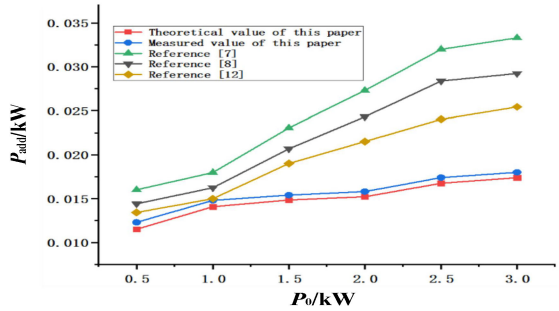

Fig. 11. Curve of the changing relationship between auxiliary circuit loss and output power.

with the hard-switching inverter, dc power supply and passive energy storage devices in the resonant pole inverters provide electric energy to the load in the dead time, which can make for the improvement of THD. Furthermore, compared with other three resonant pole inverters, the simple structure of auxiliary circuits in the new inverter brings about the lower loss of the auxiliary devices and more efficient power transmission in the dead time, which can bring about the further improvement of THD. Compared than other resonant pole inverters, dc power supply in the hard-switching inverter cannot provide electric energy to the load in the dead time, leading to the higher THD. Moreover, it can be concluded from Fig. 8 that the THD of A-phase current increases with the decrease in output frequency when the output frequency is in the range of 20–60 Hz. In addition, the conclusion obtained from Fig. 8 that the THD of A-phase current in the hard-switching inverter is higher in lower output frequency is also the same as that obtained from [12, Fig. 12(f)].

Fig. 9 exhibits the efficiency test results of each inverter when output power is in the range of 0.5–3 kW. In the experiment, the power analyzer is used to measure efficiency and power loss; output power can be changed by adjusting modulation depth in SPWM. Each inverter works under the same experimental conditions, including $U_{\rm d} = 300$ V and the same output power. When the output power changes to the rated power 3 kW, the efficiency test result of the novel inverter in this article is equal to 98.7%, which is more than the efficiency of other inverters. The efficiency test results confirm the efficiency superiority of the novel inverter.

Fig. 10 exhibits the efficiency test results of the hard-switching inverter and the novel inverter in this article when output power is in the range of 100–500 W. As indicated in Fig. 10, when the output power is less than 300 W, the efficiency of the novel inverter will start to be lower than that of the hard-switching inverter. Although soft-switching can still be achieved when the output power is in the range of 0–300 W, the total loss of auxiliary circuits in the novel inverter will be more than the reduced switching loss of main switches, leading to the failure of the improvement of the efficiency at light load. Therefore, in view of the problem, auxiliary circuits may stop working at light load that the output power is less than 300 W to avoid the disadvantage in efficiency at light load.

The changing curve of the auxiliary circuit loss $P_{\rm add}$ at different output powers is shown in Fig. 11. In Fig. 11, when output power is 3 kW, the auxiliary circuit loss of the topology designed in this article is significantly lower than that of other inverters. According to formula (53), the theoretical value of the auxiliary circuit loss is obtained. The theoretical value is a little lower than the measured value for the reason that the actual line loss is not contained in the theoretical calculation. Fig. 11 implies that the theoretical calculation is effective.

Fig. 12 exhibits the power loss distribution of soft-switching inverters in [7], [8], and [12], and the novel inverter in this article

TABLE II
NUMBER OF SWITCH AND SOFT-SWITCHING ACTION AND STRESS

Number of switch	[7]		[8]		[12]		This paper	
Auxiliary switch	12		12		0		6	
Auxiliary Diode	30		18		12		6	
Resonant capacitor	18		12		6		9	
Resonant inductor	12		6		15		3	
Soft switching	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off
Main switch	ZVS	Pseudo ZVS	ZVS	Pseudo ZVS	Pseudo ZCS	Pseudo ZVS	ZVS	Pseudo ZVS
Auxiliary switch	Pseudo ZCS	Pseudo ZVS	Pseudo ZCS	Pseudo ZVS	------	-----	Pseudo ZCS	Pseudo ZVS
Stress	Voltage	Current	Voltage	Current	Voltage	Current	Voltage	Current
Main switch	U_d	I_{omax}	U_d	I_{omax}	$5U_d/3$	$I_{omax}+I_{res}$	U_d	$I_{omax}+I_{res}$
Auxiliary switch	U_d	$I_{omax}+I_{res}$	U_d	$I_{omax}+I_{res}$	------	-----	U_d	$I_{omax}+I_{res}$

Note: I_{res} stands for the additional resonant current.

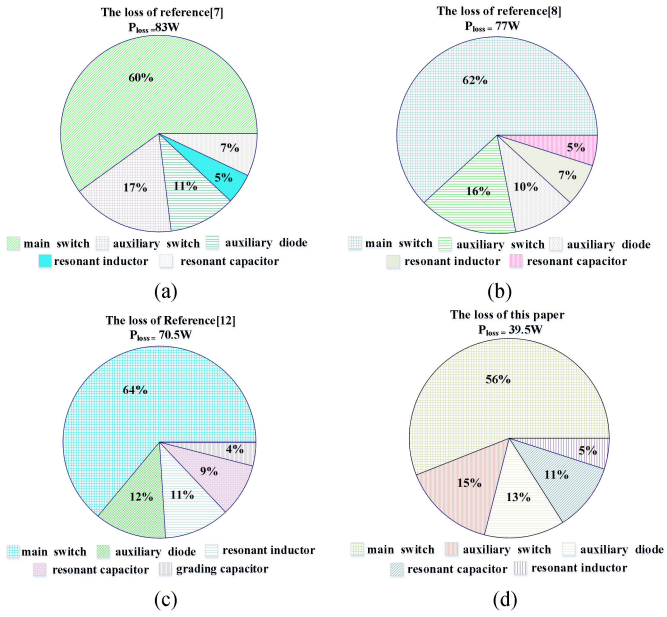

Fig. 12. Power loss distribution. (a) Reference [7]. (b) Reference [8]. (c)Reference [12]. (d) This article.

when the output power P_0 reaches 3 kW. The total loss of soft-switching inverter proposed in [7], [8], [12], and this article are 83, 77, 70.5, and 39.5 W, respectively. It can be concluded that the simple structure of auxiliary circuits is propitious to reduce the loss of auxiliary circuits.

Table II indicates the contrast of the inverters in [7], [8], [12], and this article. In contrast with [7], [8], and [12], the total number of the auxiliary devices in this article is the lowest. Although the number of auxiliary switches in this article is more than that in [12], the maximum voltage across main switches in this article is much lower than that in [12], which makes for the selection of cheaper main switches. In summary, in contrast with [7], [8], and [12], the prominent merit of the novel inverter in this article is that its structure of auxiliary circuit is simple, which is in favor of the reduction of hardware cost and power loss.

VI. CONCLUSION

This article proposes a novel high-efficiency three-phase resonant pole inverter. Compared with other resonant pole inverters, its outstanding advantages contain: the structure of the auxiliary circuit is much simpler; and the conduction time of the auxiliary switches is constant in every switching period so it is not necessary to monitor the actual load current to control the auxiliary switch, which enhances the operation reliability of the inverter. According to the experimental results, the conclusions are as follows.

1) Zero-voltage turn-ON and zero-voltage turn-OFF of the main switches come true. Zero-current turn-ON and zero-voltage turn-OFF of the auxiliary switches also come true. Soft-switching can be accomplished when I_0 is the range of –13 to 13 A. In other words, all the switches can achieve soft-switching when output power of the inverter is in the range of 0–3 kW.
2) The THD of the output phase current of the novel inverter is superior to that of other three resonant pole inverters because of more efficient power transmission in the dead time. The novel inverter can still run smoothly even if dc supply voltage or output power shows dynamic change, which proves that the auxiliary circuit arranged on each bridge arm is compatible with the inverter having no unfavorable effect on the dynamic response of the inverter.
3) When the output power is equal to 3 kW, the measured efficiency of the novel inverter is equal to 98.7%, which confirms that the novel inverter has efficiency superiority over other resonant pole inverters. When the output power changes from 0.5 to 3 kW, the theoretical value of power loss existing in the auxiliary circuit approaches the measured value, which confirms the effectiveness of theoretical calculation.

4) Although soft-switching can still be achieved at light load, the efficiency of the novel inverter at light load has no advantage over that of the hard-switching inverter. The reason is that the eliminated switching loss of main switches is less than the loss of the auxiliary circuits at light load. Hence, compared with the hard-switching inverter, the improvement of the efficiency in the soft-switching inverter depends on two conditions: first, main switches can achieve soft-switching; and second, the eliminated switching loss of main switches can offset the loss of the auxiliary circuits.
5) The power loss of auxiliary circuits in the novel inverter is lower than that in other resonant pole inverters with more complex auxiliary circuits, which confirms that the simple structure of auxiliary circuits can make for the reduction of power loss.

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