Quadrilateral Current Mode Paralleling of Power MOSFETs for Zero-Voltage Switching

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***Abstract*—This article proposes a generic zero-voltage switching (ZVS) scheme for parallel power MOSFETs. Uncoupled or inversely coupled differential-mode commutation inductors are added to the midpoints (ac terminals) of parallel MOSFET half-bridges, and a time-delay-based control scheme is applied, generating a circulating current flowing through these commutation inductors. Thus, the inductor currents are reshaped as quadrilaterals, which enable all the parallel transistors to achieve ZVS. The mode of operation of the proposed paralleling technique is entitled quadrilateral current mode (QCM) due to the quadrilateral-shaped commutation inductor currents. The operating principle of the QCM-paralleling technique is detailed mathematically, yielding accurate closed-form analytical expressions for modulation parameters. Finally, simulations and experimental results of a QCM-enabled synchronous buck dc–dc converter are presented to validate the theoretical considerations.**

***Index Terms*—Parallel power MOSFETs, quadrilateral current mode (QCM), zero-voltage switching (ZVS).**

I. Introduction

DUE to relative low fabrication yields, the current ratings of commercial discrete wide bandgap (WBG) power transistors are limited [1]–[3]. Therefore, it is necessary or even unavoidable to connect multiple WBG power transistors in parallel in high-power applications [3]–[7]. Additionally, the parallel connection of multiple low-current WBG power transistors can be more cost-effective than employing a single high-current transistor [5]–[7].

For the parallel operation of power MOSFETs, the current imbalance caused by MOSFET parameter mismatch and asymmetrical circuit layout [3], [8]–[10] poses a big challenge to efficiency and reliability; therefore, the current imbalance suppression has stimulated much academic and industrial research [6], [7], [9], [11]–[13]. The most direct measure of handling current imbalance is to symmetrize the layout of parallel transistors [10], [14]. However, it is impossible to achieve an absolute symmetrical layout, particularly in high-power-density applications. Employing active gate drivers can dynamically balance the currents flowing through parallel devices [12], [15]; however, these methods require high-bandwidth current sensors, and the realization of active gate drives is complicated and costly. By contrast, the passive approaches [6], [7], [11], [16], [17] employ additional magnetic components in parallel branches to suppress the current imbalance; the passive solutions begin prevailing due to their simplicity in implementation and robustness in operation.

In spite of balanced currents achieved with these current sharing schemes, the parallel MOSFETs may suffer uneven thermal stresses due to thermal impedance differences [18], [19]. Multiple devices in parallel significantly reduce the on-state resistance, which in turn lead to a higher parasitic output capacitance and higher switching losses [20]. Thus, for hard-switched power converters employing parallel WBG transistors, the switching loss is predominant at partial loads, and compromises the efficiency performance, particularly at high switching frequencies [21]–[23]. By utilizing the phase-shedding technique [23], [24], the effective number of parallel transistor legs can be adjusted at different loads, which reduces the switching loss at partial loads. In order to lower the partial-load switching loss while simultaneously achieving thermal balance among parallel transistors, a desynchronized control scheme is proposed in [5]; however, only part of the parallel transistors can achieve the zero-voltage switching (ZVS).

For half-bridge (HB) legs, i.e., the basic switch units of classic synchronous buck/boost converters and single-/three-phase inverters, soft-switching, i.e., ZVS or zero-current switching, can be realized by adding auxiliary resonant circuits to the dc or ac side [25]–[28], or varying the switching frequency to operate in the triangular current mode (TCM) [29]–[34]. The ac auxiliary-resonant-circuits-based soft-switching topologies are also named as the auxiliary resonant commutated pole converters [27], [28]; the main issue is that complex auxiliary switches, inductors, and capacitors are required, particularly for multiphase systems. By contrast, the dc-link auxiliary-resonant-circuit-based soft-switching topologies [25], [26] feature a lower number of auxiliary components; however, the voltage stress of switches is higher than the dc-link voltage, e.g., 1.1–2.5 times, and thus, the loop inductance must be maintained low to avoid high voltage overshoots.

The TCM multiphase interleaving technique [29], [32]–[34] enables all MOSFETs to achieve ZVS for minimized switching loss. This approach, however, requires high-speed zero-current

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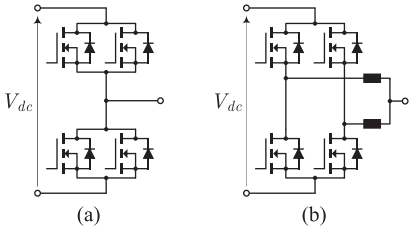


Fig. 1. Structures of (a) conventional direct and (b) DM inductor based parallel power MOSFETs. The DM inductors can be either uncoupled [5] or inversely coupled [37].

detection, featuring high implementation complexity [31]. Also, the switching frequency varies significantly with the load and output voltage [29], which complicates the electromagnetic interference (EMI) filter design and the digital control [35]. Furthermore, this technique needs relatively large (e.g., greater than several tens of microhenries in [29], [33], and [34]) output inductors, which are typically not desirable in inductive-load applications (e.g., motor drives) due to additional power loss, cost, and volume [36], [37].

In order to achieve ZVS for all parallel MOSFETs, this article proposes a quadrilateral current mode (QCM) modulation scheme. Differential-mode (DM) commutation inductors (ZVS inductors) are added to the midpoints of parallel MOSFET HB legs, and the QCM modulation scheme enables a circulating current flowing through these DM inductors. This quadrilateral-shaped circulating current helps all the parallel MOSFETs achieve ZVS, resulting in negligible switching loss. The operating principle and mathematical model are detailed, yielding closed-form analytical expressions that directly enable the calculation of the timing parameters needed for ZVS realization. This QCM paralleling technique exhibits much lower switching loss than the conventional direct parallel. In contrast to the TCM multiphase interleaving, this QCM-enabled paralleling technique has the following advantages.

1) The switching frequency can be either fixed or variable.
2) The quadrilateral-shaped DM inductor currents have a negligible impact on the output current.
3) Only miniature DM inductors (several microhenries) are required.
4) In addition to QCM, this paralleling solution is also compatible with the synchronous CCM.

The QCM-enabled paralleling technique can be applied to any topologies consisting of basic parallel MOSFET HB units, e.g., the synchronous buck/boost dc–dc converters and single-/three-phase inverters.

II. QCM Paralleling Scheme

A. Topology

Fig. 1 shows the basic structures of parallel MOSFET HB legs with and without DM commutation inductors. In contrast with the direct parallel shown in Fig. 1(a), the current imbalance caused by the mismatches of transistors and parasitic parameters can be well mitigated by the added DM inductors [5], [37] shown in Fig. 1(b). The DM inductors are typical of much lower inductance than the output filter inductance, and they can be either uncoupled [5] or inversely coupled [37] in implementation.

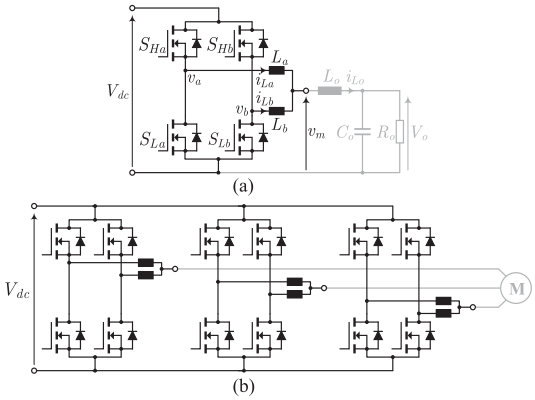


Fig. 2. Converter topologies employing the DM inductor based paralleling structure. (a) Synchronous buck dc–dc converter. (b) Three-phase traction inverter.

The DM inductor based paralleling structure can be applied to commonly used converter topologies, e.g., the synchronous buck dc–dc converter and the three-phase traction inverter, as shown in Fig. 2. It should be noted that the number of HB legs in parallel is theoretically unlimited. For simplicity, two parallel HB legs with uncoupled inductors are employed in this study.

B. QCM Switching Pattern

A QCM modulation scheme is proposed for the DM commutation inductor based parallel structure, as shown in Fig. 3. First, the parallel HB legs are divided into two groups: the leading HB leg S_{Ha}–S_{La} and the lagging leg S_{Hb}–S_{Lb}, as shown in Fig. 2(a). The gate signals of these parallel legs are desynchronized. Specifically, the turn-OFF edges between the lagging and leading low-side MOSFETs are delayed by a time of $\phi_{L\text{off}}$, whereas the turn-OFF edges between the high-side switches are delayed by a time of $\phi_{H\text{off}}$. With these two turn-OFF delays of gate signals, the switch node (midpoint) voltages of the two parallel HB legs are asynchronous, i.e., v_b lags behind v_a by times of $\delta_{L\text{off}}$ and $\delta_{H\text{off}}$ at their rising and falling edges, respectively. The DM commutation inductors L_a and L_b are assumed to be identical (i.e., $L_a = L_b = L_c$) and the commutation inductance L_c is much lower than the output filter inductance L_o. Then, the common output voltage of the parallel HB legs v_m can be obtained as

$$v_m(t) = \frac{v_a(t) + v_b(t)}{2}. \tag{1}$$

For the QCM, the common output voltage v_m has three levels $(0, +\frac{V_{\text{dc}}}{2}, +V_{\text{dc}})$ owing to the time delays between v_a and v_b, as shown in Fig. 3. Meanwhile, a nonzero voltage difference between v_a and v_b, i.e., v_{ab}, excites a controllable ac circulating current flowing through the DM commutation inductors L_a and L_b

$$\begin{cases} i_{\text{dm}}(t) = \frac{i_{La}(t) - i_{Lb}(t)}{2} \\ 2L_c \frac{\text{d}i_{\text{dm}}(t)}{\text{d}t} = v_{ab}(t). \end{cases} \tag{2}$$

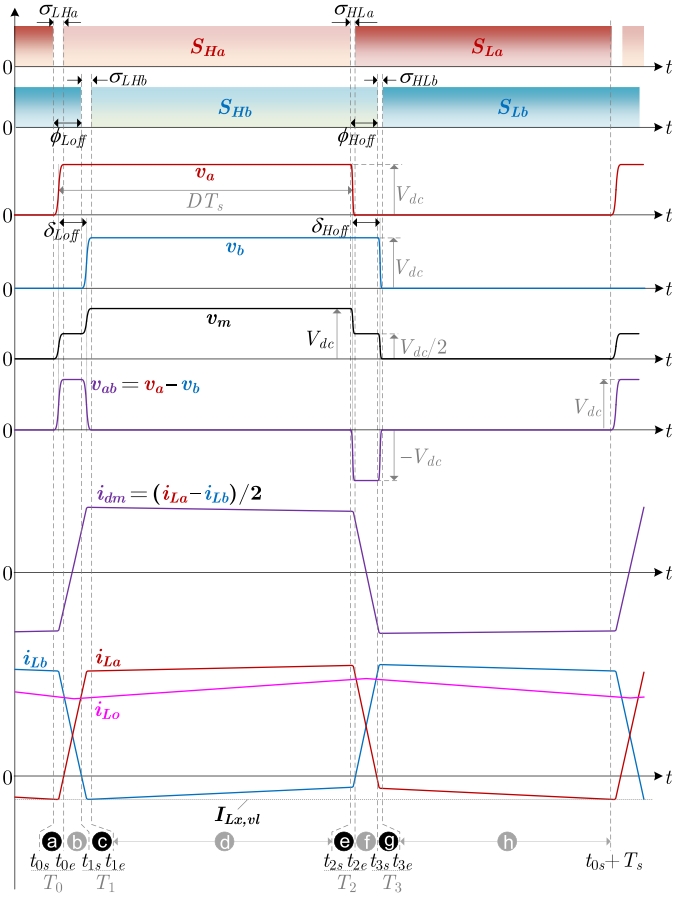


Fig. 3. Typical operating waveforms of the QCM-paralleled power MOSFET HBs [see Fig. 2(a)]. The deadtimes between high- and low-side switches are denoted as σ_{LHa} and σ_{LHb} for leg S_{Ha}–S_{La} and σ_{LHb} and σ_{HLb} for leg S_{Hb}–S_{Lb}. The turn-OFF time delays between low-side switches and between high-side switches are denoted as ϕ_{Loff} and ϕ_{Hoff}, respectively. The switch node (midpoint) voltage v_b lags behind v_a by δ_{Loff} and δ_{Hoff} for their rise and fall edges; the two time delays δ_{Loff} and δ_{Hoff} also represent the positive and negative pulsewidths of voltage v_{ab}.

The amplitude of the circulating current $i_{\rm dm}$ is mainly determined by the volt-second product of v_{ab} during the time delays δ_{Loff} and δ_{Hoff}, as shown in Fig. 3. The two time delays δ_{Loff} and δ_{Hoff} also represent the positive and negative pulsewidths of v_{ab}. That is, the circulating current $i_{\rm dm}$ is regulated by controlling the pulsewidths of v_{ab}.

The output current i_{Lo} is determined by the common output voltage v_m, the output voltage v_o, and the filter inductance L_o, i.e.,

$$L_o \frac{{\rm d}i_{Lo}(t)}{{\rm d}t} = v_m(t) - V_o. \tag{3}$$

According to Kirchhoff's circuit law, the output current can be obtained from the two inductor currents as

$$i_{Lo}(t) = i_{La}(t) + i_{Lb}(t). \tag{4}$$

From (2) and (4), the two inductor currents i_{La} and i_{Lb} can be expressed by the circulating and output currents, i.e.,

$$\begin{cases} i_{La}(t) = \frac{i_{Lo}(t)}{2} + i_{\rm dm}(t) \\ i_{Lb}(t) = \frac{i_{Lo}(t)}{2} - i_{\rm dm}(t). \end{cases} \tag{5}$$

As seen from (5) and Fig. 3, the two inductor currents i_{La} and i_{Lb} are shaped by both the output current i_{Lo} and the circulating current $i_{\rm dm}$. Increasing the amplitude of $i_{\rm dm}$ enables i_{La} and i_{Lb} to reach a negative boundary before the corresponding high-side MOSFETs S_{Ha} and S_{Hb} are turned ON. That is, the body diodes of S_{Ha} and S_{Hb} conduct first before their gates are applied with a forward bias voltage, leading to ZVS-ON for S_{Ha} and S_{Hb}. Intrinsically, the two low-side MOSFETs S_{La} and S_{Lb} can also achieve the ZVS-ON due to the sufficiently positive inductor currents i_{La} and i_{Lb} before their gate turn-ON signals are applied. Hence, by controlling the pulsewidths ($\delta_{L\rm off}$ and $\delta_{H\rm off}$) of v_{ab}, all the parallel MOSFETs are able to achieve the ZVS for minimized switching loss. The commutation inductor currents i_{La} and i_{Lb} exhibit quadrilateral shapes, and therefore, the mode of operation is termed as QCM.

C. Operating Principle

The synchronous buck dc–dc converter [see Fig. 2(a)] is taken as an application example to illustrate the operating principle of the proposed QCM paralleling scheme.

Typical operating waveforms of QCM are shown in Fig. 3 where four resonant stages, ⓐ, ⓒ, ⓔ, and ⓖ, occur during intervals T_0, T_1, T_2, and T_3, respectively. For each resonant state interval, subscript "s" denotes the starting instant and "e" denotes the ending instant, e.g., t_{0s} and t_{0e} represent the starting and ending instants of interval T_0 (resonant stage ⓐ), respectively. Four nonresonant stages are termed as ⓑ, ⓓ, ⓕ, and ⓗ in Fig. 3. Therefore, there are total eight stages within one switching cycle $[t_{0s}, t_{0s}+T_s]$ where T_s denotes the switching period. The equivalent circuits and current loops of these operating stages are shown in Fig. 4.

1) Nonresonant Stages: In operating stages ⓑ, ⓓ, ⓕ, and ⓗ, the MOSFETs are fully turned ON or OFF, operating in the ohmic region with a channel resistance of $R_{ds,\rm on}$ or in the cutoff region with an almost infinite channel resistance. In these stages, the switch node (midpoint) voltages of the parallel legs v_a and v_b are given as

$$\begin{cases} v_a(t) = s_a(t)V_{\rm dc} - i_{La}(t)R_{ds,\rm on} \\ v_b(t) = s_b(t)V_{\rm dc} - i_{Lb}(t)R_{ds,\rm on} \end{cases} \tag{6}$$

in which the bilogic variables $s_a(t)$ and $s_b(t)$ are equal to 1 and 0 when the corresponding high- and low-side MOSFETs are turned ON, respectively. In these nonresonant stages, the operation follows the differential equations in (2) and (3).

2) Resonant Stages: Operating stages ⓐ, ⓒ, ⓔ, and ⓖ represent the resonant states formed by the parasitic output capacitances of MOSFETs, the DM inductors (L_a and L_b), and the output inductor L_o. Resonant states 0 and 2 in stages ⓐ and ⓔ have the same characteristic impedance, as shown in Fig. 4(a) and (e), whereas resonant states 1 and 3 in stages ⓒ and ⓖ have the same characteristic impedance, as shown in Fig. 4(c) and (g). These characteristic impedances are obtained as

$$Z_r = \begin{cases} \sqrt{\frac{L_a + L_b \| L_o}{C_{oss,SHa} + C_{oss,SLa}}}, & \text{Resonant states 0 and 2} \\ \sqrt{\frac{L_b + L_a \| L_o}{C_{oss,SHb} + C_{oss,SLb}}}, & \text{Resonant states 1 and 3} \end{cases} \tag{7}$$

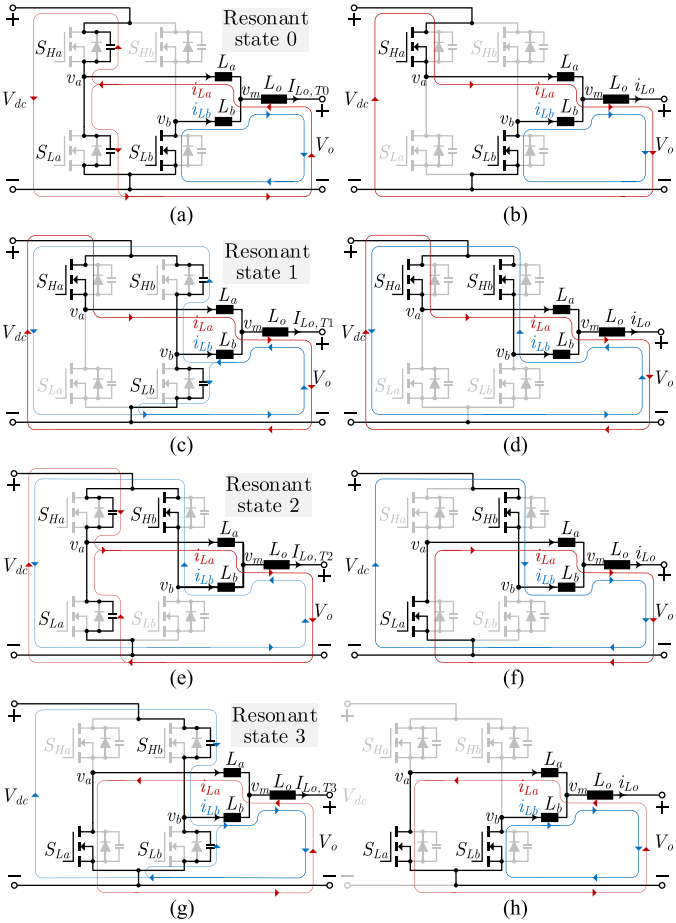


Fig. 4. Operating states of QCM-paralleled MOSFET HBs [configured as a synchronous buck dc–dc converter, see Fig. 2(a)] within a full switching cycle $[t_{0s}, t_{0s}+T_s]$. The four resonant stages, ⓐ, ⓒ, ⓔ, and ⓖ, are termed as resonant states 0, 1, 2, and 3, respectively. (a) $[t_{0s}, t_{0e}]$. (b) $[t_{0e}, t_{1s}]$. (c) $[t_{1s}, t_{1e}]$. (d) $[t_{1e}, t_{2s}]$. (e) $[t_{2s}, t_{2e}]$. (f) $[t_{2e}, t_{3s}]$. (g) $[t_{3s}, t_{3e}]$. (h) $[t_{3e}, t_{0s}+T_s]$.

where $C_{oss,SHa}$, $C_{oss,SLa}$, $C_{oss,SHb}$, and $C_{oss,SLb}$ represent the parasitic output capacitances of S_{Ha}, S_{La}, S_{Hb}, and S_{Lb}, respectively. Assuming these parasitic capacitances are equal to $C_{o,qe}$, the characteristic impedance and the resonant angular frequency can be expressed as

$$Z_r = \sqrt{\frac{L_c + L_c||L_o}{2C_{o,qe}}} \tag{8}$$

$$\omega_r = \frac{1}{\sqrt{2C_{o,qe}(L_c + L_c||L_o)}} \tag{9}$$

where the charge-equivalent capacitance $C_{o,qe}$ is a fixed capacitance that gives the same stored charge as a nonlinear parasitic output capacitor C_{oss} while the drain-source voltage v_{ds} is rising from 0 to $V_{\rm dc}$, i.e.,

$$C_{o,qe} = \frac{Q_{oss}}{V_{\rm dc}} = \frac{1}{V_{\rm dc}} \int_0^{V_{\rm dc}} C_{oss} \mathrm{d}v_{ds} \tag{10}$$

where Q_{oss} represents the charge stored in the parasitic output capacitor of a transistor at a drain-source voltage of $V_{\rm dc}$.

Considering $L_c \ll L_o$, the output inductor L_o can be regarded as a constant current source during the short resonant transitions, i.e., in stages ⓐ, ⓒ, ⓔ, and ⓖ; the output currents in the four resonant stages are represented by $I_{Lo,T0}$, $I_{Lo,T1}$, $I_{Lo,T2}$, and $I_{Lo,T3}$, respectively. The characteristic impedance and the resonant angular frequency in (8) and (9) can be further simplified as

$$Z_r = \sqrt{\frac{L_c}{C_{o,qe}}} \tag{11}$$

$$\omega_r = \frac{1}{2\sqrt{L_c C_{o,qe}}}. \tag{12}$$

3) Analysis of Operation: The state-plane diagram [31], [35], [38] depicting the trajectory of inductor current (scaled by the characteristic impedance of the resonant circuit) with respect to the switch node voltage is a useful representation for the analysis of the QCM-based ZVS operation, as illustrated in Fig. 5.

a) *Stage ⓐ (Resonant State 0): $[t_{0s}, t_{0e}]$:* Before t_{0s}, the two low-side switches S_{La} and S_{Lb} are conducting but with different directions of current flows, as shown in Figs. 3 and 4(h). At t_{0s}, S_{La} is turned OFF, and then the output capacitances $C_{oss,SLa}$ and $C_{oss,SHa}$ begin to resonate with L_a, L_b, and L_o, as shown in Figs. 3 and 4(a). The resonant transition is described in the state-plane diagrams [see Fig. 5(a) and (b)]. The resonant circle of $Z_r i_{La}(t)$ versus $v_a(t)$ is centered at (0, 0) and starting from $(0, Z_r I_{La,t0s})$ as the initial condition. The time elapsed between two points on the circular trajectory is propositional to the angle subtended at the center [38]. Likewise, the resonant circle of $Z_r i_{Lb}(t)$ versus $v_a(t)$ is centered at $(0, Z_r I_{Lo,T0})$ and starting from $(0, Z_r I_{Lb,t0s})$. The radii of the two circles $Z_r i_{La}(t)$ versus $v_a(t)$ and $Z_r i_{Lb}(t)$ versus $v_a(t)$ are identical and termed as r_0. The resonant voltage and current transitions can be described with

$$\begin{cases} i_{La}(t) = I_{La,t0s}\cos[\omega_r(t-t_{0s})] \\ i_{Lb}(t) = I_{Lo,T0} - I_{La,t0s}\cos[\omega_r(t-t_{0s})] \\ v_a(t) = -Z_r I_{La,t0s}\sin[\omega_r(t-t_{0s})] \\ v_b(t) = 0 \end{cases} \tag{13}$$

where $I_{La,t0s}$ denotes the current of i_{La} at $t = t_{0s}$. The circle radius in Fig. 5(a) can be obtained as

$$r_0 = Z_r |I_{La,t0s}|. \tag{14}$$

If the radius is not less than $V_{\rm dc}$, i.e., $r_0 \geq V_{\rm dc}$, then the switch node voltage v_a can rise to the dc-bus voltage $V_{\rm dc}$, implying $C_{oss,SHa}$ is discharged to 0 V at $t = t_{0e}$, after which S_{Ha} can be turned ON under ZVS. Otherwise, the resonant trajectories will follow the dashed lines in Fig. 5(a), and v_a cannot reach $V_{\rm dc}$ before $Z_r i_{La}$ becomes positive, resulting in incomplete ZVS (iZVS) [39] for S_{Ha}. The minimum $I_{La,t0s}$ allowing for full ZVS is termed as the valley inductor current $I_{Lx,vl}$, and it can be obtained as

$$\begin{aligned} & r_0 \geq V_{\rm dc} \\ & \Rightarrow -I_{La,t0s} \geq \frac{V_{\rm dc}}{Z_r} = V_{\rm dc}\sqrt{\frac{C_{o,qe}}{L_c}} = \sqrt{\frac{V_{\rm dc}Q_{oss}}{L_c}} = -I_{Lx,vl}. \end{aligned} \tag{15}$$

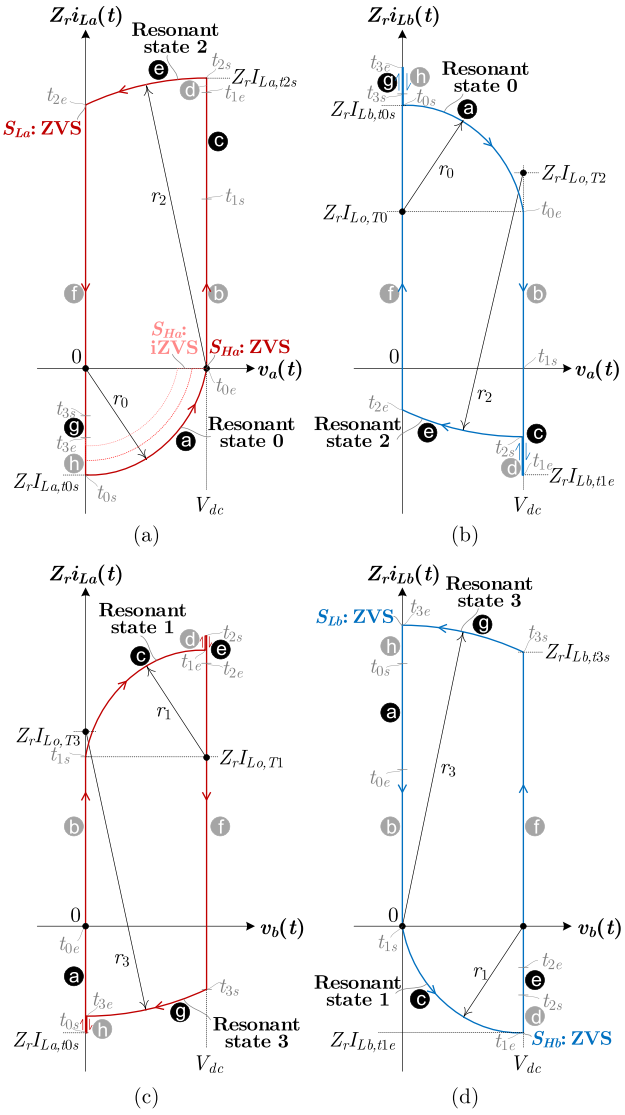


Fig. 5. State-plane diagram of the scaled inductor currents with respect to the switch node voltages for the QCM-paralleled power MOSFET HBs [see Fig. 2(a)]. (a) $Z_r i_{La}(t)$ with respect to $v_a(t)$. (b) $Z_r i_{Lb}(t)$ with respect to $v_a(t)$. (c) $Z_r i_{La}(t)$ with respect to $v_b(t)$. (d) $Z_r i_{Lb}(t)$ with respect to $v_b(t)$.

The valley current $I_{Lx,vl}$ is negative and it is independent on the duty cycle and the output voltage, which is different from the TCM scheme.

b) Stage ⓑ: $[t_{0e}, t_{1s}]$: At t_{0e}, the high-side switch S_{Ha} of the leading leg is turned ON under ZVS, whereas the low-side switch S_{Lb} of the lagging leg is still freewheeling. Compared with the dc-bus voltage, the voltage drops over S_{Ha} and S_{Lb} can be neglected. Thus, the switch node (midpoint) voltage difference v_{ab} equals the dc-bus voltage $V_{\rm dc}$, causing the inductor current i_{La} to rise linearly and i_{Lb} to fall linearly, i.e.,

$$\begin{cases} i_{La}(t) = \left(\frac{1-2D}{4L_o} + \frac{1}{2L_c}\right) V_{\rm dc}(t - t_{0e}) \\ i_{Lb}(t) = I_{Lb,t0e} + \left(\frac{1-2D}{4L_o} - \frac{1}{2L_c}\right) V(t - t_{0e}) \\ v_{ab} = V - R_{ds,}(i_{La} - i_{Lb}) \approx V_{\rm dc} \end{cases} \tag{16}$$

where $I_{Lb,t0e}$ is the current of L_b at $t = t_{0e}$.

c) Stage ⓒ (Resonant State 1): $[t_{1s}, t_{1e}]$: The low-side switch of the lagging leg S_{Lb} can be turned OFF before i_{Lb} falls to 0. For simplicity of analysis, it is considered to turn OFF S_{Lb} at t_{1s} when the inductor current $i_{Lb} = 0$. Since both switches of the lagging leg are turned OFF, their output capacitances appear and begin to resonate with the inductors. The resonant transitions are described with two circles in Fig. 5(c) and (d). The circle centers for $Z_r i_{La}(t)$ versus $v_b(t)$ and $Z_r i_{Lb}(t)$ versus $v_b(t)$ are located at $(V_{\rm dc}, Z_r I_{Lo,T1})$ and $(V_{\rm dc}, 0)$, respectively. The resonant voltage and current transitions can be described with

$$\begin{cases} i_{La}(t) = I_{Lo,T1} + \frac{V_{\rm dc}}{Z_r} \sin[\omega_r(t - t_{1s})] \\ i_{Lb}(t) = -\frac{V_{\rm dc}}{Z_r} \sin[\omega_r(t - t_{1s})] \\ v_a(t) = V_{\rm dc} \\ v_b(t) = V_{\rm dc} - V_{\rm dc} \cos[\omega_r(t - t_{1s})]. \end{cases} \tag{17}$$

The switch node voltage v_b reaches $V_{\rm dc}$ at t_{1e}, indicating the parasitic output capacitance $C_{oss,SHb}$ is discharged to 0. The switch S_{Hb} can be subsequently turned ON under ZVS. As observed in Fig. 5(d), the inductor current i_{Lb} falls to its minimum at t_{1e}, reaching $I_{Lb,t1e}$. The circle radius in Fig. 5(d) r_1 is obtained as

$$r_1 = V_{\rm dc} = Z_r |I_{Lb,t1e}|. \tag{18}$$

From (18), we have

$$I_{Lb,t1e} = -\frac{V_{\rm dc}}{Z_r} = I_{Lx,vl}. \tag{19}$$

It means that the valley current of i_{Lb} is identical to the valley of i_{La}.

3) Stage ⓓ: $[t_{1e}, t_{2s}]$: The switch S_{Hb} is turned ON under ZVS at t_{1e}. Thus, both high-side switches S_{Ha} and S_{Hb} are ON, but are carrying different currents in opposite directions, as shown in Fig. 4(d). Solving the differential equations (2) and (3) yields

$$\begin{cases} i_{La}(t) = \left(\frac{I_{Lo,T1}}{2} - \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - t_{1e})\right) \\ \qquad + I_{\rm dm,t1e} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - t_{1e})\right) + \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}} \\ i_{Lb}(t) = \left(\frac{I_{Lo,T1}}{2} - \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - t_{1e})\right) \\ \qquad - I_{\rm dm,t1e} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - t_{1e})\right) + \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}} \\ v_{ab} = -R_{ds,\rm on}[i_{La}(t) - i_{Lb}(t)] \end{cases} \tag{20}$$

where $I_{\rm dm,t1e} = \frac{I_{La,t1e} - I_{Lb,t1e}}{2}$ with $I_{La,t1e}$ and $I_{Lb,t1e}$ representing the currents of L_a and L_b at $t = t_{1e}$. This stage terminates at $t = t_{2s}$ when S_{Ha} is turned OFF.

3) Stage ⓔ (Resonant State 2): $[t_{2s}, t_{2e}]$: After S_{Ha} is turned OFF, the parasitic output capacitances of S_{Ha} and S_{La} start to resonate with L_a and L_b, as shown in Figs. 4(e), 5(a), and 5(b). The switch node voltage v_a is falling, and the two inductor currents i_{La} and i_{Lb} are decreasing and increasing, respectively. The resonant trajectories are minor arcs of two circles with centers located at $(V_{\rm dc}, 0)$ and $(V_{\rm dc}, Z_r I_{Lo,T2})$, respectively. The

equations describing the resonant transitions are obtained as

$$\begin{cases} i_{La}(t) = I_{La,t2s}\cos[\omega_r(t-t_{2s})] \\ i_{Lb}(t) = I_{Lo,T2} - I_{La,t2s}\cos[\omega_r(t-t_{2s})] \\ v_a(t) = V_{\rm dc} - Z_r I_{La,t2s}\sin[\omega_r(t-t_{2s})] \\ v_b(t) = V_{\rm dc} \end{cases} \tag{21}$$

where $I_{La,t2s}$ denotes the current of L_a at t_{2s}. The radius of the arcs is directly derived as

$$r_2 = Z_r I_{La,t2s}. \tag{22}$$

The switch node voltage v_a drops to 0 at t_{2e} after which S_{La} can be turned ON under ZVS.

3) Stage ⓕ: $[t_{2e}, t_{3s}]$: After t_{2e}, the low-side switch of the leading leg S_{La} conducts reversely, whereas the high-side switch of the lagging leg S_{Hb} remains ON. As with stage ⓑ, the voltage drops over S_{La} and S_{Hb} are far lower than the dc-bus voltage $V_{\rm dc}$, and therefore can be neglected. The inductor currents can be described as

$$\begin{cases} i_{La}(t) = I_{La,t2e} + \left(\frac{1-2D}{4L_o} - \frac{1}{2L_c}\right) V_{\rm dc}(t-t_{2e}) \\ i_{Lb}(t) = I_{Lb,t2e} + \left(\frac{1-2D}{4L_o} + \frac{1}{2L_c}\right) V_{\rm dc}(t-t_{2e}) \\ v_{ab} = -V_{\rm dc} - R_{ds,\rm on}[i_{La}(t) - i_{Lb}(t)] \approx -V_{\rm dc} \end{cases} \tag{23}$$

where $I_{La,t2e}$ and $I_{Lb,t2e}$ are the currents of L_a and L_b at $t = t_{2e}$, respectively. This stage ends with S_{Hb} being turned OFF at t_{3s}.

4) Stage ⓖ (Resonant State 3): $[t_{3s}, t_{3e}]$: As S_{Hb} turns OFF, the parasitic output capacitances of S_{Hb} and S_{Lb} begin to resonate with L_a and L_b, causing $C_{oss,SHb}$ and $C_{oss,SLb}$ to be charged and discharged, respectively. The resonant trajectories are represented by the minor arcs in Fig. 5(c) and (d). The centers of these minor arcs are located at (0, $Z_r I_{Lo,T3}$) for $Z_r i_{La}(t)$ versus $v_b(t)$ and (0, 0) for $Z_r i_{Lb}(t)$ versus $v_b(t)$. The mathematical expressions of the resonant transitions are given as

$$\begin{cases} i_{La}(t) = I_{Lo,T3} - I_{Lb,t3s}\cos[\omega_r(t-t_{3s})] \\ \qquad -\frac{V_{\rm dc}}{Z_r}\sin[\omega_r(t-t_{3s}) \\ i_{Lb}(t) = I_{Lb,t3s}\cos[\omega_r(t-t_{3s})] + \frac{V_{\rm dc}}{Z_r}\sin[\omega_r(t-t_{3s})] \\ v_a(t) = 0 \\ v_b(t) = V_{\rm dc}\cos[\omega_r(t-t_{3s})] - Z_r I_{Lb,t3s}\sin[\omega_r(t-t_{3s})] \end{cases} \tag{24}$$

where $I_{Lb,t3s}$ denotes the current of L_b at $t = t_{3s}$. The radius of the two circle arcs can be obtained as

$$r_3 = \sqrt{(Z_r I_{Lb,t3s})^2 + V_{\rm dc}^2} = Z_r I_{Lb,t3e} \tag{25}$$

where $I_{Lb,t3e}$ denotes the current of L_b at $t = t_{3e}$. The resonance terminates at $t = t_{3e}$ when v_b falls to 0 and the body diode of S_{Lb} starts to conduct. Subsequently, S_{Lb} can achieve the ZVS-ON.

5) Stage ⓗ: $[t_{3e},\ t_{0s}+T_s]$: The two low-side MOSFETs S_{La} and S_{Lb} are fully turned ON, operating in the ohmic region. Thus, the two switch node voltages v_a and v_b are determined by the channel resistances and currents of S_{La} and S_{Lb}. Solving the differential equations (2) and (3) yields the mathematical expressions of voltages and currents

$$\begin{cases} i_{La}(t) = \left(\frac{I_{Lo,T3}}{2} + \frac{DV_{\rm dc}}{R_{ds,\rm on}}\right)\exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t-t_{3e})\right) \\ \qquad +I_{\rm dm,t3e}\exp\left(-\frac{R_{ds,\rm on}}{L_c}(t-t_{3e})\right) - \frac{DV_{\rm dc}}{R_{ds,\rm on}} \\ i_{Lb}(t) = \left(\frac{I_{Lo,T3}}{2} + \frac{DV_{\rm dc}}{R_{ds,\rm on}}\right)\exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t-t_{3e})\right) \\ \qquad -I_{\rm dm,t3e}\exp\left(-\frac{R_{ds,\rm on}}{L_c}(t-t_{3e})\right) - \frac{DV_{\rm dc}}{R_{ds,\rm on}} \\ v_{ab} = -R_{ds,\rm on}[i_{La}(t) - i_{Lb}(t)] \end{cases} \tag{26}$$

where $I_{\rm dm,t3e} = \frac{I_{La,t3e} - I_{Lb,t3e}}{2}$ with $I_{La,t3e}$ and $I_{Lb,t3e}$ being the currents of L_a and L_b at $t = t_{3e}$. This stage terminates at $t = t_{0s} + T_s$ when S_{La} is turned OFF and a new switching cycle begins.

D. Simplification of Mathematical Model

The aforementioned mathematical model is nonlinear, and there are no closed-form solution for the two control variables, i.e., the two time delays $\delta_{L\rm off}$ and $\delta_{H\rm off}$ between the two switch node voltages v_a and v_b. These two time delays also represent the positive and negative pulsewidths of DM voltage v_{ab}, as shown in Fig. 3. Therefore, in the first place, a linear MOSFET HB model [29], [40] is applied. With this linear model, the switch node voltage of an HB leg jumps between 0 and $V_{\rm dc}$ with zero rise and fall time; the switch node voltage remains unchanged until the parasitic output capacitances of the MOSFET HB are injected or ejected charge of Q_{oss}. A comparison between SPICE simulations and the results with the linear MOSFET HB model is shown in Fig. 6. Due to the high nonlinearity of the parasitic output capacitances of MOSFETs with respect to the switch node voltage, the real inductor currents i_{La} and i_{Lb} during the resonant transitions are close to the case using the linear MOSFET model.

Applying the linear MOSFET model, each of the resonant stages, i.e., stages ⓐ, ⓒ, ⓔ, and ⓖ, can be split into two substages that further can be merged with its adjacent nonresonant stages, as shown in Fig. 6(b) and (c). With this linearization, only four nonresonant stages ⓑ, ⓓ, ⓕ, and ⓗ remain within one switching cycle. The boundaries between these nonresonant stages are the four time instants T_0, T_1, T_2, and T_3, as illustrated in Fig. 6(b) and (c). Also, it is seen that the currents i_{La} at T_0 and i_{Lb} at T_1 can be approximated by $I_{La,t0s}$ and $I_{La,t1e}$, respectively

$$\begin{cases} I_{La,T0} \approx I_{La,t0s} = I_{Lx,vl} \\ I_{Lb,T1} \approx I_{Lb,t1e} = I_{Lx,vl}. \end{cases} \tag{27}$$

Thus, (16), (20), (23), and (26) for stages ⓑ, ⓓ, ⓕ, and ⓗ are rewritten as (36)–(39) with modified initial conditions, as shown in the Appendix.

As aforementioned, the DM commutation inductance is relatively low (less than several microhenries), and thus, the two pulsewidths of $v_{\rm dm}$, i.e., $\delta_{L\rm off}$ and $\delta_{H\rm off}$, are much shorter compared with the switching period T_s, which means that the presence of $\delta_{L\rm off}$ and $\delta_{H\rm off}$ has a limited impact on the output current i_{Lo}. Therefore, initially it is assumed that $\delta_{L\rm off} = \delta_{H\rm off}$. When the steady state is reached, we have

$$i_{Lo}(T_0 + T_s) = i_{Lo}(T_0) \Rightarrow I_{Lo,T_0+T_s} = I_{Lo,T0}. \tag{28}$$

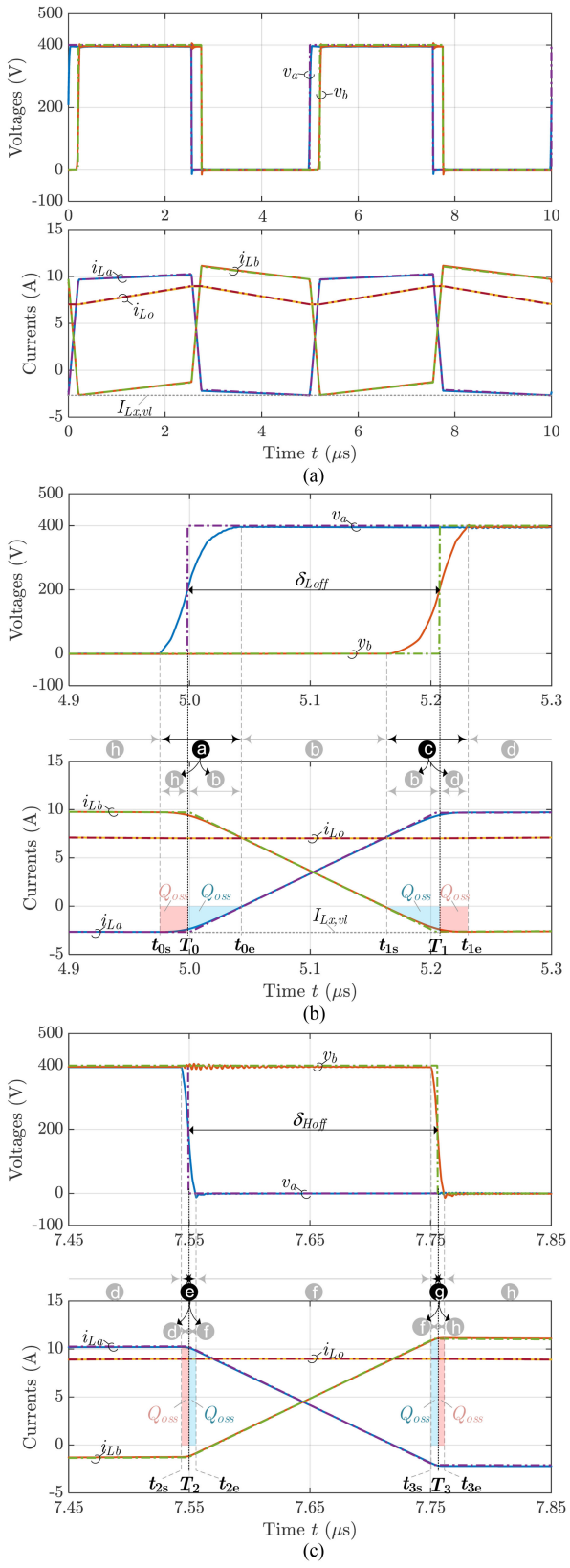


Fig. 6. Waveforms of switch node voltages and inductor currents with the SPICE simulation (solid lines) and the linear MOSFET model (dashed lines). (a) Over two switching cycles. (b) Zoomed-in waveforms from stage ⓗ to stage ⓓ. (c) Zoomed-in waveforms from stage ⓓ to stage ⓗ. The switching frequency $f_s = 200$ kHz, $V_{\rm dc} = 400$ V, $D = 0.5$, $I_{Lo} = 8$ A, and S_{Ha}–S_{Lb} are implemented with GS66508B GaN HEMTs.

Substituting the steady-state condition (28) into (36)–(39) yields the load currents at $t = T_0$ and $t = T_1$

$$\begin{cases} I_{Lo,T0} = I_{Lo} - \frac{V_{\rm dc} D[(1-D)T_s - \delta_{\rm Loff}]}{2L_o} \\ I_{Lo,T1} = I_{Lo} - \frac{V_{\rm dc}(1-D)(DT_s - \delta_{\rm Loff})}{2L_o} \end{cases} \tag{29}$$

where I_{Lo} represents the average load current. Then, the initial commutation inductor currents at T_0 and T_1 can be obtained as

$$\begin{cases} I_{La,T0} = I_{Lx,vl} \\ I_{Lb,T0} = I_{Lo,T0} - I_{Lx,vl} \\ I_{La,T1} = I_{Lo,T1} - I_{Lx,vl} \\ I_{Lb,T1} = I_{Lx,vl}. \end{cases} \tag{30}$$

Substituting (29) and (30) into (36) yields the closed-form expression for $\delta_{\rm Loff}$

$$\delta_{\rm Loff} = \frac{2L_c\left[2L_o(I_{Lo} - 2I_{Lx,vl}) - (1-D)DT_sV_{\rm dc}\right]}{(2L_o - L_c)V_{\rm dc}}. \tag{31}$$

In the steady state, the commutation inductor currents at $t = T_0 + T_s$ equals the initial currents, i.e.,

$$\begin{cases} I_{La,T0+Ts} = I_{La,T0} \\ I_{Lb,T0+Ts} = I_{Lb,T0}. \end{cases} \tag{32}$$

Substitute (32) into (36)–(39), and we can obtain the expression for $\delta_{\rm Hoff}$ as

$$\delta_{\rm Hoff} = \frac{2L_cI_{\rm dm,T2}}{V_{\rm dc}} + \frac{L_c}{R_{ds,\rm on}}{\rm W}_0\left(\frac{-2I_{\rm dm,T0}R_{ds,\rm on}}{V_{\rm dc}} \times \exp\left[R_{ds,\rm on}\left(\frac{(1-D)T_s}{L_c} - \frac{2I_{\rm dm,T2}}{V_{\rm dc}}\right)\right]\right) \tag{33}$$

where $I_{\rm dm,T0} = \frac{I_{La,T0} - I_{Lb,T0}}{2}$, $I_{\rm dm,T2} = \frac{I_{La,T2} - I_{Lb,T2}}{2}$, and W_0 is the zeroth branch of the Lambert W function.

As seen from (31) and (33), the time delays $\delta_{\rm Loff}$ and $\delta_{\rm Hoff}$ vary with the load and duty cycle.

E. Determination of Time Delays and Deadtimes of Gate Signals

The positive and negative pulsewidths of the DM voltage v_{ab}, i.e., $\delta_{\rm Loff}$ and $\delta_{\rm Hoff}$, are determined by (31) and (33), respectively. For the high-side and low-side gate signals, their falling edges are delayed by $\phi_{\rm Hoff}$ and $\phi_{\rm Loff}$, respectively. Due to the four deadtimes $\sigma_{HLa}, \sigma_{HLb}, \sigma_{LHa}$, and σ_{LHb}, the time delays $\phi_{\rm Hoff}$ and $\phi_{\rm Loff}$ are not equal to $\delta_{\rm Hoff}$ and $\delta_{\rm Loff}$, as illustrated in Fig. 3.

To determine the time delays and deadtimes of gate signals, the detailed commutation process within intervals $[t_{0s}, t_{1e}]$ and $[t_{2s}, t_{3e}]$ are shown in Fig. 7. The charge-based commutation model of power transistors [29], [41] is adopted to analyze the commutation time. The equations for time delays and deadtimes of gate signals are obtained and listed in Table I.

Fig. 8 shows the block diagram to determine the time delays and deadtimes of gate signals. In addition to the duty cycle D, the dc-bus voltage $V_{\rm dc}$ and the average load current I_{Lo} are required in (31) and (33) to calculate the theoretical time delays $\delta_{\rm Loff}$ and $\delta_{\rm Hoff}$ (i.e., the positive and negative pulsewidths of v_{ab}). After that, the derived $\delta_{\rm Loff}$ and $\delta_{\rm Hoff}$ are used to calculate the time delays and deadtimes of gate signals with Table I.

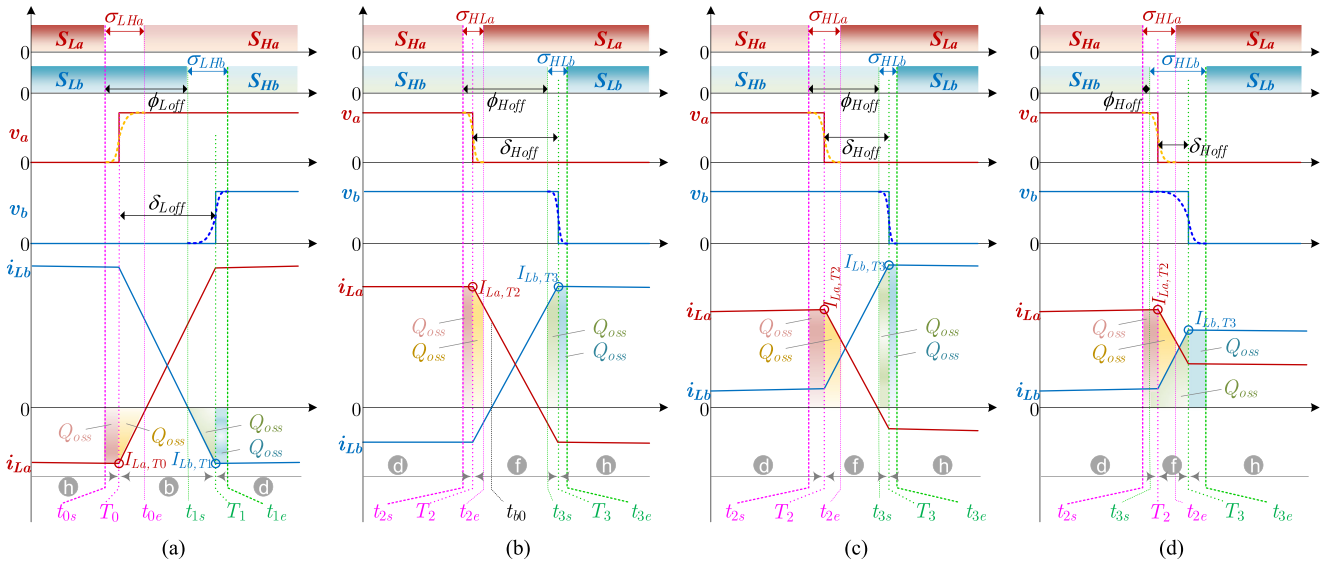


Fig. 7. Commutation modes under different conditions. (a) Commutation at $t = T_0$ and $t = T_1$. (b) Commutation at $t = T_2$ and $t = T_3$ when $I_{Lb,T2} < 0$. (c) Commutation at $t = T_2$ and $t = T_3$ when $I_{Lb,T2} \geq 0$ and $t_{3s} \geq T_2$. (d) Commutation at $t = T_2$ and $t = T_3$ when $I_{Lb,T2} \geq 0$ and $t_{3s} < T_2$.

TABLE I
DETERMINATION OF THE TIME DELAYS AND DEADTIMES OF GATE SIGNALS

	Interval $[t_{0s}, t_{1e}]$ (See Fig. 7(a))		Interval $[t_{2s}, t_{3e}]$		
			$I_{Lb,T2} < 0$ (See Fig. 7(b))	$I_{Lb,T2} \geq 0$	
				$\phi_{Hoff} \geq \frac{Q_{oss}}{I_{La,T2}}$ (See Fig. 7(c))	$\phi_{Hoff} < \frac{Q_{oss}}{I_{La,T2}}$ (See Fig. 7(d))
ϕ_{Loff}	$\delta_{Loff} - \frac{Q_{oss}}{-I_{Lx,vl}}$	ϕ_{Hoff}	$\frac{Q_{oss}}{I_{La,T2}} - \frac{2I_{Lb,T2}L_c}{V_{dc}} + \sqrt{\left(\frac{2I_{Lb,T2}L_c}{V_{dc}} + \delta_{Hoff}\right)^2 - \frac{4Q_{oss}L_c}{V_{dc}}}$		$\delta_{Hoff} + \frac{Q_{oss}}{I_{La,T2}} - \frac{Q_{oss}}{I_{Lb,T2}} + \frac{\delta_{Hoff}^2 V_{dc}}{4L_c I_{Lb,T2}}$
σ_{LHa}	$\frac{3Q_{oss}}{-I_{Lx,vl}}$	σ_{HLa}	$\frac{Q_{oss}}{I_{La,T2}} + \frac{2L_c\left(I_{La,T2} - \sqrt{I_{La,T2}^2 - I_{Lx,vl}^2}\right)}{V_{dc}}$		
σ_{LHb}		σ_{HLb}	$\delta_{Hoff} - \phi_{Hoff} + \frac{Q_{oss}}{I_{La,T2}} + \frac{Q_{oss}}{I_{Lb,T3}}$		

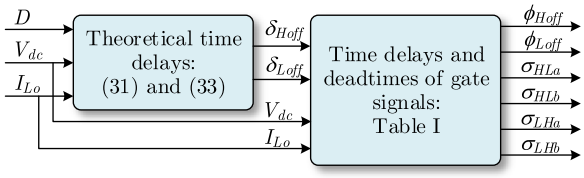


Fig. 8. Block diagram to determine the time delays and deadtimes of gate signals.

With the aforementioned mathematical model, the calculated time delays and deadtimes at different power levels are depicted in Fig. 9. It is seen that the two theoretical time delays $\delta_{H\text{off}}$ and $\delta_{L\text{off}}$ have small differences with each other. The gate signal time delay $\phi_{H\text{off}}$ is identical to $\delta_{H\text{off}}$, whereas $\phi_{L\text{off}}$ is shorter than $\delta_{L\text{off}}$ by $\frac{Q_{oss}}{-I_{Lx,vl}}$, as illustrated in Table I. For the four deadtimes, σ_{LHa} and σ_{LHb} are identical with each other and they are independent on the load, whereas σ_{HLa} and σ_{HLb} decrease with the increase of load.

F. Simulation Verification of Mathematical Model

To verify the mathematical model developed in the preceding sections, SPICE simulations of two QCM-paralleled GS66808B GaN HEMT HBs (configured as a synchronous buck dc–dc converter) were performed with LTspice, as shown in Fig. 6. In the simulations, the time delays and deadtimes of gate signals are obtained from the equations in Table I. Under the same conditions, the linearized waveforms of the switch node voltages and inductor currents obtained from the mathematical model developed in Sections II-D and E are also shown in Fig. 6. It is seen that the linearized inductor currents coincide pretty well with the simulations, which verifies the accuracy of the aforementioned mathematical model in calculating the time delays and predicting the inductor currents.

III. Performance Characterization, Implementation Considerations, and Comparison

A. Power Loss Characteristics of HB Legs

With the aforementioned mathematical models, we can generate the inductor and output current waveforms at different load currents, as shown in Fig. 10. In spite of the continuous conduction mode (CCM) output current i_{Lo}, the two commutation inductor currents i_{La} and i_{Lb} are reshaped as quadrilaterals. As the load rises, both $\delta_{L\text{off}}$ and $\delta_{H\text{off}}$ increase, and thus, the peaks of i_{La} and i_{Lb} become higher. But the valleys of i_{La} and i_{Lb} remain negative at $I_{Lx,vl}$ such that the two high-side transistors can achieve ZVS.

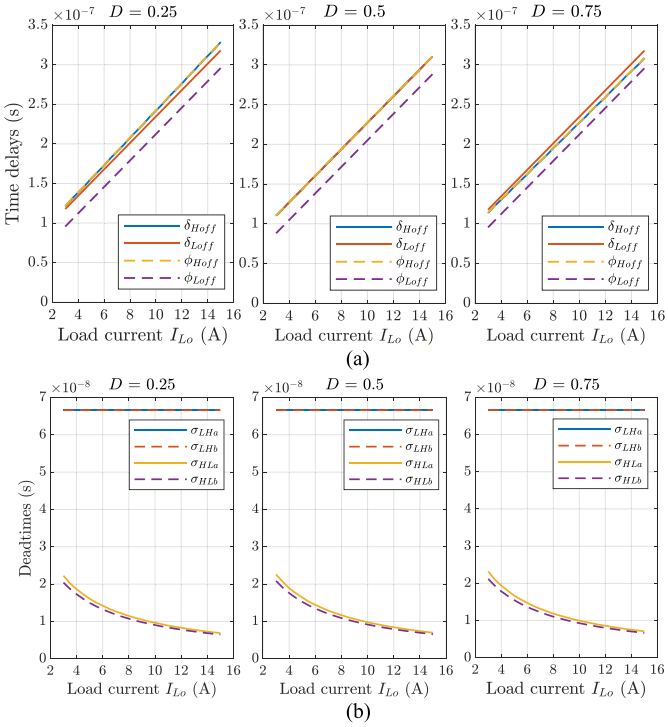


Fig. 9. Calculated (a) time delays and (b) deadtimes at different load currents and duty cycles. S_{Ha}–S_{Lb} are implemented with GS66508B GaN HEMTs.

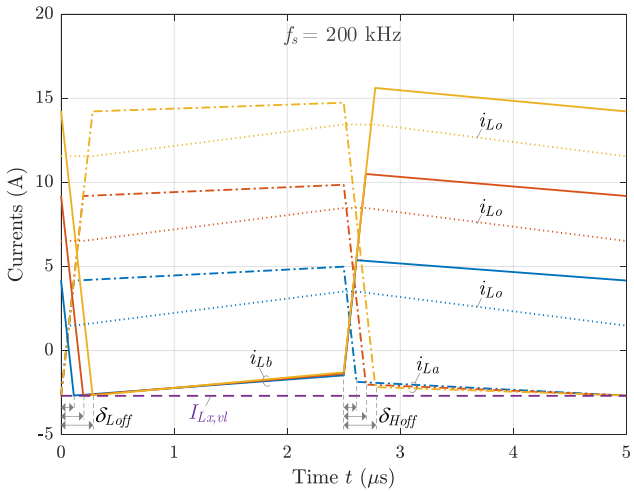


Fig. 10. Inductor current waveforms at different loads and time delays. These waveforms are generated with the analytical expressions presented in Section II.

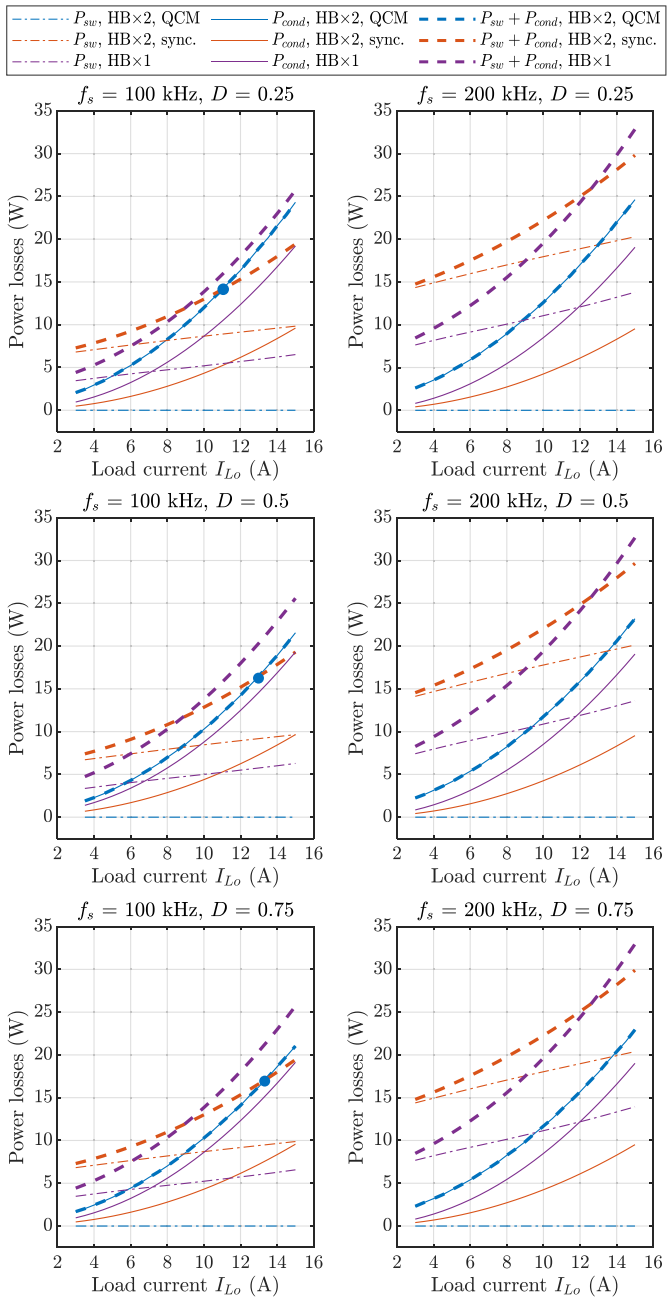


Fig. 11. Comparison of power losses among three schemes: two HBs in QCM, two HBs in synchronous CCM, and one HB in CCM. Each switch is implemented with a GS66508B GaN HEMT and its switching loss characteristic is obtained by double-pulse tests.

At different switching frequencies, duty cycles, and load currents, the calculated power losses of two parallel GS66508B HEMT HBs operating in the conventional synchronous CCM and in the proposed QCM are shown in Fig. 11. The power loss characteristics of one HB leg operating in CCM is also shown in Fig. 11 for reference. Overall, the duty cycle has a limited impact on the power loss characteristics. Instead, it is the switching frequency and the load current that affect the power losses for the three schemes.

Compared with two parallel HB legs, the one HB legs has smaller switching loss due to the halved output capacitance of power transistors. Thus, at light loads, the nonparallel HB leg has lower power loss than the two parallel HB legs in CCM. As the load rises, the conduction loss increases and eventually the one HB leg generates higher power loss than the two parallel legs in CCM. Considering the transistor cooling surface area, the nonparallel structure suffers from even higher thermal stress than the two parallel legs.

With the proposed QCM scheme, ZVS can be achieved for all power transistors, and the switching loss can be significantly reduced. Thus, the QCM operation has the lowest power loss

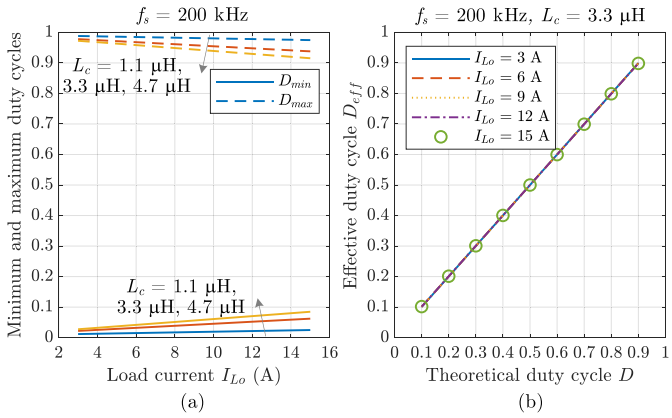


Fig. 12. Duty cycle characteristics in QCM. (a) Duty cycle range allowed for QCM realization. (b) Effective duty cycle versus theoretical duty cycle at different load currents.

than the other two schemes. Nevertheless, the QCM operation increases the conduction loss. At low switching frequencies and high load currents (e.g., at $f_s = 100$ kHz and $I_{Lo} = 14$ A), the switching loss reduction is not as significant as the increase in conduction loss. Thus, the QCM operation generates higher total power loss than the two parallel HB legs in CCM. In this case, the operation mode of the two parallel HB legs should be switched from QCM to synchronous CCM. The DM inductor based paralleling structure [see Fig. 1(b)] supports both the QCM and the synchronous CCM. This two-mode compatibility enables the parallel HB legs to maintain low power losses from light to heavy loads.

B. Effective Duty Cycle

It is seen from Fig. 3 that the duty cycle D in the QCM scheme should satisfy

$$\begin{cases} DT_s \geq \delta_{L\text{off}} \\ (1-D)T_s \geq \delta_{H\text{off}} \end{cases} \Rightarrow \frac{\delta_{L\text{off}}}{T_s} \leq D \leq 1 - \frac{\delta_{H\text{off}}}{T_s}. \quad (34)$$

At a switching frequency of 200 kHz, the allowed minimum and maximum duty cycles at different load currents and DM inductances are shown in Fig. 12(a). As I_{Lo} and L_c increase, the two time delays $\delta_{L\text{off}}$ and $\delta_{H\text{off}}$ rise, and accordingly, the duty cycle range becomes smaller. Overall, the duty cycle range for QCM is wide. For instance, at $I_{Lo} = 12.5$ A and $L_c = 3.3$ μH, the duty cycle ranges are [0.05, 0.95] and [0.025, 0.975] for $f_s = 200$ kHz and $f_s = 100$ kHz, respectively. In the case of the duty cycle beyond the range, the operation mode can be switched to the synchronous CCM.

The pulsewidth of the common output voltage v_m represents the effective duty cycle D_{eff} of the parallel HB legs, as shown in Figs. 2 and 3. Within the duty cycle range, the effective duty cycle can be obtained as

$$D_{\text{eff}} = \frac{DT_s + \delta_{H\text{off}}/2 - \delta_{L\text{off}}/2}{T_s} = D + \frac{\delta_{H\text{off}} - \delta_{L\text{off}}}{2T_s}. \quad (35)$$

As seen in Fig. 9, the difference between the two time delays $\delta_{L\text{off}}$ and $\delta_{H\text{off}}$ is extraordinarily small (< 10 ns versus the switching period 5000 ns). Therefore, the effective duty cycle is almost equal to the theoretical duty cycle, as illustrated in Fig. 12(b). It implies that the introduction of QCM has a negligible impact on the duty cycle control that is used to regulate the output voltage, current, or power.

C. Design Optimization of DM Inductors

1) DM Inductance L_c: As L_c increases, the absolute value of valley current $I_{Lx,vl}$ becomes smaller, leading to lower rms currents. On the other hand, a higher L_c brings a smaller duty cycle range [as shown in Fig. 12(a)] and a larger inductor size. Therefore, the selection of the DM inductance L_c involves multiple tradeoffs regarding duty cycle range, power loss, and volume. In this article, $L_c = 3.3\,\mu$H is chosen; the resulting duty cycle range and valley inductor current are [0.05, 0.95] (at $I_{Lo} = 12.5$ A) and -2.73 A, respectively.

2) Loss-Volume Pareto-Optimization of DM Inductors: In spite of the low inductance, the DM (commutation) inductors suffer from high current ripples, particularly at high load currents, as shown in Fig. 10. Thus, the DM inductors are prone to high fluctuations of magnetic flux density and high ac rms currents. Accordingly, the core and winding losses or the inductor size can be significant without design optimization. Taking into account two objectives, i.e., power loss and volume, design optimization is conducted for the DM inductors implemented in the proposed QCM scheme. The details, e.g., the definitions of PQ magnetic core dimensions, the fixed and variable design parameters, and the flowchart of design optimization, are shown in the Appendix.

The design optimization point is chosen at the full load, i.e., $P_o = 2.5$ kW. The design results are shown in Fig. 13 where the black and purple dotted lines represent the theoretical and practical Pareto fronts, respectively. As can be seen, the Pareto-optimal power loss decreases with the increase of inductor volume. With custom PQ cores, the power loss of each commutation inductor can be lowered to 0.6 W at an inductor size $V_{ol,Lc} = 21.6$ cm^3. With standard PQ cores, however, the inductor power loss is increased by approximately 0.25 W. Nevertheless, the power losses of the two DM inductors are still reasonably low ($\frac{0.85\times 2}{2500} = 0.068\%$) compared to the output power. When switching to the synchronous mode, the DM inductors are of lower current ripples. In this case, the inductor losses of the Pareto-optimal solutions are indicated by the black and purple squares in Fig. 13. It is seen that the DM inductors have negligible (< 0.1 W) power losses in the synchronous mode.

To reduce the inductor size, the final design adopts the PQ20/20 cores (ferrite, PC95) and #42 American wire gauge (AWG) Litz wires (660 strands, 6 turns). The final inductor has a volume of 6.72 cm^3, and the full-load ($P_o = 2.5$ kW) power loss is 1.19 W when operating in QCM.

D. Gate Signal Swapping Between Parallel Legs

In the QCM scheme, the parallel power MOSFETs have different rms currents although all can achieve ZVS, as shown in Fig. 3. Specifically, when leg a (S_{Ha}–S_{La}) leads leg b (S_{Hb}–S_{Lb}), the two diagonal transistors S_{Ha} and S_{Lb} are prone to higher rms currents than their opposite MOSFETs; when leg b leads leg a,

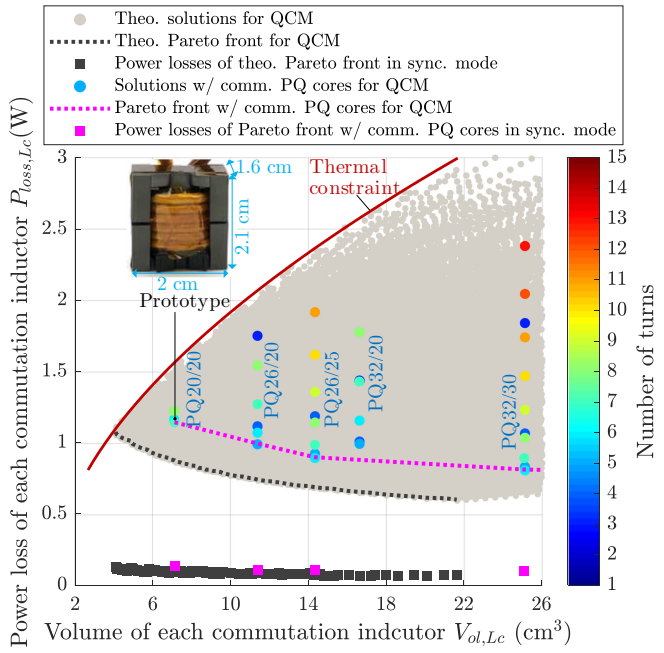


Fig. 13. Results of loss-volume Pareto optimization of the DM (commutation) inductors at the full load ($P_o = 2.5$ kW). The gray and black dots/squares/lines represent theoretical solutions. The colored dots/squares/lines are practical solutions with commercial standard PQ cores.

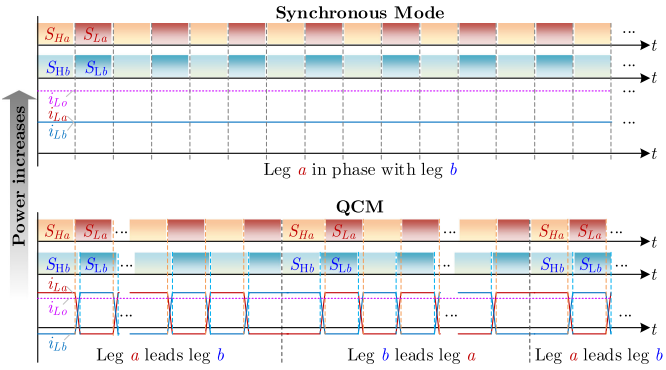


Fig. 14. Gate signal swapping between parallel legs for QCM operation. As the output current continues rising, the conduction loss may dominate the total power loss (depending on the switching frequency, see Fig. 11); in this scenario, the QCM can be switched to the synchronous mode to reduce the conduction loss and improve efficiency.

then it is the two antidiagonal MOSFETs S_{Hb} and S_{La} that are prone to higher rms currents. In order to achieve balanced rms current and thermal stress between the parallel legs, a gate signal swapping scheme is introduced, as shown in Fig. 14. The essence is that one of the two parallel legs leads another alternately.

As illustrated in Fig. 11, the QCM operation may not be as efficient as the conventional synchronous mode when the load current exceeds a certain value, e.g., $I_{Lo} > 13$ A at $f_s = 100$ kHz. In this case, the operation of parallel HB legs should be switched to the synchronous mode such that the total power loss can be reduced. This DM-inductor-based paralleling structure [see Fig. 1(b)] supports both the new QCM and the conventional CCM.

E. Comparison With Two-Phase Interleaved CCM and TCM

A comprehensive comparison among the proposed QCM-enabled paralleling, the two-phase CCM interleaving, and the two-phase TCM interleaving techniques is shown in Table II. To ensure the comparison is fair, these solutions share the same specifications as follows.

1) Each switch is implemented with a GS66508B GaN HEMT.
2) The dc-bus voltage $V_{\rm dc} = 400$ V.
3) The output voltage $V_o = 100$–300 V.
4) The maximum load current $I_{Lo,\rm max} = 12.5$ A.
5) The minimum frequency of output current ripple $f_{iLo,\rm min} = 200$ kHz.

The switching frequency of the proposed QCM-enabled paralleling and the CCM interleaving solutions can be fixed, whereas that of the TCM interleaving scheme increases significantly with the decrease of load, e.g., $f_s = 725$ kHz at $I_{Lo} = 1.25$ A. The megahertz or submegahertz switching frequencies at light loads complicate the EMI filter design and the digital control [35]. Moreover, the dynamic ON-resistance of GaN HEMTs increases significantly when the switching frequency is pushed to submegahertz or megahertz [44], leading to higher conduction losses.

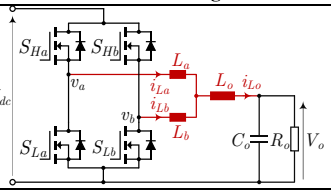
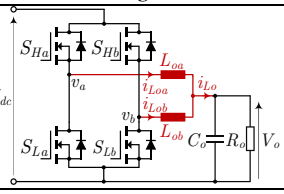
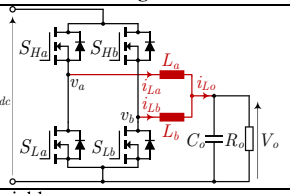
To equalize the minimum frequencies of output current ripples for all schemes, the required ZVS inductance in the interleaved TCM is $L_a = L_b = 53$ μH. Thus, the maximum energy stored in the TCM ZVS inductors is 9.23 mJ; by contrast, the ZVS inductors for QCM only process a maximum energy of 0.8 mJ. Since the volume and power loss of an inductor is proportional to the maximum energy storage [45], [46], the ZVS inductors for QCM can be of much lower power loss and smaller size than the TCM solution.

Taking into account the output filter inductor, the two-phase interleaved TCM scheme has the minimum inductance and the minimum inductive energy storage in all the three solutions; however, its output current ripple is the maximum, resulting in higher output capacitance and higher capacitive energy storage than the others.

The main issue with the CCM interleaving is that only the low-side MOSFETs can achieve the ZVS, whereas the other two solutions enable full-range ZVS for all power transistors. Nevertheless, the CCM operation has the lowest rms currents and thereby the lowest conduction losses. Hence, the CCM scheme is widely adopted in high power applications. By comparison, both the TCM interleaving and the QCM paralleling feature higher rms currents and higher conduction losses. Fortunately, the QCM-enabled paralleling scheme also supports CCM operation without changes to the output filter. Specifically, the operation mode of the QCM-paralleled power devices can be switched to the synchronous CCM when the conduction loss becomes more significant in total power losses, e.g., at heavy loads or at low switching frequencies. This flexibility makes the QCM-enabled paralleling more suitable for high power applications than TCM.

When powering motors, the motor leakage inductances are typically used as the output inductors. In this case, the high ZVS inductances in the TCM scheme are not desirable due to

TABLE II
COMPARISON AMONG DIFFERENT PARALLELING AND INTERLEAVING TECHNIQUES: THE QCM-ENABLED PARALLELING, THE CCM INTERLEAVING, AND THE TCM INTERLEAVING

Parameters	QCM-Enabled Paralleling	CCM interleaving	TCM Interleaving
Schematic			
Switching frequency f_s	Fixed or variable	Fixed or variable	Variable High switching frequencies at light loads
Output current ripple frequency f_{iLo}	$f_{iLo} = f_s$	$f_{iLo} = 2f_s$	$f_{iLo} = 2f_s$
Time delays between HB legs	Less dependent on f_s δ_{Loff} and δ_{Hoff}: (31), (33)	Directly dependent on f_s $\frac{1}{2f_s}$	Directly dependent on f_s $\frac{1}{2f_s}$
ZVS inductors L_a and L_b	3.3 μH × 2	N/A	53 μH × 2 [a]
Max. current in each ZVS inductor	15.6 A	N/A	13.32 A
Max. energy stored in L_a and L_b	0.8 mJ	N/A	9.23 mJ
Output inductor L_o	119 μH [b]	134 μH × 2 [c]	N/A
Max. current in each output inductor	14.38 A	9.98 A	N/A
Max. energy stored in output inductors	12.3 mJ	13.35 mJ	N/A
Total energy stored in ZVS and output inductors	13.1 mJ	13.35 mJ	9.23 mJ
Worst peak-to-peak current ripple in output inductors	3.75 A, 200 kHz at I_{Lo} = 12.5 A and $D = 0.5$	3.75 A, 200 kHz at I_{Lo} = 12.5 A and $D = 0.25$ or 0.75	9.43 A, 200 kHz at I_{Lo} = 12.5 A and $D = 0.25$ or 0.75
Required min. output capacitance C_o to meet the output voltage ripple requirement ($\Delta V_{o,pp} \leq 0.5\% V_o$) [d]	5.25 μF	5.25 μF	16.3 μF
Max. energy stored in output capacitor	236.6 mJ	236.6 mJ	735 mJ
ZVS for all MOSFETs	Yes	No ZVS only for low-side MOSFETs	Yes
RMS current stress of MOSFETs	High	Low	Medium
Enable CCM to reduce conduction loss	Yes	N/A	No
Application suitability to inductive loads	High The output inductor and capacitor are optional for inductive loads	Low The large output inductors are not desirable for inductive loads	Low The large ZVS inductors are not desirable for inductive loads
Possibility of integration of ZVS inductors with MOSFETs	High Due to the small ZVS inductors	N/A	Low Due to the large ZVS inductors

Notes:
a) This ZVS inductance enables the TCM interleaving scheme to have the minimum output current ripple frequency of 200 kHz that is identical to the QCM and CCM schemes.
b) and c) These output inductances are selected such that the maximum output current ripple ratio is 30% at the full load ($I_{Lo} = 12.5$ A).
d) It is assumed that the output capacitors are implemented with 450-V metalized polypropylene film capacitors with a dissipation factor of $\tan\delta = 0.8 \times 10^{-3}$ at 1 kHz [42]. The variation of $\tan\delta$ over frequency is obtained based on the data in [43].
For a fair comparison, the three schemes share the same specifications, as listed in Section III-E.

the added volume and power loss. By contrast, the QCM scheme only requires small ZVS inductors (e.g., 3.3 μH), meaning lower power loss and volume. Furthermore, the small ZVS inductors can be integrated within or in close proximity to MOSFET device packages, making the QCM-enabled parallel devices an inclusive power building block that may directly replace conventional power circuits for motor drives.

IV. EXPERIMENTAL VERIFICATION

Two GS66508B GaN HEMT HBs are connected in parallel, and two 3.3-μH inductors (loss-volume Pareto optimal, 6.72 cm^3 for each, see Fig. 13) are fabricated to implement L_a and L_b, as shown in Fig. 15. Then, this setup is configured as a synchronous buck dc–dc converter prototype by adding an LC filter to the output. In addition to the two DM inductors, the output inductor is also optimized in terms of its power loss and volume. The parameters of the final output inductor are as follows: 133 μH, PQ50/50 core (N95 ferrite), 24 turns (#38 AWG Litz wire, 500 strands), 110 cm^3, 2.16-W power loss at the full load ($I_{Lo} = 12.5$ A).

Fig. 16 shows the experimental waveforms of the buck converter with the proposed QCM scheme. As can be seen, the measurements coincide well with the theoretical analysis (cf. Figs. 3 and 6). While the waveform of the output inductor current i_{Lo} is similar to the conventional CCM operation, the commutation inductor currents i_{La} and i_{Lb} are reshaped as quadrilaterals by the nonzero DM voltage v_{ab} ($v_{ab} = v_a - v_b$).

The two low-side switches S_{La} and S_{Lb} inherently achieve the ZVS due to the sufficiently positive peak inductor currents [see Fig. 16(a) and (b)]. In addition, the two quadrilateral-shaped inductor currents i_{La} and i_{Lb} reach the valley current $I_{Lx,vl}$ [−2.73 A, see Fig. 16(a) and (c)] such that S_{Ha} and S_{Hb} can achieve ZVS as well. The measured four commutation times $\sigma_{LHa}, \sigma_{LHb}, \sigma_{HLa}$, and σ_{HLb} are equal to 71.4, 71.9, 17.6, and 16.5 ns, respectively; the corresponding theoretical values are

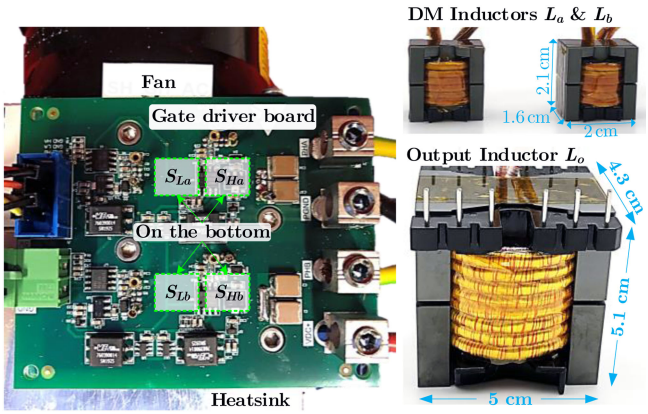


Fig. 15. Hardware prototype of two parallel-connected GaN HEMT HB legs with DM inductors. Each DM inductor is of 3.3 μH, and is fabricated with PQ20/20 cores (material: PC95 ferrite) and #42 AWG Litz wires (660 strands, 6 turns). The paralleled HB legs are configured as a buck converter by adding an LC filter at the output. The output inductor (133 μH) is fabricated with PQ50/50 cores (material: N95 ferrite) and #38 AWG Litz wires (500 strands, 24 turns).

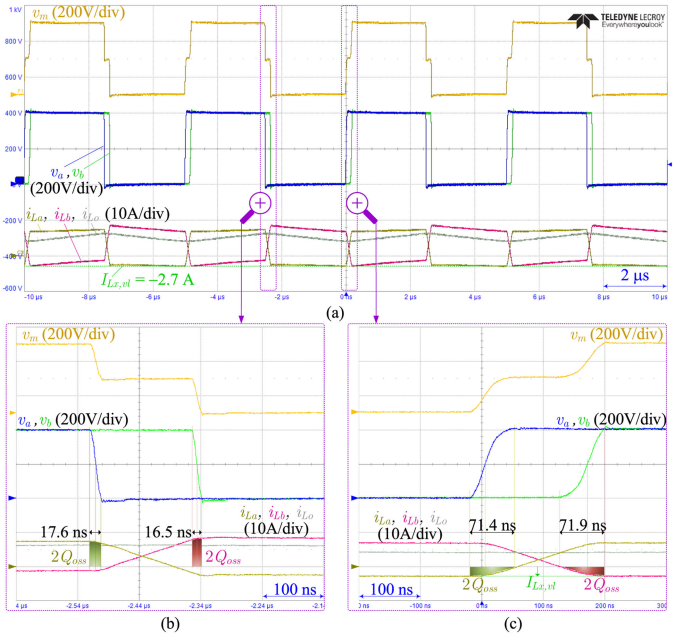


Fig. 16. Experimental waveforms of the GaN HEMT based buck dc–dc converter [see Fig. 2(a)] with the proposed QCM scheme. The input voltage $V_{\rm dc} = 400$ V, the duty cycle $D = 0.5$, the switching frequency $f_s = 200$ kHz, and the output power $P_o = 1050$ W. (a) Midpoint voltages and inductor currents. (b) Zoomed-in waveforms from S_{Ha} and S_{Hb} OFF to S_{La} and S_{Lb} ZVS-ON. (c) Zoomed-in waveforms from S_{La} and S_{Lb} OFF to S_{Ha} and S_{Hb} ZVS-ON.

67, 67, 15.9, and 14.8 ns [see Fig. 9(b)]. The time errors are 4.4, 4.9, 1.7, and 1.7 ns; these small time errors are attributed to the extra parasitic node capacitance from printed circuit boards. To avoid shoot-through in the experiment, the deadtimes are set as 75, 75, 40, and 40 ns for $\sigma_{LHa}, \sigma_{LHb}, \sigma_{HLa}$, and σ_{HLb}, respectively. It is noted that the longer deadtimes result in slightly higher conduction losses but have a negligible effect on the ZVS realization.

The measured drain-source and gate-source voltages of the QCM-paralleled GaN HEMTs at 1.95 kW are shown in Fig. 17.

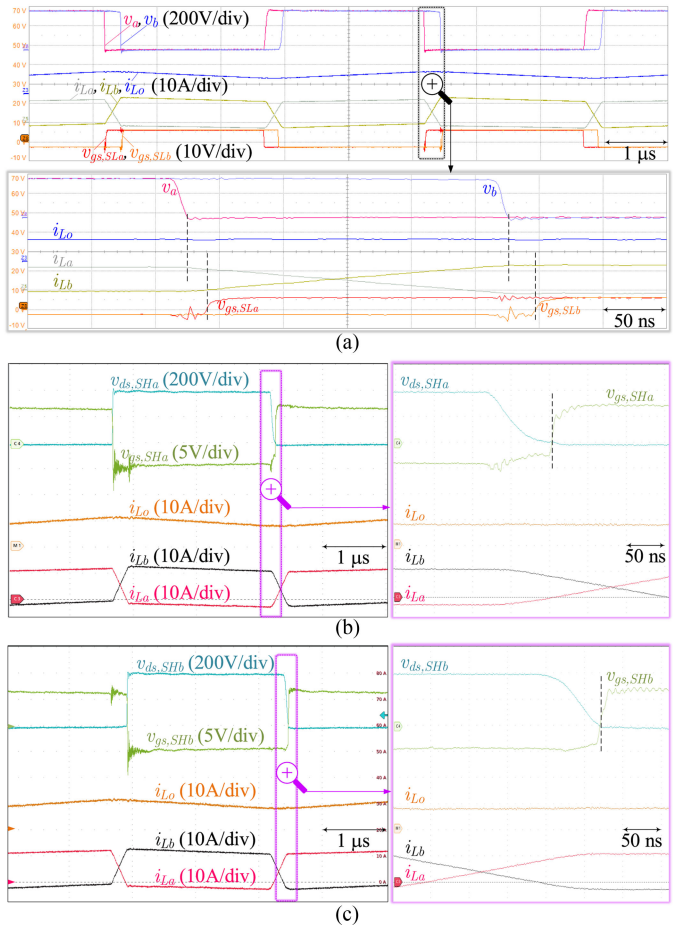


Fig. 17. Experimental ZVS waveforms of the QCM-paralleled GaN HEMTs at 1.95 kW. Drain-source and gate-source voltages of (a) the two low-side power transistors S_{La} and S_{Lb}, (b) the leading high-side transistor S_{Ha}, and (c) the lagging high-side transistor S_{Hb}. The low-side drain-source and gate-source voltages are measured using 500-MHz passive voltage probes, whereas the high-side voltages are measured with lower bandwidth (100 MHz) differential voltage probes.

The drain-source voltages have been decreased to 0 before the corresponding gate-source voltages rise to the threshold voltage, indicating that ZVS-ON is achieved for all the GaN HEMTs.

The experimental state-plane diagrams of the scaled inductor currents ($Z_r i_{La}$ and $Z_r i_{Lb}$) with respect to the switch node voltages (v_a and v_b) are shown in Fig. 18. The trajectories match with the theoretical ones shown in Fig. 5. The measured radii $r_0 = 409$ V and $r_1 = 401$ V, which are slightly higher than the dc bus voltage $V_{\rm dc} = 400$ V. The close matches of radii verify the state-plane analysis presented in Section II-C.

Fig. 19 shows the experimental waveforms with the gate signal swapping scheme for the QCM-paralleled GaN HEMT HB legs. One of the two parallel legs leads another alternately [e.g., every 500 switching cycles (2.5 ms) in Fig. 19]. Smooth transitions are achieved for the gate signal swapping. Meanwhile, the gate signal swapping has a negligible impact on the output inductor current i_{Lo}.

The measured efficiencies of the buck converter operating in the proposed QCM and the conventional synchronous CCM are shown in Fig. 20. As can be seen, the QCM scheme enables the

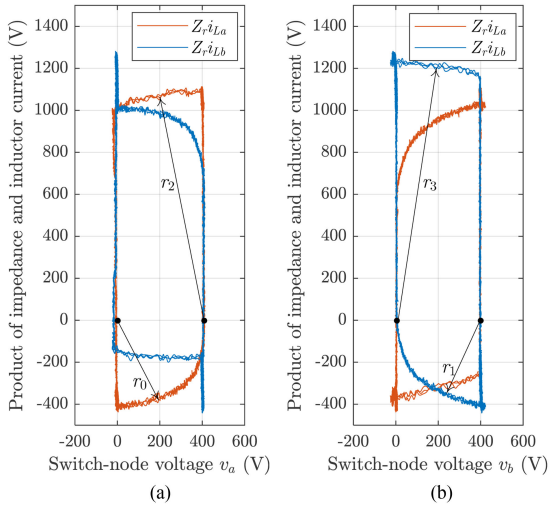


Fig. 18. Experimental state-plane diagram of the scaled inductor currents with respect to the switch node voltages for the QCM-paralleled power MOSFET HBs [see Fig. 2(a)]. (a) $Z_r i_{La}$ and $Z_r i_{Lb}$ with respect to v_a. (b) $Z_r i_{La}$ and $Z_r i_{Lb}$ with respect to v_b. The charge-equivalent capacitance of a GS66508B GaN HEMT at $V_{\rm dc} = 400$ V is calculated as $C_{o,qe} = 149$ pF based on the datasheet [47], and thus the characteristic impedance in the resonant states is obtained as $Z_r = 147\ \Omega$.

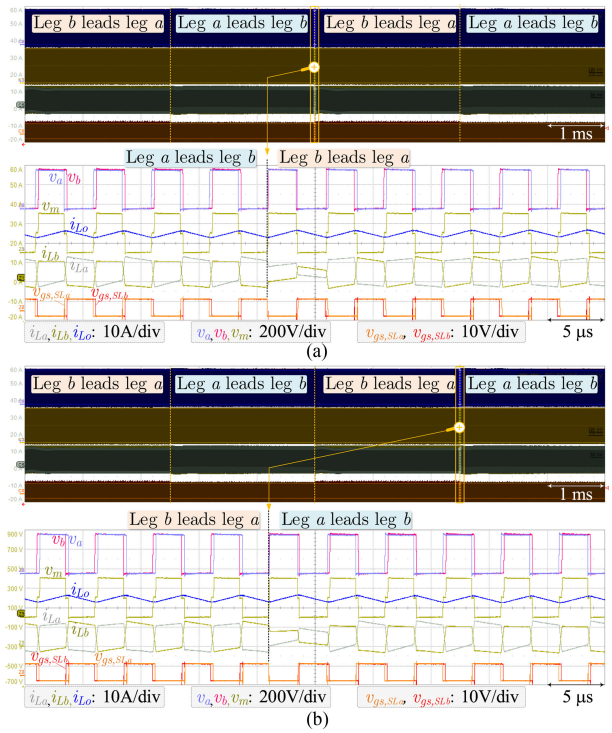


Fig. 19. Experimental waveforms with the gate signal swapping scheme for the two QCM-paralleled GaN HEMT HB legs. The output power $P_o = 1.95$ kW. (a) Transition from HB leg a leading leg b to leg b leading leg a. (b) Transition from HB leg b leading leg a to leg a leading leg b.

parallel GaN HEMT HBs to achieve high efficiencies, ranging from 98% to 99.3% when the power is above 330 W. By contrast, the efficiency of conventional synchronous CCM operation is 0.2% – 2.8% lower.

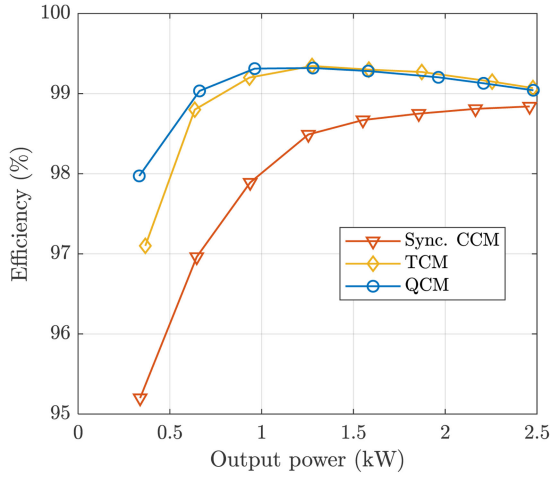


Fig. 20. Measured efficiencies of the buck dc–dc converter with different modulation schemes: synchronous CCM, interleaved TCM, and QCM.

Furthermore, the two GaN HEMT HB legs are also configured as a two-phase interleaved TCM buck converter by adding two output inductors at the output. As with the DM and output inductors for the QCM operation, the two TCM inductors are also optimized regarding their power loss and volume. The parameters of each TCM inductor prototype are as follows: 73 μH, PQ40/40 core (N97 ferrite), 25 turns (#38 AWG Litz wire, 280 strands), 60 cm^3, 4.5-W power loss at $I_{Lo} = 12.5$ A.

The measured TCM efficiencies are also shown in Fig. 20. At light loads, the QCM scheme enables higher efficiencies than the TCM solution. It is related to the high light-load switching frequency in TCM (e.g., 490 kHz at 320 W). In this case, the TCM inductor loss and the dynamic $R_{ds,\rm on}$ (conduction loss) of GaN HEMTs are pronounced. As the load increases, the TCM can achieve higher efficiencies than the QCM due to the relatively lower rms currents in TCM. On the other hand, the QCM has lower inductor losses than TCM. Therefore, at heavy loads, the QCM has close but slightly lower efficiencies compared with the TCM operation.

The proposed QCM scheme features fixed switching frequency and also has a much smaller DM inductor size: the total volume of the DM inductors for QCM is 6.72 cm^3 + 6.72 cm^3 = 13.44 cm^3; by comparison, the volume of TCM inductors is 60 cm^3 + 60 cm^3 = 120 cm^3. Therefore, the QCM scheme is more suitable for applications where only small added inductors are allowed, e.g., traction inverters.

The power loss distribution in the three operation modes (TCM, QCM, and synchronous CCM) is shown in Fig. 21. The switching loss of high-side switches, i.e., $P_{{\rm sw},SHa\&b}$, represents the highest share in the synchronous CCM operation. By comparison, the proposed QCM scheme leads to negligible switching loss due to the ZVS realization for all transistors; meanwhile, the increases in DM inductor loss and conduction loss are relatively small. Therefore, the total power loss can be reduced, particularly at partial loads. The two QCM inductors (3.3 μH) have much lower power losses than the two TCM inductors (73 μH). Therefore, at light loads, the QCM scheme has lower power losses than TCM. However, the QCM scheme

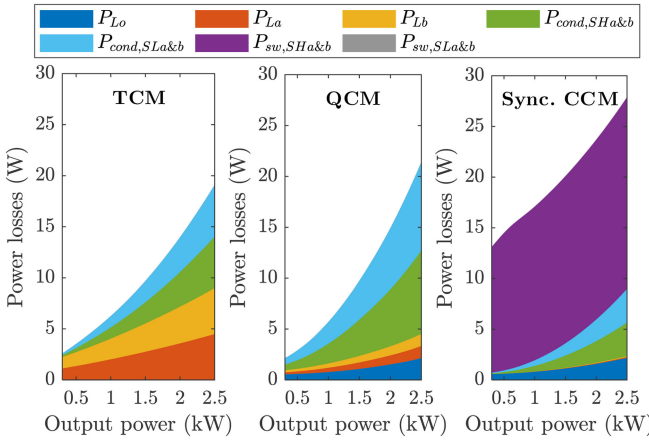


Fig. 21. Comparison of power loss distribution among three schemes: TCM, QCM, and synchronous CCM.

is of higher rms currents and higher conduction losses than the TCM, particularly at heavy loads. Thus, the resulting total heavy-load power loss in QCM is also higher.

V. Conclusion

A time-delay-based QCM ZVS scheme is proposed for parallel power MOSFETs. The operating principle, mathematical model, performance characteristics, and implementation are explored in detail. Compared with the interleaved TCM solution, this QCM-enabled paralleling scheme has higher application generality as follows.

1) The switching frequency can be either fixed or variable.
2) The operation mode can be switched from the QCM to the synchronous CCM in scenarios where the conduction loss dominates the total power loss (e.g., at low switching frequencies and high load currents).
3) This QCM-enabled paralleling solution is more suitable for inductive applications (e.g., traction inverters) due to the added much smaller commutation inductors.

A 2.5-kW 200-kHz GaN-based synchronous buck dc–dc converter prototype has been built and tested. In contrast to the synchronous operation of parallel HBs, the QCM ZVS scheme significantly minimizes the switching loss despite the increased conduction and inductor losses. As a result, the total power loss can be reduced, leading to efficiency improvements of 0.2%–2.8% within the power range of [330, 2480] W. While the measured QCM efficiencies are slightly lower than the interleaved TCM scheme at heavy loads (> 1.25 kW), the QCM operation exhibits higher efficiencies at light loads due to the much lower inductor losses.

Appendix

A. Simplified Steady-State Equations

The resonant stages are split and simplified by their adjacent nonresonant stages, as shown in Fig. 6. After the simplification, the inductor currents i_{La} and i_{Lb} within one switching cycle $[T_0, T_0 + T_s]$ are rewritten as follows.

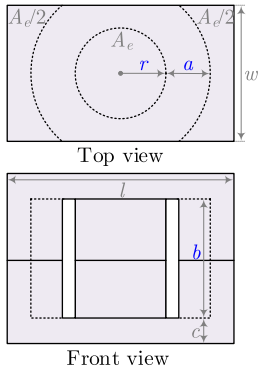


Fig. 22. Geometry and dimensions of simplified PQ magnetic cores.

Stage ⓑ $[T_0, T_1]$ [see Fig. 6 (b)]:

$$\begin{cases} i_{La}(t) = I_{La,T0} + \left(\frac{1-2D}{4L_o} + \frac{1}{2L_c}\right) V_{\rm dc}(t - T_0) \\ i_{Lb}(t) = I_{Lb,T0} + \left(\frac{1-2D}{4L_o} - \frac{1}{2L_c}\right) V_{\rm dc}(t - T_0) \end{cases} \tag{36}$$

where $I_{La,T0}$ and $I_{Lb,T0}$ are the currents of L_a and L_b at $t = T_0$, respectively.

Stage ⓓ $[T_1, T_2]$ [see Fig. 6 (b)]:

$$\begin{cases} i_{La}(t) = \left(\frac{I_{Lo,T1}}{2} - \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - T_1)\right) \\ \qquad +I_{\rm dm,T1} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - T_1)\right) + \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}} \\ i_{Lb}(t) = \left(\frac{I_{Lo,T1}}{2} - \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - T_1)\right) \\ \qquad -I_{\rm dm,T1} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - T_1)\right) + \frac{(1-D)V_{\rm dc}}{R_{ds,\rm on}} \end{cases} \tag{37}$$

where $I_{\rm dm,T1} = \frac{I_{La,T1} - I_{Lb,T1}}{2}$ with $I_{La,T1}$ and $I_{Lb,T1}$ representing the currents of L_a and L_b at $t = T_1$, respectively.

Stage ⓕ $[T_2, T_3]$ [see Fig. 6 (c)]:

$$\begin{cases} i_{La}(t) = I_{La,T2} + \left(\frac{1-2D}{4L_o} - \frac{1}{2L_c}\right) V_{\rm dc}(t - T_2) \\ i_{Lb}(t) = I_{Lb,T2} + \left(\frac{1-2D}{4L_o} + \frac{1}{2L_c}\right) V_{\rm dc}(t - T_2) \end{cases} \tag{38}$$

where $I_{La,T2}$ and $I_{Lb,T2}$ are the currents of L_a and L_b at $t = T_2$, respectively.

Stage ⓗ $[T_3, T_0 + T_s]$ [see Fig. 6 (c)]:

$$\begin{cases} i_{La}(t) = \left(\frac{I_{Lo,T3}}{2} + \frac{DV_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - T_3)\right) \\ \qquad +I_{\rm dm,T3} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - T_3)\right) - \frac{DV_{\rm dc}}{R_{ds,\rm on}} \\ i_{Lb}(t) = \left(\frac{I_{Lo,T3}}{2} + \frac{DV_{\rm dc}}{R_{ds,\rm on}}\right) \exp\left(-\frac{R_{ds,\rm on}}{2L_o}(t - T_3)\right) \\ \qquad -I_{\rm dm,T3} \exp\left(-\frac{R_{ds,\rm on}}{L_c}(t - T_3)\right) - \frac{DV_{\rm dc}}{R_{ds,\rm on}} \end{cases} \tag{39}$$

where $I_{\rm dm,T3} = \frac{I_{La,T3} - I_{Lb,T3}}{2}$ with $I_{La,T3}$ and $I_{Lb,T3}$ being the currents of L_a and L_b at $t = T_3$, respectively.

B. Parameters and Flowchart for Loss-Volume Pareto Optimization of DM Inductors

A PQ-core similar geometry is constructed, as shown in Fig. 22. The three-dimensional parameters r, a, and b are chosen as design variables. The remaining dimensions can be

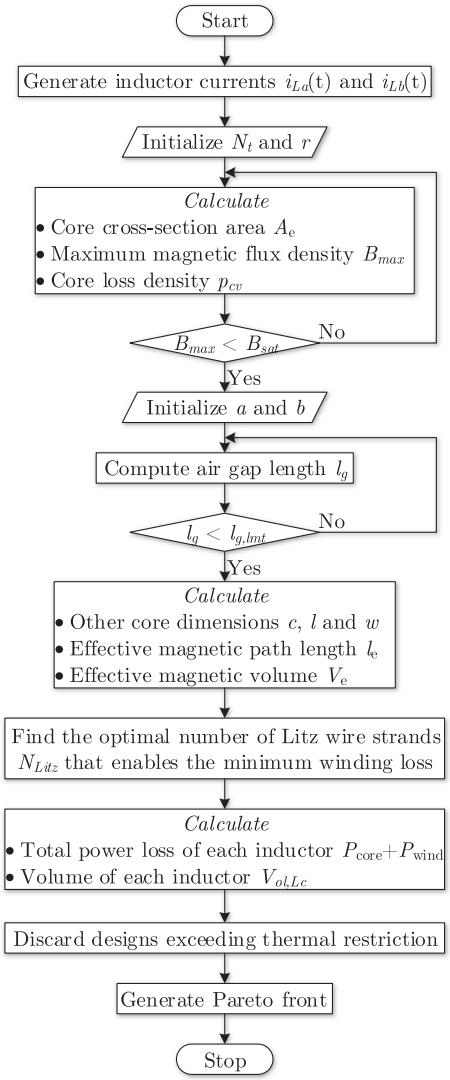


Fig. 23. Flowchart for the loss-volume Pareto optimization of DM inductors.

determined based on the same cross-sectional area along with the magnetic path.

1) The fixed DM inductor parameters are as follows.
   1) Inductance $L_c = 3.3\,\mu$H.
   2) Core material: ferrite PC95.
   3) Core shape: PQ.
   4) Coil type and wire gauge: Litz wire, #42 AWG.
   5) Optimization point: $V_{\text{dc}} = 400$ V, $V_o = 200$ V, and $P_o = 2.5$ kW.
   6) Minimum saturation current: 20 A.
2) The variable design parameters and their ranges are summarized as follows.
   1) Number of turns $N_t \in [1, 20]$.
   2) Radius of center leg of PQ core $r \in [0.15, 1.0]$ in centimeter.
   3) Window width $a \in [0.2, 1.0]$ in centimeter.
   4) Window height $b \in [0.25, 2.5]$ in centimeter.
3) The design optimization considers the following constraints.
   1) Maximum fill factor: 60%.
   2) Maximum air gap length: $b/3$.
   3) Maximum hot-spot temperature rise: 60°C.

The flowchart for the loss-volume Pareto optimization of the DM inductors is shown in Fig. 23. The core loss calculation is based on the improved generalized Steinmetz equation [48]. The Steinmetz parameters are extracted from the power loss data provided in [49]. The ac resistances of Litz wire at different current harmonic frequencies are computed using the equation given in [50].

Assume that the PQ magnetic components are cooled by natural convection, and thus, the hotspot-ambient thermal resistance model can be obtained by fitting the data given in [51]

$$R_{\text{th},ha} = 82.85 V_e^{-0.562} \tag{40}$$

where V_e represents the effective volume in cubic centimeter and the thermal resistance $R_{\text{th},ha}$ is in kelvins per watt.

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REFERENCES

[1] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy, and H.-P. Nee, "Challenges regarding parallel connection of SiC JFETs," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1449–1463, Mar. 2013.

[2] S. G. Kokosis, I. E. Andreadis, G. E. Kampitsis, P. Pachos, and S. Manias, "Forced current balancing of parallel-connected SiC JFETs during forward and reverse conduction mode," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1400–1410, Feb. 2017.

[3] J. Qu, Q. Zhang, X. Yuan, and S. Cui, "Design of a paralleled SiC MOSFET half-bridge unit with distributed arrangement of dc capacitors," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10879–10891, Oct. 2020.

[4] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100kW systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 3049–3056.

[5] Y. Shen, L. Shillaber, H. Zhao, Y. Jiang, and T. Long, "Desynchronizing paralleled GaN HEMTs to reduce light-load switching loss," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9151–9170, Sep. 2020.

[6] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[7] Q. Wu, M. Wang, W. Zhou, and X. Wang, "Current balancing of paralleled SiC MOSFETs for a resonant pulsed power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5557–5561, Jun. 2020.

[8] H. Li *et al.*"Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[9] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with Kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.

[10] J. Lu and R. Hou, "Parasitics optimization for GaN HEMTs in conventional housing-type power modules," in *Proc. Renewable Energy Energy Manage. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion*, May 2019, pp. 1–7.

[11] Z. Miao, Y. Mao, G. Lu, and K. Ngo, "Magnetic integration into a silicon carbide (SiC) power module for current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11026–11035, Nov. 2019.

[12] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 1563–1569.

[13] "Design considerations of paralleled GaN HEMT-based half bridge power stage," GaN Systems, Tech. Rep., Aug. 2016. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/01/GN004_Design-consider ations-of-paralleled-GaN-HEMT_20170612.pdf

[14] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.
[15] J. Ao, Z. Wang, J. Chen, L. Peng, and Y. Chen, "The cost-efficient gating drivers with master-slave current sharing control for parallel SiC MOSFETs," in *Proc. IEEE Transp. Electrific. Conf. Expo, Asia-Pacific*, 2018, pp. 1–5.
[16] Z. Wang, Y. Wu, J. Honea, and L. Zhou, "Paralleling GaN HEMTs for diode-free bridge power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 752–758.
[17] Y. Mao, Z. Miao, C. Wang, and K. D. T. Ngo, "Passive balancing of peak currents between paralleled MOSFETs with unequal threshold voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3273–3277, May 2017.
[18] J. Hu, O. Alatise, J. A. O. Gonzlez, R. Bonyadi, L. Ran, and P. A. Mawby, "The effect of electrothermal nonuniformities on parallel connected SiC power devices under unclamped and clamped inductive switching," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4526–4535, Jun. 2016.
[19] U.-M. Choi, I. Vernica, and F. Blaabjerg, "Effect of asymmetric layout of IGBT modules on reliability of motor drive inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1765–1772, Feb. 2018.
[20] A. Avila, A. Garcia-Bediaga, A. Rodriguez, L. Mir, and A. Rujas, "Analysis of optimal operation conditions for GaN-based power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1932–1939.
[21] S. L. Mantia, L. Abbatelli, C. Brusca, M. Melito, and M. Nania, "Design rules for paralleling of silicon carbide power MOSFETs," in *Proc. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2017, pp. 1–6.
[22] J. Lu, R. Hou, and D. Chen, "Loss distribution among paralleled GaN HEMTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1914–1919.
[23] M. R. Rogina, A. Rodriguez, A. Vazquez, and D. G. Lamar, "Improving the efficiency of SiC-based synchronous boost converter under variable switching frequency TCM and different input/output voltage ratios," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7757–7764, Nov./Dec. 2019.
[24] S. Waffler and J. W. Kolar, "Efficiency optimization of an automotive multi-phase bi-directional dc-dc converter," in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, May 2009, pp. 566–572.
[25] G. Venkataramanan, D. M. Divan, and T. M. Jahns, "Discrete pulse modulation strategies for high-frequency inverter systems," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 279–287, Jul. 1993.
[26] N. He, M. Chen, J. Wu, N. Zhu, and D. Xu, "20-kW zero-voltage-switching SiC-MOSFET grid inverter with 300 kHz switching frequency," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5175–5190, Jun. 2019.
[27] R. De Doncker and J. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, 1990, pp. 1228–1235.
[28] W. Dong, D. Peng, H. Yu, F. C. Lee, and J. Lai, "A simplified control scheme for zero voltage transition (ZVT) inverter using coupled inductors," in *Proc. IEEE 31st Annu. Power Electron. Specialists Conf.*, 2000, vol. 3, pp. 1221–1226.
[29] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[30] A. Rodriguez, A. Vazquez, M. R. Rogina, and F. Briz, "Synchronous boost converter with high efficiency at light load using QSW-ZVS and SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 386–393, Jan. 2017.
[31] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in^3 MHz GaN totem-pole PFC rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.
[32] Y. Liu, Y. Syu, N. A. Dung, Chen-Chen, K. Chen, and K. A. Kim, "High switching frequency TCM digital control for bidirectional interleaved buck converters without phase error for battery charging," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2111–2123, Sep. 2020.
[33] W. Konrad, G. Deboy, and A. Muetze, "A power supply achieving titanium level efficiency for a wide range of input voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 117–127, Jan. 2017.
[34] Z. Yao and S. Lu, "A simple approach to enhance the effectiveness of passive currents balancing in an interleaved multiphase bidirectional dc–dc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7242–7255, Aug. 2019.
[35] O. Knecht, D. Bortis, and J. W. Kolar, "ZVS modulation scheme for reduced complexity clamp-switch TCM dc–dc boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4204–4214, May 2018.
[36] F. Luo *et al.*"Analysis of CM volt-second influence on CM inductor saturation and design for input EMI filters in three-phase DC-fed motor drive systems," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1905–1914, Jul. 2010.
[37] T. Fuchslueger, H. Ertl, and M. A. Vogelsberger, "Reducing dv/dt of motor inverters by staggered-edge switching of multiple parallel SiC half-bridge cells," in *Proc. Renewable Energy Energy Manage. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion*, May 2017, pp. 1–8.
[38] R. Oruganti and F. C. Lee, "State-plane analysis of parallel resonant converter," in *Proc. IEEE Power Electron. Specialists Conf.*, 1985, pp. 56–73.
[39] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[40] S. J. Settels, J. L. Duarte, J. van Duivenbode, and E. A. Lomonova, "A 2-kV charge-based ZVS three-level inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3450–3465, Apr. 2020.
[41] F. Qi, Z. Wang, and Y. Wu, "Analysis of calculation models for device resonance in critical mode converters," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, Oct. 2018, pp. 225–230.
[42] "Metallized polypropylene film capacitors (MKP)," EPCOS AG (TDK), Tech. Rep., Feb. 2019. [Online]. Available: https://www.tdk-electronics.tdk.com/download/530754/480aeb04c789e45ef5b b9681513474ba/pdf-generaltechnicalinformation.pdf
[43] "Film capacitors, general technical information," EPCOS AG (TDK), Tech. Rep., Jun. 2018. [Online]. Available: https://www.tdk-electronics.tdk.com/download/530754/480aeb04c789e45ef5b b9681513474ba/pdf-generaltechnicalinformation.pdf
[44] G. Zulauf, M. Guacci, J. M. Rivas-Davila, and J. W. Kolar, "The impact of multi-MHz switching frequencies on dynamic on-resistance in GaN-on-Si HEMTs," *IEEE Open J. Power Electron.*, vol. 1, pp. 210–215, 2020.
[45] H. Zhao, Y. Shen, W. Ying, S. S. Ghosh, M. R. Ahmed, and T. Long, "A single- and three-phase grid compatible converter for electric vehicle on-board chargers," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7545–7562, Jul. 2020.
[46] S. Maniktala, *Switching Power Supplies A-Z*. Amsterdam, The Netherlands: Elsevier, 2012.
[47] "GS66508B, bottom-side cooled 650 V E-mode GaN transistor: Datasheet," GaN Systems, 2020. [Online]. Available: https://gansystems.com/wp-content/uploads/2020/04/GS66508B-DS-Rev-20040 2.pdf
[48] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.
[49] "Mn-Zn ferrite material characteristics," TDK, Tech. Rep., Mar. 2020. [Online]. Available: https://product.tdk.com/info/en/catalog/datasheets/ferrite_mn-zn_materi al_characteristics_en.pdf
[50] C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2667–2674.
[51] EPCOS, "Ferrites and accessories—Application notes," EPCOS AG (TDK), Tech. Rep., May 2017. [Online]. Available: https://www.tdk-electronics.tdk.com/download/531536/133c4190b4d8aac6ea0 8cc21352bf2d8/pdf-applicationnotes.pdf

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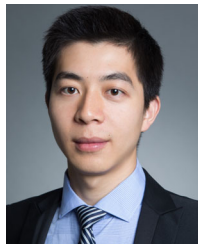

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