Online Thermal Resistance and Reliability Characteristic Monitoring of Power Modules With Ag Sinter Joining and Pb, Pb-Free Solders During Power Cycling Test by SiC TEG Chip

Dongjin Kim, *Student Member, IEEE*, Shijo Nagao, *Member, IEEE*, Chuantong Chen, *Member, IEEE*, Naoki Wakasugi, Yasuyuki Yamamoto, Aiji Suetake, Tetsu Takemasa, Tohru Sugahara, and Katsuaki Suganuma, *Fellow, IEEE*

***Abstract*—Despite the rapid progression of silicon carbide (SiC) power devices, the thermal characteristic evaluation during power cycling at high temperature (>200 °C) is an issue. In this article, a fast and miniaturized evaluation system with online thermal characteristic measurement function was introduced by an n-doped 4H SiC thermal engineering group (TEG) chip. Online thermal resistance measurement of a power module structure by Ag sinter joining with micron/submicron Ag particles paste in low temperature, low pressure, and cooling system by a thermal interface material bonding was performed. High-temperature reliability was systemically investigated by power cycling tests by switching ON/OFF the power source which is connected to the SiC-TEG chip by Au wires. The total thermal resistance of the power module from the SiC-TEG chip to the cooling system increased from 0.5 to 0.53 K/W with the enhanced power source, and remained almost same after 20 000 power cycling at a swing temperature ΔTj of 150 °C. Furthermore, the SiC-TEG power module structure with the die attached with Pb and Pb-free solders, alongwith the same power source as sinter Ag paste was also measured. The Ag sinter joint possesses the lowest thermal resistance and highest high temperature reliability during power cycling compared with Pb and Pb-free die-attach materials.**

***Index Terms*—Die-attach, online thermal resistance measurement, power cycle, SiC-TEG chip, sinter Ag paste.**

Manuscript received April 21, 2020; revised July 10, 2020 and September 3, 2020; accepted October 6, 2020. Date of publication October 16, 2020; date of current version January 22, 2021. This work was supported in part by the METI project: Standardization for Energy Conservation as International Standardization of Thermal Property Measurements for Next Generation Power Electronics, in part by the JST Advanced Low Carbon Technology Research and Development Program (ALCA) project “Development of a high frequency GaN power module package technology” under Grant JPMJAL1610, and in part by a project (JPNP14004) commissioned by the New Energy and Industrial Technology Development Organization (NEDO). Recommended for publication by Associate Editor K. Ngo. *(Corresponding author: Chuantong Chen.)*

Dongjin Kim, Shijo Nagao, Chuantong Chen, Aiji Suetake, Tetsu Takemasa, Tohru Sugahara, and Katsuaki Suganuma are with the Institute of Scientific and Industrial Research, Osaka University, Ibaraki 567-0047, Japan (e-mail: djkim@eco.sanken.osaka-u.ac.jp; shijo.nagao@sanken.osaka-u.ac.jp; chenchuantong@sanken.osaka-u.ac.jp; asuetake@sanken.osaka-u.ac.jp; ttakemasa@senju.com; sugahara@sanken.osaka-u.ac.jp; suganuma@sanken.osaka-u.ac.jp).

Naoki Wakasugi is with the Yamato Scientific Co. Ltd., Tokyo 135-0047, Japan (e-mail: naoki.wakasugi@yamato-net.co.jp).

Yasuyuki Yamamoto is with the Tokuyama Co. Ltd., Yamaguchi 746-0006, Japan (e-mail: yasu-yamamoto@tokuyama.co.jp).

This article has supplementary downloadable material available at https://ieeexplore.ieee.org, provided by the authors.

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Digital Object Identifier 10.1109/TPEL.2020.3031670

I. INTRODUCTION

POWER systems are important components in modern industries to achieve high-energy efficiency. Power electronics have become a key technology for energy generation, conversion, and storage [1]–[4].

In power electronics, the greatest aspect of power loss during the power conversion process depends on the performance of the semiconductor devices [5]. To improve this limitation of conventional silicon (Si)-based power devices, wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have been introduced and have revolutionized the power electronics components [6]–[10]. SiC and GaN can overcome the limitation of Si devices due to their excellent physical properties [11]–[18], such as a WBG (>3 eV), high critical electric field (>3 MV/cm), and a high-saturation velocity (>2×10^7 cm/s) [7]. In addition, WBG semiconductors can be operated at much higher temperatures (>250 °C) than traditional Si-based power devices (<150 °C) [5], [13], [19], [20].

Despite the technological advances of WBG semiconductor devices, the thermal characteristic evaluation and reliability in harsh conditions remain important issues [11], [21]–[23]. For instance, in the case of SiC power module, when the p-n junction on the SiC devices develops by switching ON with the number of killowatt (kW), a high temperature of over 250 °C is generated on its surface. The heat passes through the die, substrate, and thermal interface material (TIM). It reaches the base-plate and dissipates, leading to crack or delamination failure especially at the die-attached bonded interface after a long time [24]–[26]. In this process, the high-temperature reliability and thermal conduction performance of the die attach material requirements are driven by thermal considerations [24], [27]. In automotive power module qualification (AQG 324), electronic device failure is usually determined by changes in the internal thermal resistance, when the thermal resistance is increased by 20% [28], [29].

Until now, the measurement of thermal resistance characteristics and power cycling reliability for power module structures

such as SiC MOSFETs require two equipment systems. One is the power cycling system and the other is the transient thermal resistance measurement mechanism (T3Ster). The T3Ster is applied to understanding package thermal metrics and structure, calibration of thermal simulation models, reliability, and quality assessment, which can detect failure phenomenon nondestructively. For example, failures have been reported in structures around semiconductor chips, joint structures of chip-substrate-metal base plate and in joint structures [30]. However, both systems are expensive and need large space, due to which it has been difficult to apply in a wide range of applications in the power electronics domain. Most importantly, to measure the thermal resistance by T3Ster, the power cycling test must be stopped, which means that online thermal characteristic measurement of the power module structure during power cycling is impossible. Usually it is needed to stop the power cycling test many times to obtain the change of the thermal resistance and failure conditions, which influences the measurement accuracy itself. Hence, a fast and miniaturized evaluation system with online thermal resistance record functioning is needed.

Currently, lead (Pb) solders and Pb-free solders such as Sn–Cu-based solder and Sn–Ag–Cu (SAC)-based solder have been developed as die attach materials and widely applied in electrical devices. However, Pb solder is not good for human health, environment, and Pb is subject to restriction of hazardous substances regulation [31]–[35]. Sn–Cu-based solders and SAC-based solders may have issues related to mechanical reliability and thermal conduction due to low melting point and intermetallic compound (IMC) layer generation [36]–[42]. To cope with the high-temperature operation of SiC power devices, Ag sinter joining by Ag nano-paste is emerging as a die-attach material that can withstand harsh conditions such as temperatures exceeding 300 °C [43]–[46], and the sintered Ag possesses superior electrical and thermal conductivity [47]–[50]. Although some studies reported that Ag nano-paste can be sintered at low temperature and low pressure conditions [51], [52], mostly Ag sinter joining by Ag nano-paste still needs a large pressure during sintering process. Recently, some papers discussed about the reliability of the Ag nano-paste sintering die attachment and Pb solder or Pb-free solder die attachment materials during the thermal [53]–[56] or power cycling [57]–[62]. However, the maximum junction temperature T_j for the power cycling test was set as 125 °C in some papers [57], which was low and was not suitable for the WBG power device in high temperature applications. In addition, the sintering pressure of the Ag sinter joining was very high ($\sim$30 MPa) [58]–[61], which is easily lead to a damage of the chips during the sintering, and thus is very difficult application in practice.

Recently, micron/submicron Ag particles paste was reported as the die attachement and showed an excellent thermal stability and thermal-shock resistance properties [63], [64], which is demonstrated by the large number of patents filed and granted in the last five years. The main advantage for the micron/submicron Ag particles paste was its low cost, which was about one-tenth of Ag nano-paste because the micron/submicron Ag particles were very easier to make and save than that Ag nanoparticles. The micron/submicron Ag particles paste can be sintered at a low temperature low pressure (0.4 MPa) even less-pressure conditions [65], [66]. Low-cost and simply sintering process should be changed to a trend for the Ag sinter joining technology to widely apply in practice. Therefore, comparing solder joints and Ag sinter joining by Ag micon/submicron particles paste in low temperature low pressure in a power cycling tests with the maximum junction temperature $T_{j\max}$ 200 °C should be helpful to understand the thermal performance, mechanical properties, and joint reliability for next-generation power modules, and thus, choose die-attach materials in actual applications.

In this article, we present a significant advance in the measurement of thermal resistance through the junction temperature during the operation of an assembled SiC power module structure, where the thermal resistance can be measured online by using a thermal test engineering group (TEG) chip at the first instance. The junction temperature and temperature distribution of the SiC-TEG chip with input power was analyzed by experiment and simulation. In Section II, the design methodology and the details of the experiment including the SiC-TEG chip specimens and die attach structure were introduced. In Section III, the characteristics of temperature-electrical resistance of the Pt probe wire on the SiC-TEG chip were performed. In Section IV, the power cycling test was implemented by the SiC-TEG chip, which was attached on direct bonded copper (DBC) substrate by Ag sinter joining. The thermal resisitance, microstructure evolution, and fracture mode after power cycling test were discussed. Finally, in Section V, based on this characterization, the power cycling performance including the thermal performance and mechanical reliability of the SiC-TEG power module structure with Ag sinter joining was systematically evaluated and compared with that of Pb solder and Pb-free solder.

II. Experiment

A. Design Methodology

TEG chip has been widely investigated in different fields such as gas sensors, flow sensors, and other microsystems [67], [68]. In this work, the SiC-TEG chip was combined with a heater wire and a temperature sensor, both of which were evaporated together by using electron-beam evaporator process on SiC substrate. Therefore, the temperature can be measured online even with the power ON/OFF switching, which was similar with the power cycling test for the actual power device. To achieve a low power consumption and short thermal response time, the heater wire and the temperature sensor were designed with a membrane structure. Platinum (Pt) material was used as a heater wire and a temperature sensor wire due to its high heat dissipate, lower temperature coefficient of resistance and coefficients of linear expansion, ability to withstand high temperatures and high antioxidation [69]–[71]. In addition, power source with the objective to achieve fast transient response on heater wire, uniform temperature across the heater are also important, which are specifically designed and optimized by a finite-element analysis in this study and will be introduced in Section II-F.

The design methodology of the SiC-TEG chip and the thermal resistance of the die-attached structure were introducted as following. First, if a voltage source is connected across the Pt

microheater wire, it results in a current through the circuit. The Joule heat generated by the Pt heater wires on the SiC-TEG chip during operation is given as follows:

$$Q = I^2 * R \tag{1}$$

where *I* is the current traveling through the Pt heater that can be set by the power source. *R* is the electrical resistance of the Pt heater wire, which depends on the temperature and was proofread before the power cycling test. The resistance of any resistive layer is given by

$$R = Rs\,\frac{L}{W} \tag{2}$$

Here, R_S, L, and W represent the resistance, length, and width of the Pt heater wire, respectively. The heater wire resistance (R_S) is given by

$$R_s = \frac{\rho}{t}\,. \tag{3}$$

Here, ρ is resistivity of the heater wire and t is the thickness of the microheater. The heat generated by the resistive heating circuit is given as

$$\Delta Q = P\Delta t. \tag{4}$$

Here, Δt is the time. The heat produced by the heating circuit is dissipated in the ambient.

In addition, for the die-attached power modules structure, when the power source is applied, the heat generated (*Q*) by the Pt heater wire on the SiC-TEG chip passes through the die-attach material, and is finally cooled by circulating water. The thermal flow by heat conduction occurs in accordance with Fourier's law, and is proportional to the temperature gradient. Fourier's equation is as follows:

$$J = -\lambda \mathrm{gradT}. \tag{5}$$

Here, *J* is the heat flux [J/m^3], λ is the thermal conductivity [W/m^2], and *T* is the temperature [*K*]. In this system, when the temperature gradient (grad *T*) is in steady state, the thermal resistance can be calculated by

$$R_{\mathrm{th}} = \Delta T/Q \tag{6}$$

where *Q* [*W*] is the Joule heat generated by the Pt heater wires on the SiC-TEG as introduced in (1). The temperature difference ΔT can be calculated as

$$\Delta T = T_x - T_y \tag{7}$$

where T_x is the temperature of the top surface of the SiC-TEG chip, which can be measured by the temperature probe wire and T_y is the temperature of the bottom surface of the DBC substrate that can be measured by the cooling block using thermocouple measurement.

The SiC-TEG chip with the Pt heater and the Pt probe wire were introduced in Section II-B, and the die-attached power module structure in which SiC-TEG chip was attached for bonding to the DBC substrates was introduced in Section II-C, thermal resistance measurement and the power cycling test conditions were introduced in Section II-C and II-D, respectively, and finally, the finite element method (FEM) simulation for the temperature distribution of the die-attached structure in power cycling was introduced in Section II-E.

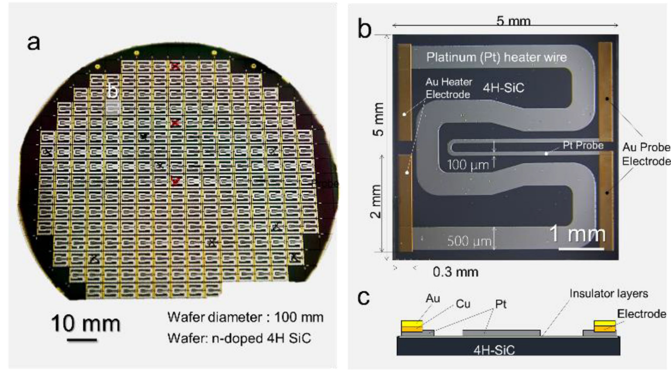

Fig. 1. (a) n-doped 4H SiC wafer. (b) Heater pattern on the SiC-TEG chip. (c) Schematic diagram of the cross section of the SiC-TEG chip.

B. SiC-TEG Chip

For this study, n-doped 4H SiC semiconductor with the dimensions of $5 \times 5 \times 0.35$ mm^3 was introduced as a TEG chip, which could be mass fabricated by a lithography technique on n-doped 4H SiC wafer as observed in Fig. 1(a). The heater pattern on the SiC-TEG chips for heat generation consisted of four components, i.e., the heater wire, heater electrode, temperature probe wire, and probe electrode as displayed in Fig. 1(b). The Pt thin film was used as the heater, which had a width of 500 μm and thickness of 200 nm. The Pt probe wire plays the temperature sensor function, which had a width of 100 μm and thickness of 200 nm. An oxide insulator layer (Al_2O_3) with a thickness of 1 μm under the Pt thin film was employed for uniform heat generation without any electrical shorting as shown in Fig. 1(c). At the electrode, Ti/Cu/Ti/Au layers were used and were orderly coated by electron-beam evaporator process on the SiC surface via a predesigned metal mask.

C. Die-Attached Structure

In this article, the SiC-TEG chip was attached for bonding the DBC substrates (Cu/Si_3N_4/Cu) by a micron/submicrion Ag paste mixed with solvent and Ag fillers, which consisted of micron-sized Ag flake particles and submicron Ag spherical particles [72]. In our previous study, DBC substrates with Si_3N_4 ceramic exhibit a better thermal stability than that with Al_2O_3 and AlN ceramics, regardless of the metallization type [73]. One side of the Cu layer on the DBC substrates was divided into five parts as shown in Fig. 2(a). The central part with a size of 6 $\times$ 6 mm^2 was used to bond with the SiC-TEG chip. Prior to Ag sinter joining, Ti with a thickness of 100 nm and Ag with a thickness of 2 μm were sputtered sequentially on the back side of the SiC-TEG chip and on the side of the five parts of the Cu layer on the DBC substrates. Ti acted as a diffusion barrier layer and Ag acted as an adhesion layer to attach the Ag paste. The Ag paste was printed on the metallized DBC substrate, and then the SiC-TEG chips were put on the hybrid Ag paste to obtain a joint structure that was mounted on a hot plating machine.

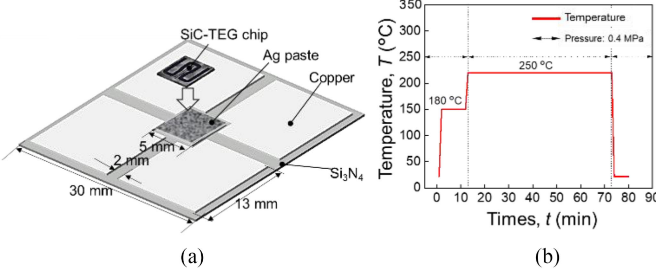

Fig. 2. (a) DBC substrate and die-attached structure. (b) Profile of the sintering process.

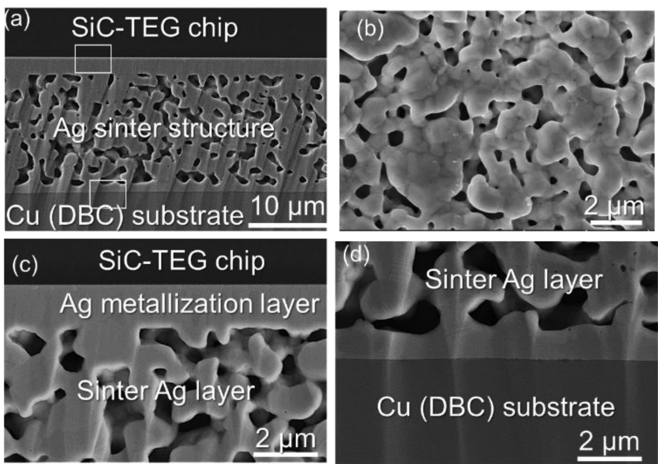

Fig. 3. (a) Cross section of the die-attached structure by sinter Ag joining. (b) Sintered Ag surface at the sintering temperature of 250 °C. (c) Bonding interfaces between the SiC-TEG and sintered Ag paste. (d) Sintered Ag paste and DBC substrate.

The sintering temperature was set as 250 °C and the sintering time was 30 min with a low-assisted pressure 0.4 MPa during the sintering process. The temperature rate and presintering temperature are displayed in Fig. 2(b). Fig. 3(a) and(b) shows the cross section of the die-attached structure by Ag sinter joining, and the surface of the sintered Ag paste, respectively, where the sintered Ag paste exhibited a micron-sized porous structure with Ag particles causing necking growth. The bonding interfaces between the SiC-TEG and sintered Ag paste, sintered Ag paste, and DBC substrate are shown in Fig. 3(c) and (d), respectively, where the sintered Ag paste tightly adheres to the chip and substrate by interface necking growth and interdiffusion with Ag metallization.

D. Online Thermal Resistance Measurement System

To evaluate the steady-state thermal resistance of the die-attached power modules, a measurement system of thermal property characterization was constructed with the SiC-TEG chip, power supplier, and controller as shown in Fig. 4(a). The SiC-TEG power device that was attached on a DBC substrate by Ag sinter joining was fixed on a water cooling system at the temperature of 25 °C by a TIM. The power source electrode was applied on Cu islands of DBC substrates, which transported to the SiC-TEG chip at the Au electrodes of the cathode and anode

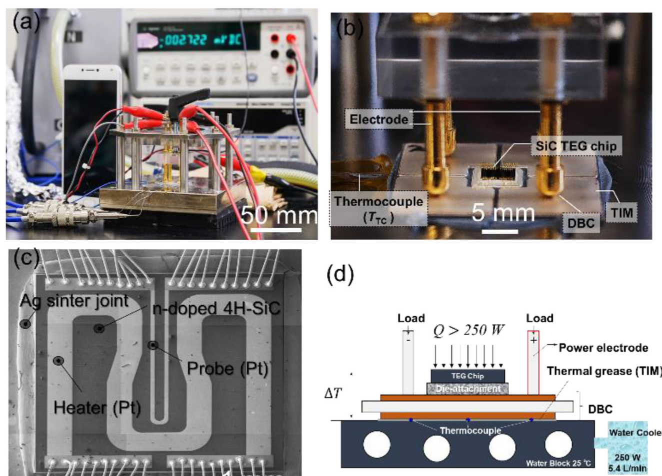

Fig. 4. (a) Measurement system of thermal property characterization. (b) Power source electrode applied on the DBC substrate. (c) SEM image of the SiC-TEG chip connected to the DBC by Au wires. (d) Schematic diagram of the thermal characterization evaluation system of the SiC-TEG chip die-attached structure.

through Au wires as shown in Fig. 4(b). The diameter of the Au wire was 0.45 μm and there were ten Au wires connected to one heater electrode. The probe electrode was similarly connected to the Cu islands on the DBC substrate as the actual SiC chip surface temperature sensor electrode as observed in Fig. 4(c). The power source could achieve a maximum value of 240 W to heat the SiC-TEG chip by the Joule heat of the Pt heater wires. Nano-diamond thermal grease (Ainex, JP-DX1) was applied as a TIM between the DBC substrate and water-cooling heat sink in this experiment. The generated heat on the SiC-TEG chip surface was transferred to the water cooling plate throughout the sintered Ag paste and the DBC substrate, and finally dissipated by the external circulation cooling system. Fig. 4(d) shows the schematic of the thermal characterization evaluation system of the SiC-TEG chip die-attached structure.

E. Power Cycling Test

In this article, the condition of the power cycling test was switched ON for 2 s and then switched OFF for 5 s up to maximum power 240 W (I = 2 A and $V \leq$ 120 V) repetitively. The temperature of the cooling water was controlled to be 25 °C by using a water circulation unit system. The water flow rate was 5.4 L/min. The constant current (I = 2 A) mode for heating was tested, and constant current was necessary to suppress the surge spike when the SiC-TEG chip heating started. The change of temperature of the SiC-TEG chip and the input voltage and power during one power cycling test is exhibited in Fig. 5(a). The temperature was calculated from the electrical resistivity of Pt, which was the Pt heater wire temperature and was proofread before the power cycling test. It was seen that the maximum junction temperature $T_{j\max}$ was approximately 200 °C at the power on state and was approximately 50 °C at the power OFF state. The swing temperature ΔT_{j} in this study was 150 °C. The paramaters for the power cycling test are listed in Table I. When

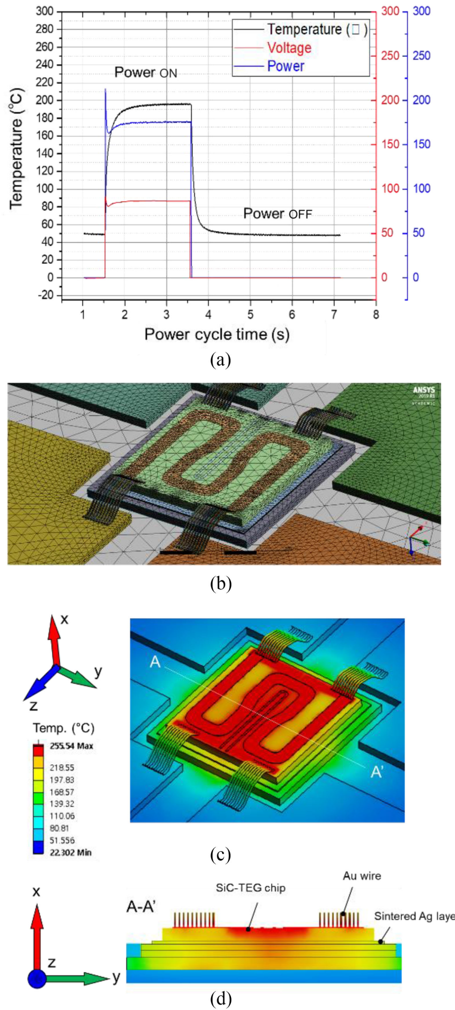

Fig. 5. (a) Change of temperature of the SiC-TEG chip and the input voltage and power during one cycling test. (b) Simulation model with meshed size. (c) Temperature distribution in the case of the power source being ON by finite element simulation. (d) Temperature distribution in the vertical direction.

TABLE I
POWER CYCLING TEST CONDITIONS

Stress current (I_s)	Stress volatge (V)	Stress time (s)	Cooling time (s)	Minimum junction temperature (T_j °C)	Maximum junction temperature (T_j °C)	Temperature Swing (ΔT_j °C)	PCT cycles (N)
2	110	2	5	50	200	150	20 000

the power source was in ON mode, the temperature difference between the top of the SiC-TEG chip and the bottom of the DBC substrate and the thermal resistance of the die-attached power module were automatically calculated and recorded during the power cycling test. The change of the temperatures of the heater and probe could be monitored online during the power cycling test through this system.

F. Finite Element Simulation Methodology

In this study, thermal simulation was performed to understand temperature distribution of SiC die-attached each layers at the maximum junction temperature $T_{j\max}$. A commercial finite-element analysis (FEA) solver of ANSYS workbench with the version of R1 was applied for the thermal simulation. The type of FEM simulation was steady-state thermal analysis. The finite-element model, boundary condition, and material properties are provided in the supporting information file. The refinement mesh ordering level 3 in ANSYS workbench was first applied for all the model parts, which divided to all faces by an auto mesh generation method without mesh sizing function in order to reduce the error of calculation. In addition, to ensure the analysis accuracy, the main observation object in the die-attachment layer was made to generate a refine mesh in three layers by using refinement function in ANSYS workbench. In this process, no optimization program was applied. The total nodes of the meshed model were 235 065 and the elements number were 102 100. The minimum mesh size was 5 μm in this simulation model. In addition, the type of mesh was dominantly divided by four-node tetrahedral elements, and the mesh quality of the part to be observed is a value of 0.75, which is close to 1, an ideal value by the mesh metric evaluation. Fig. 5(b) shows the meshed model in the magnified view of SiC-TEG.

After the mesh division, the material properties are assigned to the module components (see the supporting information). As the boundary conditions for this FEM analysis, 220 W was applied into the Pt heating wire on the SiC chip, and the temperature of 50 °C was set in the heatsink which was under the DBC substrate. The conditions are same as the cooling condition shown in Fig. 5(a). In addition, since the mechanical response by the heat is not calculated, geometric boundary conditions, e.g., fixed support, Ux, Uy, Uz = 0 are not applied. In particular, due to the actual power cycling test (PCT) is performed at room temperature, only heat transfer at the surface of the FE model were considered as boundary conditions were considered only heat transfer due to natural heat convection at the surface of the model.The heat convection on the model surface was set as $5 \times 10E\text{-}6$ W/mm^2.

Then, assuming that the thermal conductivity coefficient (k) is isotropic, it can be calculated by the 3-D Fourier's thermal conductivity equation as follows [74]:

$$\frac{\partial T^2}{\partial x^2} + \frac{\partial T^2}{\partial y^2} + \frac{\partial T^2}{\partial z^2} + \frac{\dot{e}_{gen}}{k} = \frac{1}{a}\frac{\partial T}{\partial t} \tag{8}$$

$$a = \frac{k}{\rho c} \tag{9}$$

where T is temperature in x-, y-, and z-directions, a is a thermal diffusivity, c is a specific heat, and ρ is a density of material. In this process, since the actual chip surface was isolation/insulated by sputtered deposition from the air, the analysis conditions are assumed to be insulated.

Fig. 5(c) shows the temperature distribution in the case of the power source being ON by finite-element simulation, where the red zone represents the Pt heater wire with the maximum temperature about 250 °C. It can be observed that the temperature was almost uniformly distributed on the SiC-TEG chip surface and was maximum at the Pt heater wire. In addition, the yellow zone on the SiC surface represents the actual temperature of

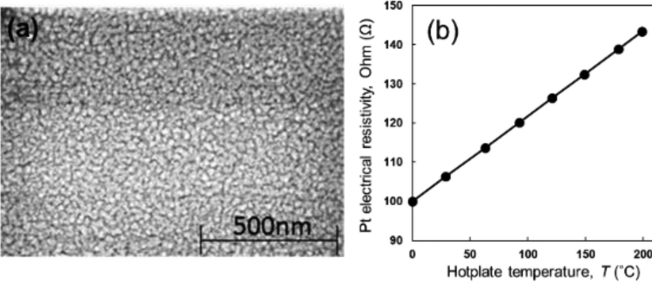

Fig. 6. (a) SEM image of the surface microstructure of the Pt probe wire. (b) Linear relationship between the electrical resistance and temperature characteristics of the Pt probe wire.

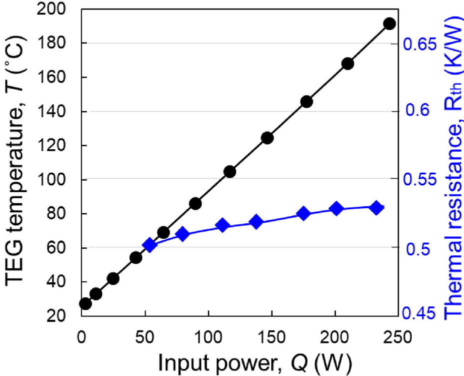

Fig. 7. Relationship between the SiC-TEG temperature, thermal resistance of the power module, and input power.

SiC chip, which was equal to the temperature of the Pt probe wire. The temperature can be simulated from the contour with the temperature range from 197 to 218 °C. The temperature was close to the actual temperature of the die attach material for the SiC device. Fig. 5(d) shows the cross section of the temperature distribution when the power source was ON. For the sintered Ag layer, the temperature has a range from 168 to 197 °C, which was an acceptable range to compare with the measured value from the experiment.

III. Temperature–Electrical Resistance

A. *Voltage Precursor Parameter Monitoring in PCT*

Fig. 6(a) exhibits the SEM image of the surface microstructure of the Pt probe wire deposited on the chip by lithography process. The grain size of the Pt probe wire was approximately 30 nm, which was smaller than that of the bulk Pt grains. Therefore, the electrical resistance and temperature characteristics of the Pt probe wire on the SiC-TEG chip could differ from that of bulk Pt. Hence, the temperature characteristics of the Pt probe wire on the SiC-TEG chip were calibrated before proceeding with the power cycling test. In order to evaluate the relationship between the electrical resistance and temperature characteristics, the SiC-TEG chip was bonded on the DBC substrate by Ag sinter joining as introducted in Section II. The joint structure was mounted on a hot plate where the heating temperature was changed from room temperature to 200 °C. When the input power was applied to the chip, the electrical resistance of the Pt heater wire can be calculated by (1) in Section II. The change in the electrical resistance value of the Pt probe wire was recorded by the standardized least-squares method. In addition, to obtain an accurate temperature of the Pt probe wire, two thermocouples were set on the Pt probe wire surface during the hot plate heating. Therefore, the relationship between the electrical resistance and temperature characteristics of the Pt probe wire can be obtained by changing the temperature of hotplate. It was confirmed that the electrical resistivity increased with higher temperature and a linear relationship was observed as shown in Fig. 6(b). The Pt probe was found to be approximately 0.725 Ω/°C. The Pt probe wire formed on the TEG chip can be used as a resistance thermometer.

Based on the temperature–electrical resistance of the measured voltage characteristics of the Pt probe wire, its temperature can be calculated using the input power for the SiC-TEG die-attached DBC structure bonded by Au wires as shown in Fig. 4(b). A constant current ($I = 2$ A) was set for the input power, and the voltage was adjusted from 0 to 120 V. The relationship between the input power and temperature of the Pt probe wire was obtained. As the Pt probe wire was coated on SiC, its calculated temperature could represent the SiC-TEG temperature. The linear relationship between the SiC-TEG temperature and the input power was successfully obtained as shown in Fig. 7. The maximum temperature was approximately 200 °C at the input voltage of 120 V. Therefore, it has been verified that the SiC-TEG chip can measure the heat through this linear electrical–thermal characteristic. Fig. 7 also shows the relationship between the thermal resistance R_{th} of the SiC-TEG power module with input power. The current in this case was also set as 2 A. The R_{th} was calculated using (2), and it changed from 0.5 to 0.53 K/W with increase of the input power from 50 to 240 W. The slight increase of the thermal resistance R_{th} may have been induced by the increase of the thermal conduction of the materials at higher temperature.

IV. Power Cycling Test

A. *Thermal Resistance Evaluation*

The steady-state thermal resistance is an important indicator for evaluating the thermal performance of die attach materials. Since the temperature of Pt heater wire and Pt heater probe can be measured online, the temperature change during the power cycling can be recorded, which can judge the power modules' reliability because the temperature should increase when some parts in the power modules fail. In addition, by recording the temperature of the thermocouple under the DBC substrate, the thermal resistance of the whole SiC-TEG power module can be calculated online. Fig. 8(a) shows the temperature change during power cycling in the power ON-state, including the Pt heater wire, Pt heater probe, and the temperature measured by the thermocouple under the DBC substrate. The temperature of the Pt heater wire and Pt heater probe slightly changed during the power cycling, and finally increased approximately 4% after 20 000 cycles. The temperature under the DBC substrate measured by the thermocouple changed minimally.

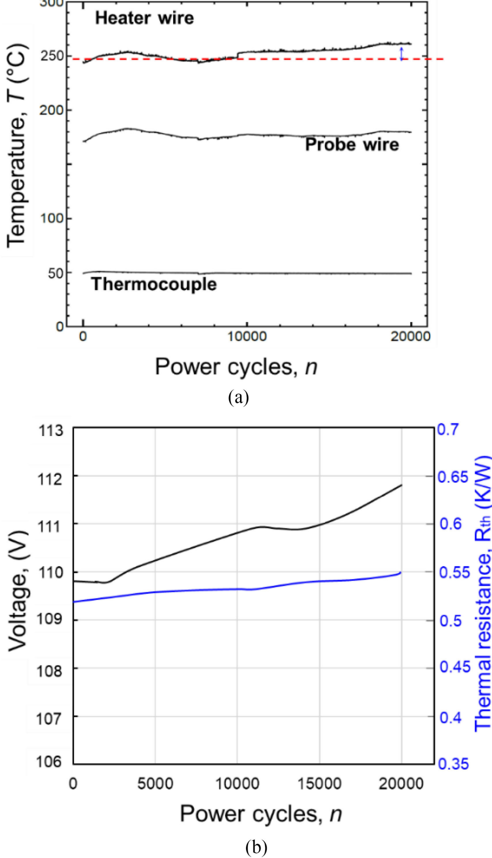

Fig. 8. (a) Temperature change of the Pt heater wire, Pt heater probe, and the temperature measured by thermocouple under the DBC substrate during power cycling. (b) Actual measured voltage and thermal resistance of the die-attached power module during the power cycling test.

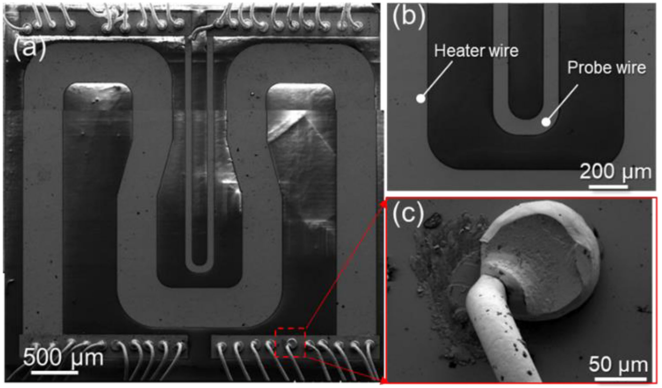

Fig. 9. (a) SEM image of the SiC-TEG surface after 20 000 power cycles. (b) Enlarged view of the Pt heater wire and Pt probe wire at the corner. (c) Liftoff of one of the Au wires.

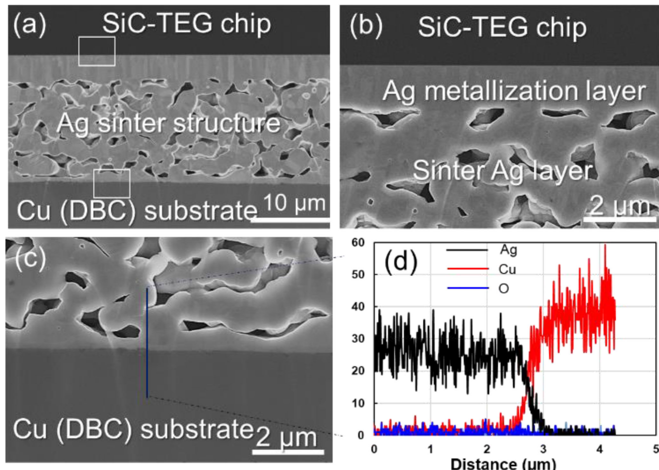

Fig. 10. (a) Cross section of the die-attached structure by Ag sinter joining after 20 000 power cycles. (b) Bonding interface between SiC-TEG and sintered Ag paste. (c) Bonding interface between the sintered Ag paste and DBC substrate. (d) EDS element line mapping of the interface between the sintered Ag paste and substrate.

The power cycling test was applied for 2 s ON and 5 s OFF up to 220 W ($I = 2$ A and $V = 110$ V) repetitively. Although the applied voltage remains 110 V, the measured voltage was increased during the power cycling as shown in Fig. 8(b), which also is an indicator to check the device's reliability. The increase of voltage is analyzed and discussed in the next subsection by investigating the microstructure evolution of sintered Ag and Au wire bonding state. In addition, the thermal resistance R_{th} of the SiC-TEG power die-attached structure by sinter Ag joining was recorded during the power cycling, which increased slightly from the initial value 0.53 to 0.55 K/W after 20 000 cycles. These results indicate that the SiC-TEG power die-attached structure fabricated by Ag sinter joining possessed excellent thermal stability and power cycling reliability. The slight increase in the thermal resistance R_{th} was analyzed by SEM cross section observations and is introduced in the next subsection.

B. Failure Analysis and Microstructure Evolution

In order to analyze the voltage increase during power cycling, the SiC-TEG was observed after power cycling as shown in Fig. 9(a). The Pt heater wire and Pt probe wire were still tightly connected to the SiC chip. There were no microcracks or delamination in SiC even in the corner as observed in Fig. 9(b). Therefore, the voltage increase could not have been induced by the Pt heater wire or Pt probe wire. However, it was found that one of the Au wires delaminated from the Au heater electrode. The surface of the Au heater electrode was also damaged around the Au wire bonding, which may have been caused by excessive heat transfer at the location of the bonding after the development of cracks and delamination. In general, the damage of the wire bonding initiates from a tiny crack and can propagate over time to cause open-circuit or short-circuit failure [75]–[77]. In addition, the deformation of the bond wires and their length variation can also escalate the damage. The increase of the measured voltage is mainly induced by the damage or crack generation in the Au wires during the power cycling test.

Fig. 10(a) shows the SEM image of the cross section of the die-attached structure by Ag sinter joining after 20 000 power cycles. The bonding interfaces between the SiC-TEG and sintered Ag paste, sintered Ag paste, and DBC substrate are shown in Fig. 10(b) and (c), respectively, where the sintered Ag paste is still tightly connected to the chip and substrate. No interface

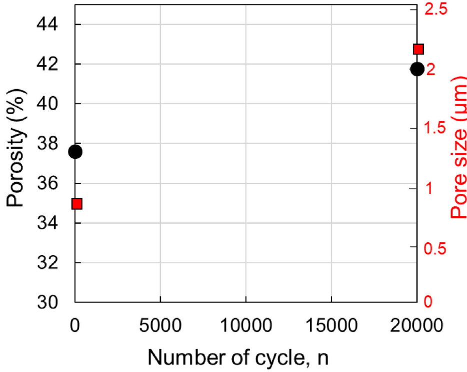

Fig. 11. Average pore size and change in porosity of the sintered Ag paste before and after power cycling.

voids or interface delamination generation are observed after the power cycling test. Fig. 10(d) shows the energy dispersive X-ray spectroscopy (EDS) line analysis of the bonded interface of the sintered Ag paste and DBC substrate after power cycling. The Ag and Cu interface appears to have undergone slight interdiffusion. Oxygen is not detected at both the sintered Ag layer and Cu substrate, and the bonding interface, which means that there is no Cu metal oxide generation. Therefore, the interface thermal resistance between the sintered Ag layer and chip, sintered Ag layer, and substrate is not significantly influenced during the power cycling test.

However, compared with the initial sintered Ag layer as shown in Fig. 3(a), Ag grain coarsening phenomenon can be observed after power cycling. This implies that both the Ag grain size and pore size become coarser, while the number of pores decreases significantly [78], [79]. The average pore size is measured by the area of all the pores (porosity $*$ given area) divided by the number of pores, which increases from 0.85 to 2.15 μm after power cycling. In addition, the porosity of the sintered Ag paste also increases from the initial value of 35% to 42% after power cycling. As the thermal conduction of the sintered Ag layer largely depends on its porosity, the thermal resistance $R_{\rm th}$ changes as shown in Fig. 8(b). This may have been induced by the increase of the porosity of the sintered Ag layer during power cycling as shown in Fig. 11.

C. Shear Strength and Fracture Mode

As the die shear strength is a key index for evaluating the performance of the die-attached structure, the shear strength is also evaluated. The initial die shear strength of the 5 $\times$ 5 mm^2 sized chip with the same Ag hybrid paste and for the same sintering process as this study can be referred in our previous studies, where the die shear strength was evaluated as 33.3 MPa [80]. After 20 000 power cycles, to evaluate the die shear strength, the Au wires were cut from the chip and substrate. The die shear strength of the power module structure was evaluated by a shear tester (Nordson Dage 4000, Japan) with the shear speed of 50 μm/s. The die shear strength was evaluated as 21.3 MPa after 20 000 power cycles. The degradation of the die shear strength may be attributed to the porosity and pore size changes after power cycling. Compared with most solder materials that have an initial die shear strength less than 25 MPa [81]–[83], Ag sinter joining shows excellent power cycling reliability.

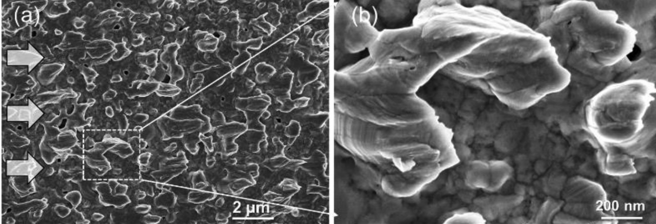

Fig. 12. (a) Fracture surface of the DBC substrate after the die shear test. (b) Magnified view of the fracture surface.

TABLE II
PHYSICAL PROPERTIES OF PB AND PB-FREE SOLDER MATERIALS

Materials	Melting temperature (°C)	Thermal conductivity (W/mK)	CTE (×10^{-6}/K)	Young's modulus (GPa)
Ag sinter paste	>900	250	22.7	12.9
Pb–5Sn	312	36	28.4	28.4
Sn–Cu–Ni–P solder	230	64	21.0	54.2
Sn–Ag–Cu–Sb solder	226	57	24.2	46.2

Fig. 12. (a) SEM image of the fracture surface of the DBC substrate after the die shear test. The direction of the arrow represents the direction of shear loading. It can be clearly observed that the fracture occurred at the Ag grain necking location near the interface between the sintered Ag paste layer and DBC substrate. Large plastic deformation at each Ag grain necking location appeared as observed in (b), implying that the Ag grain necking were subjected to a large shear stress before ductile fracture.

V. MATERIAL JOINTS

A. Thermal Resistance Evaluation

Furthermore, the thermal resistances of the SiC-TEG power module structures fabricated by dies attached with Pb and Pb-free solders with the same power source as Ag sinter joining were also measured to evaluate the reliability of Pb and Pb-free solders and compare with Ag sinter joining. In this study, Pb-5Sn solder and Pb-free solders including Sn–Cu based solder (Sn–Cu–Ni–P) and SAC-based solder were employed for the comparison of the thermal performance and power cycle reliability as they are commonly used as high temperate solders in current power devices. The physical properties such as the melting point and thermal conductivity of these solder materials and Ag sinter paste are shown in Table II. The Pb and Pb-free solder material joints and processes are shown in supporting information. In order to obtain structurally sound bonding without any critical defect, the soldering and cooling process was performed under formic and nitrogen gas atmosphere. The thermal resistance of

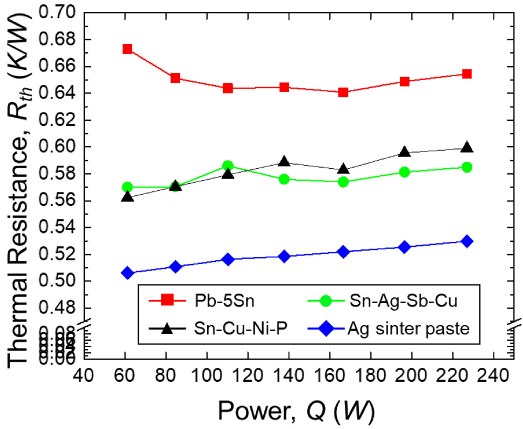

Fig. 13. Thermal resistance of the SiC-TEG chip die-attached structure by various die attach materials at different input power.

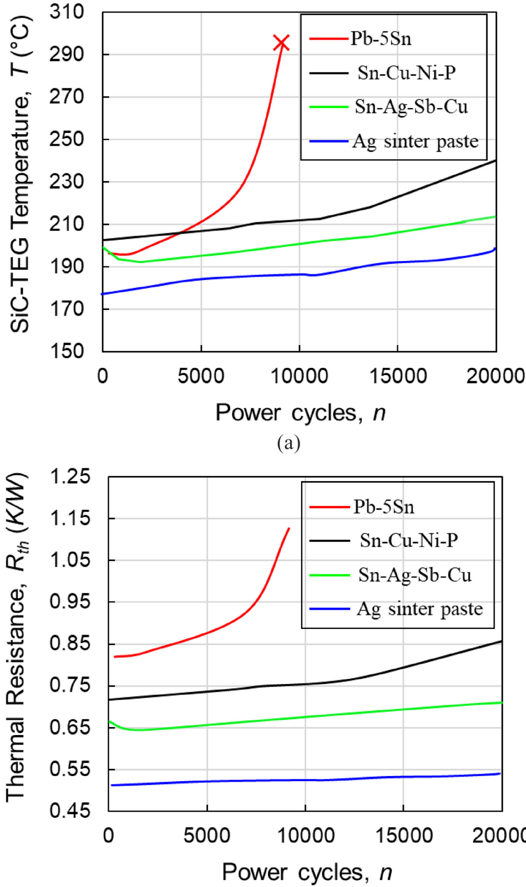

Fig. 14. (a) SiC-TEG chip temperature. (b) Change of thermal resistance of the die-attached structures by various solders and Ag sinter joining during power cycling.

each SiC-TEG chip die-attached structure fabricated by various solder materials was measured based on the measurement system of Fig. 4.

Fig. 13 shows the thermal resistance of SiC-TEG chip die-attached structures fabricated by various die attach materials in steady-state thermal resistance measurements with different input power. The magnified interface bonding views revealed that the Ag_3Sn and Cu_6Sn_5 IMC layer were generated in the Pb-5Sn solder joint and also some voids generated around the IMC layer. Initial state of Sn–Cu–Ni–P solder joints also show structurally sound bonded both side of interfaces without any serious defect. The thermal resistance of the die-attached structures by Pb-free solder materials and Ag sinter paste show an increasing trend with larger input power values, where the current is always set as 2 A. The thermal resistance of Sn–Cu based solder joint is increased from 0.56 to 0.59 K/W, that of SAC-based solder joint is increased from 0.57 to 0.58 K/W, and from 0.5 to 0.52 K/W for Ag sinter joining. The thermal resistance of Pb-5Sn solder joint shows a slight decrease and remains almost unchanged with the increase of input power. However, at the same input power, the Pb-5Sn solder joint appears to possess the highest thermal resistance and Ag sinter joint has the lowest value among these die attach materials. The result corresponds to the thermal conductivity properties of these materials as shown in Table II. A lower thermal resistance value implies quicker heat dissipation characteristics of the SiC-TEG die-attached structure due to better thermal properties of the die attach material itself.

Fig. 14 shows the results of the power cycling test for various solder and Ag sinter joint structures. The input power for all kinds of die-attached structures was 220 W with current constant mode where the current was 2 A and the input voltage was 110 V. The maximum cycle number was set as 20 000 as this value is sufficient for the reliability test of most solder materials. The SiC-TEG chip temperature was calculated by the measured voltage and electrical resistivity of the Pt heater probe, which was recorded in the power ON-state during power cycling as observed in Fig. 14(a). All temperature changes induced by the input electrical power changes were stored in real time in the controller machine during the power cycling tests. The temperature of Pb-5Sn increased to greater than 290 °C after 8800 cycles and automatically stopped working. The increase of temperature and thermal resistance were analyzed in detail by the observation of the cross section of Pb-5Sn joint after power cycling, which will be introduced in the next section.

Lead-free solders start operating at a significantly higher thermal resistance than the Ag sinter joint, and the thermal resistance rises gradually as switching increases up to 20 000 cycles as shown in Fig. 14(b). This occurred because different SiC-TEG power modules were used for power cycling, the thermal resistance value in Fig. 13 was a little different from the thermal resistance value at the start of the power cycle test in Fig. 14(b). Difference in thermal resistance between Figs. 13 and 14(b) is attributed to not only the different module used for the power cycling test but also the setting during the cycle test is different. The thermal resistance R_{th} can also be recorded online for the SiC-TEG die-attached structures with various solders and Ag sinter joining. Similar to the increasing trend of SiC-TEG chip temperature, the thermal resistance R_{th} of the

die-attached structure by Pb-5Sn significantly increases until the structure fails. The thermal resistances R_{th} also increase with Pb-free solders and Ag sinter joint during power cycling and the thermal resistance behavior of Ag sinter joint surprisingly exhibits the lowest value and is kept intact in the same condition as the starting point of the power cycling test. This is due to its excellent thermal performance, which rapidly dissipates the Joule heat generated during repetitive switching, thereby suppressing mechanical damage. The power dependence of thermal resistance can be readily expected due to the inherent thermal conductivity differences in the ON state. In addition, in the case of ON/OFF switching, the mechanical properties inherent to the material, which are modified by repetitive heat generation and heat sink, are also taken into account, and result in thermal resistance increase due to high thermal density generation on the device surface.

B. Failure Analysis and Microstructure Evolution

The formation of cracks and voids in SiC-TEG die-attached structures with solders and Ag sinter paste joining before and after the power cycling test were observed by nondestructive inspection through a micro focus 3-D computed tomography (CT) X-Ray system (XVA-160N, Uni-Hite System Corporation, Japan). It is found that there are no voids or delamination occurences in the sinter Ag joined structure before and after the power cycling test as shown in Fig. 15(a) and , respectively. Hence, it can be inferred that the sinter Ag joined structure had an appropriate interface bonding ratio during the sintering process and high power cycling reliability. For the Pb-5Sn solder joint, there are many voids inside the solder and at the bonded inferface after the soldering process as shown in Fig. 15(c), which concurs with other studies [63], [84]. The number of voids increases and the void size is also enlarged in Fig. 15(d) after the power cycling test for 8800 cycles, which must have been induced by the generated thermal stress and unstable phase transition of Pb-5Sn during the high-temperature operation. The initial Sn–Cu based [Fig. 15(e)] and SAC-based solder joints [Fig. 15(g)] also exhibit many voids during the soldering process, and the number and size of voids also grow after the power cycling test similar to the Pb-5Sn solder joint as observed in Fig. 15(f) and (h). As the thermal resistance properties of the die-attached structure should be considerably influenced by the void formation rate or interface crack generation, the rapid increase of the thermal resistances R_{th} of the Pb solder and Pb-free solder joints during the power cycling test as shown in Fig. 14 must be related with the number of voids and their growth.

Another reason for the increase of the thermal resistances R_{th} of the Pb solder and Pb-free solder joints may be attributed to the generation of complex and fatal defects such as IMCs due to repetitive heat generation. Fig. 16 shows the SEM cross section image of the IMC growth behavior of the Pb and Pb-free solders after power cycling tests. Large voids are generated inside the solder as well as at the bonded interface in the Pb-5Sn solder joint as observed in Fig. 16(a). The IMC layer increases at both bonded interfaces as observed in Fig. 16(b)

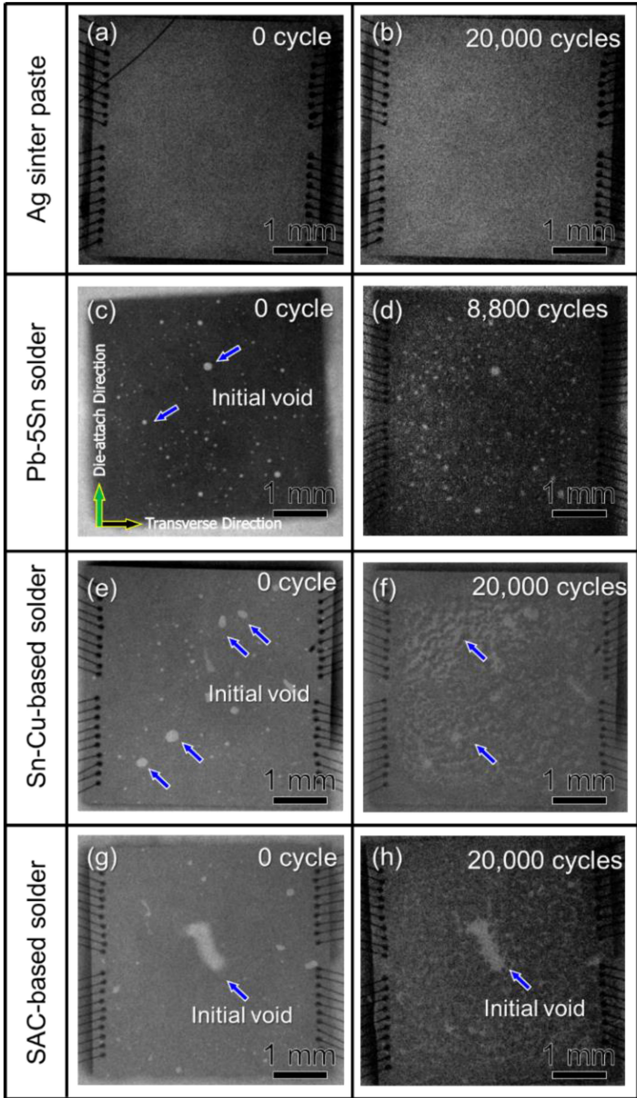

Fig. 15. X-ray image of Ag sinter paste, Pb-5Sn solder, Sn–Cu-based solder, and SAC-based solder (a), (c), (e), and (g) before and (b), (d), (f), and (h) after power cycling.

and (c), where the solder materials reacted with the metallization layers on the bottom side of SiC and the top side of the DBC substrates. The composition of the generated IMC layers are marked in the corresponding figures and were analyzed by EDX element mapping. After power cycling, voids and empty spaces significantly occurred between SiC-TEG and Pb-5Sn interface, main defect formed between SiC-TEG and Pb-5Sn solder joint with massive void space with Ag–Sn systems IMC. For the Sn–Cu based solder joint as shown in Fig. 16(d), no large voids are generated inside the solders after the power cycling test. However, many large cracks and voids are generated along the bonding interfaces [Fig. 16(e) and (f)], especially at the interface between the solder and DBC substrate as observed in Fig. 16(f), where continuous cracks are generated.

It is also found that the IMC and void generation for the SAC-based solder joint in Fig. 16(g) is different from the Cu–Sn based

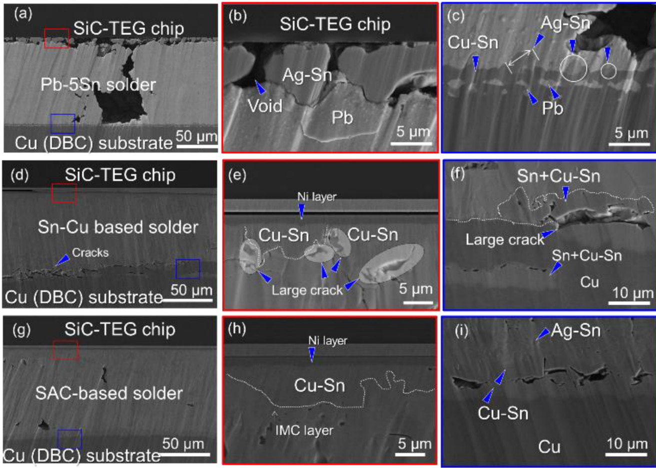

Fig. 16. SEM cross section image of the (a) Pb-5Sn solder joint, (d) Sn–Cu based solder joint and (g) the SAC-based solder joint, (b), (e), and (h) the bonded interface between the SiC-TEG chip and solder materials, and (c), (f), and (i) the bonded interface between the solder materials and DBC substrate after power cycling test.

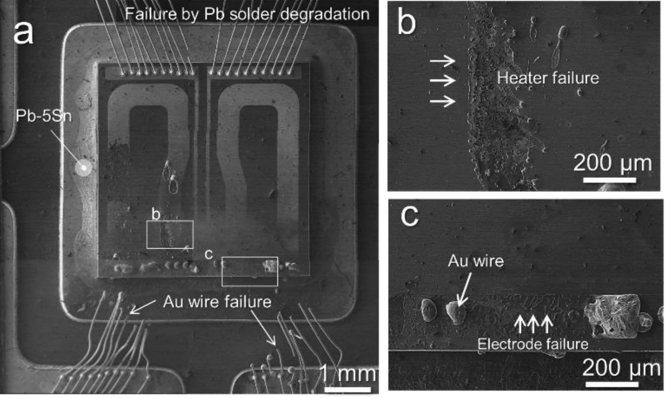

Fig. 17. (a) SEM of the top surface of SiC-TEG of the Pb-5Sn joint structure after power cycling. (b) Magnified view of the heater wire. (c) Magnified view of the electrode.

solder joint after the same number of power cycles, where the voids are mainly generated at the interface between the solder and DBC substrate [Fig. 16(h) and (i)], but the cracks are not as severe as compared with the case of the Cu–Sn based solder joint. In addition, in all solder joints, the thickness of the IMC layers has grown approximately twice than in as-bonded state (see the supporting information). Here, the type of IMC was additionally found where $(Cu_{1-x}Ni_x)_6Sn_5$ near Ni layer on the SiC-TEG side was analyzed with the Ni: 2.49, Sn: 42.04, and Cu: 20.31 (element at%). IMC growth will be considered more precisely with TEM investigation or XRD analysis in future work. Thus, it can be clearly observed that IMC growth is an inevitable result of ON/OFF switching of the power conversion system for all kinds of solder materials.

For the Pb-5Sn solder joint, the failure occurred after 8800 cycles, which was lesser than that of the other Pb-free solder and Ag sinter paste joints. The reasons were further investigated by the SEM of the top surface of SiC-TEG after failure as observed in Fig. 17(a). The Pt heater wire and Pt probe wire were seriously damaged. The magnified view of the heater wire can be observed in Fig. 17(b). The surface of the Pt heater wire was subjected to severe cracks and damage on SiC. However, it was found that all the Au wires delaminated from the Au heater electrode and the tip of the Au wires assumed a large spherical shape, which usually is induced when metal wires are subjected to a high temperature. The surface of the Au heater electrode was also completely damaged around the Au wire bonding, which may have been caused by excessive heat transfer at the bonding location after the occurrence of cracks and delamination.

VI. Conclusion

In this article, an online direct thermal characterization measurement system was introduced during a power cycling test in a 4H SiC-TEG chip die-attached power module. In the case of die attach materials, four kinds of die attach materials are compared. These include lead/lead-free solders and Ag sinter paste for performance evaluation in steady state. The order of performance in terms of the thermal resistance has been found to be Ag sinter paste, lead-free solders, and lead solder. This is due to the excellent thermal performance of the micro-porous Ag sinter die attach interconnection material, which possesses a superior heat-sink ability with minimized thermal contact resistance as an interconnection material. In addition, a power module structure assembled by this active SiC-TEG chip attached on a DBC substrate by sinter Ag paste has been fixed on a water cooling system by a TIM. The steady-state thermal resistance of this SiC-TEG power module system has been measured online and its high-temperature operation reliability has been systematically investigated during the power cycling test by switching ON/OFF the power source that is connected to the SiC-TEG chip by Au wires. The total thermal resistance of the power module from the SiC-TEG chip to the cooling system remains almost unchanged after 20 000 power cycles. The SEM cross section shows that there are no interface cracks and delamination occurrences after power cycling. The results show that SiC-TEG can accurately evaluate the thermal characteristics with different die attach materials. Additionally, the sinter Ag joint possesses the lowest thermal resistance and highest high-temperature reliability during power cycling compared with Pb and Pb-free die attach materials.

These results prove the possibility of a precise measurement method of the junction temperature and thermal resistance at high power density, which is no longer limited by the actual SiC direct bonded power module structure. This technology can be extended to perform reliability test standardization for all WBG semiconductors by providing a method that can record the information of the thermal and electrical properties online, but with a fast and miniaturized evaluation system. The SiC-TEG technology can benefit the controlled and site-specific power conversion industries and may lead to new avenues for power

electronics design with the capability to perform well at increased junction temperature.

ACKNOWLEDGMENT

The authors are grateful to all the members of the standardization project.

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Dongjin Kim (Student Member, IEEE) received the D.Eng. degree from the Department of Adaptive Machine Systems, Osaka University, Suita, Japan, in 2020.

He was a specially appointed Researcher with the Institute of Scientific and Industrial Research, Osaka University, from 2017 to 2018. He was involved in Pb/Pb-free soldering, Ag sinter joining, power electronic substrates, thermal characteristic standardization, and multiphysics finite-element simulations for long-term reliability of power electronic applications. He is currently part of the thermal management team for the Production Engineering Research Institute, LG Electronics, Inc., Pyeongtaek, South Korea. His current research interests include lead-free soldering, heat sink design, the simulation of power electronics, metallization technology, and thermal design as well as the simulation of power electronics for high reliability.

Shijo Nagao (Member, IEEE), photograph and biography not available at the time of publication.

Chuantong Chen (Member, IEEE) received the M.S. and Ph.D. degrees from the Nagoya Institute of Technology, Nagoya, Japan, in 2012 and 2015, respectively, both in mechanical engineering.

From 2015 to 2016, he was a Postdoctoral Fellow with the Institute Scientific and Industrial Research, Osaka University, Japan, where, since 2016, he an Assistant Professor. He is currently an Associate Professor with Osaka University. His research interest includes lead-free soldering, Ag sinter joining, mechanical properties, power electronics packaging, printing ink technology, and power devices design.

Dr. Chen was the recipient of some awards and honors including the Best Paper of the Japan Society of Mechanical Engineers and the IEEE CPMT Japan Chapter Young Award in 2017.

Naoki Wakasugi, photograph and biography not available at the time of publication.

Yasuyuki Yamamoto, photograph and biography not available at the time of publication.

Aiji Suetake, photograph and biography not available at the time of publication.

Tetsu Takemasa, photograph and biography not available at the time of publication.

Tohru Sugahara received the Ph.D. degree in materials science and engineering from the Kyushu University.

He is currently an Associate Professor with the Institute of Scientific and Industrial Research (ISIR), Osaka University. He held two Postdoc positions with Kyushu University, and Osaka University. He has authored or coauthored more than 90 scientific prereview publications, about ten book chapters, and ten patents in the field of packaging and ceramics coating. His professional interests focus on the development of thermoelectric devices for energy harvesting and thermal management, and ceramics coating with several substrate, such as plastic, glass and metals for addition of physical and chemical functions. He is PI and Co-PI of large NEDO (New Energy and Industrial Technology Development Organization) and JST (Japan Science and Technology Agency) projects of "Development of autonomous decentralized thermoelectric conversion power supply system for IoT sensor devices to realize the Society 5.0", and "Development of innovative functional materials based on large-scale search for new crystals".

Katsuaki Suganuma (Fellow, IEEE) received the Dr. Eng. degree from Tohoku University, Sendai, Japan, in 1982.

He was a Research Assistant with the Institute of Scientific and Industrial Research (ISIR), Osaka University, Suita, Japan, in 1982, an Associate Professor with the National Defense Academy in 1986, and a Professor with ISIR, in 1996. From 2007 to 2009, he was the Director of the Nanotechnology Center, Yokosuka, Japan, and from 2010 to 2012, the Deputy Director of ISIR, where he has been the Director since 2018. He is currently the Director of Flexible 3D System Integration Laboratory, Osaka University. He has authored several books both on lead-free soldering and on printed electronics. He was involved in lead-free soldering, conductive adhesive, power electronics packaging, and printed electronics.

Dr. Suganuma is currently in charge of several projects such as the printed electronics standardization IEC TC119 Japan committee, and is the Chairman of Standardization of Thermal Property Evaluation of WBG Power Devices/JFCA and of the WGB system integration consortium.