New DC–DC Converter With Direct Power Transfer Capability

Milad Zareie, *Student Member, IEEE*, Behzad Poorali, *Member, IEEE*, Suzan Eren, *Member, IEEE*, and Majid Pahlevani, *Senior Member, IEEE*

***Abstract*—This article presents a novel isolated dc–dc converter circuit topology, which is able to offer high performance for a wide range of operating conditions. The prominent features of the proposed circuit topology include its direct power transfer (DPT) capability, quasi-rectangular waveform for the input current, and soft-switching performance for a wide range of operating conditions. The amount of power processed by the power switches and transformer is reduced through DPT. In addition, the quasi-rectangular waveform of the input current decreases its peak and root-mean-square values, leading to reduced conduction losses associated with the magnetics and power semiconductors. In the proposed structure, the power switches benefit from zero-voltage-switching characteristics, while the output diodes operate under zero-current-switching conditions. Thus, the proposed topology minimizes both the conduction and switching losses, thereby improving the overall efficiency. Extensive simulation and experimental results are provided to verify the feasibility of the proposed circuitry and demonstrate its superior performance.**

***Index Terms*—Coupled inductors, dc–dc converters, direct power transfer, soft-switching, zero-current-switching (ZCS), zero-voltage-switching (ZVS).**

I. Introduction

INCREASING energy demand along with concerns over climate change requires a significant paradigm shift toward renewable energy sources. A reliable and efficient architecture is required to harvest energy from renewable sources and supply loads. The idea of microgrids is a fairly new and attractive concept to efficiently integrate renewable energy sources into the power system. In particular, dc microgrids have recently gained a lot of interest due to their tremendous advantages such as efficient operation [1]–[3]. Many renewable energy sources such as solar panels, fuel cells, and wind turbines generate dc power (although wind turbines along with generators produce ac power, the ac power is of variable frequency and amplitude, so that it is required to be converted to dc). Also, almost all energy storage systems (ESSs) are based on batteries, which are naturally dc. In addition, the landscape of loads has recently been changing as there are now many dc loads such as electronic devices (smart phones, tablets, etc.) and LED lighting [4]. Thus, dc systems seem to be a natural fit for the future grid with dc sources, dc loads, and dc ESSs. DC systems have better efficiency, do not require to deal with reactive power, and are not sensitive to harmonics. Thus, they are generally superior compared to their ac counterparts [5]. The introduction of dc-powered homes is a testament to the huge potential of dc microgrids [6], [7].

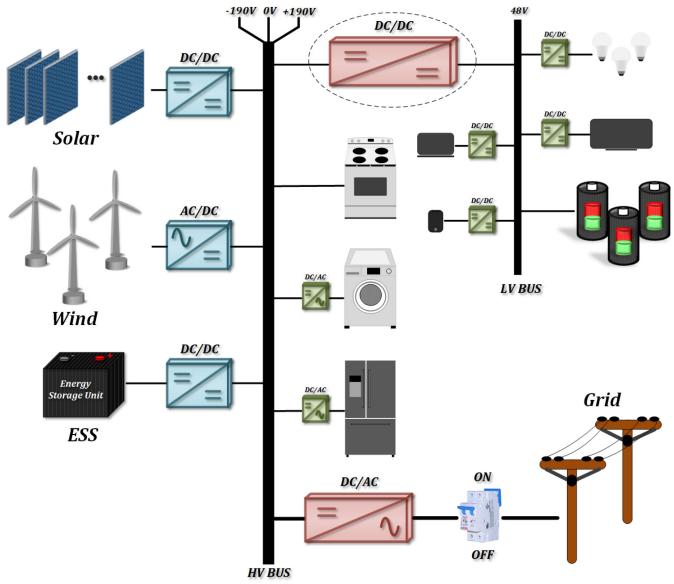

Fig. 1. Structure of a dc microgrid.

Fig. 1 shows an exemplary arrangement of a dc microgrid that can be used for dc-powered homes. According to this diagram, the dc microgrid includes a high-voltage (HV) bus (i.e., ±190 V) and a low-voltage (LV) bus (i.e., 48 V). The high-power components such as the main ESS, renewable energy sources, and high-power loads are connected to the HV bus, whereas the LV bus feeds low-power loads such as LED lighting and electronics [8]–[10]. A dc–dc converter is used between the HV bus and the LV bus to maintain the LV dc-bus voltage within a desired range. High efficiency, high power density, galvanic isolation, and low output current/voltage ripple are desired attributes for this dc–dc converter. Although this converter may have bidirectional power flow capability for some applications, unidirectional power flow

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Milad Zareie and Behzad Poorali are with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB T2N 1N4, Canada (e-mail: milad.zareiekhabjani@ucalgary.ca; behzad.pooraliriabi@ucalgary.ca).

Suzan Eren and Majid Pahlevani are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: suzan.eren@queensu.ca; majid.pahlevani@ucalgary.ca).

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suffices for this application due to the fact that the LV bus is merely responsible for feeding the loads and not for providing power for the HV bus.

One of the most popular circuit topologies utilized for dc–dc power conversion in the range of a few kilowatts is the full-bridge (FB) circuit topology. Thus far, extensive research studies have been carried out to achieve high-performance converters based on this structure. In particular, phase-shifted modulation (PSM) offers desirable features such as zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) for semiconductor devices in the FB structure. Due to its simple structure and attractive features, PSM FB converters have widely been used in industrial products. However, these circuit topologies suffer from several performance issues such as voltage spikes across the output diodes, free-wheeling intervals, duty-cycle loss, high circulating currents, and hard-switching operation at light loads [11], [12]. Many research studies have attempted to address the aforementioned issues [13]–[20].

Resonant-type converters are another popular circuit topologies for dc–dc power conversion [21]. In particular, series resonant converters (SRCs) is one of the fundamental structures, which can provide superior performance compared to PSM FB converters. SRCs normally operate above the resonant frequency to achieve ZVS with continuous current [22], [23]. The other main resonant structure is the LLC-type resonant converter, which has many attractive features and is currently used in many industrial products for various applications [24]–[27]. Despite their simple structures, resonant-type converters lose soft-switching at light loads. In fact, there is a trade-off between the ZVS range and the resonant tank current stress (to achieve ZVS at light loads, high reactive current circulating through the resonant tank is required, which increases the current stress and conduction losses).

Higher order resonant converters have been introduced to address this issue and improve the performance. For instance, a CLLC-type resonant converter can achieve ZVS at the primary side and ZCS at the secondary side over a wide range of operation [28]. In addition, a CLTC-type resonant converter is introduced in [29] by integrating the LLC, SRC, and CLLC structures. In this topology, an auxiliary transformer and extra resonant capacitor are used to achieve full-range ZVS characteristics. In [30], a dual-active-bridge (DAB) SRC with a new modulation strategy is proposed to achieve both an extended soft-switching range and reduced resonant tank current stress. In addition, another resonant DAB converter, introduced in [31], is able to achieve the same objectives by reconfiguring the converter structure under different load conditions. These circuit topologies offer excellent performance over entire load range and are well-suited for bidirectional applications. However, they are not suitable for unidirectional applications (having diodes instead of active switches at the secondary side).

In [32], a nonresonant current-driven FB converter is introduced for unidirectional applications, which is able to provide full-range soft-switching performance using a simple passive auxiliary circuit. However, the reactive current provided by the auxiliary circuit can increase the current stress. Another current-driven FB converter is introduced in [33] to eliminate the need for the auxiliary circuit. Further improvement of this structure is found in [34] to reduce the effects of parasitic components. In [35], the nonresonant current-driven structure has been extended to ac–dc converters. Fig. 2(a) shows the circuit diagram of this single-stage ac–dc converter that integrates a bridgeless boost power factor corrector with a dc–dc stage. As shown in Fig. 2(b), the dc–dc stage is a half-bridge (HB) structure derived from the current-driven converter introduced in [33]. For convenience, the circuit topology illustrated in Fig. 2(b) is referred to as the current-driven HB converter (CDHBC) in the rest of this article. The ac–dc converter of Fig. 2(a) offers a simple structure and naturally provides ZVS over a wide range of operation with a simple control system. Although this power circuit topology offers many advantages, it has some setbacks. Operation of the input inductor in the discontinuous conduction mode (DCM) results in high peak currents. Consequently, the root-mean-square (rms) value of the current is high, leading to high conduction losses. The other drawback of this topology is that the entire power is processed by the power switches and the high-frequency transformer. This increases the current stress and conduction losses, which requires more effective thermal management.

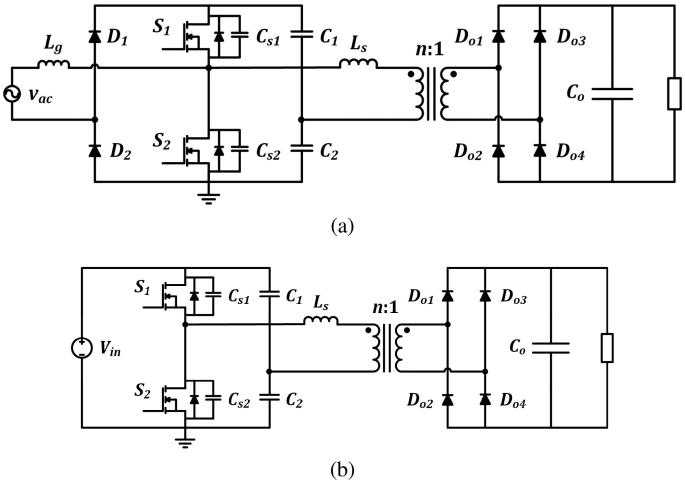

Fig. 2. (a) Single-stage ac–dc converter proposed in [35]. (b) Its dc–dc stage.

In summary, compared to basic resonant converters with unidirectional power flow, non-resonant current-driven structures can naturally achieve an extended ZVS range due to the series inductance size and the triangular nature of the transformer current. On the other hand, this triangular current results in high peak and rms currents, thereby increasing the overall conduction losses. To achieve ZVS over a wide range of operation as well as reduced current stress, a new dc–dc converter based on the non-resonant current-driven structure is proposed in this article, which offers a simple solution for unidirectional applications. This power circuit topology has been derived from the structure proposed in [35] for ac–dc applications. The main feature of the proposed converter is its direct power transfer (DPT) capability that effectively reduces the amount of power processed by the power semiconductors. In other words, a portion of the input power is directly transferred to the output, resulting in

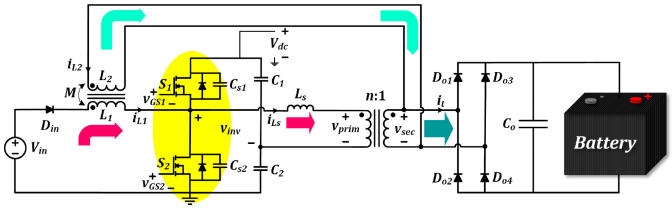

Fig. 3. The proposed dc–dc converter.

reduced current stress on the power switches and high frequency transformer. The other main advantage of the proposed structure is that the input current has a quasi-rectangular shape, which offers lower peak and rms values compared to one with triangular waveform. Thus, the proposed circuit can benefit from reduced conduction losses. Furthermore, this converter naturally provides ZVS for the power switches at the primary side and ZCS for the output diodes at the secondary side for a wide range of operation. As a result, the proposed circuit topology takes advantage of the inherent features of the current-driven structures having extended soft-switching range, while its current stress and conduction losses are maintained low.

The rest of this article is organized as follows. The proposed converter is introduced in Section II and its operating principles are explained. In Section III, the circuit is mathematically analyzed and Section IV discusses some guidelines to design the converter. Simulation and experimental results are provided in Sections V and VI, respectively. Finally, Section VII concludes the article.

II. Proposed DC–DC Converter With DPT

In this section, the proposed dc–dc converter with DPT capability is introduced. Then, the operating principles of the proposed circuit topology are described. Fig. 3 shows the schematic diagram of the proposed circuit. According to this figure, the input power is transferred to the output through two different paths. A portion of the power is processed through the power semiconductors and the other portion is directly transferred to the transformer secondary side through a coupled inductor (providing the DPT capability). In this power circuit, the amount of power processed through the power semiconductors and the transformer is reduced. Thus, this configuration can offer highly efficient power transfer. The other main feature of the proposed converter is the quasi-rectangular waveform of the input current that effectively reduces its peak and rms values, leading to lower conduction losses and higher efficiency. The proposed converter also provides galvanic isolation between the input and output as well as soft-switching over a wide range of operating conditions.

The proposed converter has seven operating intervals (modes) within one switching cycle. Equivalent circuits of the proposed circuit topology in different modes are shown in Fig. 4 and the key waveforms are depicted in Fig. 5. In order to obtain the currents flowing through the coupled inductor windings during each mode, the following set of equations describing the relation between the currents and voltages of a coupled inductor

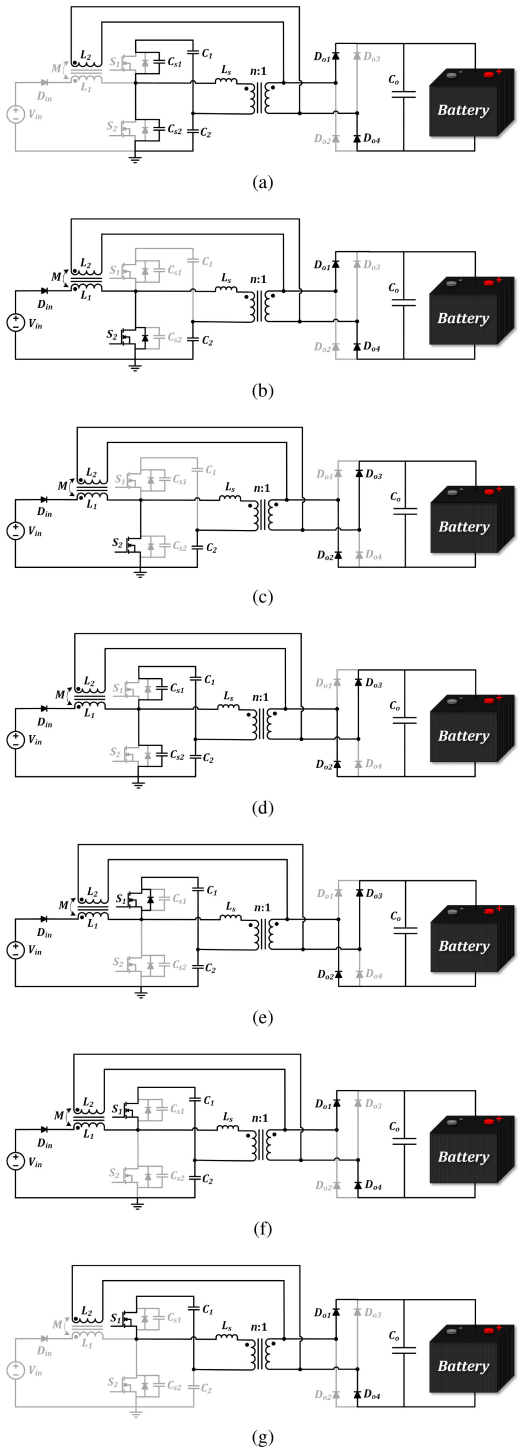

Fig. 4. Equivalent circuits of the proposed converter within different operating modes.

is employed:

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} + M \dfrac{di_{L2}}{dt} \\ v_{L2} = M \dfrac{di_{L1}}{dt} + L_2 \dfrac{di_{L2}}{dt}. \end{cases} \tag{1}$$

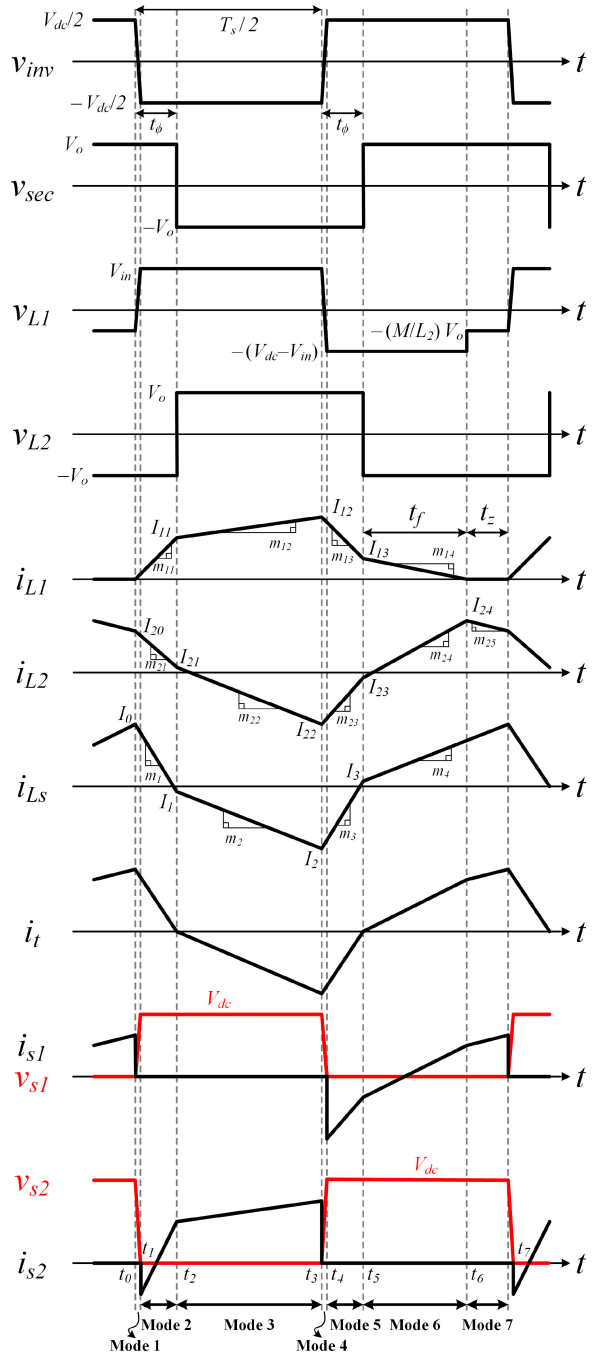

Fig. 5. Key waveforms of the proposed converter.

From (1), the current derivatives can be written in terms of the voltages as

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{L_2}{L_t^2}v_{L1} - \dfrac{M}{L_t^2}v_{L2} \\ \dfrac{di_{L2}}{dt} = -\dfrac{M}{L_t^2}v_{L1} + \dfrac{L_1}{L_t^2}v_{L2} \end{cases} \tag{2}$$

where

$$L_t = \sqrt{L_1L_2 - M^2}. \tag{3}$$

The operating modes are described as follows. Prior to Mode 1, it is assumed that the input current is zero, the power switch S_1 is ON, and the output diodes D_{o1} and D_{o4} are conducting.

Mode 1 [t_0, t_1]: At t_0, the switch S_1 is turned OFF under ZVS condition due to existence of the snubber capacitors C_{s1} and C_{s2}. The current i_{Ls} charges the capacitor C_{s1} and discharges the capacitor C_{s2}. As a result, the voltage across S_1 linearly rises, while the voltage across S_2 linearly reduces to zero.

Mode 2 [t_1, t_2]: When the voltage across S_2 becomes zero, its body diode starts conducting. Then, S_2 turns ON under ZVS condition. Consequently, $v_{\text{inv}} = -V_{dc}/2$ and $v_{L1} = V_{in}$. At the output side, since the total current i_t (the sum of ni_{Ls} and i_{L2}) flowing through the output bridge diodes is positive, D_{o1} and D_{o4} are still conducting. As a result, $v_{\text{sec}} = V_o$ and $v_{L2} = -V_o$. On the other hand, the voltage across the inductance L_s is obtained as

$$v_{Ls} = v_{\text{inv}} - nv_{\text{sec}}. \tag{4}$$

From (4), the slope of the current i_{Ls} during this mode is equal to

$$m_1 = -\frac{V_{dc} + 2nV_o}{2L_s}. \tag{5}$$

According to the voltages applied to L_1 and L_2, i_{L1} linearly rises from zero, while i_{L2} starts decreasing. Therefore, the input diode D_{in} turns ON under ZCS condition. The slopes of i_{L1} and i_{L2} are obtained using (2) as

$$m_{11} = \frac{L_2V_{in} + MV_o}{L_t^2} \tag{6}$$

$$m_{21} = -\frac{MV_{in} + L_1V_o}{L_t^2}. \tag{7}$$

Since both the currents i_{Ls} and i_{L2} are decreasing, the current i_t decreases as well. When it reaches zero, D_{o1} and D_{o4} turn OFF under ZCS condition and this mode ends.

Mode 3 [t_2, t_3]: As the direction of the current i_t reverses and it becomes negative, the output diodes D_{o2} and D_{o3} turn ON under ZCS condition. Thus, the polarity of the voltage across the transformer secondary winding as well as across the coupled inductor secondary winding is reversed, i.e., $v_{\text{sec}} = -V_o$ and $v_{L2} = V_o$. As the switch S_2 is still ON, the inverter output voltage as well as the voltage across L_1 remains the same as the previous mode ($v_{\text{inv}} = -V_{dc}/2$ and $v_{L1} = V_{in}$). Using (4), the slope of i_{Ls} during this mode is expressed as

$$m_2 = -\frac{V_{dc} - 2nV_o}{2L_s}. \tag{8}$$

From (2), the slopes of i_{L1} and i_{L2} are also obtained

$$m_{12} = \frac{L_2V_{in} - MV_o}{L_t^2} \tag{9}$$

$$m_{22} = \frac{-MV_{in} + L_1V_o}{L_t^2}. \tag{10}$$

Mode 4 [t_3, t_4]: At t_3, the switch S_2 is turned OFF under ZVS condition. The sum of magnitudes of the currents i_{Lg1} and i_{Ls} charges the capacitor C_{s2} and discharges the capacitor C_{s1}.

As a result, the voltage across S_2 linearly rises, while the voltage across S_1 linearly reduces to zero.

Mode 5 [t_4, t_5]: When the voltage across S_1 becomes zero, its body diode starts conducting. Then, S_1 turns ON under ZVS condition. As a result, $v_{\text{inv}} = V_{dc}/2$ and $v_{L1} = V_{in} - V_{dc}$. At the output side, diodes D_{o2} and D_{o3} are still conducting since the current i_t is negative. Thus, v_{sec} and v_{L2} are the same as the previous mode. Similarly, the slopes of the currents i_{Ls}, i_{L1}, and i_{L2} during this mode can be obtained as

$$m_3 = \frac{V_{dc} + 2nV_o}{2L_s} = -m_1 \tag{11}$$

$$m_{13} = -\frac{L_2(V_{dc} - V_{in}) + MV_o}{L_t^2} \tag{12}$$

$$m_{23} = \frac{M(V_{dc} - V_{in}) + L_1V_o}{L_t^2}. \tag{13}$$

On the other hand, magnitude of the current i_t linearly reduces to zero. When the current becomes zero, D_{o2} and D_{o3} turn OFF under ZCS condition and this mode ends.

Mode 6 [t_5, t_6]: As the direction of the current i_t reverses and it becomes positive, D_{o1} and D_{o4} turn ON under ZCS condition. As a result, $v_{\text{sec}} = V_o$ and $v_{L2} = -V_o$. On the other hand, S_1 is still ON, hence, $v_{\text{inv}} = V_{dc}/2$ and $v_{L1} = V_{in} - V_{dc}$. Slopes of the currents i_{Ls}, i_{L1}, and i_{L2} during this mode can be obtained as

$$m_4 = \frac{V_{dc} - 2nV_o}{2L_s} = -m_2 \tag{14}$$

$$m_{14} = \frac{-L_2(V_{dc} - V_{in}) + MV_o}{L_t^2} \tag{15}$$

$$m_{24} = \frac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}. \tag{16}$$

This mode ends when the current i_{L1} becomes zero and D_{in} turns OFF under ZCS condition.

Mode 7 [t_6, t_7]: During this mode, the input current i_{L1} is zero. The voltages v_{inv}, v_{sec}, and v_{L2} are the same as the previous mode. Also, the current i_{Ls} keeps rising with the slope given in (14). Since the input current is zero, (2) implies that the voltage across L_1 is determined by v_{L2}, i.e., $v_{L1} = (M/L_2)v_{L2}$. The slope of i_{L2} is obtained as

$$m_{25} = -V_o/L_2. \tag{17}$$

III. Steady-State Analysis

In this section, the proposed converter is mathematically analyzed in detail under steady-state conditions. The dc–dc conversion stage can be simplified as depicted in Fig. 6. In this figure, the voltage v_{inv} represents a square waveform alternating between $V_{dc}/2$ and $-V_{dc}/2$ as switches turn ON and OFF (with a 50% duty cycle). The polarity of the voltage applied to the transformer secondary winding depends on the direction of the total high-frequency current $i_t = ni_{Ls} + i_{L2}$ flowing through the output diode rectifier. When i_t is positive, D_{o1} and D_{o4} conduct and $v_{\text{sec}} = V_o$. Alternatively, $v_{\text{sec}} = -V_o$ when i_t is negative. Thus, the output part is represented by a current-controlled voltage source.

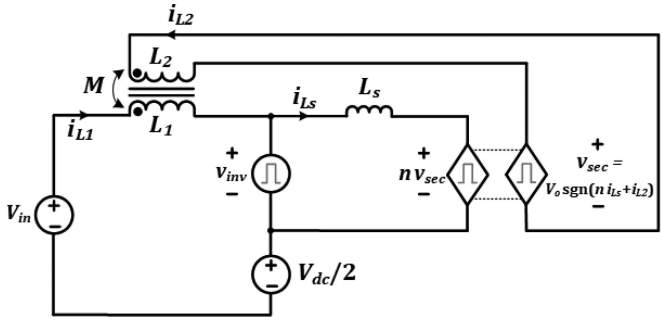

Fig. 6. Simplified circuit of the proposed converter.

A. Output Power P_o

As established earlier, the input power in the proposed power circuit topology is transferred to the output through two paths: 1) through the power switches and the high-frequency transformer; and 2) through the coupled inductor. The amount of power transferred through the transformer can be obtained quite similar to the one for DAB converters [36]. For this purpose, i_{Ls} is first calculated.

Since time duration of Modes 1 and 4 is short enough compared to the other modes, they are neglected in the analysis. According to Fig. 5 and assuming $t_0 = 0$, i_{Ls} can be expressed by four linear equations within each switching cycle as

$$i_{Ls1}(t) = m_1 t + I_0 \qquad t \in [0,\ t_\phi] \tag{18}$$

$$i_{Ls2}(t) = m_2(t - t_\phi) + I_1 \qquad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{19}$$

$$i_{Ls3}(t) = m_3\left(t - \frac{T_s}{2}\right) + I_2 \qquad t \in \left[\frac{T_s}{2},\ \frac{T_s}{2} + t_\phi\right] \tag{20}$$

$$i_{Ls4}(t) = m_4\left(t - \frac{T_s}{2} - t_\phi\right) + I_3 \quad t \in \left[\frac{T_s}{2} + t_\phi,\ T_s\right] \tag{21}$$

where m_1 through m_4 are given in (5), (8), (11), and (14), respectively. The constants I_0, I_1, and I_2 are obtained by evaluating (18), (19), and (20), respectively, at t_ϕ, $T_s/2$, and $T_s/2 + t_\phi$

$$I_1 = -\frac{V_{dc} + 2nV_o}{2L_s}t_\phi + I_0 \tag{22}$$

$$I_2 = -\frac{V_{dc} - 2nV_o}{2L_s}\frac{T_s}{2} - \frac{2nV_o}{L_s}t_\phi + I_0 \tag{23}$$

$$I_3 = -\frac{V_{dc} - 2nV_o}{2L_s}\left(\frac{T_s}{2} - t_\phi\right) + I_0. \tag{24}$$

Substituting (5), (8), (11), (14), and (22)–(24) into (18)–(21), the four linear pieces of i_{Ls} are obtained:

$$i_{Ls1}(t) = -\frac{V_{dc} + 2nV_o}{2L_s}t + I_0 \tag{25}$$

$$i_{Ls2}(t) = -\frac{V_{dc} - 2nV_o}{2L_s}t - \frac{2nV_o}{L_s}t_\phi + I_0 \tag{26}$$

$$i_{Ls3}(t) = \frac{V_{dc} + 2nV_o}{2L_s}t - \frac{V_{dc}}{L_s}\frac{T_s}{2} - \frac{2nV_o}{L_s}t_\phi + I_0 \tag{27}$$

$$i_{Ls4}(t) = \frac{V_{dc} - 2nV_o}{2L_s}t - \frac{V_{dc} - 2nV_o}{2L_s}T_s + I_0. \tag{28}$$

To calculate the averaged power P_{tran} transferred to the secondary side of the high-frequency transformer, the instantaneous power $v_{\text{inv}}(t).i_{Ls}(t)$ is integrated over one switching period.

$$\begin{aligned} P_{tran} = \frac{1}{T_s}\Bigg[& -\frac{V_{dc}}{2}\int_0^{t_\phi} i_{Ls1}(t)dt - \frac{V_{dc}}{2}\int_{t_\phi}^{T_s/2} i_{Ls2}(t)dt \\ & + \frac{V_{dc}}{2}\int_{T_s/2}^{T_s/2+t_\phi} i_{Ls3}(t)dt \\ & + \frac{V_{dc}}{2}\int_{T_s/2+t_\phi}^{T_s} i_{Ls4}(t)dt\Bigg]. \end{aligned} \tag{29}$$

Substituting (25)–(28) into (29) and calculating the integrals yield the averaged power as

$$P_{tran} = \frac{V_{dc}nV_o}{2L_s}t_\phi(1 - 2t_\phi f_s). \tag{30}$$

By defining a new parameter $n_\phi = t_\phi/T_s$ (t_ϕ normalized to the switching period), (30) is simplified to

$$P_{\text{tran}} = \frac{V_{dc}nV_o}{2L_s f_s}n_\phi(1 - 2n_\phi). \tag{31}$$

Equation (31) shows that P_{tran} reaches its maximum value at $n_\phi = 0.25$. Moreover, it is inversely proportional to the switching frequency. In other words, the amount of power transferred through the transformer is decreased with the switching frequency.

In addition to the power transferred through the power switches and the transformer, a portion of power is transferred to the output through the coupled inductor. To calculate this portion, it is required to derive the current i_{L2} flowing through the secondary winding of the coupled inductor.

According to Fig. 5, i_{L2} can be expressed by five linear pieces within one switching cycle

$$i_{L2,1}(t) = m_{21}t + I_{20} \qquad t \in [0,\ t_\phi] \tag{32}$$

$$i_{L2,2}(t) = m_{22}(t - t_\phi) + I_{21} \qquad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{33}$$

$$i_{L2,3}(t) = m_{23}(t - \frac{T_s}{2}) + I_{22} \qquad t \in \left[\frac{T_s}{2},\ \frac{T_s}{2} + t_\phi\right] \tag{34}$$

$$i_{L2,4}(t) = m_{24}\left(t - \frac{T_s}{2} - t_\phi\right) + I_{23} \quad t \in \left[\frac{T_s}{2} + t_\phi, T_s - t_z\right] \tag{35}$$

$$i_{L2,5}(t) = m_{25}(t - T_s + t_z) + I_{24} \quad t \in [T_s - t_z,\ T_s] \tag{36}$$

where the current slopes m_{21} through m_{25} are given by (7), (10), (13), (16), and (17). Also, t_f is the time duration of Mode 6 for which the current i_{L1} reduces to zero as indicated in Fig. 5. Evaluating (32)–(35) at t_ϕ, $T_s/2$, $T_s/2 + t_\phi$, and $T_s/2 + t_\phi + t_f$, respectively, yields the following constants (I_{21}, I_{22}, I_{23}, and I_{24}).

$$I_{21} = -\frac{MV_{in} + L_1V_o}{L_t^2}t_\phi + I_{20} \tag{37}$$

$$I_{22} = \frac{-MV_{in} + L_1V_o}{L_t^2}\frac{T_s}{2} - \frac{2L_1V_o}{L_t^2}t_\phi + I_{20} \tag{38}$$

$$\begin{aligned} I_{23} = & \frac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}t_\phi \\ & + \frac{-MV_{in} + L_1V_o}{L_t^2}\frac{T_s}{2} + I_{20} \end{aligned} \tag{39}$$

$$\begin{aligned} I_{24} = & \frac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}(t_\phi + t_f) \\ & + \frac{-MV_{in} + L_1V_o}{L_t^2}\frac{T_s}{2} + I_{20}. \end{aligned} \tag{40}$$

By substituting (7), (10), (13), (16), (17), and (37)–(40) into (32)–(36), the linear pieces of i_{L2} are obtained.

$$i_{L2,1}(t) = -\frac{MV_{in} + L_1V_o}{L_t^2}t + I_{20} \tag{41}$$

$$i_{L2,2}(t) = \frac{-MV_{in} + L_1V_o}{L_t^2}t - \frac{2L_1V_o}{L_t^2}t_\phi + I_{20} \tag{42}$$

$$\begin{aligned} i_{L2,3}(t) = & \frac{M(V_{dc} - V_{in}) + L_1V_o}{L_t^2}t \\ & - \frac{MV_{dc}}{L_t^2}\frac{T_s}{2} - \frac{2L_1V_o}{L_t^2}t_\phi + I_{20} \end{aligned} \tag{43}$$

$$\begin{aligned} i_{L2,4}(t) = & \frac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}t \\ & + \frac{-MV_{dc} + 2L_1V_o}{L_t^2}\frac{T_s}{2} + I_{20} \end{aligned} \tag{44}$$

$$i_{L2,5}(t) = -\frac{V_o}{L_2}t + \frac{V_o}{L_2}T_s + I_{20}. \tag{45}$$

The averaged power that is directly transferred to the output through the coupled inductor, P_{DPT}, is derived by integrating the instantaneous power $-v_{L2}.i_{L2}$ over one switching cycle

$$\begin{aligned} P_{DPT} = \frac{1}{T_s}\Bigg[& V_o\int_0^{t_\phi} i_{L2,1}(t)dt - V_o\int_{t_\phi}^{T_s/2} i_{L2,2}(t)dt \\ & - V_o\int_{T_s/2}^{T_s/2+t_\phi} i_{L2,3}(t)dt \\ & + V_o\int_{T_s/2+t_\phi}^{T_s/2+t_\phi+t_f} i_{L2,4}(t)dt \\ & + V_o\int_{T_s/2+t_\phi+t_f}^{T_s} i_{L2,5}(t)dt\Bigg]. \end{aligned} \tag{46}$$

By substituting (41)–(45) into (46) and calculating the integral, P_{DPT} is derived as

$$P_{DPT} = \frac{V_o f_s}{2L_t^2}\left\{MV_{in}\left[\frac{T_s^2}{4} - (t_\phi + t_f)^2 + T_s(t_\phi - t_f)\right] + MV_{dc}(t_f^2 - t_\phi^2 + 2t_\phi t_f) - \frac{M^2 V_o}{L_2}\left(\frac{T_s}{2} - t_\phi - t_f\right)^2\right\}. \tag{47}$$

Defining a new parameter $n_f = t_f/T_s$ (t_f normalized to the switching period), (47) is simplified to

$$P_{DPT} = \frac{V_o}{2L_t^2 f_s}\{MV_{in}[0.25 - (n_\phi + n_f)^2 + n_\phi - n_f] + MV_{dc}(n_f^2 - n_\phi^2 + 2n_\phi n_f) - \frac{M^2 V_o}{L_2}(0.5 - n_\phi - n_f)^2\}. \tag{48}$$

Equation (48) shows that P_{DPT}, similar to P_{tran}, is inversely proportional to the switching frequency. Consequently, as the switching frequency rises, the amount of power transferred to the output through both paths (through the transformer and through the coupled inductor) is decreased. Having both P_{tran} and P_{DPT} determined, the total output power is expressed as

$$P_o = P_{\text{tran}} + P_{\text{DPT}} \tag{49}$$

where P_{tran} and P_{DPT} are given by (31) and (48), respectively.

B. Averaged Input Current I_{in}

The other important parameter is the averaged input current I_{in}. For this purpose, i_{L1} is first formulated. According to Fig. 5, i_{L1} can be expressed by five linear pieces within each switching cycle

$$i_{L1,1}(t) = m_{11}t \qquad t \in [0,\ t_\phi] \tag{50}$$

$$i_{L1,2}(t) = m_{12}(t - t_\phi) + I_{11} \qquad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{51}$$

$$i_{L1,3}(t) = m_{13}(t - \frac{T_s}{2}) + I_{12} \qquad t \in \left[\frac{T_s}{2},\ \frac{T_s}{2} + t_\phi\right] \tag{52}$$

$$i_{L1,4}(t) = m_{14}\left(t - \frac{T_s}{2} - t_\phi\right) + I_{13} \quad t \in \left[\frac{T_s}{2} + t_\phi,\ T_s - t_z\right] \tag{53}$$

$$i_{L1,5}(t) = 0 \qquad t \in [T_s - t_z,\ T_s] \tag{54}$$

where m_{11} through m_{14} are given in (6), (9), (12), and (15). The constants I_{11}, I_{12}, and I_{13} can be calculated by evaluating (50), (51), and (52) at t_ϕ, $T_s/2$, and $T_s/2 + t_\phi$, respectively

$$I_{11} = \frac{L_2 V_{in} + MV_o}{L_t^2} t_\phi \tag{55}$$

$$I_{12} = \frac{L_2 V_{in} - MV_o}{L_t^2}\frac{T_s}{2} + \frac{2MV_o}{L_t^2} t_\phi \tag{56}$$

$$I_{13} = \frac{-L_2(V_{dc} - V_{in}) + MV_o}{L_t^2} t_\phi + \frac{L_2 V_{in} - MV_o}{L_t^2}\frac{T_s}{2}. \tag{57}$$

By substituting (6), (9), (12), (15), and (55)–(57) into (50)–(53), the four linear pieces of i_{L1} are derived.

$$i_{L1,1}(t) = \frac{L_2 V_{in} + MV_o}{L_t^2} t \tag{58}$$

$$i_{L1,2}(t) = \frac{L_2 V_{in} - MV_o}{L_t^2} t + \frac{2MV_o}{L_t^2} t_\phi \tag{59}$$

$$i_{L1,3}(t) = \frac{-L_2(V_{dc} - V_{in}) - MV_o}{L_t^2} t + \frac{L_2 V_{dc}}{L_t^2}\frac{T_s}{2} + \frac{2MV_o}{L_t^2} t_\phi \tag{60}$$

$$i_{L1,4}(t) = \frac{-L_2(V_{dc} - V_{in}) + MV_o}{L_t^2} t + \frac{L_2 V_{dc} - 2MV_o}{L_t^2}\frac{T_s}{2}. \tag{61}$$

According to its definition, the averaged input current I_{in} is obtained as

$$I_{in} = \frac{1}{T_s}\left[\int_0^{t_\phi} i_{L1,1}(t)dt + \int_{t_\phi}^{T_s/2} i_{L1,2}(t)dt + \int_{T_s/2}^{T_s/2+t_\phi} i_{L1,3}(t)dt + \int_{T_s/2+t_\phi}^{T_s/2+t_\phi+t_f} i_{L1,4}(t)dt\right]. \tag{62}$$

By substituting (58)–(61) into (62) and calculating the integrals yield the averaged input current as

$$I_{in} = \frac{f_s}{2L_t^2}\left\{L_2 V_{in}\left(\frac{T_s}{2} + t_\phi + t_f\right)^2 - L_2 V_{dc}(t_\phi + t_f)^2 + MV_o\left[(t_\phi + t_f)^2 + T_s(t_\phi - t_f) - \frac{T_s^2}{4}\right]\right\}. \tag{63}$$

Rewriting (63) in terms of n_ϕ and n_f results in the following simplified equation:

$$I_{in} = \frac{1}{2L_t^2 f_s}\left\{L_2 V_{in}(0.5 + n_\phi + n_f)^2 - L_2 V_{dc}(n_\phi + n_f)^2 + MV_o\left[(n_\phi + n_f)^2 + n_\phi - n_f - 0.25\right]\right\}. \tag{64}$$

Equation (64) implies that the averaged input current (or equivalently, the input power) is inversely proportional to the switching frequency. This is well aligned with the fact that the output power linearly decreases with the switching frequency as given by (31) and (48).

C. DC-Bus Voltage V_{dc}

In the proposed converter, the dc-bus voltage V_{dc} is determined such that the charge/discharge current balance for the

dc-bus capacitors is satisfied. The steady-state dc-bus voltage level can be derived by equating the averaged input power P_{in} with the output power P_o (the converter conduction losses are neglected). Thus, the following equation must be satisfied:

$$V_{in}I_{in} = P_{\text{tran}} + P_{\text{DPT}}. \tag{65}$$

By substituting (31), (48), and (64) into (65), the dc-bus voltage, V_{dc}, can be derived as given by (66), shown at the bottom of this page.

D. Normalized Parameters n_ϕ and n_f

According to Fig. 5, t_ϕ represents the phase difference between the square voltages v_{inv} and v_{sec}. The voltage v_{inv} is dependent on the switching state. However, the voltage v_{sec} is equal to V_o sgn$(ni_{Ls} + i_{L2})$ as shown in Fig. 6. According to Fig. 5, $i_t = 0$ at $t = t_2$ and at $t = t_5$. Thus, the following equations are valid:

$$\begin{cases} nI_1 + I_{21} = 0 \\ nI_3 + I_{23} = 0. \end{cases} \tag{67}$$

The following equations are derived by substituting (22), (24), (37), and (39) into (67):

$$\begin{cases} nI_0 + I_{20} = n\dfrac{V_{dc} + 2nV_o}{2L_s}t_\phi \\ \qquad\qquad + \dfrac{MV_{in} + L_1V_o}{L_t^2}t_\phi \\ nI_0 + I_{20} = n\dfrac{V_{dc} - 2nV_o}{2L_s}\left(\dfrac{T_s}{2} - t_\phi\right) \\ \qquad\qquad - \dfrac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}t_\phi \\ \qquad\qquad - \dfrac{-MV_{in} + L_1V_o}{L_t^2}\dfrac{T_s}{2}. \end{cases} \tag{68}$$

Since the left-hand side terms of the equations given in (68) are the same, the right-hand side terms must be equal. After some mathematical manipulation, n_ϕ is derived as

$$n_\phi = \frac{nL_t^2(V_{dc} - 2nV_o) - 2L_s(L_1V_o - MV_{in})}{4V_{dc}(ML_s + nL_t^2)}. \tag{69}$$

According to Fig. 5, t_f is the time duration of Mode 6 during which i_{L1} linearly reaches zero. This time can be calculated by evaluating (61) at $t = T_s/2 + t_\phi + t_f$. Thus, t_f is calculated from the following equation:

$$i_{L1,4}\left(\frac{T_s}{2} + t_\phi + t_f\right) = 0. \tag{70}$$

From (70), n_f is given by

$$n_f = \frac{1}{2}\frac{L_2V_{in} - MV_o}{L_2(V_{dc} - V_{in}) - MV_o} - n_\phi \tag{71}$$

where n_ϕ is given in (69).

E. ZVS Range

Generally, in power converters, snubber capacitors provide the turn-OFF ZVS operation by reducing the current–voltage overlap for the power switches. The snubber capacitors must be fully discharged before the respective switch turns ON. This is achieved by charging/discharging the snubber capacitors through a resonance with an inductor when the other switch of the leg turns OFF. Therefore, it is necessary for the inductor to have enough energy to charge/discharge the snubber capacitors. Thus, the following equation must be satisfied:

$$\frac{1}{2}L_{eq}I_{Leq}^2 \geq \frac{1}{2}C_{eq}V_{Ceq}^2 \tag{72}$$

where L_{eq} is the equivalent inductance resonating with the equivalent capacitance C_{eq}, I_{Leq} is the current of L_{eq} at the switch turn-OFF instant, and V_{Ceq} is the equivalent capacitance voltage.

According to the operating principles of the proposed circuit topology, the inductor current i_{L1} increases the current stress of S_2 while decreases the current stress of S_1, compared to a conventional CDHBC shown in Fig. 2(b). Since S_1 turns OFF at a lower current level (with respect to S_2), it is essential to evaluate the ZVS operation at t_0 when S_1 is switched OFF. Therefore, (72) can be rewritten as

$$\frac{1}{2}L_sI_0^2 \geq \frac{1}{2}C_sV_{dc}^2 \tag{73}$$

where $C_s = C_{s1} + C_{s2}$.

IV. Design Considerations

In this section, the design procedure for the proposed converter is described in detail. The procedure is mainly based on the theoretical analysis presented in the previous section. According to the waveform of i_{L1} shown in Fig. 5, as the time duration of Mode 7 (in which $i_{L1} = 0$) approaches zero, or equivalently, $n_\phi + n_f$ approaches 0.5, the peak and rms values of the input current for a given averaged current are minimized. Additionally, transferring the maximum possible power directly through the coupled inductor minimizes the amount of power processed by the power switches. Thus, it is desirable to design the proposed converter such that it achieves the maximum possible direct power transfer with $n_\phi + n_f$ close to 0.5.

To simplify the analysis, a new parameter is defined as

$$x = M/L_2. \tag{74}$$

By using this definition, (48), (64), and (71) can be rewritten as

$$P_{DPT} = \frac{V_oL_2}{2f_sL_t^2}\left\{xV_{in}[0.25 + n_\phi - n_f - (n_\phi + n_f)^2] + xV_{dc}(n_f^2 - n_\phi^2 + 2n_\phi n_f) - x^2V_o(0.5 - n_\phi - n_f)^2\right\} \tag{75}$$

$$V_{dc} = \frac{L_s}{L_2}\frac{L_2^2V_{in}^2(0.5 + n_\phi + n_f)^2 + 2ML_2V_oV_{in}[(n_\phi + n_f)^2 - 0.25] + M^2V_o^2(0.5 - n_\phi - n_f)^2}{nV_oL_t^2n_\phi(1 - 2n_\phi) + L_2L_sV_{in}(n_\phi + n_f)^2 + ML_sV_o(n_f^2 - n_\phi^2 + 2n_\phi n_f)} \tag{66}$$

$$I_{in} = \frac{L_2}{2f_sL_t^2}\left\{V_{in}(0.5+n_\phi+n_f)^2 - V_{dc}(n_\phi+n_f)^2 + xV_o[(n_\phi+n_f)^2+n_\phi-n_f-0.25]\right\} \quad (76)$$

$$n_\phi + n_f = \frac{1}{2}\frac{V_{in}-xV_o}{V_{dc}-V_{in}-xV_o}. \quad (77)$$

From (77), the parameter x is derived as

$$x = \frac{0.5V_{in}-(n_\phi+n_f)(V_{dc}-V_{in})}{(0.5-n_\phi-n_f)V_o}. \quad (78)$$

Since x is the ratio of two inductances (M/L_2), it must be positive. According to (78), it is observed that the denominator is positive. Thus, its numerator must be positive as well. This results in the following equation:

$$V_{dc} < \frac{0.5+n_\phi+n_f}{n_\phi+n_f}V_{in}. \quad (79)$$

This equation imposes a maximum limit on choosing the dc-bus voltage. In addition, according to (75) and (76), the normalized direct power transferred through the coupled inductor $P_{DPT,n}$ is derived in (80), as given at the bottom of this page.

As the variation intervals of the parameters n_ϕ and n_f are limited to $0 < n_\phi, n_f < 0.5$ under the condition $n_\phi + n_f < 0.5$, it is possible to obtain the normalized direct transferred power in terms of different values of n_ϕ and n_f using (78) and (80). Among all different combinations of n_ϕ, n_f, and $P_{\text{DPT},n}$, the one that achieves the maximum direct power transfer, while $n_\phi + n_f$ close to 0.5, can be selected as the desired operating point.

The ratio of L_2/L_t^2 can be calculated using (76) as

$$\frac{L_2}{L_t^2} = (2f_sI_{in})/\left\{V_{in}(0.5+n_\phi+n_f)^2 + xV_o[(n_\phi+n_f)^2+n_\phi-n_f-0.25] - V_{dc}(n_\phi+n_f)^2\right\}. \quad (81)$$

For a coupled inductor, the mutual inductance is defined as

$$M = k\sqrt{L_1L_2}. \quad (82)$$

The ratio of L_1/L_2 is obtained using (74) and (82) as

$$L_1/L_2 = (x/k)^2. \quad (83)$$

By using (3) and (74), L_2 can be derived as

$$L_2 = \frac{L_t^2/L_2}{(L_1/L_2)-x^2}. \quad (84)$$

By substituting (81) and (83) into (84), the following equation is obtained:

$$L_2 = \frac{k^2}{2f_sI_{in}x^2(1-k^2)}\left\{V_{in}(0.5+n_\phi+n_f)^2 + xV_o[(n_\phi+n_f)^2+n_\phi-n_f-0.25] - V_{dc}(n_\phi+n_f)^2\right\} \quad (85)$$

Having the parameters n_ϕ, n_f, and x determined, the inductance L_2 is designed using (85). Then, the inductances M and L_1 are determined according to the values of M/L_2 and L_1/L_2, respectively.

From (31), the ratio of L_s/n is given by

$$\frac{L_s}{n} = \frac{V_{dc}V_o}{2P_{\text{tran}}f_s}n_\phi(1-2n_\phi). \quad (86)$$

where $P_{\text{tran}} = P_o - P_{\text{DPT}}$ and P_{DPT} is given by (80). After some mathematical manipulation, (69) is rewritten as

$$n = \frac{L_t^2V_{dc} - 2(\frac{L_s}{n})(L_1V_o - MV_{in}) - 4n_\phi V_{dc}(M\frac{L_s}{n}+L_t^2)}{2V_oL_t^2}. \quad (87)$$

By substituting L_s/n given in (86) into (87), the desired turns ratio of the transformer is designed. The inductance L_s is then obtained based on the values of L_s/n and n.

The snubber capacitors C_{s1} and C_{s2} are designed such that the turn-OFF switching losses are reduced to a desired level by decreasing the current–voltage overlap of a power switch when it turns OFF. For this purpose, the following equation can be used [37]:

$$C_{s1,2} \geq \frac{I_{sw}t_{fi}}{4k_vV_{sw}} \quad (88)$$

where I_{sw} is the switch current right before it turns OFF, t_{fi} is the fall time of the switch current, i.e., the time that it takes for the switch current to become zero from I_{sw}, k_v determines the amount of current–voltage overlap for the switch, and V_{sw} is the final value that the switch voltage reaches when it turns OFF. As S_2 carries more current than S_1, (88) must be evaluated at t_3 when S_2 is switched OFF. Therefore, (88) is rewritten as

$$C_{s1,2} \geq \frac{(I_{12}-I_2)t_{fi}}{4k_vV_{dc}} \quad (89)$$

where I_2 and I_{12} are given in (23) and (56), respectively.

V. Simulation Verification

In this section, the proposed converter is first designed using the guidelines given in the previous section for this specific application (i.e., charging a 48 V battery from a 190-V dc grid with the nominal power of 450 W). Then, it is simulated using the OrCAD PSPICE software package to verify the theoretical analysis. Also, in order to demonstrate the merits of the proposed circuit topology, its performance is compared to that of the SRC (as a resonant structure) as well as the CDHBC (as a current-driven structure) through simulation. These circuits have been selected for the comparison, since they have similar structures as the proposed converter with unidirectional power flow. The proposed converter is designed such that the minimum frequency (at the nominal power) will be 140 kHz.

The first step in the design of this converter is to choose a proper dc-bus voltage using (79). As mentioned earlier, it is desired to achieve $n_\phi + n_f$ close to 0.5. On the other hand, to ensure DCM operation of the proposed converter, $n_\phi + n_f$ should

$$P_{\text{DPT},n} = \frac{P_{\text{DPT}}}{P_o} = \frac{V_o}{V_{in}}\frac{xV_{in}[0.25+n_\phi-n_f-(n_\phi+n_f)^2] + xV_{dc}(n_f^2-n_\phi^2+2n_\phi n_f) - x^2V_o(0.5-n_\phi-n_f)^2}{V_{in}(0.5+n_\phi+n_f)^2 + xV_o[(n_\phi+n_f)^2+n_\phi-n_f-0.25] - V_{dc}(n_\phi+n_f)^2} \quad (80)$$

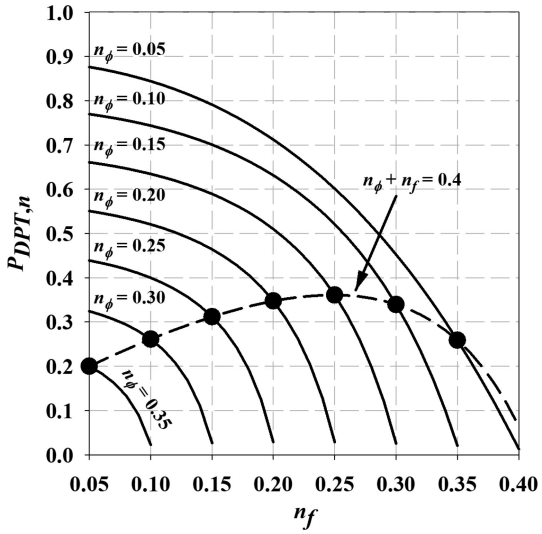

Fig. 7. Plot of $P_{DPT,n}$ in terms of different values of n_ϕ and n_f.

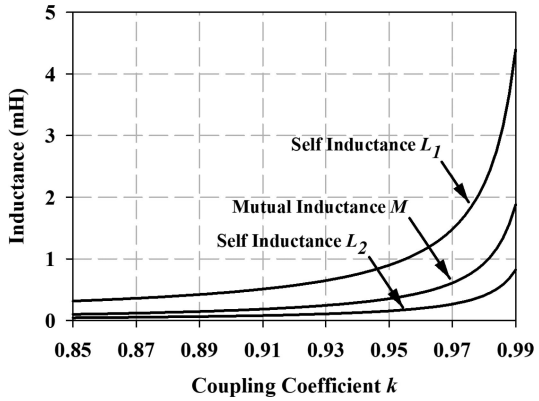

Fig. 8. Plot of the inductances L_1, L_2, and M in terms of the coupling coefficient k.

TABLE I
LIST OF THE PARAMETERS USED IN SIMULATION

Parameter	Value
Input voltage V_{in}	190 V
Output volage V_o	48 V
Output power P_o	450 W
Switching frequency f_s	140 kHz
Coupled inductor L_1, L_2, M	620 μH, 120 μH, 255 μH
Transformer turns ratio n	2.8
Series inductor L_s	40 μH
DC-bus capacitors C_1, C_2	10 μF
Snubber capacitors C_{s1}, C_{s2}	680 pF
Output capacitor C_o	22 μF

be sufficiently less than 0.5. Considering $n_\phi + n_f$ equal to 0.4, (79) implies that V_{dc} should be less than 427.5 V. Therefore, V_{dc} is selected to be 400 V.

The next step is to calculate the normalized direct power transferred $P_{\text{DPT},n}$ in terms of different values of n_ϕ and n_f using (78) and (80) as plotted in Fig. 7. This figure shows the plot of $P_{\text{DPT},n}$ in terms of different values of n_f in the range of $0 < n_f < 0.5 - n_\phi$ for several values of n_ϕ equal to 0.05, 0.10, 0.15, 0.20, 0.25, 0.30, and 0.35. Also, the dashed line illustrates the curve of $P_{\text{DPT},n}$ in terms of different values of n_ϕ and n_f that satisfy $n_\phi + n_f = 0.4$. According to this figure, $P_{\text{DPT},n}$ reaches its maximum value of 36% at $n_\phi = 0.15$ and $n_f = 0.25$. However, with $n_\phi = 0.1$ and $n_f = 0.3$, $P_{\text{DPT},n}$ is 34% which is near the maximum value. This results in $P_{\text{DPT}} =$ 153 W and $P_{\text{tran}} = 297$ W. In other words, around 150 W is transferred to the output directly through the coupled inductor and around 300 W through the transformer.

Having n_ϕ and n_f determined, x is obtained equal to 2.29 using (78). According to (82)–(85), the design of the inductances L_1, L_2, and M is dependent on the value of the coupling coefficient k. Fig. 8 demonstrates how this parameter affects the design of these inductances. As observed, all the inductances L_1, L_2, and M tend toward large values as k approaches unity. Therefore, with a sufficiently small coupling coefficient, it is possible to use small inductances. According to Fig. 8, having a coupling coefficient in the range of $0.9 < k < 0.95$ results in reasonable values for the inductances. Moreover, achieving this range for the coupling coefficient does not complicate implementing the coupled inductor. Considering $k = 0.93$, (85) results in $L_2 = 107\,\mu$H. Consequently, M and L_1 are determined as 244 and 647 μH, respectively, based on the values of M/L_2 and L_1/L_2 given in (74) and (83).

Using (86) and (87), the series inductance and the transformer turns ratio are obtained as $L_s = 43\,\mu$H and $n = 2.4$. Considering $t_{fi} = 10$ ns and $k_v = 0.1$, (89) implies that the snubber capacitors C_{s1} and C_{s2} should be greater than 640 pF to significantly reduce the current–voltage overlap of the power switches at their turn-OFF instants. An adaptive technique is used to set the required dead time based on the load. Here, the maximum required dead time is considered to be 200 ns, which is nearly 2.5% of the switching period.

The proposed converter is simulated with the parameters listed in Table I and its waveforms are illustrated in Fig. 9. Fig. 9(a) and (b) shows the waveforms of the power switches S_1 and S_2, respectively. As observed, when one of the switches is turned OFF, the body diode of the other switch turns ON, thereby providing ZVS turn-ON conditions. In addition, current–voltage overlap at turn-OFF instants is sufficiently small for both the switches. It is also observed that the dc-bus voltage is near 400 V. Fig. 9(c) illustrates the currents i_{L1} and i_{L2} flowing through the primary and secondary windings of the coupled inductor. It is observed that the input current has a quasi-rectangular waveform. Moreover, t_f is equal to 2.4 μs, which is 34% of the switching cycle. In other words, the parameter n_f is slightly greater than the desired value of 0.3. Voltage waveforms of the inverter output and the transformer primary winding as well as current waveform of the series inductor are illustrated in Fig. 9(d). As observed, the square voltages have a 0.7 μs delay (almost 10% of the switching cycle). In other words, the parameter n_ϕ is approximately equal to the designed value of 0.1. Fig. 9(e) shows the voltage waveform of the transformer secondary winding v_{sec} and the current

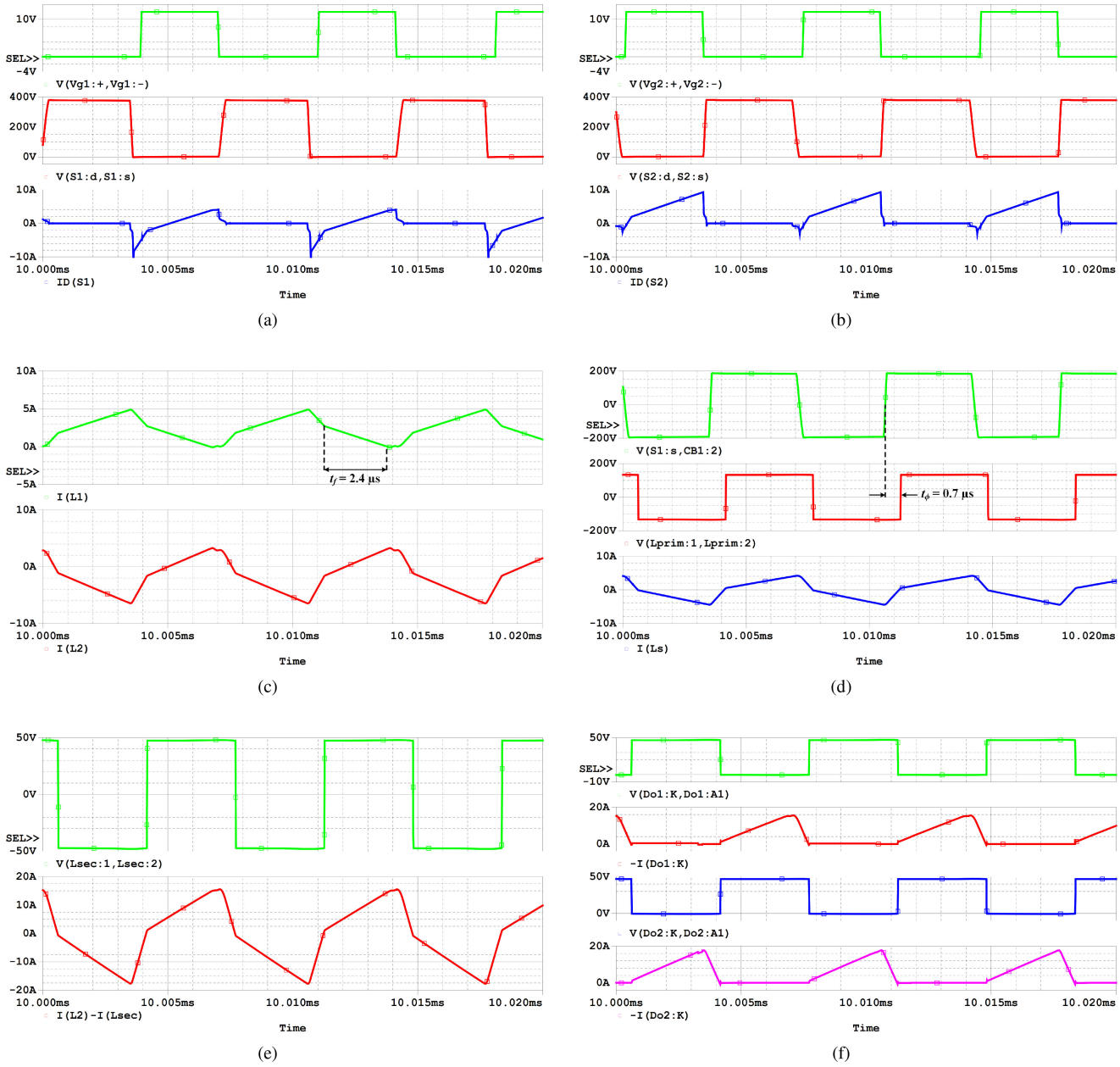

Fig. 9. Simulation results at the nominal load. (a) Waveforms of the switch S_1. (b) Waveforms of the switch S_2. (c) Current waveforms of the coupled inductor. (d) Waveforms of v_{inv}, v_{prim}, and i_{Ls}. (e) Waveforms of v_{sec} and i_t. (f) Current and voltage waveforms of the output diodes D_{o1} and D_{o2}.

waveform flowing through the output bridge diodes i_t. As explained earlier, direction of this current determines the polarity of the voltage applied to the transformer secondary winding. According to Fig. 9(f), showing the current and voltage waveforms of D_{o1} and D_{o2}, the output diodes turn ON and OFF under ZCS conditions.

From (31) and (48), it can be obtained how the power transferred through the transformer P_{tran} as well as the power directly transferred to the output P_{DPT} are inversely proportional to f_s. Thus, as shown in Fig. 10, both the power components will keep their ratio over the entire f_s range.

As signified by the mathematical equation derived for V_{dc} given in (66), the proposed converter benefits from an almost constant dc-bus voltage over the entire load range. However, possible variations of the inductance values can result in V_{dc} variation. Therefore, it is required to investigate the sensitivity of V_{dc} in the proposed converter to the inductance values. For this purpose, V_{dc} is obtained using (66) having each of the inductances L_1, L_2, and L_s individually vary in the range of $\pm 5\%$ of its nominal value. According to Fig. 11, the deviation of the dc-bus voltage from its desired value as a result of variations of the inductances is less than 15%, which is not significant.

To investigate the impact of variation of each parameter on the overall performance of the proposed converter, the output power is obtained having each of the inductances L_1, L_2, M, and L_s individually vary in the range of $\pm 10\%$ of its nominal value. According to Fig. 12, the impact of the coupled inductor parameters (L_1, L_2, and M) on the output power is more than

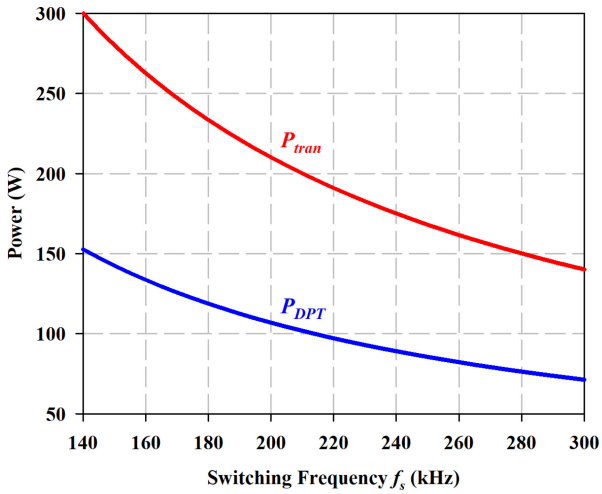

Fig. 10. Variation of the output power components P_{tran} and P_{DPT} with the switching frequency f_s.

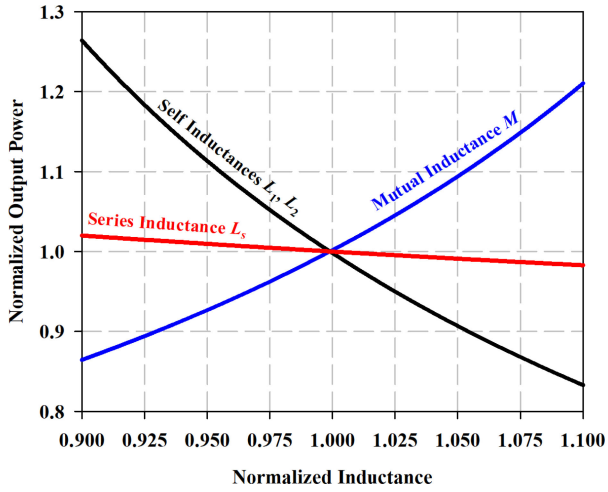

Fig. 12. Impact of variation of the converter parameters on the output power.

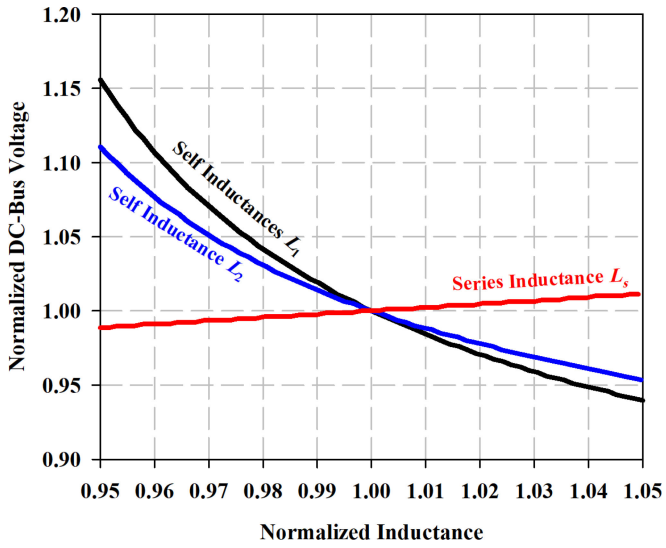

Fig. 11. Impact of Variation of the Converter Inductances on the dc-bus Voltage.

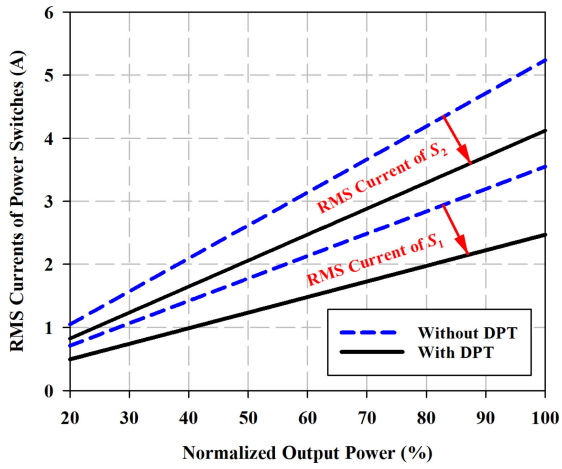

Fig. 13. RMS currents of the power switches for the proposed converter with and without the DPT capability.

TABLE II
LIST OF THE COMPONENTS USED IN THE IMPLEMENTED PROTOTYPE

Component	Value or part number
Power switches S_1 and S_2	IPB60R280P7
Input diode D_{in}	TPMR10G
Output diodes $D_{o1} - D_{o4}$	VB30100S-E3
Coupled inductor L_1, L_2, M	620 μH, 120 μH, 254 μH
Transformer turns ratio n	2.8
Series inductor L_s	40 μH
DC-bus capacitors C_1, C_2	10 μF
Snubber capacitors C_{s1}, C_{s2}	680 pF
Output capacitor C_o	4 $\times$ 4.7 μF

that of the series inductance L_s. As the coupled inductor is located at the converter input, it has an important role in the operation of the converter. However, the deviation of the output power from its nominal value due to the variation of L_s can be readily compensated by adjusting the switching frequency.

In order to investigate how the DPT capability can result in reduced current stress and conduction losses, the rms currents of the power switches S_1 and S_2 as well as the peak and rms values of the input current are obtained for the proposed circuit topology for two different cases, with and without DPT. In the case of not having DPT, it is assumed that the inductor L_2 no longer exists. In this situation, the other components are redesigned using the guidelines given in the previous section, assuming k is zero and L_2 approaches infinity. The components are obtained as $L_1 = 114\,\mu$H, $L_s = 46\,\mu$H, and $n = 2.5$. Fig. 13 illustrates the rms currents of S_1 and S_2 for the two cases. As observed, the rms currents are reduced with the DPT capability. Also, Fig. 14 shows how the proposed converter with the DPT capability benefits from reduced peak and rms values for the input current due to its quasi-rectangular shape instead of triangular waveforms.

To compare the performance of the proposed circuit topology with that of the SRC and the CDHBC, these circuits are

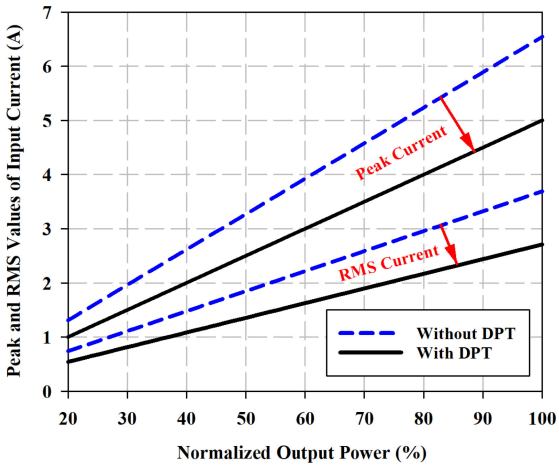

Fig. 14. Peak and rms values of the input current for the proposed converter with and without the DPT capability.

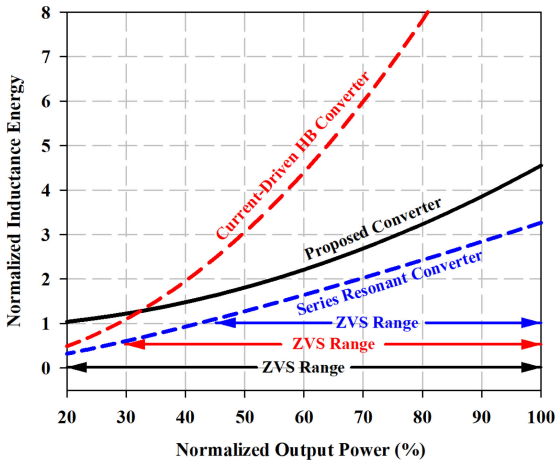

Fig. 15. ZVS range of the power switches for the proposed converter, the SRC, and the CDHBC.

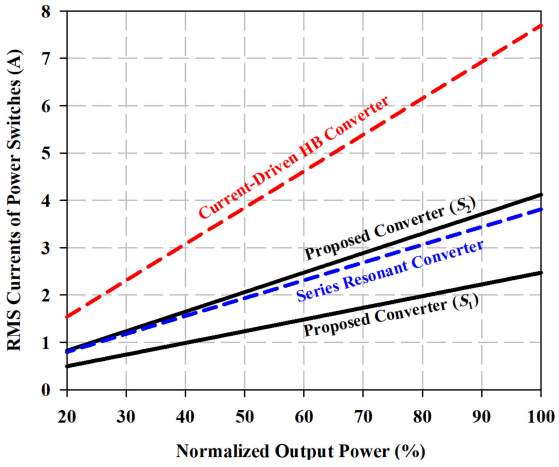

Fig. 16. rms currents of the power switches for the proposed converter, the SRC, and the CDHBC.

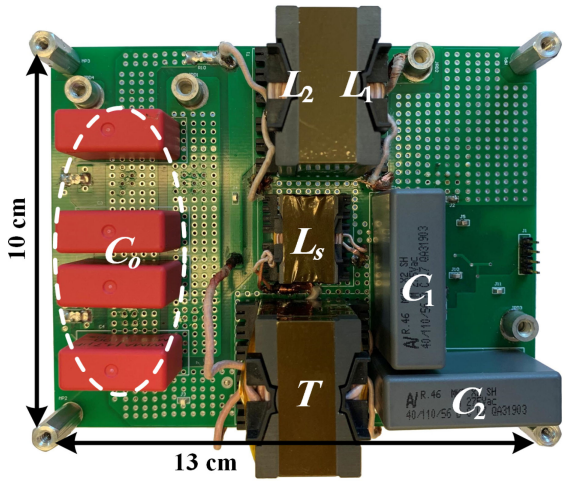

Fig. 17. Photograph of the implemented prototype.

TABLE III
CONDUCTION LOSSES OF THE COMPONENTS USED IN THE IMPLEMENTED PROTOTYPE

Component	Resistance [mΩ]	RMS current [A]	Power loss [W]
Power switch S_1	280	2.47	1.71
Power switch S_2	280	4.12	4.75
Inductor L_1	115	2.71	0.84
Inductor L_2	55	3.23	0.57
Inductor L_s	80	2.58	0.53
Primary coil L_{prim}	190	2.58	1.26
Secondary coil L_{sec}	35	6.74	1.59
Component	**Voltage drop [V]**	**Average current [A]**	**Power loss [W]**
Input diode D_{in}	0.60	2.48	1.49
Output diodes D_{o1-4}	0.35	4.67	4×1.63
Total			19.26

designed and simulated for the same specifications (190 V input voltage, 48 V output voltage, 450 W rated power, and 140 kHz nominal switching frequency). The SRC is designed based on the guidelines given in [38] to have minimum stress for its resonant components and semiconductor devices. For this purpose, the converter components are obtained to be $L_r = 5.9\,\mu$H, $C_r = 400\,$nF, and $n = 1.88$. Similarly, the components of the CDHBC are calculated as $L_s = 6.7\,\mu$H and $n = 1$ according to the design considerations provided in [33].

The ZVS range for each circuit can be achieved using (72). For this purpose, the snubber capacitors $C_{s1,2}$ are first designed using (88). Considering the same values for t_{fi} and k_v, the snubber capacitors are obtained as $C_{s1,2} = 780\,$pF for the SRC and as $C_{s1,2} = 2.7\,$nF for the CDHBC. To achieve the ZVS range, the inductor energy for each converter is obtained using the left-hand side term in (72) at different output powers and is then normalized to the corresponding capacitor energy using the right-hand side term in (72).

Fig. 15 illustrates the ZVS range of the power switches for the proposed converter as well as the SRC and the CDHBC.

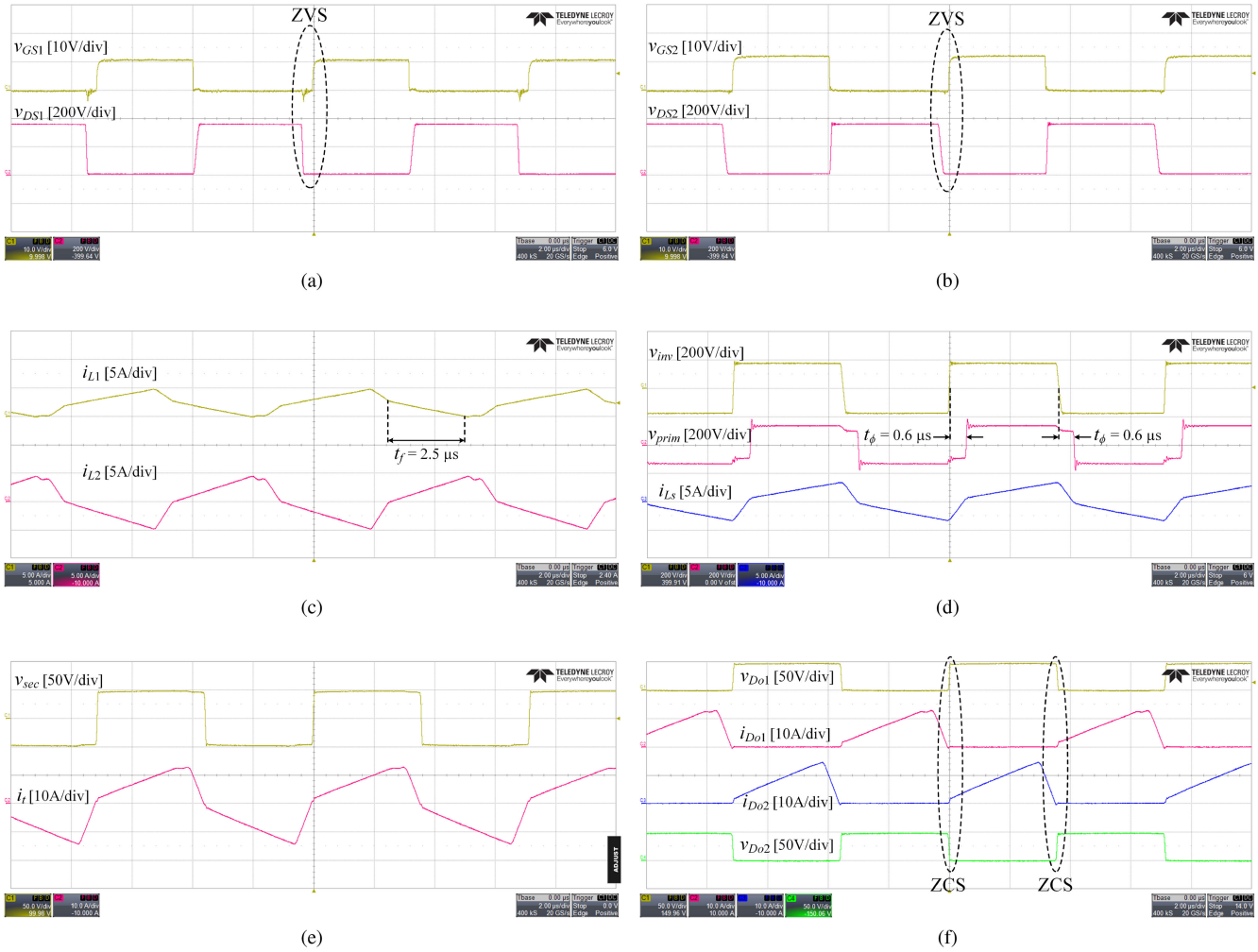

Fig. 18. Experimental waveforms obtained from the implemented prototype at full-load. (a) Waveforms of switch S_1. (b) Waveforms of switch S_2. (c) Current waveforms of the coupled inductor. (d) Waveforms of v_{inv}, v_{prim}, and i_{Ls}. (e) Waveforms of v_{sec} and i_t. (f) Current and voltage waveforms of the output diodes D_{o1} and D_{o2}.

As expected, the CDHBC offers ZVS performance over a wider operating range compared to the SRC. As the SRC has been designed for the minimum tank current stress, its ZVS operation is lost at light loads. On the other hand, the proposed converter achieves the ZVS characteristics over the entire load range from 20% to 100% of the rated power. Fig. 16 shows the rms currents of the power switches for these three converters at different output powers. It should be noted that in the SRC and the CDHBC, both power switches have the same current, while the low-side power switch (S_2) in the proposed circuit has higher current compared to the other switch (S_1). As observed, the CDHBC suffers from much higher current stress with respect to the SRC. On the other hand, the rms current of S_2 in the proposed converter is slightly higher than that of the SRC, whereas the rms current of S_1 is significantly lower. However, the sum of rms currents of both switches for the proposed converter is less than that of the SRC. In summary, the proposed converter benefits from the main feature of the current-driven structures having ZVS characteristics over a wide range of operation without high current stress for the power switches.

VI. Experimental Results

In order to examine the performance of the proposed converter in practice, a 450-W laboratory prototype is implemented for the given application and its experimental results are presented. A battery simulator is used in the experimental setup to model the ESS. The model of the battery system is NHR 9210 from NH Research Inc. and the equipment is configured to have a discharged voltage of 42 V and a fully charged voltage of 50 V. The components used in the prototype are listed in Table II and its photograph is depicted in Fig. 17. According to the power rating and dimensions of the implemented prototype shown in Fig. 17, its power density is obtained as 0.989 W/cm^3.

Fig. 18 shows the experimental waveforms obtained from the implemented prototype under the full-load condition. These experimental waveforms are in good accordance with the theoretical and simulation waveforms illustrated in Figs. 5 and 9, respectively. Particularly, according to Fig. 18(c) and (d), $t_f = 2.5\,\mu$s and $t_\phi = 0.6\,\mu$s, which are almost the same as the simulation values. To examine the proposed converter performance under different load conditions, the waveforms obtained

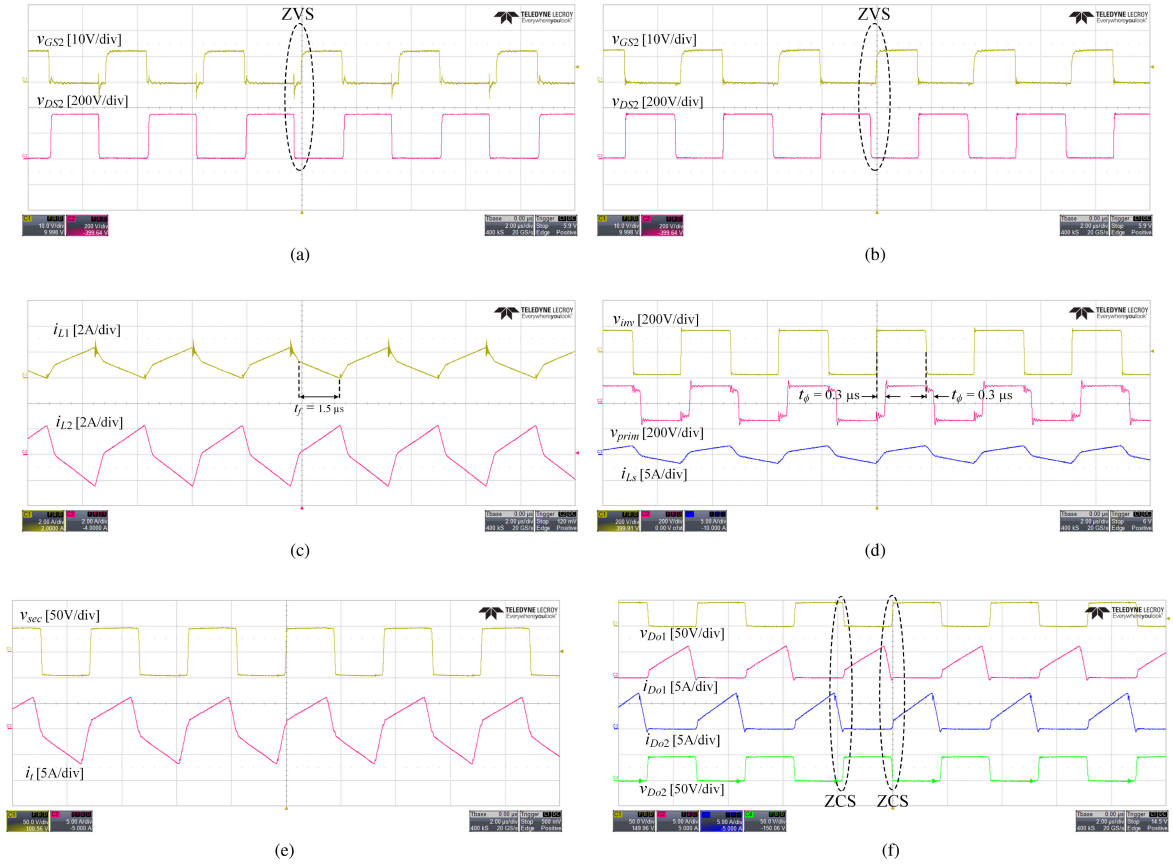

Fig. 19. Experimental waveforms obtained from the implemented prototype at half-load. (a) Waveforms of switch S_1. (b) Waveforms of switch S_2. (c) Current waveforms of the coupled inductor. (d) Waveforms of v_{inv}, v_{prim}, and i_{Ls}. (e) Waveforms of v_{sec} and i_t. (f) Current and voltage waveforms of the output diodes D_{o1} and D_{o2}.

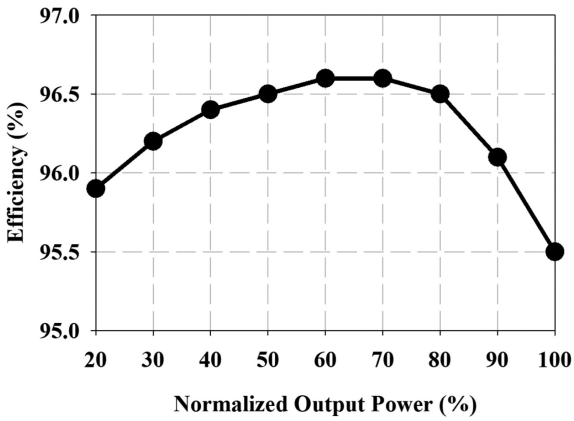

Fig. 20. Efficiency plot of the implemented prototype.

from the implemented prototype at 50% of the nominal power are also illustrated in Fig. 19. In order to reduce the power delivered to the output to half the rated power, the switching frequency is increased to 280 kHz. According to Fig. 19(a) and (b), showing the voltage waveforms of S_1 and S_2, the power switches operate with ZVS characteristics. In addition, it is observed that the dc-bus voltage is still the same as that for the rated power. In other words, the proposed converter benefits from a nearly constant dc-bus voltage under different load conditions. From Fig. 19(c) and (d), it is observed that t_f is 1.5 μs ($n_f = 0.4$), slightly greater than its value at full-load, while t_ϕ is 0.3 μs ($n_\phi = 0.1$), equal to the desired value. In this case, $n_\phi + n_f$ is near 0.5 or, equivalently, time duration of Mode 7 is short enough. This results in low peak and rms values for the input current. In other words, the proposed converter keeps the quasi-rectangular waveform for the input current under different load conditions.

Fig. 20 shows the efficiency measured from the implemented prototype from 20% to 100% of the rated power. As observed, with reducing power from full-load to light-load, efficiency first rises from 95.5% (at the nominal power) to a peak value of 96.6% (at 70% of the nominal power) and, then, it starts decreasing. As mentioned earlier, the output power reduces with the switching frequency in the proposed converter. Consequently, decreasing the output power results in lower conduction losses, however, higher switching losses. It is worth mentioning that switching losses are negligible compared to conduction losses in low frequencies due to the ZVS performance of the proposed converter. However, as the output power decreases below 70% of the rated power, switching losses become considerable and, consequently, efficiency starts degrading.

To analyze how each component contributes to the total power losses, the loss breakdown of the implemented prototype is illustrated in Fig. 21 under full-load and half-load conditions. As observed, the power losses associated with output diodes

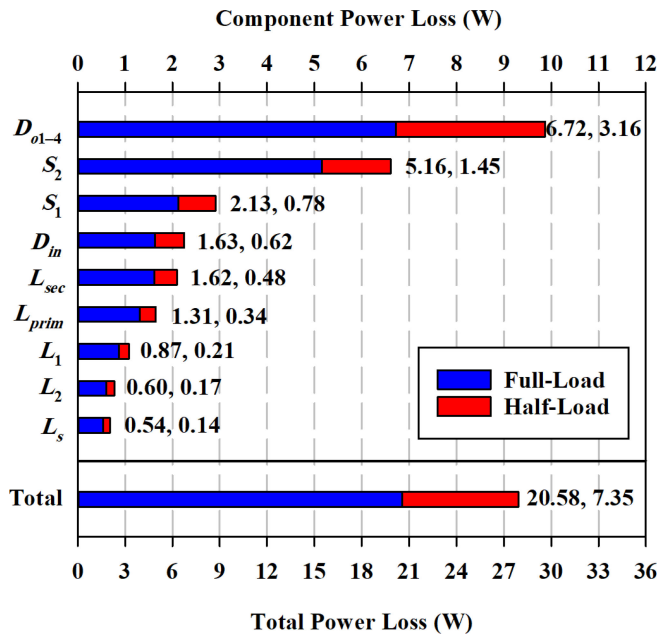

Fig. 21. Loss breakdown of the implemented prototype.

D_{o1}–D_{o4} and power switch S_2 constitute the major portion of the total losses. Considering the high output current level and the fact that in the proposed circuit topology, S_2 conducts an increased current, it is reasonable that these components show higher losses with respect to the other components. However, the power losses associated with output diodes D_{o1}–D_{o4} can be reduced by using the synchronous rectification technique. To further investigate the power losses, Table III lists the conduction loss of each component at the rated power calculated by measuring its rms or average current. It should be mentioned that the reported ON-resistances of the power switches are found in their datasheets, while the ohmic resistances of the inductors and coils as well as the voltage drops of the diodes are measured from the implemented prototype. From Fig. 21 and Table III, it can be observed that the conduction losses are dominant compared to the switching losses, which is expected due to the soft-switching performance.

VII. Conclusion

A novel isolated dc–dc converter circuit topology has been proposed in this article, which is able to demonstrate high performance for a wide range of operating conditions. This isolated dc–dc converter is well-suited for dc microgrid applications, where the converter should be able to maintain the dc voltage level of an LV bus within a desired range. The proposed converter is able to minimize both the conduction and switching losses. The power semiconductors on the primary side of the converter operate under ZVS while the output diodes operate under ZCS. One of the main features of this converter is its DPT capability, which reduces the power processed by the power semiconductors and minimizes the conduction losses. A portion of the power can directly be transferred to the output, which reduces the power ratings of the components and their costs. Another advantage of this structure is the quasi-rectangular waveform of the input current. This feature effectively reduces the peak and rms values of the input current. Consequently, the conduction losses in this power circuitry can be reduced significantly. Simulation and experimental results confirm the superior performance of the proposed structure.

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Milad Zareie (Student Member, IEEE) received the bachelor's degree in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2016, and the MASc. degree from Queen's University, Kingston, ON, Canada, in 2018. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB, Canada.

He has conducted more than five industrial projects in renewable energy systems and LED drivers. He has authored more than eight journal and conference proceeding papers and is the holder of two U.S. patents (pending). His research focuses on battery chargers, light emitting diode drivers, and control and integration of distributed energy sources into microgrids.

Mr. Milad has served as the reviewer of the IEEE Applied Power Electronics Conference (APEC) for the last three years. He has also received numerous awards such as the "Eyes High Doctoral" Award from the University of Calgary and "Mitacs Research Accelerate" Award.

Behzad Poorali (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2013, 2015, and 2019, respectively.

Since 2019, he has been a Postdoctoral Associate with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, Canada. His research interests include switched-mode power supplies, high step-up converters, light-emitting diode drivers, and control design of power converters.

Suzan Eren (Member, IEEE) received the B.Sc. (with first class honours), M.Sc., and Ph.D. degrees in electrical engineering from Queen's University, Kingston, ON, Canada, in 2006, 2008, and 2013, respectively.

She is an Assistant Professor with the ECE Department, Queen's University. She has received several academic scholarships, including the 2011–2012 Bert Wasmund Scholarship for Sustainable Energy Research, and has extensive academic and industrial experience developing highly efficient power converters. She has authored 48 peer-reviewed papers, holds 11 U.S. patents. Her research interests include the control and design of power converters used in microgrids and renewable energy systems.

Dr. Eren was a recipient of the Professor of the Year Award by the Second-Year Electrical Engineering Student Body in 2017 and 2018. She is a member of ePOWER, the Queen's Centre for Energy and Power Electronics Research. She is currently the IEEE Kingston Section Chair.

Majid Pahlevani (Senior Member, IEEE) received the Ph.D. degree from Queen's University, Kingston, ON, Canada, in 2012.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Queen's University. He was an Assistant Professor with the University of Calgary, Calgary, AB, Canada, from 2016 to 2019. He was also the Chief R&D Engineer and then the VP of Technology with SPARQ Systems, Inc., from 2011 to 2016. At SPARQ, he invented multiple innovative power circuitry and digital control techniques for SPARQ's main product and QUAD microinverter. He collaborated with Freescale Semiconductor, Inc., where he was the Leader of a research team working on the design and implementation of the power converters for a pure electric vehicle from 2008 to 2011. He has conducted more than 20 industrial projects in renewable energy systems, energy storage systems, electric vehicles, and energy devices. He has authored more than 150 journal and conference proceeding papers and is the holder of 50 U.S. patents (issued/pending).

Dr. Pahlevani is the Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and a member of the IEEE Power Electronics Society. He has also received numerous awards such as the Early Research Excellence Award form Alberta, Canada, Research Achievement Award and Teaching Achievement Award from the University of Calgary, Engineering and Applied Sciences Outstanding Thesis Award from Queens University, Kingston, ON, Canada, Research Excellence Award from IEEE Canada, and Distinguished Research Award from the University of Calgary.