Multiresonant and Multimode Operation of the Switched-Resonator Converters

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***Abstract*—The multiresonant and multimode operations of the switched-resonator converter are revealed in this article. Distributed inductors of a switched-resonator converter can be operated either in resonant or linear modes. As a result, there are four operation regimes that cannot be observed in the conventional resonant and hybrid switched-capacitor converters. The duty ratio modulation of the control signals not only switches the converter operation between different regimes but also regulates output voltage while having soft switching. In addition to that, the switching frequency of the converter can be modulated to achieve the aforementioned objectives. Realization of a switched-resonator converter based on this concept having buck–boost characteristics is presented in this article. Operation of the proposed converter is analyzed, and it is verified using experimental results.**

***Index Terms*—Buck–boost gain, multimode, multiresonant, pulsewidth modulation, switched-resonator converter (SwRC), switching-frequency modulation.**

I. Introduction

SWITCHED-capacitor converter (SCC) is a viable option to increase the power density of dc–dc converters eliminating magnetic elements [2]. There is an increasing trend to use them in mobile computing, portable electronics, and renewable energy applications. In portable electronics applications, positive output buck–boost converters are essential when the output voltage is in the mid-range of the battery cells. The common examples are 3.3-V output with a 3–4.2 V Li cell input and 5-V output with a 3.6–6 V four-cell alkaline battery input [3]. But SCCs have topology specific fixed voltage conversion ratios either buck or boost (but not both), low energy conversion efficiency due to exponential charge distribution and unidirectional energy flow [4]. Moreover, the effective resistance of an SCC is frequency-dependent, and that property is employed to regulate a converter output voltage modulating switching frequency [5]. As a result, SCC behaves as a conventional linear regulator having gain-dependent energy conversion efficiency.

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The voltage regulation of these SCCs is extended, merging a buck output stage in [6]. The converter merging concept has been further advanced, sharing elements among cascaded stages in [7]. On the other hand, the charge distribution characteristics of SCCs are modified by adding an inductor in series with the capacitor in [8]. The resultant converter is called a resonant SCC (ReSCC). The modified current waveforms help turn-ON and -OFF semiconductor devices having zero-current switching (ZCS). The output voltage of the ReSCCs is regulated modulating the switching frequency [9] and dynamic off-time [10]. In the early developments, the inductor is placed in series with the energy transfer capacitor compared to the later cases, which are based on an output inductor. The ReSCCs based on the output inductor is called as hybrid ReSCCs (HybReSCC). These HybReSCCs have three resonant operation modes, which can be identified examining the effective resistance, and the relationship between the resonant and switching frequencies, as explained in [11]. Further analyzing effective resistance and operation sequence in the converters, multimode operation in the HybReSCC has been identified and reported in [12]. In the extra operation regime, the inductor current is quasi-resonant, and it is operated in both resonant and linear modes. Similar behavior can be observed in the newest addition to the SC converter family, which is called as switched-resonator converters (SwRCs). There are multiple resonators based on distributed inductors in the SwRC, as demonstrated in [13]. Later, several converter families based on the SwRC concept have been proposed in [14]–[19]. The direct resonant cell proposed in [20] is extended in [17] to derive converters based on the multiresonant operation. The SwRC proposed in [20] has continuous buck gain that can be varied by modulating pulsewidth of the control signals. Another variant of SwRC and several families of converters having buck, boost, and buck–boost properties are proposed in [21] and [22]. Those converters are based on a single resonator switched in between the source and load to transfer energy. The inductor is operated in both linear and resonant modes to vary the converter gain modulating the switching frequency. The concept is further extended to realize a multiport converter in [23]. SwRC based on a single resonator proposed in [24] has continuous buck–boost gain in a wide range, and its output voltage is regulated using pulse-density modulation. Converter families presented in [24] and [25] have efficiencies independent from the voltage gain, and this feature cannot be observed in SCCs. Another variant of the converter family called as switched tank converter has been proposed in [26] based on the distributed inductors and capacitors. In these converters, the switching frequency is modulated in a

wide band to regulate the output voltage when there are changes in the line voltage or load changes. The switching frequency modulation is not beneficial designing the remaining parts of the power conversion system, especially when the power converter has magnetic energy transfer elements [27]–[29]. Therefore, SwRCs based on the pulsewidth modulation are more useful.

The SwRCs are based on distributed inductors and one or more energy transfer capacitors. Hence, they give rise to a converter having similar or different resonant frequencies. These resonators can be operated at same [17] or different [14]–[16] time intervals to transfer energy. As similar to the ReSCs, the inductor current could be in one of the three operation modes that can be identified based on the relationship between the switching and resonant frequencies [15]. However, it depends on the switches that enable resonators. When switches support bidirectional current conduction, then the converters can be identified as indirect and otherwise they are called direct. As a result, the voltage gain is a function of the ratio between the switching to resonant frequencies. Switches of these converters experience ZCS when resonator currents complete a one-half cycle within the resonator active time interval and otherwise, they have zero-voltage switching (ZVS). The ZCS helps eliminate losses due to the voltage and current overlap during the switching transition. The ZVS reduces both losses rise from the voltage and current overlap and the energy stored in the output capacitance of a metal–oxide–semiconductor field-effect transistor (MOSFET). The distributed inductors can be operated in either resonant or linear modes, as similar to the HybReSCC converters.

The multimode operation of the distributed inductors to regulate the output voltage by modulating the pulsewidth of the control signal is demonstrated in [20]. The patent is based on the two operation regimes that can be observed in converters based on the multiple resonators. Therefore, a thorough investigation of the multimode (resonant and linear) operation of the SwRC is presented in this manuscript. To this end, an SwRC derived using a switched capacitor network (SCN) and distributed inductors are employed. The basic idea behind an SwRC realization and its four operation regimes (I to IV) are explained in Sections II and III, respectively. The derived converter and its operation in two out of four operation regimes are thoroughly investigated in Sections IV–VII, including converter operation validation using simulation and experimental results. The advantages of the multiresonant and multimode operation of the derived SwRC can be summarized as follows.

1) The load-independent ZCS in all semiconductor devices in operation regime I.
2) The converter is a voltage doubler in operation regime I.
3) The load-independent ZCS at turn-ON in all semiconductor devices and turn-OFF in the switches connected to the input-side resonator in operation regime II.
4) The converter has a buck–boost gain (ideally from 0 to 2) in operation regime II and gain can be varied modulating either pulsewidth or frequency of the switch control signals.
5) Change the voltage regulation range adjusting the inductance ratios at the design stage when there are fixed inductors. This can be done dynamically by using a variable inductor, as demonstrated in [30].

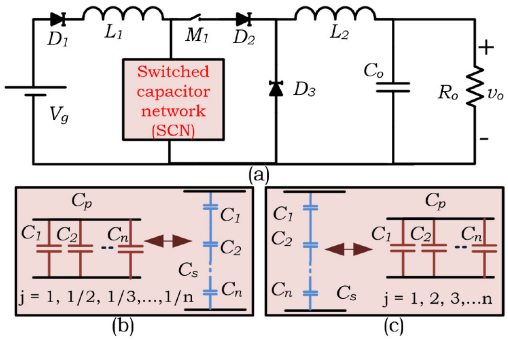

Fig. 1. SwRC (a) conceptual realization, (b) and (c) SCN behavior, where j is the voltage conversion ratio when converter is in the operation regime I and it depends on the number of capacitors (n) in the SCN.

II. Switched-Resonator Converter

The realization of SwRC can be explained using the high-level circuit diagram shown in Fig. 1(a). The two inductors (L_1 and L_2) should be integrated with the SCN alternatively to form resonators having similar or different characteristic frequencies with the help of the switch M_1. To this end, there should be a semiconductor switching network within the SCN to switch capacitors C_1 to C_n to form capacitor banks C_p and C_s, as shown in Fig. 1(b) and (c), alternatively. Moreover, there are diodes (D_1 and D_2) at the input and output sides of the converter to make L_1 and L_2 currents unidirectional. Hence, this converter can be treated as a direct SCC. Furthermore, the unidirectional switch (D_3) at the output side recycles energy stored in the inductor L_2. As a result, the inductor L_2 can be operated in the linear mode without interfering with the resonators. The resultant converter gain depends on the sequence of connecting the capacitor banks (C_p and C_s) with the inductors during different subintervals within a single switching cycle. The maximum gain of such an SwRC is given by (1), where j depends on the number of capacitors in the SCN and their connecting sequence. The realization of an SwRC having maximum gain 2 ($j = \frac{1}{2}$) is considered in this manuscript as a case study. Such an SwRC has four different operation regimes, and its operation in those regimes can be explained considering a converter based on the resonators L_1C_p and L_2C_s, as shown in Fig. 1(b). A similar description can be employed if resonators are based on L_1C_s and L_2C_p, as shown in Fig. 1(c). The converter operation is explained assuming ideal semiconductor and passive devices and high-quality factors of the resonators

$$V_o = \frac{V_g}{j}. \tag{1}$$

III. Multiresonant and Multimode Operation

The four operation regimes of the converter are identified using operation modes of each inductor current, as summarized in Table I. The inductor operation could be in either resonant or linear modes. In this study, resonant current waveforms

TABLE I
IDENTIFICATION OF THE FOUR OPERATION REGIMES

Regime	L_1 inductor current (i_{L_1})	L_2 inductor current (i_{L_2})
1	Resonant	Resonant
2	Resonant	Resonant+linear
3	Quasi-resonant	Quasi-resonant
4	Quasi-resonant	Quasi resonant+linear

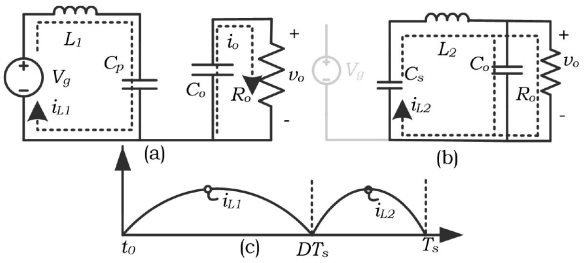

Fig. 2. Equivalent circuits of the converter when it is in operation regime I: (a) L_1C_p and (b) L_2C_s resonators exist; and (c) ideal waveforms.

having two characteristic frequencies within a one-half cycle are called as quasi-resonant. The characteristic frequency of the input inductor resonant current (i_{L1}) may have either single or multiple values within a one-half period of the operation. The output inductor (L_2) current could be in either linear or resonant modes. In the resonant mode, it has either single or multiple characteristic frequencies within a one-half cycle as similar to i_{L1}. However, both inductors have zero initial currents when the respective resonator is enabled.

A. Operation Regime I

In this regime, both inductor currents (i_{L1} and i_{L2}) complete a one-half cycle, as shown in Fig. 2(c). The corresponding equivalent circuits are shown in Fig. 2(a) and (b). The characteristic frequencies of each resonator (ω_1 and ω_2) are given by

$$\omega_1 = \frac{1}{\sqrt{L_1C_p}}, \quad \omega_2 = \frac{1}{\sqrt{L_2C_s}} \tag{2}$$

$$f_s < \pi\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right). \tag{3}$$

Therefore, the maximum switching frequency ($f_s = \frac{1}{T_s}$) of the converter is given by (3). i_{L1} completes a one-half cycle when the resonator L_1C_p is enabled during $t_0 \leq t < DT_s$ interval, as shown in Fig. 2(a). The energy stored in the SCN during previous subinterval discharges into C_o and the load when L_2C_s is enabled during $DT_s \leq t < T_s$ interval, as shown in Fig. 2(b). Both inductor currents are zero at the beginning and end of each subinterval since they complete a one-half cycle within the respective subintervals. Hence, all semiconductor devices are turned ON and OFF having ZCS. The switching frequency of the converter can be lowered by keeping resonator enable time longer than DT_s and $(1-D)T_s$. But converter operation remains unchanged since negative inductor currents are blocked by the switches. Hence, there will be time intervals that neither inductors conduct. The load power will be provided by the output capacitor (C_o) during those intervals. The converter gain is a constant in this operation regime and it is $\frac{1}{j}$, where j depends on the number of capacitors (n) in the SCN and the order of connecting C_p and C_s. For example, if the capacitor bank consists of two capacitors and they connected in the order shown in Fig. 1(b), then converter gain ($M = \frac{V_o}{V_g}$) is 2. If the capacitor bank connected in the order shown in Fig. 1(c), then the converter gain (M) is 0.5. This operation regime is implemented in a derived converter based on the aforementioned SCN concept to obtain uncontrolled voltage output in Section IV-A.

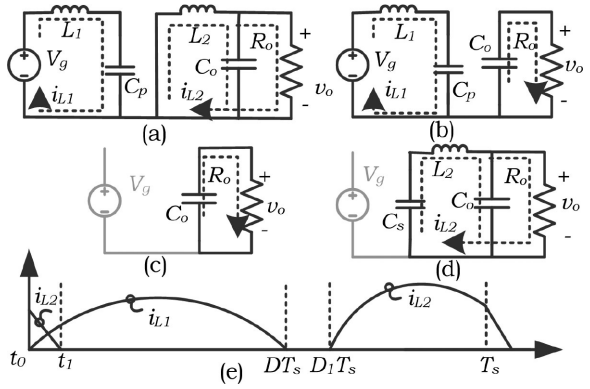

Fig. 3. Converter equivalent circuit when: (a) L_1C_p resonator exists and L_2 inductor in linear mode; (b) L_1C_p resonator exists; (c) neither inductor conducts current; (d) L_2C_s resonator exists; and (e) ideal waveforms in the operation regime II.

B. Operation Regime II

This operation regime exists when duty ratio (D_1) that enables the resonator L_1C_p is larger than the duty ratio (D) in regime I while having the same switching frequency (f_s). The ideal inductor current waveforms during each subintervals are shown in Fig. 3(e). The resonator L_1C_p completes a one-half cycle having equivalent circuits shown in Fig. 3(a) and (b) during $t_0 \leq t < DT_s$ interval. However, the equivalent circuit depicted in Fig. 3(a) exists for a short interval ($t_o \leq t \leq t_1$) at the beginning, until the energy stored in L_2 completely discharges to the load. This is because the interval ($D_1T_s < t < T_s$), which enables the L_2C_s resonator, is not sufficient to dissipate energy transferred from capacitor C_s into L_2. The energy stored in L_2 dissipates while operating it in the linear mode without interfering with the L_1C_p conducting current through D_3. The equivalent circuit shown in Fig. 3(c) exists once the L_1 current reaches zero at $t = DT_s$, as shown in Fig. 3(e). As a result, neither inductor conducts since the SCN does not enable the resonator L_2C_s yet. The capacitor bank C_p is reformed to C_s using the SCN at $t = D_1T_s$ having the equivalent circuit shown in Fig. 3(d) and it exists until the end of the switching cycle. Therefore, L_2 has its operation in resonant and linear modes. Similar behavior in the circuit can be observed even though making the interval $DT_s < t < D_1T_s$ zero, because there is no energy transfer within the resonators. In that case, the switching frequency of the converter will be higher than f_s. This operation regime is used in a derived

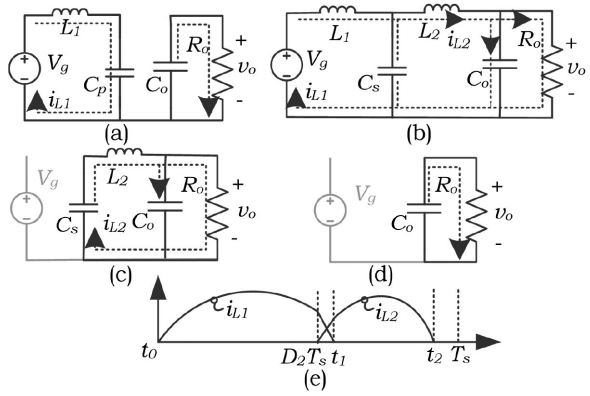

Fig. 4. Converter equivalent circuit when: (a) L_1C_p; (b) $L_1C_sL_2$, and (c) L_2C_s resonators exist; (d) none of the inductors conduct; and (e) ideal waveforms in the operation regime III.

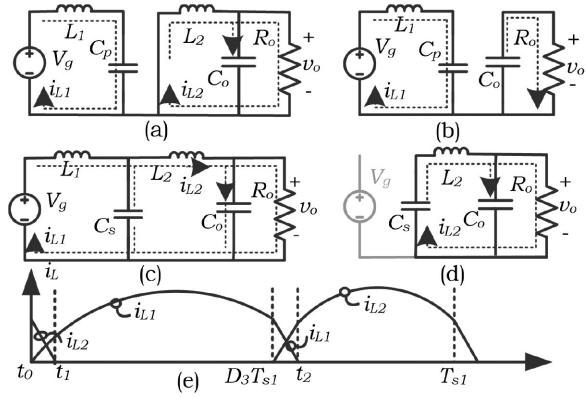

Fig. 5. Converter equivalent circuit when: (a) L_1C_p resonator exist and L_2 in linear mode; (b) L_1C_p resonator exist; (c) L_2C_s resonator exist and L_1 in linear mode; (d) L_2C_s resonator exist; and (e) ideal waveforms.

converter based on the aforementioned SCN concept to obtain controlled output voltage in Sections IV-B and IV-C.

C. Operation Regime III

A similar switching frequency (f_s) as in regimes I and II is used in this regime while using a duty ratio D_2 lower than the regime I. As a result, L_1C_p resonator does not complete a one-half cycle, as shown in Fig. 4(e), during interval $t_0 \le t \le D_2T_s$. Instead, L_1 inductor is a part of the L_1C_p resonator having characteristics frequency ω_1 during $t_0 \le t \le D_2T_s$ subinterval, as shown in Fig. 4(a), and then become a part of the $L_1C_sL_2$ resonator during the subinterval $D_2T_s \le t \le t_1$, as shown in Fig. 4(b), once L_2C_s resonator is enabled. The characteristic frequency of the resonator (ω_3) is given by (4). The equivalent circuit when L_1 inductor current reaches zero is shown in Fig. 4(c) and it exists until L_2 inductor current completes a one-half cycle. The equivalent circuit shown in Fig. 4(d) exists once both inductor currents reach zero at $t = t_2$ before T_s. A detailed analysis of the converter in this regime can be performed similarly as in Section IV. In the voltage gain analysis, calculation of $D_2T_s < t < t_1$ ends up with a third-order differential equation, which does not have a closed-form solution. Therefore, regime III operation to regulate the output voltage is not further considered

$$\omega_3 = \sqrt{\frac{L_1 + L_2}{L_1L_2C_s}}. \tag{4}$$

D. Operation Regime IV

This operation regime exists when the SCN is controlled using a higher switching frequency $f_{s1}(= \frac{1}{T_{s1}} > f_s)$ compared to the aforementioned three regimes. Inductor L_1 current is resonant although it has two characteristics frequencies and inductor L_2 operates in both resonant and linear modes, as shown in Fig. 5(e). During the time interval $t_0 \le t \le t_1$, both inductors are conducting. The inductor L_2 dissipates stored energy to the load operating in the linear mode while inductor L_1 resonating with the capacitor C_p having characteristics frequency ω_1, as shown in Fig. 5(a). During the next subinterval $t_1 \le t \le D_3T_s$, the inductor L_1 is in the resonant mode until D_3T_s having equivalent circuit shown in Fig. 5(b). There is stored energy in L_1 at the end of that time period since $D_3T_s < DT_s$. Therefore, L_1 become part of the $L_1C_sL_2$ resonator once the SCN enables the capacitor C_s, as shown in Fig. 5(c) at D_3T_s. The characteristic frequency of the resonator is ω_3. This time interval ends when inductor (L_1) current reaches zero at $t = t_2$. Hence, inductor L_2 resonates with C_s to transfer the energy stored in the capacitor bank during the previous subinterval having resonant frequency ω_2 until $t = T_s$. The equivalent circuit is shown in Fig. 5(d). A detailed analysis of the converter in this regime can be performed similarly as in Section IV. In the voltage gain analysis, calculation of $D_3T_{s1} < t < t_2$ ends up with a third-order differential equation, which does not have a closed-form solution. Therefore, regime IV operation to regulate the output voltage is not further considered.

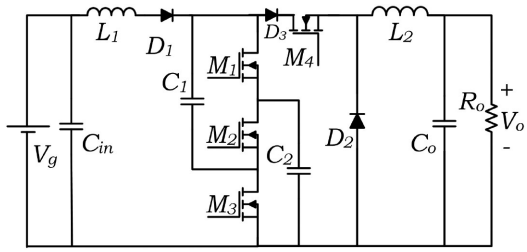

Fig. 6. Realization of buck–boost converter using unidirectional switches.

IV. Realization of a Buck–Boost Converter Using the Operation Regimes I and II

The operation regimes I and II are further considered to derive a converter having desired characteristics, less complex behavior, and analysis, as follows [1]. Realization of the SCN having the sequences shown in Fig. 1(b) is depicted in Fig. 6. The switches M_1 and M_3 are turned-ON together to connect two capacitors C_1 and C_2 in parallel. Later, the switches M_2 and M_4 are turned-ON to connect the capacitors in series. The diode D_1 limits the resonator consists of inductor L_1 to a one-half cycle as similar to the diode D_3, which limits L_1 inductor current into one direction. The input (C_{in}) and output (C_o) filter capacitors are selected at least ten orders higher than the capacitance of C_1

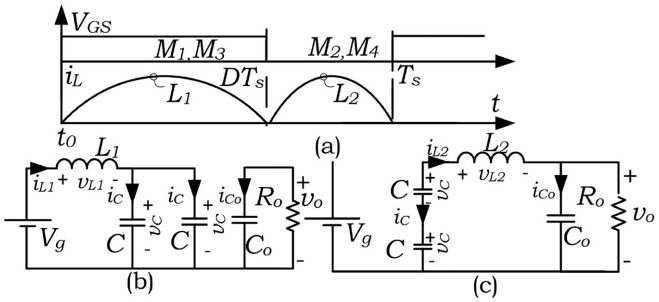

Fig. 7. SwR buck–boost converter's (a) ideal waveforms, and (b) and (c) equivalent circuits during each subinterval of the operation in regime I.

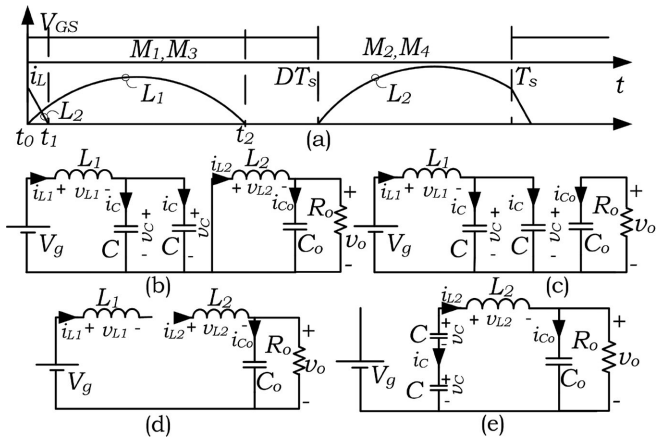

Fig. 8. SwR buck–boost converter's (a) ideal waveforms, and (b)–(e) equivalent circuits during each subinterval of operation in regime II when pulsewidth modulation is adapted.

and C_2 to avoid interference with the resonant operation. Their large capacitance eliminates large ripple in the input and output voltages due to the resonant operation. The capacitors C_1 and C_2 are selected to have equal capacitance ($C_1 = C_2 = C$) to reduce converter design and implementation complexity. Operation of the converters is explained in the following section assuming ideal semiconductor and passive devices. It is assumed that the filter capacitors (C_{in} and C_o) are large enough to maintain constant terminal voltages. Moreover, it is assumed that the quality factor of the resonators is significantly high to assume sinusoidal inductor currents. The diode (D_2) in the output side let inductor L_2 to dissipate stored energy without interfering with the remaining part of the circuit.

A. Converter Operation in Regime I

The converter operation in regime I is explained using the ideal waveforms and equivalent circuits shown in Fig. 7. Both inductor currents complete a one-half cycle when the respective resonator is enabled, as shown in Fig. 7(a).

1) Interval I—[t_0–t_1; Fig. 7(b)]: The resonator consists of inductor L_1 is enabled by the SCN while placing two capacitors in parallel, as shown in Fig. 7(b), by turning-ON switches M_1 and M_3. Hence, they are turned-ON with ZCS since there is zero initial inductor current. The inductor current (i_{L_1}) and the capacitor voltage (v_C) during this interval are given by (5)–(7), where V_2 is the capacitor voltage at the beginning of each switching cycle. At the end of this subinterval, the inductor current (i_{L_1}) completes a one-half cycle at $t = DT_s$. The load power is provided by the output capacitor C_o since the resonator consists of L_2 is not enabled yet

$$i_{L_1}(t) = 2(V_g - V_2)C\omega_1 \sin(\omega_1 t) \tag{5}$$

$$v_C(t) = V_g + (V_2 - V_g)\ \cos(\omega_1 t) \tag{6}$$

$$\omega_1 = \frac{1}{\sqrt{2L_1 C}}. \tag{7}$$

2) Interval III—[DT_s–t_2; Fig. 7(c)]: At the beginning of this interval, the switches M_2 and M_4 are turned-ON to enable the resonator consists of series-connected capacitors and inductor (L_2), as shown in Fig. 7(c). The switches are turned-ON having ZCS since the initial inductor (L_2) current is zero. The inductor current (i_{L_2}) and capacitor voltage (v_C) are given by (8)–(10).

The energy transferred into the capacitor bank during Interval I transfers into the load and output capacitor C_o during this interval. This subinterval ends when inductor current (i_{L_2}) reaches zero completing a one-half cycle since diode D_3 blocks negative L_2 current

$$i_{L_2}(t) = \frac{C}{2}(4V_g - 2V_2 - V_o)\omega_2 \sin(\omega_2 t) \tag{8}$$

$$v_C(t) = \frac{1}{2}\left[V_o + (4\,V_g - 2V_2 - V_o)\cos(\omega_2 t)\right] \tag{9}$$

$$\omega_2 = \sqrt{\frac{2}{L_2\,C}}. \tag{10}$$

An expression for V_2 is obtained considering the average inductor current (i_{L2}), as in (11). It is a function of the load resistance (R_o) and the switching frequency (f_s) besides the resonant capacitors (C). The charge balance of a capacitor (C) is considered to obtain a relationship between the input and output voltages, as in (12). There is a constant gain in this regime according to (12) and it is not depending on either duty ratio or switching frequency (f_s)

$$V_2 = V_g\left[1 - \frac{1}{R_o C f_s}\right] \tag{11}$$

$$V_o = 2V_g. \tag{12}$$

B. Converter Operation in Regime II—With Pulsewidth Modulation

The converter operation in this regime is explained using the ideal waveforms and the equivalent circuits illustrated in Fig. 8. The converter operation changes into this regime by increasing the duty ratio (D) of the switches M_1 and M_3 while keeping the switching frequency (f_s) at a constant value. In this regime, the duty ratio (D) is modulated to control the output voltage.

1) Interval I—[t_0–t_1; Fig. 8(b)]: During this subinterval, both inductors conduct current, as shown in Fig. 8(b) when switches M_1 and M_3 are turned-ON. The inductors (L_1 and L_2) are in resonant and linear modes, respectively. Switches M_1 and

M_3 are turned-ON having ZCS since there is zero current in L_1 at the beginning. The capacitor bank stores energy while resonating with the inductor L_1. The inductor L_2 dissipates the stored energy during the previous subinterval conducting current through the diode (D_2) without interfering with the resonator. The inductor current (i_{L_1}) and the capacitor voltage (v_C) are given by (5)–(7), where V_2 is the capacitor voltage at the beginning of each switching cycle. The inductor current (i_{L2}) is given by (13), where $\alpha = \omega_2(1-D)T_s$. This subinterval ends when inductor current (i_{L2}) reaches zero at $t = t_1$

$$i_{L_2}(t) = -\frac{V_o}{L}t + \frac{C}{2}(4V_g - 2V_2 - V_o)\omega_2 \sin\alpha. \tag{13}$$

2) Interval II—[t_1–t_2; Fig. 8(c)]: The inductor current (i_{L1}) completes a one-half cycle within this interval having the equivalent circuit shown in Fig. 8(c). The inductor current (i_{L_1}) and the capacitor voltage (v_C) are given by (5)–(7). This subinterval ends when the inductor current (i_{L_1}) reaches zero.

3) Interval III—[t_2–DT_s; Fig. 8(d)]: Neither inductor conducts during this subinterval since both inductors are disengaged from the SCN. The output capacitor (C_o) provides load current, as shown in Fig. 8(d). The switches M_1 and M_3 are turned-OFF with zero current at $t = DT_s$.

4) Interval IV—[DT_s–T_s; Fig. 8(e)]: The resonator consists of the inductor L_2 and series combination of the capacitors is enabled at the beginning of this subinterval having ZCS in the switches M_2 and M_4. The equivalent circuit of the converter is shown in Fig. 8(e) and the inductor current (i_{L_2}) and capacitor voltage (v_C) are given by (8)–(10). However, the switches M_2 and M_4 have a hard turn-OFF at the end of this interval since they are turned-OFF at the end of switching cycle although inductor current is not zero.

An expression for the capacitor voltage (V_2) at the beginning of each switching cycle is obtained considering the charge balance of C as in the following:

$$V_2 = \frac{4V_g\cos\alpha + V_o(1-\cos\alpha)}{2(1+\cos\alpha)}. \tag{14}$$

An expression for the voltage gain (M) of the converter is obtained, as in (15), considering the relationship between the average inductor (L_2) and the load currents. The converter gain depends on the duty ratio (D), the switching frequency (f_s), and the load resistance (R_o). Therefore, either pulsewidth of the control signal (D) or switching frequency (f_s) can be modulated to vary the output voltage

$$M = \frac{V_o}{V_g} = \frac{4}{2+k};\ k = \frac{-b+\sqrt{b^2-4ac}}{2a}$$
$$a = \frac{C(1-\cos 2\alpha)}{8T_s(1+\cos\alpha)^2},\ b = \frac{C(1-\cos\alpha)}{2T_s(1+\cos\alpha)},\ c = -\frac{1}{R_o}. \tag{15}$$

C. Converter Operation in Regime II—With Frequency Modulation

The converter operation with the switching frequency (f_s) modulation is explained using the ideal waveforms and the equivalent circuits shown in Fig. 9. The converter is operated at a higher switching frequency ($\frac{1}{T_{s,1}} = f_{s1} > f_s$) when frequency modulation is adopted and $D_1 T_{s,1} = \pi\sqrt{2L_1 C}$. The only difference in the converter operation is the lack of subinterval $t_2 - DT_s$ shown in Fig. 8. The basic converter operation remains unchanged although since neither inductors conduct during this interval and the capacitor retains its charge without discharging. Hence, the converter gain is given by (15).

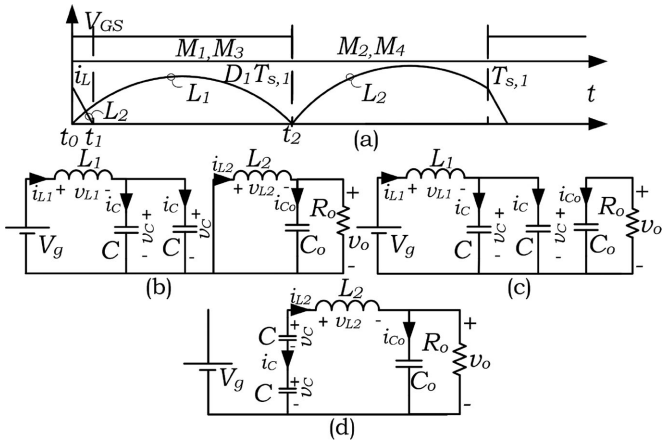

Fig. 9. SwR buck–boost converter's (a) ideal waveforms, and (b)–(d) equivalent circuits during each subinterval of operation in regime II when frequency modulation is adapted.

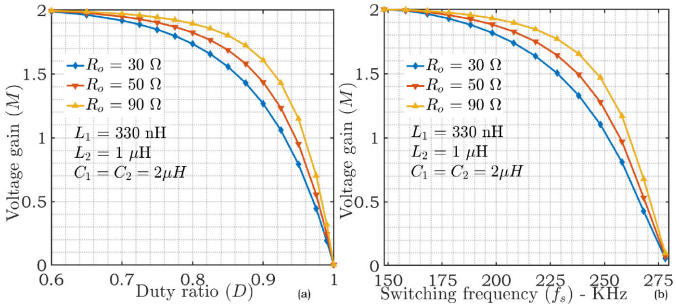

Fig. 10. Ideal voltage gain (M) of the converter with (a) pulsewidth (D), and (b) switching frequency (f_s) modulation at different loading conditions.

The voltage gains (M) of the converter when pulsewidth (D) and frequency (f_s) modulation adopted at different load levels are compared in Fig. 10(a) and (b). There is a higher voltage gain at a given duty ratio when load resistance increases. The gain difference between the load levels decreases at the lower duty ratios when the converter is operated more close to the regime I. This difference is significant at the higher duty ratios, as shown in Fig. 10(a). Similar behavior in the voltage gain plots obtained modulating the switching frequency can be observed, as shown in Fig. 10(b).

Based on the aforementioned analysis, the key advantages of the proposed converter can be compared against the other reported converter in the literature using the parameters listed in Table II. The considered conventional resonant converters [31], HybReSCC [12], [32], and SwRCs [14]–[16], [18] have either

TABLE II
COMPARISON OF PROPOSED CONVERTER WITH OTHER RESONANT DC–DC CONVERTERS

Topology	Semi. devices MOSFET/diode	Inductors	Capacitors	Voltage gain	Voltage control	Soft-switching ZCS/ZVS	Efficiency
Proposed	4/3	2	2	buck-boost (0-2)	pulse-width and frequency modulation	load independent ZCS	95.91%
[12]	6/0	1	2	fixed (4 to 1)	frequency modulation	ZCS	95%
[14]	2/2	1	2	boost (1-2)	frequency modulation	ZVS	98.3%
[15]	2/3	2	1	boost (1-2)	frequency modulation	ZCS	97.8%
[16]	2/4	1	2	boost (1-3)	frequency modulation	ZVS	98%
[18]	3/4	2	2	boost (1-3)	frequency modulation	load dependent ZCS	95.7%
[17]	2/4	3	3	boost (1-3)	frequency modulation	load dependent ZCS	95.9%
[20]	2/2	2	2	buck (2-1)	pulse width	load dependent ZCS	99.25 %
[21]	2/3	1	1	buck (.381-.312)	frequency modulation	ZCS	$\approx$ 92.8%
[24]	7/0	1	1	buck-boost (0.5-2)	pulse density	ZCS	96%
[31]	3/2	3	2	Cuk	pulse-width	load dependent ZCS/ZVS	97.1%
[32]	12/0	1	7	fixed (8 to 1)	split-phase	-	96%

step-up or -down property. However, the proposed converter has both output voltage step-up/down capability. A similar step-up and -down property can be observed in [24] and its output voltage is regulated in the range of 0.5–2, having ZCS. The conventional resonant converters have load-dependent soft-switching characteristics, but the proposed converter has load-independent ZCS at turn-ON and -OFF instances. This property can be seen in other SwRCs as well. However, the switching frequency should be varied in significant range to regulate the output voltage when there are variations in the line voltage or output load. This is not desirable when designing electromagnetic interference avoidance filter in the power conversion systems [27]–[29]. The proposed converter regulates the output voltage in regime II using pulsewidth modulation as similar to the conventional nonisolated dc–dc converters besides the switching frequency modulation, as similar to the conventional SwRCs. The pulsewidth modulation has similar capability to regulate the output voltage compared to the frequency modulation, as shown in Fig. 10. Although converter has all these advantages, it has a moderate number of semiconductor and passive devices compared to the conventional nonisolated resonant dc–dc converters and other members of the SCC family. The two out of three diodes are employed to realize the direct resonant cells, and the remaining diode is used to operate the output side inductor in the linear mode in operation regime II. The peak efficiency (95.91%) of the converter can be compared against the other converters, and it is in the same range. More details behind converter efficiency and loss sources are provided in the following sections.

D. Converter Design Considering Regulation Range

The regulation range of the converter can be adjusted at the design stage. In both regimes I and II, the input-side resonator completes a one-half cycle within DT_s interval. Therefore, that D becomes the minimum value of the duty ratio range that can be used to adjust the converter gain in regime II. Hence, the duty ratio D along with the switching frequency (f_s) are selected as the input of the converter design process. The ratio between the inductors ($\frac{L_1}{L_2}$) is obtained considering the regime I operation. The ratio is given by (16) and it is obtained using (7) and (10). The required capacitance for C_1 and C_2 is selected considering off-the-shelf capacitors. With the help of D and f_s, the inductor values can be calculated using (16) and $\pi(\frac{1}{\omega_1}+\frac{1}{\omega_2})=\frac{1}{f_s}$

$$\left(\frac{D}{1-D}\right)^2=\frac{4L_1}{L_2}. \tag{16}$$

V. VOLTAGE STRESSES ON THE DEVICES

The device stress is a function of the input, output, and capacitor voltages. The peak capacitor voltages in regimes I and II are given as follows:

$$v_{C,m_I}=V_g\left[1+\frac{1}{R_oCf_s}\right] \tag{17}$$

$$v_{C,m_{II}}=\frac{4V_g-V_o(1-\cos\alpha)}{2(1+\cos\alpha)}. \tag{18}$$

The maximum blocking voltages of the active switches are given by (19), where V_{C,m_x} is the capacitor peak voltage in the respective operating regime

$$V_{M_{1,2,3}}=V_{C,m_x}, V_{M_4}=V_o-2V_2, V_{C,\text{peak}}=2V_g-V_2. \tag{19}$$

There are higher voltage stresses on the switches at high-load conditions (at low R_o). Moreover, (17) and (18) show that higher switching frequency (f_s) can be used to minimize the stresses on active devices. However, this gives rise to higher losses in semiconductor devices when there is hard switching. Therefore, suitable f_s should be decided considering the facts emerge from the converter loss analysis.

VI. CONVERTER LOSS ANALYSIS

Loss model of the converter in regime I is obtained assuming the ON-resistance of the metal oxide semiconductor device as r_1, the diode is r_2, the equivalent series resistance of the inductor as r_3, C_{oss} output capacitance of a MOSFET, and the forward voltage drop of a diode as V_d. In this analysis, core losses of the magnetic devices are neglected by assuming the comparably low volume of the cores. The loss model of the converter (P_{l_t}) is derived in (21) calculating the root mean square ($i_{L_{1,r}}$ and $i_{L_{2,r}}$) and average ($i_{L_{1,a}}$ and $i_{L_{2,a}}$) inductor currents from the respective peak currents ($i_{L_{1,p}}$ and $i_{L_{2,p}}$), where $P_{l_{t1}}$ and $P_{l_{t2}}$ are the losses

in the devices during two subintervals of the operations

$$i_{L_{1,p}} = \frac{4\pi V_g f_1}{R_o f_s},\ i_{L_{2,p}} = \frac{2\pi V_g f_2}{R_o f_s} \tag{20}$$

$$P_{l_{t1}} = i_{L_{1,r}}^2\left(\frac{r_1}{2} + r_2 + r_3\right) + i_{L_{1,a}} V_d + f_s C_{oss} v_{C,m_I}^2$$

$$P_{l_{t2}} = i_{L_{2,r}}^2(2r_1 + r_2 + r_3) + i_{L_{2,a}} V_d + 0.5 f_s C_{oss} v_{C,m_I}^2 + 0.5 f_s C_{oss} V_{M_4}^2$$

$$P_{l_t} = P_{l_{t1}} + P_{l_{t2}}. \tag{21}$$

The converter loss model in operation regime II is obtained to estimate power losses when either pulsewidth or frequency modulation employed to control the output voltage. The peak currents of the inductors (i_{p1} and i_{p2}) in this regime are given as follows:

$$i_{L_{1,\text{peak}}} = I_{p_1} = C\omega_1 V_g\left(\frac{2\,k}{2+k}\right)\left(\frac{1-\cos\alpha}{1+\cos\alpha}\right) \tag{22}$$

$$i_{L_{2,\text{peak}}} = I_{p_2} = \frac{C\omega_2 V_g}{(1+\cos\alpha)}\left(\frac{2\,k}{2+k}\right). \tag{23}$$

Also, the L_2 inductor current (I_1) at the beginning of each switching cycle is given as follows:

$$I_1 = \frac{C\omega_2 V_g}{(1+\cos\alpha)}\left(\frac{2\,k}{2+k}\right)\sin\alpha. \tag{24}$$

The converter loss model is derived as in (25) using (22)–(24), where D_d is the duty ratio of the time interval t_0–t_1 shown in Figs. 8(a) and 9(a), $P_{l_{M_1,M_3,L_1}}$ is power losses in M_1, M_3, and L_1, $P_{l_{M_2,M_4}}$ is power losses in M_2 and M_4, $P_{l_{L_2}}$ is losses in L_2, and $P_{l_{D_2}}$ is losses in D_2. t_f is the switch turn-OFF time of the MOSFETs

$$P_{l_{M_1,M_3,L_1}} = \frac{I_{p_1}^2}{4}\left(\frac{r_1}{2} + r_3\right) + f_s C_{oss} v_{C,m_{II}}^2$$

$$P_{l_{M_2,M_4}} = \frac{I_{p_2}^2}{2}\left(1 - \frac{\sin 2\alpha}{2\alpha}\right)(1-D)2r_1 + \frac{I_1 V_{M_2} t_f f_s}{2} + \frac{I_1 V_{M_4} t_f f_s}{2} + 0.5 f_s C_{oss} v_{C,m_{II}}^2 + + 0.5 f_s C_{oss} V_{M_4}^2$$

$$P_{l_{L_2}} = \left[\frac{I_1^2}{3} D_d + \frac{I_{p_2}^2}{2}\left(1 - \frac{\sin 2\alpha}{2\alpha}\right)(1-D)\right] r_3$$

$$P_{l_{D_1}} = \frac{I_{p_1}^2}{4} r_3 + \frac{I_{p_1}}{\pi} V_d$$

$$P_{l_{D_2}} = \frac{I_1^2}{3} D_d r_2 + \frac{I_1}{2} D_d V_d$$

$$P_{l_{D_3}} = \frac{I_{p_2}^2}{2}\left(1 - \frac{\sin 2\alpha}{2\alpha}\right)(1-D)r_2 + I_2 V_d$$

$$D_d = \frac{k f_s \sin\alpha}{\omega_2(1+\cos\alpha)}$$

TABLE III
PARAMETERS USED IN THE EXPERIMENT TO VALIDATE THE EXISTENCE OF THE FOUR OPERATION MODES

Component	Value
Inductors ($L_{1,2}$)	0.22 μH
ESR of inductors ($L_{1,2}$)	30 $m\Omega$
Input capacitor (C_{in})	220 μF
Output capacitor (C_o)	220 μF
Resonant capacitor ($C_{1,2}$)	47 μF
MOSFET ($M_{1,SCN}$)	NTD4858N
Diode ($D_{1,2,3}$)	FERD30H60C

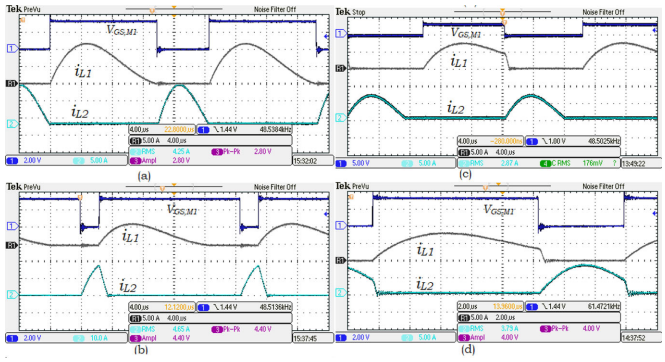

Fig. 11. Inductor current (i_{L_1} and i_{L_2}) waveforms along with the resonator L_1C_p activating signal in the operation regimes (a) I, (b) II, (c) III, and (d) IV.

$$I_2 = \frac{I_{p2}(1-\cos(\alpha))}{2\pi}$$

$$P_{l_t} = P_{l_{D_1}} + P_{l_{D_2}} + P_{l_{D_3}} + P_{l_{L_2}} + P_{l_{M_2,M_4}} + P_{l_{M_1,3,L_1}}. \tag{25}$$

The results obtained using the aforementioned loss models are compared with the experimental results in the following section.

VII. EXPERIMENTAL RESULTS

The existence of four operation regimes of a SwRC are experimentally verified using a discrete converter prototype with resonators L_1C_p and L_2C_s having parameters listed in Table III. The inductor currents i_{L_1} and i_{L_2} are observed in the four regimes and obtained waveforms are depicted in Fig. 11(a)–(d) along with the L_1C_p resonator activating signal. The respective waveforms of the operation regimes I–III are obtained using a constant switching frequency ($f_s = 48.5$ kHz) while changing the duty ratio. The converter operation changes into the regime IV by increasing f_s to 61.4 kHz. In all waveforms, the inductor currents i_{L_1} and i_{L_2} deviate from pure sinusoidal form due to the low-quality factor of the resonant circuits. However, the converter has intended behavior, as explained in Section II. All semiconductor devices are turned-ON and -OFF having ZCS in the operation regime I since all the inductor currents reach zero before transfer operation from one resonator to the other. However, there is hard switching in the switches when L_2C_s resonator operation terminates in the operation regime II although the L_1 current reaches zero before the switching transitions. Similar behavior can be observed in the switches

TABLE IV
PARAMETERS USED IN THE EXPERIMENTS TO VALIDATE THE PERFORMANCE OF THE PROPOSED CONVERTER

Component	Exp 1	Exp 2
Input inductor (L_1)	330 nH	82 nH
Output inductor (L_2)	1 μH	1 μH
Resonant capacitor (C)	2 μF	2 μF
Input capacitor (C_{in})	22 μF	22 μF
Output capacitor (C_o)	47 μF	47 μF
Switching frequency (f_s)	166 kHz	220.5 kHz
MOSFET ($M_1 - M_4$)	SiR124DP	SiR124DP
Diode ($D_1 - D_3$)	FSV15100V	FSV15100V
Input voltage (V_g)	10-30 V	10-30 V
Output voltage (V_o)	0-60 V	0-60 V
Load (R_o)	24.9-88 Ω	24.9-88 Ω

when they terminate the inductor current when it is nonzero in operation regimes III and IV.

The derived buck–boost converter operation is verified using results obtained from an experimental prototype rated up to 80 W. The parameters and components used in the prototype are listed in Table IV, and they are calculated using the method explained in the converter design section. The obtained inductor currents (i_{L_1} and i_{L_2}) and the capacitor voltage (v_C) with reference to the gate-to-source voltage of the switch M_1 are shown in Fig. 12(a) and (b). The inductor current waveforms are skewed due to the low-quality factor of the resonators, although they show the expected behavior. Both inductor currents complete one half-cycle, as shown in Fig. 12(a), when converter in operation regime I and $D = 0.6$. The average value of the capacitor voltage (v_C) equals the source voltage (V_g), and it reaches peak value when the inductor current i_{L_1} completes a half-cycle. v_C decreases when the switching network enables the second resonator. In the operation regime II, v_C reaches its peak values when the input-side resonator is enabled and remains at that value until the output side resonator is enabled, as depicted in Fig. 12(b). The input-side inductor current (i_{L_1}) completes a one-half cycle, and the output-side inductor is in both resonant and linear modes.

There is ZCS at all switching instances when the converter is in regime I, as illustrated by Figs. 13(a)–(c) and 14(a) and (b). Switching waveforms of M_2 and M_3 are shown in Figs. 13 and 14 since switches M_4 and M_1 have the similar behavior. The device current reaches zero before turning-ON or -OFF the switch and increasing/decreasing the switch voltage. As a result, there are zero losses due to nonoverlapping voltage and current waveforms. A similar property can be observed in the switch M_2 in the operation regime II, as shown in Fig. 13(d)–(f). There is a high-frequency ringing at the turn-OFF instant of the switch current waveform of M_3, as shown in Fig. 14(c). This ringing is due to the resonance between the MOSFET drain-to-source capacitor ($C_{\rm DS}$) and the inductor. This is evident that ZCS operation does not help eliminate the switching losses results due to the stored charge in the drain-to-source capacitance of MOSFETs. Similar behavior is observed in the switch M_3 when it is in the operation regime II.

The converter gains (M) at different duty ratios are tested, and the obtained results are shown in Fig. 15(a). The converter gain reaches its maximum value (1.9) when the duty ratio is 0.6, and it

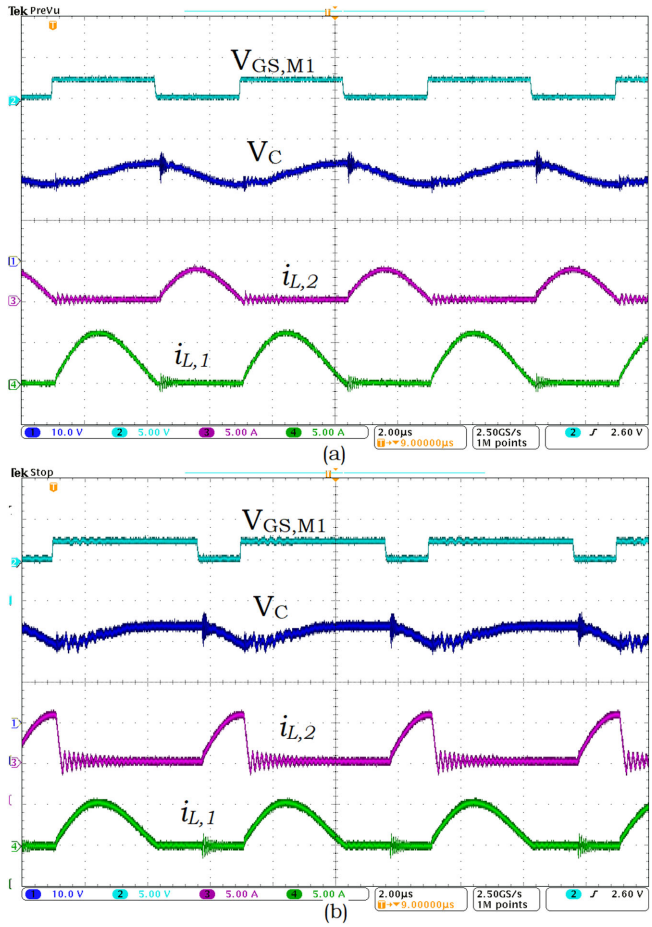

Fig. 12. Inductor currents (i_{L_1} and i_{L_2}) and resonant capacitor voltage (v_C) obtained using the experiment in (a) regime I and (b) regime II of the converter.

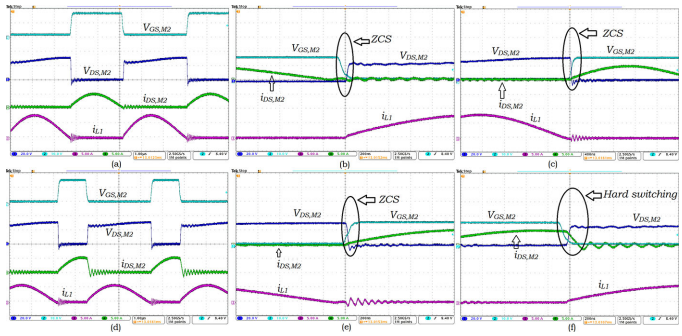

Fig. 13. Switch M_2 (a) drain-to-source current ($i_{{\rm DS},M_2}$), drain-to-source voltage ($V_{{\rm DS},M_2}$), and gate-to-source voltage ($V_{{\rm gs},M_2}$) along the inductor current (i_{L1}), (b) zoomed waveforms at the turn-ON, and (c) zoomed waveforms at the turn-OFF instances in the operation regime I. Same set of waveforms are shown in (d)–(f) when converter is in the operation regime II.

is in regime I. It does not reach expected maximum value because of the forward voltage drop of the diodes, ON-resistances of the semiconductor devices, and other parasitic resistances of the printed circuit board. The converter gain (M) varies with the duty ratio (D) in regime II, as expected from the theoretical analysis. Also, the influence of the load resistance (R_o) on the voltage

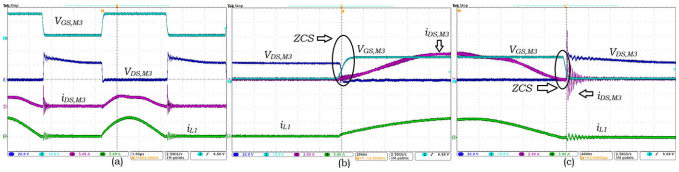

Fig. 14. Switch M_3 (a) drain-to-source current (i_{DS,M_3}), drain-to-source voltage (V_{DS,M_3}), and gate-to-source voltage V_{gs,M_3} along the inductor current (i_{L1}), (b) zoomed waveforms at the turn-ON, and (c) zoomed waveforms at the turn-OFF instances in the operation regime I.

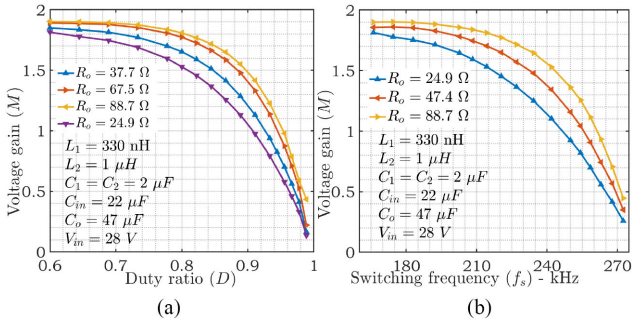

Fig. 15. Converter gain (M) at different (a) duty ratios (D) and (b) switching frequencies (f_s) under different loading conditions obtained using experiment.

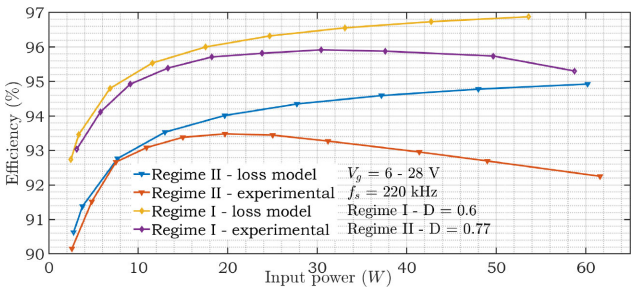

Fig. 16. Efficiency of the converter at different load levels in the operation regimes I and II of the converter. Both experimental and predicted losses using the loss model in (25) are shown.

gain (M) is validated using the results obtained at different R_o values shown in Fig. 15(a). The output voltage regulation capability at the high load conditions is better than the low load levels. Furthermore, the converter gain regulation by modulating the switching frequency (f_s) is validated using results shown in Fig. 15(b). Fig. 15(b) shows that switching frequency (f_s) should be varied in a wide band to vary the gain in the expected range. Moreover, the converter parameters are changed to test converter regulation range adjustment property and a new set of voltage gains (M) reading is obtained, as depicted in Fig. 17(a). In experiment 2, the maximum gain of 1.91 is obtained at the 0.4 duty ratio. Similar behavior in the voltage gain curves at different loading conditions is observed.

The converter efficiency at different input power levels are tested in the operation regimes I and II, and the obtained results are shown in Fig. 16. The efficiency measurements are obtained changing the input voltage and keeping the load resistance at 37.3 Ω in regime I and 47.4 Ω in regime II. The converter

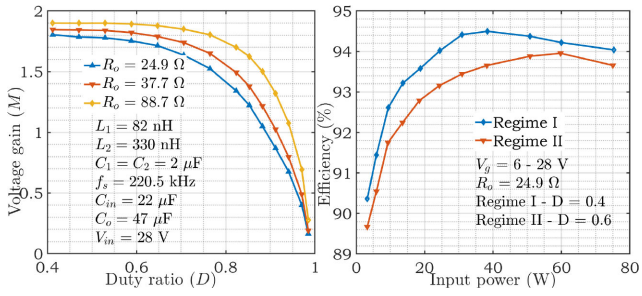

Fig. 17. Converter gain (M) at different duty ratios (D) to demonstrate the converter voltage regulation range.

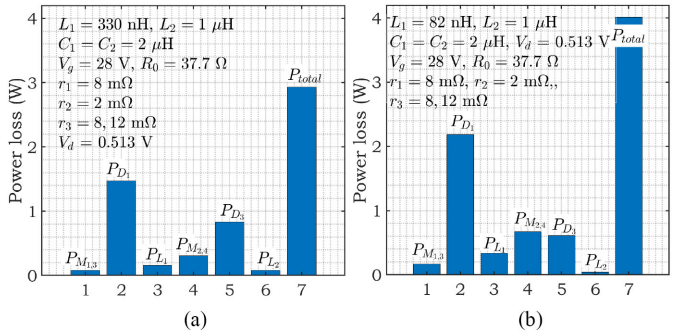

Fig. 18. Loss distribution among active and passive devices in regime I in experiments (a) 1 and (b) 2.

has a peak efficiency of 95.9% in regime I and it is 93.48% in regime II. The reason behind this difference is switching losses due to the hard switching operation of M_2 and M_4. This result is further validated using the derived converter loss model in (25). Fig. 16 shows that there is a close match between the experimental results and the predicted values at low power level, although there are small differences at high power levels. The reason behind this difference is unmodeled losses in the printed circuit board and other parasitic elements. The converter efficiency in experiment 2 is recorded, and the results are shown in Fig. 17(b). The peak efficiencies in both regimes I and II are lower in experiment 2, and the reason behind this reduction is validated using the values predicted using the loss model in (21). The results show that losses in the elements connected to the input-side resonator increase due to the change in the ratio between $\frac{f_1}{f_s}$ and $\frac{f_2}{f_s}$, as given by (20). The loss distribution among the elements of the circuit is obtained using the derived loss models. Fig. 18(a) and (b) shows that diode D_1 and D_2 significantly contributes to the total loss of the converter. This is due to the forward voltage drop and on-resistance of the diode. A similar loss distribution can be observed in the SwRCs based on the direct resonators proposed in [15] and [17].

The load transient response of the converter is tested in both regimes, and obtained waveforms are shown in Figs. 19 and 20. The inductor currents (i_{L_1} and i_{L_2}) and the output voltage (v_o) waveforms are observed when there is a step-change in load resistance in between 24.9 to 47.4 Ω when the input and output voltages are 18 and 16 V, respectively. The regime I waveforms are obtained under the open-loop condition, and the

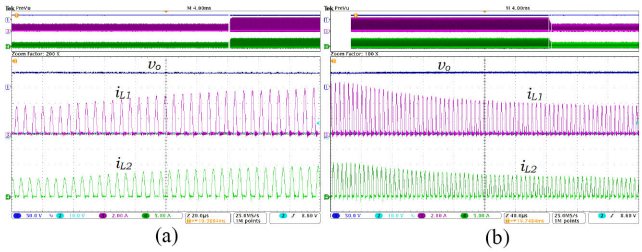

Fig. 19. Load transient response of the converter in the operation regime I at the load (a) step-up and (b) step-down instances. The output voltage (v_o) and both inductor currents (i_{L_1} and i_{L_2}) are shown along with the zoomed waveforms.

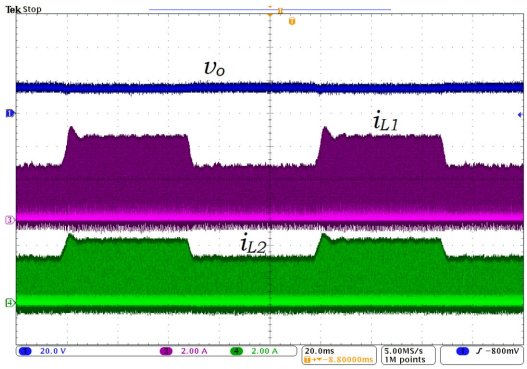

Fig. 20. Load transient response of the converter in operation regime II. The output voltage (v_o) and both inductor currents (i_{L_1} and i_{L_2}) are shown.

output voltage in regime II is regulated using voltage feedback. The error between the measured output voltage and the reference value is compensated using a PI controller implemented on a TMS230F28335 digital signal processor. In regime I, the inductor currents reach the end values within several switching cycles and, hence, there is not any significant change in the output voltage waveform. In the operation regime II, similar behavior is observed, although there is an insignificant dip in the load voltage. This property validates the converter's ability to give null-response under the load transient conditions. The reason behind this behavior is the availability of charged series-connected capacitors with the output inductor to provide the required charge to fulfill deficit in the output capacitor under the load transient.

VIII. Realization of a Converter Having Buck Properties Using the Operation Regimes I and II

A converter having only buck properties is derived by using the reconfigurable SCN and operation regimes I and II. The derived converter using the SCN configurations shown in Fig. 1(c) is depicted in Fig. 21(a). The converter has unregulated output when it is operated in regime I, using switching control signals and ideal waveforms shown in Fig. 21(b). The voltage gain (M) of the converter in this regime is 0.5. When the converter is operated at the same switching frequency (f_s) and high duty ratios ($D' > D$), then the converter is in the operation regime II. The converter has the ideal waveforms shown in Fig. 21(c) and its

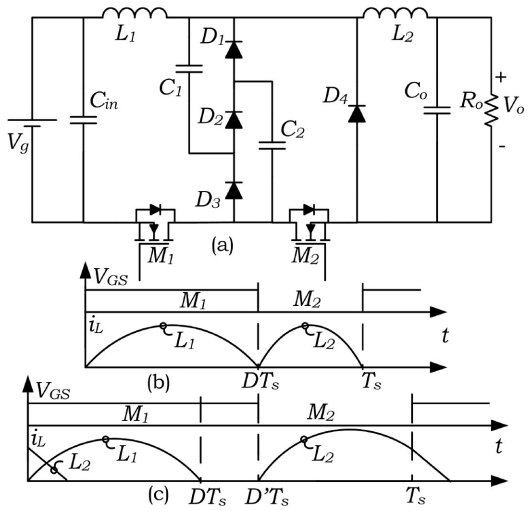

Fig. 21. SwRC is employed (a) to derive a converter having buck properties, its ideal waveforms in the operation regime (b) I and (c) II.

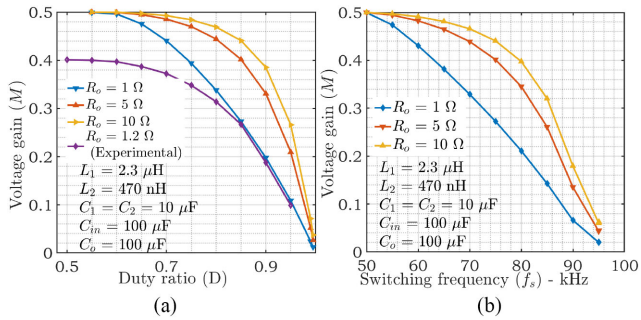

Fig. 22. Voltage gain (M) of the converter when (a) pulsewidth (D) and (b) switching frequency (f_s) modulation is adapted.

voltage gain (M) is given by (26). According to (26), the voltage gain can be adjusted in between 0 and 0.5 either modulating duty ratio (D) or switching frequency (f_s) very similar to the buck–boost converter. The simulated converter gain (M) under both control strategies is shown in Fig. 22. The parameters used in the simulation are shown in Fig. 22 and a similar set of values are used in an experimental prototype to validate the simulation results. The obtained converter gains are shown in Fig. 22(a) when the pulsewidth modulation is adopted. The converter gain does not reach its expected maximum value due to the voltage drops in the parasitic resistances in the semiconductor and passive devices besides the forward voltage drop in the diodes. Moreover, the inductor currents (i_{L_1} and i_{L_2}) are observed in both modes, and they are depicted in Fig. 23. Similar analysis as the buck–boost converter can be performed to further validate the buck converter operation. The presented buck realization is not optimum due to the number of diodes. The diode D_1, D_2, and D_3 can be replaced using active current unidirectional switches, such as GaN FET, that do not conduct in the third quadrant on the VI plane. Such a realization may help increase the voltage

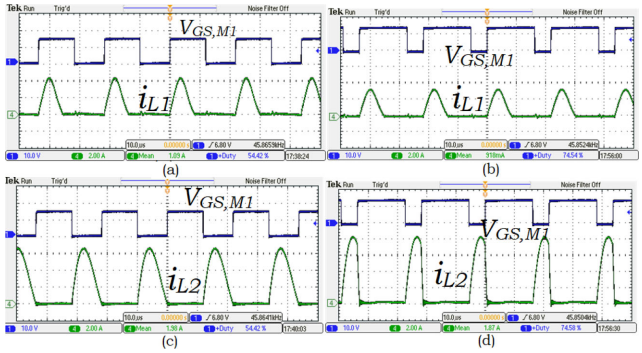

Fig. 23. Inductor current (i_{L_1} and i_{L_2}) waveforms of the buck converter with reference to the gate-to-source voltage (V_{GS,M_1}) when the converter is in the operation regimes (a) and (b) I and (c) and (d) II.

gain and converter efficiency

$$M = \frac{V_o}{V_g} = \frac{1}{2+k};\ k = \frac{-b+\sqrt{b^2-4ac}}{2a}$$
$$a = \frac{C(1-\cos 2\alpha)}{2T_s(1+\cos\alpha)^2},\ b = \frac{2C(1-\cos\alpha)}{T_s\,(1+\cos\alpha)},\ c = -\frac{1}{R_o}. \quad (26)$$

IX. Conclusion

Multiresonant and multimode operation of SwRCs can be effectively used to develop converters having buck–boost and buck properties. The multiresonant operation is obtained using two distributed inductors and an SCN. The voltage regulation range of the derived converters can be adjusted by changing the ratio between the two inductors. The converter voltage can be regulated either modulating pulsewidth of the control signal without changing the switching frequency. Also, the switching frequency can be modulated to change the converter gain in the desired range, having a similar regulation capability to the pulsewidth modulation. There is a load-independent ZCS operation when the converter is in operation regime I. There is ZCS turn-ON in all switches when the converter is in operation regime II. The switches that are connected to the inductor operating in the linear mode have a hard turn-OFF when the converter is in the operation regime II.

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